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APPLIED RESEARCH

A SBC-Based Data Acquisition System: A Case Study on Smart Reclosers and Multiagent Systems

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ABSTRACT Efficiently handling faults and analyzing signals in power distribution systems is a persistent challenge. Previous studies proposed using smart devices, but most evaluations considered simulated environments. In this paper, we propose a novel approach to address signal acquisition and processing using a single board computer (SBC) to provide more local computational capabilities to reclosers. This paper addresses the challenge of using multiple software programs to digitize signals, monitor faults, and communicate with other reclosers for fault handling. We show the high-level software on the SBC can meet the requirements of the data acquisition system and provide high computational power for various local data processing tasks. The proposed hardware enables real-time signal acquisition with low latency and a reduced probability of sample loss, which is vital for accurate signal detection and analysis. We evaluate our approach in an in-house embedded system with communication capabilities, taking into account the multi-agent approach for handling faults in power distribution systems. Our results demonstrate the proposed system provides signals to the application without sample loss. Regarding noise levels, we measured error lower than 1%, and harmonic distortions smaller than 5% of the 50/60 Hz waveform, indicating minimal circuitry impact. We measured latencies around a few microseconds, which is crucial for fault detection. Finally, we present an evaluation setup that demonstrates an efficient process for restoring energy service in power distribution systems. Therefore, the proposed hardware shows promising performance for smart reclosers and other real-time data acquisition systems that require intensive local computations.

INDEX TERMS Embedded systems, power distribution, digital signal processing, recloser, multi-agent systems.

I. INTRODUCTION

Power distribution systems may be subject to fault events, which can be cleared by protective devices designed that detect abnormal conditions. These events can affect the energy supply to customers and worsen reliability indices. As repairing of a failed component may take a considerable amount of time, one solution to contour these events is to isolate the area under failure and restore the energy supply in other areas via network reconfiguration. The network

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may be reconfigured to achieve restoration using switching devices such as reclosers, which are popular circuit interrupting devices for distribution systems [1]. Some restoration approaches require reclosers with communication capabilities [2], in which reclosers communicate either with a central controller or neighboring reclosers aiming to locate the fault, isolate the faulted section, and to restore the energy service to the customers.

The concept of multi-agent system (MAS) [3] can be fairly applied to manage recloser switching actions with the purpose of achieving energy service restoration [2], [4], [5], [6]. MAS are systems composed of multiple interacting computing elements called agents, which are capable of handling problems by taking autonomous actions or by interacting with other agents. In this context, MAS can use high level abstractions, such the Agents & Artifacts approach [7], [8], to embed agent-based restoration procedures designed by power engineers. MAS can be deployed to segment a network into sub-networks, each controlled by a local agent, which communicates and coordinates to solve problems. Each agent can sense its environment (e.g., by measuring voltage and currents) and react to changes autonomously or in accordance with other agents to isolate problems and reestablish service to a maximum number of customers.

The related works present evaluations based on simulated environments or models, such as IEEE 123 node test feeder, which may hide some real-word issues. As power distribution systems will likely suffer from real-world issues, they need to be evaluated before putting such systems in production. Bearing these concepts in mind, the main contribution of this paper is the proposal of a hardware and software approach to monitor signals in real-time, which is part of the features needed to implement MAS in power distribution systems. The specific contributions are the following: 1) the paper addresses an issue that may arise due to the use of multiple software programs needed to digitize signals, monitor faults and communicate with other reclosers to quickly handle the faults; 2) we propose a solution based on software and hardware to allow sampling the signals without sample loss and with low latency. Moreover, to the best of the authors knowledge, there is not in the literature a test bed implementation aiming to test and validate agent-based restoration procedures designed with the Agents & Artifacts approach. Thus, as a third contribution, we present 3) a small-scale evaluation of restoration using an implementation based on MAS.

The hardware-related part of the contributions of this paper consists in the development details of an embedded system, which is based on an single-board computer (SBC) integrated with a Data Acquisition (DAQ) board that together can be used to test and validate MAS-based procedures devoted to power distribution system restoration. The SBC provides a significant computational capability and is compatible with Linux, which can provide the benefit of reusing several available applications and protocols. The DAQ subsystem has been designed to sample voltage and current waveforms from three-phase distribution lines, allowing power quality and event analysis, as well as MAS-based restoration procedures. Furthermore, the proposed system is also capable of long-range communicating with the adoption of the IEEE 802.15.4g, using the upper layers defined by IPv6 over the TSCH mode of IEEE 802.15.4e (6TiSCH), which enables the connection among agents or with a web server to implement real-time remote monitoring. This combination of features in the hardware presents good performance for smart reclosers, which can also be valuable to other real-time data acquisition systems that require intensive local computations.

This paper is organized as follows. Section II presents a literature review on embedded systems for signals acquisition. Section III provides details about the system hardware and software proposed in this work. Section IV presents quantitative evaluations, such as signal quality analysis and latency evaluation of the DAQ. Section V shows an example of a power grid restoration using MAS running over the proposed hardware. Section VI outlines the final remarks.

II. LITERATURE REVIEW

The so-called SBCs are devices that have computation capabilities close to conventional computers, in terms of the diversity of applications. They are in general implemented in a single printed circuit board, which includes all the required peripherals, such as memory, storage, communications, and others. They might be less capable in terms of processing due to, for instance, energy constraints and heat dissipation, but they can run nearly all software and operating system (OS) standard computers can do. Such capabilities bring a significant advantage of providing a myriad of software, for instance, network protocol implementations, compression tools, digital signal processing libraries, etc.

In this section we review recent applications and evaluations, which relied on SBCs, and the discussion is directed to requirements and suitability for being adopted in MAS. In summary, the suitability can be based on the cost of building the system, availability of long range communication, and on features of the sampling of signals. The cost of the systems is important, as a possible high number of instances can be deployed to cover, for example, a whole city or a large area, which also rises the need for an efficient long range communication capability. Lastly, features present on the sampling of signals are also of interest in these systems, such as simultaneous sampling of distinct input signals on the same hardware, and synchronized sampling on geographically separated hardware. In the following paragraphs we discuss some related work and highlight these features, and in Table 1 we provide a summary of the presented discussion. Moreover, Table 1 also presents specifications of the CPU, RAM and storage present in these platforms, which allow comparing with the one present in the platform adopted in this work, presented in Section III.

Due to their features, SBCs have been adopted in several embedded systems applications [13], [14], [15], [16], [17], [18], [19]. In [13] the authors evaluate the performance of SBCs in projects to monitor sensors and analyze the most

TABLE 1. Comparison among DAQ systems and their suitability for using in a multi-agent-based power distribution.

Ref.	OS & Platform	Comm.	Sampling	Suitability to multi-agent for power distribution
[9]	Linux, BeagleBone Black, ARM Cortex A8 @1 GHz, 512 MB RAM, 4 GB Storage	Ethernet	8 channels simultaneous, 16 bits, >200 kHz, GPS synchronized	Focus on synchronized signals sampling. No further
[10]	Linux, industrial controller FPGA+quad-core CPU@1.91 GHz, 2 GB RAM, 16 GB Storage	Ethernet	2 channels simultaneous, 24-bit ADC, >50 kHz, GPS synchronized, dedicated analog front-end	FPGA and industrial equipment may result high power consumption and more expensive design Focus on synchronized signals sampling
[11]	Linux, FPGA+dual-core ARM Cortex A9 @1 GHz, 1 GB RAM, Micro SD Storage	Ethernet	8 channels simultaneous, 12-bit ADC, >64 kHz, dedicated analog front-end	FPGA may result high power consumption and more expensive design. Low range communications with Ethernet. Front-end design for up to 800 V
[12]	Proprietary/LabVIEW, laboratory equipment (programmable logic controller and daughter boards)	TCP/IP	64 channels, 16-bit ADC, >250 kHz, dedicated analog front-end	Laboratory equipment are not suitable for evaluation with a high number of instances. No further detail is provided about the communication

popular platforms based on cost, processing capacity, integrated processing technology, open source license, power consumption, reliability, programming flexibility, availability of support and electronic utilities. The paper [13] also presents an example application that monitors several sensors and evaluates different storage and monitoring options.

A category of application that can benefit from the low-power and embedded computing capabilities is environmental monitoring, which could be battery-powered due to a lack of power supply infrastructure in the environment it is installed. In these systems, SBCs can be used to interface to one or more sensors, and the SBCs can read data, optionally process, and send data to a remote unit, with the advantage of resulting in minimal impact on the monitored environment due to its compact size. Some examples of real-time DAQ systems are [9], [10], [11] and references therein.

In [9], the authors propose an embedded system for GPS-synchronized acquisition of analog signals. The paper [9] focuses only on the real-time data acquisition unit, which can happen synchronously to other instances of the system due to the GPS-synchronized sampling capability. This approach can reduce development time for instruments requiring synchronous sampling spread in a wide area. The paper focuses only on sampling data, which is sent to another computation unit via User Datagram Protocol (UDP) datagrams. The authors utilize the SBC BeagleBone Black to implement real-time sampling with synchronized timestamps. Two significant drawbacks of this work are that the signal processing is not performed on the proposed hardware and the wired Ethernet connectivity adopted. The lack of signal processing may result in a potentially high amount of sampled data that should be sent to a remote unit, which is not a severe issue in the paper due to the application of Ethernet-based connectivity. However, relying on cabled connectivity may result in severe limitations on the infrastructure needed for the system to work.

In the context of smart grid applications, the paper [10] proposes an FPGA-based system, which, as [9], is also synchronized and adopts Ethernet-based connectivity. Other FPGA-based systems are proposed in [11] and [10], which are platforms for smart grid measurements. The adoption of FPGAs can provide a highly parallel computational processing capability, but, in general, FPGAs are more power-hungry and more expensive in relation to embedded processors. Accordingly, these characteristics may inhibit the deployment of FPGA-based embedded systems in applications that adopt battery as the power source and require a high number of instances of the embedded system, due to the multiplicative factor of the number of instances to the cost.

These papers show the importance of communication capabilities in modern smart grid applications. Due to the geographical reach of the power distribution systems, wireless long-range communication is a significant differential feature. For example, the paper [12] presents a communication-assisted fault localization, isolation, and restoration method for microgrids based on a multi-agent system. It also shows that the communication between multiple agents at distinct places of the network can be used to restore power for different customer loads by changing the configuration of the system. The paper [12] presents evaluations of the technique based on an experiment in a laboratory environment. The presented evaluations were made with equipment in a laboratory environment, or with models or simulated data, without focusing on the implementation aspect of the algorithms and its interactions with other software needed. Thus, in this paper we intend to fill one of these gaps. We present the challenges of using multiple software programs to digitize signals, monitor faults, and communicate with other reclosers for fault handling, then we present a hardware and software based approach to deal with these challenges.

III. PROPOSED SBC-BASED DATA ACQUISITION SYSTEM

An overview of the proposed system is shown in Fig. 1, with the implemented hardware and the software stack. A detailed discussion about the hardware is conducted in Section III-A and a detailed discussion about the software stack is presented in Section III-B. The hardware is comprised of a DAQ, an SBC and a long-range communication board. The DAQ is capable of sampling multiple analog signals simultaneously and delivering the sampled data to the SBC. The SBC is capable of running Linux OS, which allows benefiting from already available applications that can speed up the

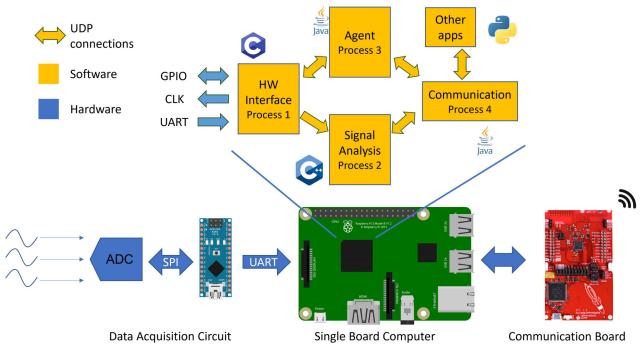

FIGURE 1. Proposed data acquisition system using a single board computer.

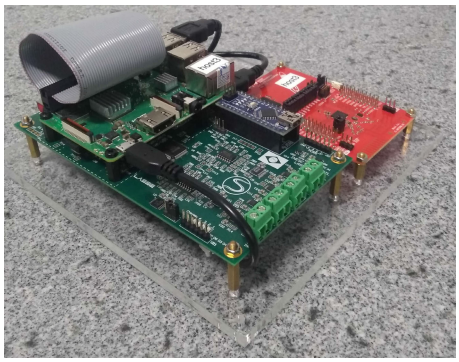

FIGURE 2. The assembled hardware with the SBC, the LAUNCHXL-CC1350, and the in-house developed PCB.

development of additional ones in different languages. Besides, the SBC has enough processing power to perform several calculations in real-time that can be needed in several monitoring applications. Lastly, an external board is connected to the SBC and allows communication via a long-range wireless link with the 6TiSCH over IEEE 802.15.4g technology.

Fig. 1 also shows a high-level representation of the software implemented on the SBC and their corresponding programming language, to illustrate the versatility of the SBC. Process 1 and 2 are implemented in C/C++, while Process 3 and 4 are implemented in JAVA. Besides these four processes, the SBC is also able to run other software in any language (e.g., Python), depending on the demands of the application. Regardless of the programming language used to build the processes, in this work all of them use the lightweight UDP to communicate with each other, where each process has a specific UDP port, which is facilitated by the network stack included in the OS. By using UDP, applications become more modular and the tests of the prototype can be accelerated. For instance, Process 1 could be configured to send samples to a server without the interference of processes 2 and 3, by simply changing the port and IP address in command-line parameters or configuration files.

A. HARDWARE AND DATA ACQUISITION DESIGN

The hardware is composed of the DAQ, the SBC and the communication board, as shown in Fig. 2. The SBC is an off-the-shelf Raspberry Pi 3b+, which includes a quad-core 64-bits processor with a maximum frequency of 1.4 GHz, dual-band wireless LAN, Bluetooth 4.2/BLE, Ethernet and USB ports, 1 GB LPDDR2 SDRAM, and a 40-pin GPIO header. A separate Printed Circuit Board (PCB) has been developed to be compatible with the 40-pin GPIO header of the SBC, thus other compatible SBCs could be used to substitute the applied Raspberry Pi model. The developed PCB also holds the components of the DAQ, as discussed in the next paragraphs. The communication subsystem is implemented with the LAUNCHXL-CC1350 evaluation board, which includes a microcontroller (MCU) that is able to communicate in the Sub-1 GHz and 2.4 GHz bands. The communication board enables the implementation of the 6TiSCH and is connected to the SBC through the USB port, which allows providing both power and commands to send and receive packets.

The DAQ subsystem is composed of analog conditioning circuits to amplify and filter the analog signals before digitization, an analog-to-digital converter (ADC) with multiple synchronous inputs, and an MCU, which is responsible for receiving samples from the ADC and forwarding them to the SBC via a Universal Asynchronous Receiver/Transmitter (UART) interface. All the signal conditioning is placed on the PCB, as shown in Fig. 2. The reason for using an MCU between the ADC and SBC is to guarantee that certain quick periodic or random events on the signals are sampled in time [20]. For example, the SBC is capable of running Linux, which brings some benefits but also results in some limitations. One of the limitations may appear due to the several software layers, which could impact the capture of real-time events due to eventual interruptions. Thus, the MCU is an optional component that can be used to deal with those real-time or quick events in synergy with the high-level software running in the SBC.

To better illustrate when the MCU could be required, we present briefly more details about the operation of the ADC adopted in this work. The ADC generates periodic pulses with rate of the sampling frequency to indicate that a new sample is ready to be collected, which must be done timely before the next sampling period finishes, otherwise, the samples are overwritten. The SBC may eventually lose some of these pulse because the OS can be busy with other tasks while the event occurs and consequently lose the new sample indicated by that pulse.

There are some interruption service routines that can be programmed over the OS, which operate with lower priority than other routines running in the own OS. One workaround for this problem could be changing the OS and implementing specialized drivers for handling the interruption with the highest priority, but another solution with lower development time is to use the UART buffer offered by the OS [21, Section 3.3]. In the latter, the MCU gets samples from the

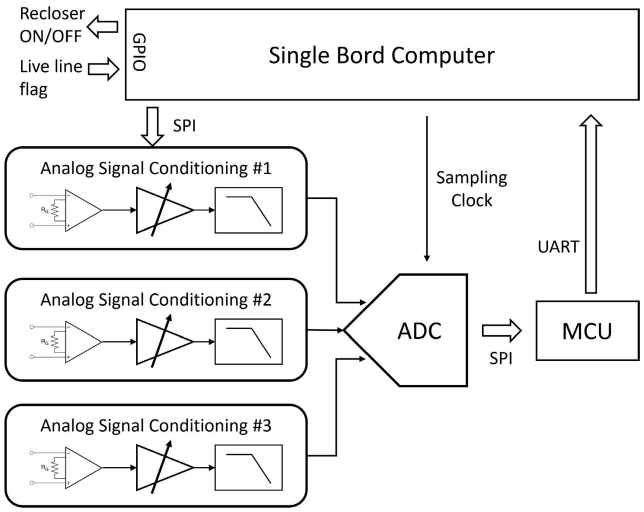

FIGURE 3. Block diagram of the DAQ hardware.

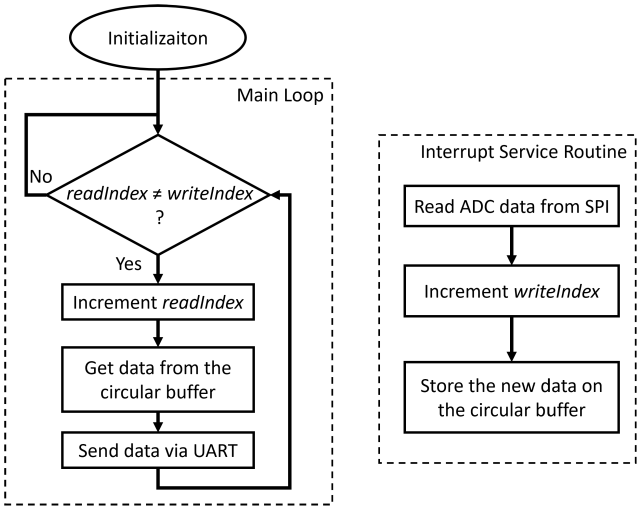

FIGURE 4. Flowchart of the firmware of the MCU.

ADC and forwards them to the SBC, which accommodates the received data in the UART buffer, as shown later in this section.

Fig. 3 shows a simplified block diagram of the developed hardware. At a high level, the DAQ is composed of three similar conditioning paths, which include a cascade of two amplifiers (G1 and G2), a low-pass filter, and the ADC. The amplifier G1 is the component INA826, which is an instrumentation amplifier that has a configurable gain controlled in the range of 1 and 1000 that is set by an external resistor. The amplifier G2 is implemented with the programmable gain amplifiers (PGAs) LTC6912 component, which can be configured via a serial peripheral interface (SPI) interface. The active low-pass filters act as anti-aliasing to allow the sampling by the ADC. Lastly, all the conditioning paths finish in the multi-channel ADC AD7606-4 with a resolution of 16 bits, which samples all the inputs simultaneously. Moreover, the sampled data is sent to the MCU ATmega328, which, in turn, forwards the data to the SBC through the UART.

The SBC sets the PGAs gains via SPI and provides the ADC sampling clock with the frequency of 15360 Hz. The hardware can receive three analog inputs with different dynamic ranges, thanks to the programmable gains in the PGA. Then, each PGA output is filtered by a 4th-order anti-aliasing filter implemented with Sallen-Key Topology. The cutoff frequency is 3 kHz. The filtered signal is delivered to the ADC, which uses a sampling frequency of 15360 Hz, yielding 256 samples per cycle at 60 Hz.

Each time a new sample is ready, the ADC generates a pulse. This pulse launches an interrupt service routine (ISR) on the MCU, which executes commands to read the digital samples from ADC via SPI. Then, these samples are sent to the SBC via the UART interface. A flowchart that represents the firmware implemented on the MCU is shown in Fig. 4, where *writeIndex* and *readIndex* are the indexes of the circular buffer for writing and reading, respectively. When *readIndex* is different from *writeIndex*, it indicates that there is data on the circular buffer that has not been read yet.

With the mentioned operations the MCU needs to transport the digital samples via UART with a baud rate of at least $3 \times 16 \times 15360 = 737280$ bps. However, in practice, there are some processing time wasted within the MCU during, e.g., context exchange, data moving, etc. So, we used 2 Mbps of bit rate, which higher than the theoretical one to avoid data loss. The MCU sends the data to the SBC, and when the SBC receives them, it accommodates in a UART buffer implemented by the own Linux Kernel, which provides enough capacity [21, Section 3.3]. Thus, the received samples are not lost and the system is not interfered by any delays caused by the OS.

The digitization of the waveforms are performed between -5 V and $+5$ V. The voltages and currents on the power distribution system can be well higher than the recommended operating conditions of the hardware. They can be as high as some kilo-volts and hundreds of Amperes. So, it is essential to adequate such waveforms before digitization. In this context, the equipment could be implemented with instrument transformers or current transforms (CT) to decrease the level of the current. Then, the current in the CT's secondary could be transformed into voltage with different approaches, e.g., by using shunt resistors or hall effect sensors. Finally such a low power signal has the same waveform of the desired current on the line, and this low voltage signal is amplified, filtered and digitized, as shown on Fig. 3. The detection of live line binary flag could be implemented with voltage transformers followed by rectifiers or rectifiers followed by resistor voltage divider.

B. SOFTWARE AND COMMUNICATION

The SBC subsystem runs most of the software stack. The SBC is able to run many applications simultaneously in

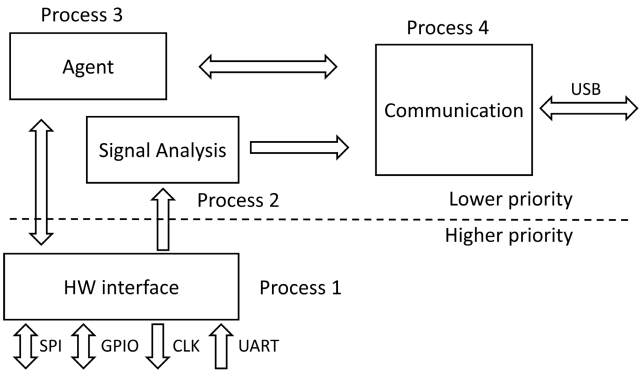

FIGURE 5. Block diagram of the software implemented on the SBC.

different languages. In the proposed systems there are four main processes, as shown in Fig. 5, namely: *Hardware Interface* (Process 1), *Signal Analysis* (Process 2), *Agent* (Process 3) and *Communication* (Process 4). All the processes communicate with UDP datagrams, allowing modular and independent development, and are described as follows.

Process 1 is responsible for controlling all the hardware in the system and serving other processes with information from the hardware. It is included in the operation of Process 1 tasks such as SPI data exchange, General Purpose Input Output (GPIO) set and read, ADC clock configuration, and receiving data from UART. For instance, Process 1 reads and sets the GPIOs, configures the sampling clock for the ADC and forwards samples received from the UART to Process 2. Furthermore, Process 1 is executed with a higher priority on the OS and also implements some system safety operations, such as detecting if there is voltage on the line or opening the recloser when the measured current exceeds some threshold value.

Process 2 is responsible for performing evaluation of the sampled signals, such as calculating the frequency deviation and the total harmonic distortion (THD) of the analog signals, finding events, etc. A simplified flowchart of Process 2 is shown in Fig. 6. Process 2 waits for packets until it receives 10 periods of the 60 Hz signals (2560 samples) of the three monitored phases. For each packet, it verifies if the flag with overcurrent is set. If so, an analysis of the fault is performed on the last 15360 samples, i.e., including the signal previous to the moment when the recloser was opened. Then, the next step is to calculate the amplitude and phase of the signals. Finally, if one second of the signal (15360 samples) is completed, then other metrics are evaluated such as frequency deviation and THD.

Process 3 implements an instance of a computational agent, designed with the Agents & Artifacts approach [7], [8], aiming to provide restoration capabilities to power distribution systems. It is a specific software for controlling reclosers using local data and information conveyed by other agents, targeting the identification and isolation of faulted sections as well as service restoration of areas not directly affected by faults. All agent-based restoration procedures executed

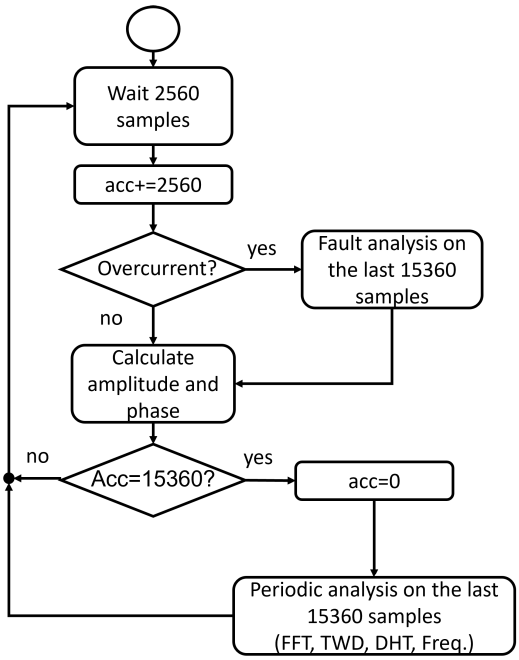

FIGURE 6. Flowchart of the signal analysis performed by Process 2.

in Process 3 are thoroughly described in [22]. Summarily, agents are employed to achieve three main goals: handle local faults, help neighbors with their own faults, and return to normal operation. Each agent is provided with a unique identifier; recloser artifact information such as voltage presence (true/false), switch status (open/closed), lockout (true/false), live line (true/false), condition (normal, fault); as well as lists of neighboring agent identifiers, priority loads/sections, and recloser identifiers within the coverage/neighboring sections. Following the Contract Net Protocol [23], an agent that detects the need for an alternative source of supply plays the role of initiator, beginning the protocol by sending a "call for proposal" to participants with its load demand, estimated with pre-fault load current data. A participant may answer with a proposal or a refusal message depending on whether physical connection and restoration capacity is available. Process 3 uses a bidirectional communication with Process 1 since the agents must be notified if Process 1 performed any action on the recloser (open/close). Moreover, an agent (Process 3) can send commands to open or close the recloser, to isolate a fault and create a temporary different grid configuration.

Process 4 handles all the external communications, i.e., it implements all the necessary actions to interface with the communication board, to control the external radio and the corresponding long-range protocol. The external radio is a node in a long-range wireless network connected to the Internet. Such a long-range communication capability allows all the processes in the SBC to exchange signals, information and commands with other nodes on the wireless network or on the Internet.

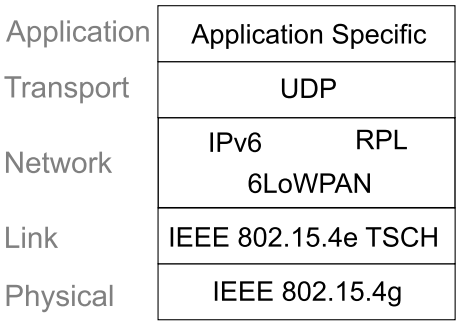

FIGURE 7. Communication protocol stack used in Process 4, based on the 6TiSCH and the IEEE 802.15.4g.

In order to provide such a robust communication platform, the external radio uses the 6TiSCH over IEEE 802.15.4g. While the IEEE 802.15.4g defines the lower layers to allow long-range communication, the 6TiSCH combines many protocols to enable the use of a mesh topology. Such a combined suite of protocols also brings IPv6 to low-capacity devices through technologies such as Neighbor Discovery, IP-in-IP encapsulation, header compression, and IEEE802.15.4 TSCH link layer, which is the root of the IETF 6TiSCH protocol suite [24]. It is also important to notice that 6TiSCH is used in important standards such as Wireless Smart Ubiquitous Network (Wi-SUN).

More specifically, in this work, we use the protocol stack defined by 6TiSCH while using the 802.15.4g protocol at the physical layer. As summarized in Fig. 7, from the lower to upper layers, the following protocols are utilized: the 802.15.4g is used at the physical layer, which is suitable for Smart Metering Utility Networks (SUN) where multiple nodes must operate over shared network resources; the TSCH mode of the 802.15.4e is used at the link layer, which combines the time-division multiple access (TDMA) for collision-free access while using channel hopping for robustness to deal with interference and multipath fading; at the network layer, it is used the IPv6 for standardization and robustness, the IPv6 over Low power Wireless Personal Area Networks (6LoWPAN) due to its compression mechanisms, and the Routing Protocol for Low-Power and Lossy Networks (RPL) which is suitable for networks with low power consumption; at the transport layer, the UDP is used due to its connectionless and lightweight characteristics; and an application specific protocol in the application layer. The application protocol used by Process 4 allows the transmission of unconfirmed and confirmed UDP packets in which the latter allows the automated retransmission in case of package loss. In this work, a mesh topology is used while also having a network root acting as a border router, which is achieved through the use of the RPL protocol. Such an approach allows the transmission of UDP packets to other agents and to external servers. From the results presented in [25], we have that hundreds of nodes are able to operate in a single 6TiSCH mesh network and that, using the standard parameters defined by the 6TiSCH for the slotframe length and duration [26], the latency increases by approximately 2 seconds per hop in the communication process. Furthermore, the maximum communication distance between nodes ranges from hundreds to a few thousand meters, depending on the communication scenario.

IV. QUANTITATIVE EVALUATIONS

In this section, we present evaluations of the proposed system to quantify its capabilities in terms of the quality of the digitized signals and latency of the sample acquisition, considering restrictions of algorithms and techniques required in power distribution systems. Section IV-A provides an analysis of the quality of the signals sampled by the DAQ and Section IV-B describes an evaluation of the latency from the input of the DAQ up to an application running at the SBC.

Specifically, the results presented in the following subsections show that the signals are sampled with low distortion and low latency. For example, regarding signal quality, we show that the signals present low distortion due to the conditioning and sampling circuitry, which is important to allow estimating parameters of the 50/60 Hz waveform with a minimum or negligible impact from the circuits. To provide a more practical view, there is a recommendation for harmonic distortions of up to 5% [27], while we show numbers in the order of 0.5% and 0.05% for signals with low and high amplitudes, respectively. We also show low latency in the signal acquisition. It is important to allow the detection of phenomena such as traveling waves [28], which require a measure to be taken with delay in the order of sub-millisecond after the fault happens.

A. SAMPLED SIGNAL QUALITY

To evaluate the quality of the signal acquisition with the proposed system, we connected outputs of an Arbitrary Waveform Generator (AWG) to three of the inputs of the proposed system. The input signals are clean phased sinusoids with a frequency of 60 Hz. The goal is to estimate the amount of noise and distortion added to the sampled signals in the conditioning chains. The input signals were generated with amplitudes of 1 mV, 10 mV, 100 mV, 1 V, 3.5 V, 3.8 V and 4 V. These signal amplitudes allow evaluation in low amplitudes, in which the noise in the conditioning chain is more evident, and in high amplitudes, in which characteristics, such as distortion, intermodulation, and harmonic distortions can be evaluated. The signals were sampled by the ADC, read by the MCU and forwarded to the SBC. In turn, the SBC packed the samples in UDP packets and sent them to a Matlab script running on a computer in the same network.

An analysis of the signals captured is shown in Fig. 8. Fig. 8a and Fig. 8c show the periods (256 samples) of the input signals overlapped. From each phase, a thousand periods (256×10^3 samples) were saved, and all the periods from each phase were plotted in Fig. 8 overlapped. The overlapped plot help to identify sample losses in the signal acquisition chain, which includes sampling by the ADC, processing by

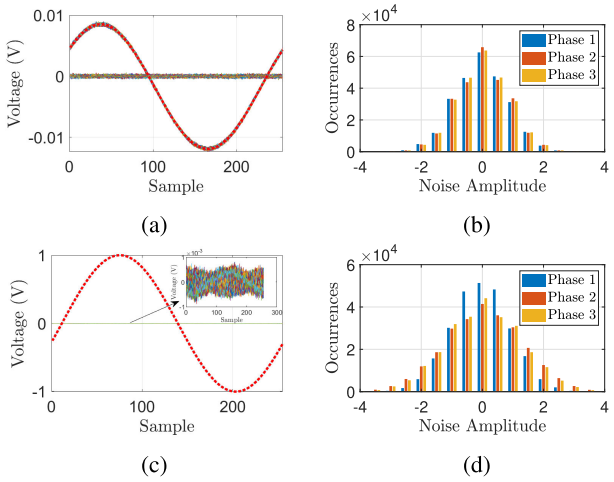

FIGURE 8. Overlapped periods of the sampled signals for all the phases for signals with 10 mV (a) and 1 V (c) of amplitude; and noise estimated from the overlapped signals for signals with 10 mV (b) and 1 V (d).

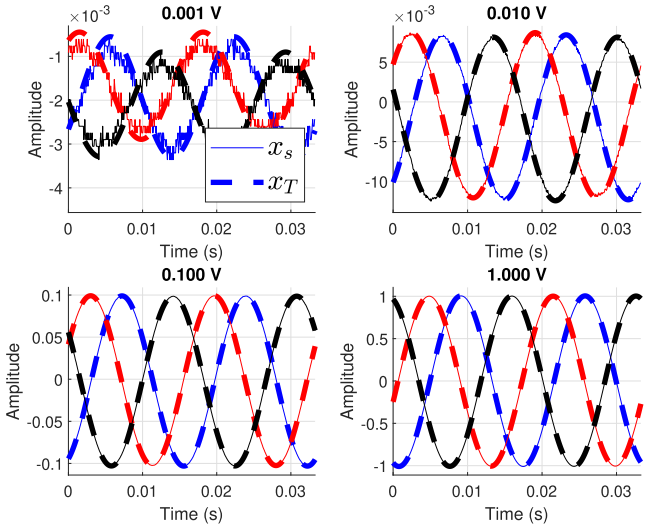

FIGURE 9. Comparison of the sampled signals with signals generated digitally with the same offset and amplitude.

the MCU and forwarding to the SBC, packet organization and dispatch to Matlab. In case samples are lost, the periods would eventually become unaligned, and the overlapped plot of Fig. 8a and Fig. 8c would no be possible. Therefore, it helps to show that there is no samples loss, as all the periods overlapped keep their alignment.

With the periods overlapped, it is possible to calculate the mean value of each position (sample index) of the period, which allows estimating the noise by subtracting it from the samples of the periods. The estimated noise samples are also shown in Fig. 8a and Fig. 8c as the lines that have values close to zero. Moreover, Fig. 8b and Fig. 8d show the distributions of the estimated noise for the 10 mV and 1 V inputs, respectively. The distributions are approximately Gaussian, with standard deviations of 1.29×10^{-4} for the signals with 10 mV of amplitude, and 1.94×10^{-4} for the signals with 1 V of amplitude. This small increase in the amplitude of noise samples is expected, as signals with higher amplitudes generate stronger distortions due to the non-linearities of the components in the conditioning chain. However, it is a small increase in noise amplitude when it is compared to the increase in the amplitude of the signal of interest, i.e., the sinusoidal signals. An increase of 100 times in the amplitude of the sinusoidal signals resulted in an increase by a factor of $1.94/1.29 \approx 1.5$ in the standard deviation of the noise.

A second evaluation consists of a comparison of the sampled signals with perfect sinusoidal signals generated synthetically. Hereinafter, the sampled signals are referred to as $x_s^R[n]$, $x_s^S[n]$ and $x_s^T[n]$, which represent the three phases. Similarly, $x_T^R[n]$, $x_T^S[n]$ and $x_T^T[n]$ are used to denote the signals generated digitally, in which T indicates the "true" signals. To generate $x_T^R[n]$, $x_T^S[n]$ and $x_T^T[n]$, we calculated the average values μ_s^R, μ_s^T and μ_s^T of $x_s^R[n]$, $x_s^S[n]$ and $x_s^T[n]$, respectively. Note that, in this evaluation we calculated the mean values with all the samples for each signal, while in the previous evaluation we calculated mean value of each position in the period. The mean values in this evaluation represent the DC offset added in the conditioning chain, as the output of the AWG is assumed to be perfectly generated. The mean value of the peaks P_s^R, P_s^T and P_s^T of $x_s^R[n]$, $x_s^S[n]$ and $x_s^T[n]$, respectively, were also calculated. Finally, we estimated the phase θ_s^R, θ_s^T and θ_s^T of the first sample of the input signals.

We generated x_T using the parameters previously estimated. Note that we dropped here R, S and T to simplify the notation. By using the parameters, the digital signals were generated as

$$x_T[n] = \mu_s + P_s \cos(2\pi 60\, nT_s + \theta_s). \tag{1}$$

The results of this signal generation is illustrated in Fig. 9, in which x_T and x_s are plotted together for four distinct input peak amplitudes, namely, 1 mV, 10 mV, 100 mV and 1 V. Fig. 9 shows x_T as dash lines and x_s as solid lines, and the colors red, blue and black represent each input chain, or equivalently a phase.

Figure 9 provides a visual insight of the sampling quality. Furthermore, to provide a better perspective of the quality of the sampled signals, a more accurate evaluation is required. By subtracting x_T and x_s it is possible to estimate the error each signal presents. Then, the error can be compared to the peak values P_s as reference to have a percent error calculation, i.e., $e_{\%} = 100 \times (x_T - x_s)/P_s$. Figure 10 shows the error estimated with this approach. This figure shows graphs with two vertical axes, with the amplitude of the signals of interest at the left-hand side, and the percent error at the right-hand side. For relatively small amplitude levels, e.g., 0.1 V, it presents errors in the order of 1%, and it is kept for higher amplitudes, as shown for 1 V and 3.5 V in Figure 10. Moreover, for very weak signals it can still present low error levels, as it is shown for signals with 10 mV of amplitude, which present error of up to 5%.

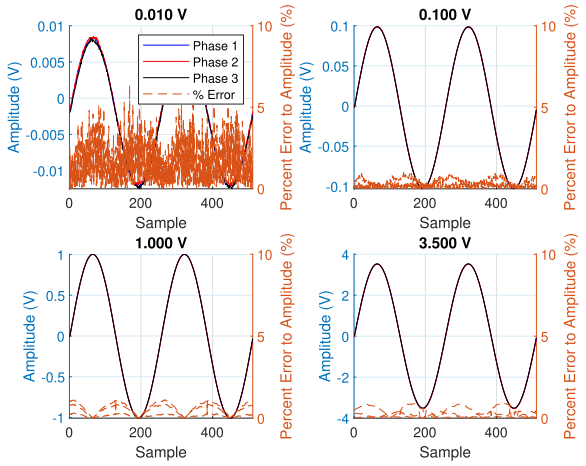

FIGURE 10. Error in relation to the peak amplitude.

A third evaluation considered the Individual Harmonic Distortion (IHD) and the THD, which is shown in Fig. 11. In this evaluation we considered the individual contribution from each harmonic in the sampled version of the input signals with frequency of 60 Hz for each x_s. The IHD is calculated as

$$\text{IHD}^k_{\%} = 100 \times \frac{|X_s[k]|}{|X_s[1]|}, \tag{2}$$

where X_s (upper case X) is the Discrete Fourier Transform (DFT) of x_s, k is the index of the k-th harmonic. The THD is calculated as

$$\text{THD}_{\%} = 100 \times \frac{\sqrt{\sum_k |X_s[k]|^2}}{|X_s[1]|}. \tag{3}$$

By evaluating each harmonic up to the $k = 40$-th, we found all IHD values below 1%, with decreasing contribution as the frequency of the harmonic increases. The $k = 40$-th is equivalent to a frequency of 2400 Hz, which is within the passband of the anti-aliasing filter of the conditioning chains. By analyzing the magnitude of each harmonic, we found the mean values of 2.65 μV and 21.93 μV for the input signals with amplitude of 10 mV and 1 V, respectively. In other words, with an increase factor of 100 in the input signal, we have an average increase in the amplitude of the harmonics by a factor of 10. Therefore, it results in smaller THD of signals with greater amplitudes. For the same input signals we analyzed before, i.e., signals with 10 mV and 1 V of amplitude, we calculated a THD of about 0.5% and 0.05%, respectively.

The IHD for frequencies up to 960 Hz is shown in Fig. 11a and Fig. 11b for each sampled signal. These bar graphs are produced for each input signal and for each harmonic, and are limited to 960 Hz to allow better visualization. Notwithstanding, for higher-order harmonics, the decreasing behavior is kept. Fig. 11a and Fig. 11b also exhibit a summary of the THD in their upper right corner. In both cases, the THD is

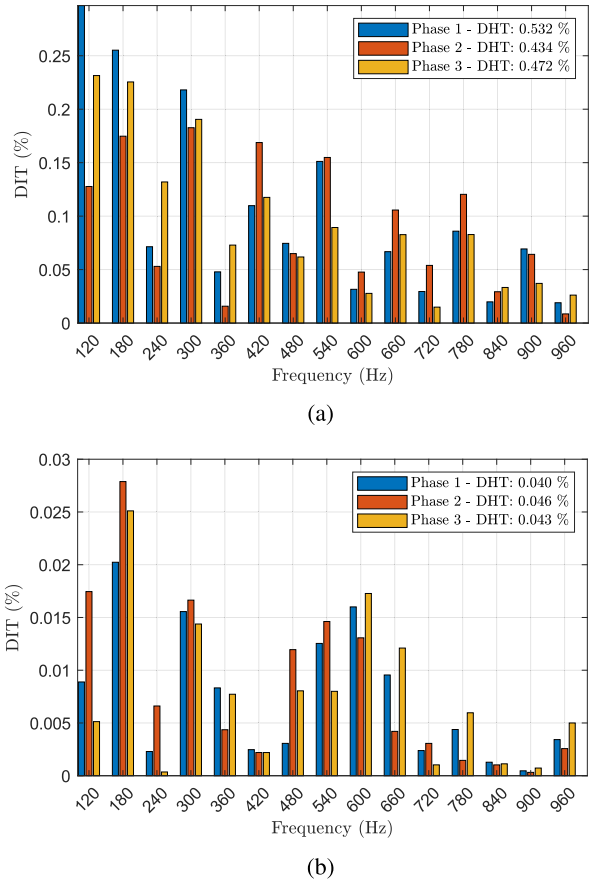

FIGURE 11. Harmonic distortion estimation for input signals with 10 mV (a) and 1V (b) of amplitude.

estimated as less than 1%, considering frequencies up to the $k = 40$-th harmonic (which are not shown on the graphs).

B. DAQ INPUT TO APPLICATION LATENCY

In several application it may be needed to detect fast events, such as impulsive noise and others random quick events. Thus, it is desirable for a DAQ system to have a low latency in the path of analog signal, as well as a quick response in its software. Therefore, in this section we present an assessment of the response time of the developed system.

In summary, in this test we generated a logic high output signal with one of the GPIOs of the SBC, and simultaneously sampled the timestamp of the SBC. The GPIO output was fed to one of the inputs of the signal conditioning chain. The path traveled by the signal in the setup of this test is shown in Fig. 12. The path is composed of the signal conditioning chain, the ADC, the MCU and the SBC.

In the SBC, the samples are stored in the UART buffer until read by the hardware interface software (Process 1), which was slightly modified to generate a periodic pulse, get the timestamp t_1 on the rise edge of the output signal and capture a second timestamp t_2 on the rising edge of the sampled signal. Then, the estimated latency is measured as $L = t_2 - t_1$ and the process is repeated many times to acquire

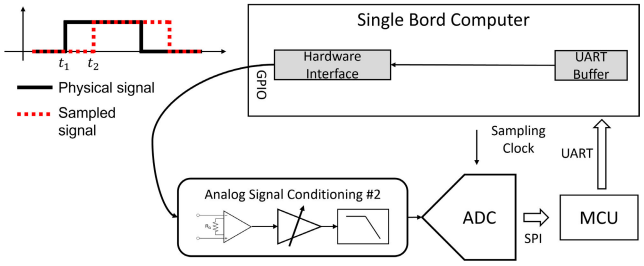

FIGURE 12. Hardware and software setup to measure latency of the conditioning chain in the MCU and SBC.

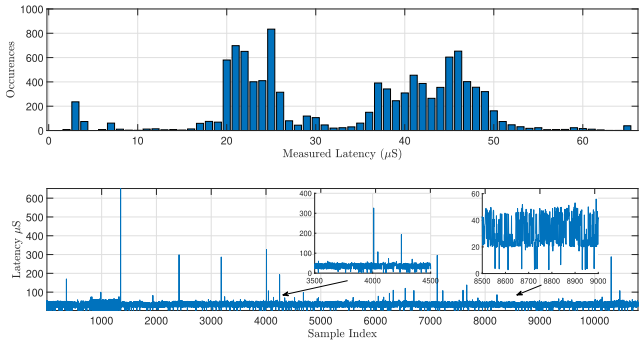

FIGURE 13. Measured latency of analog system plus hardware interface (bottom) and its histogram (top).

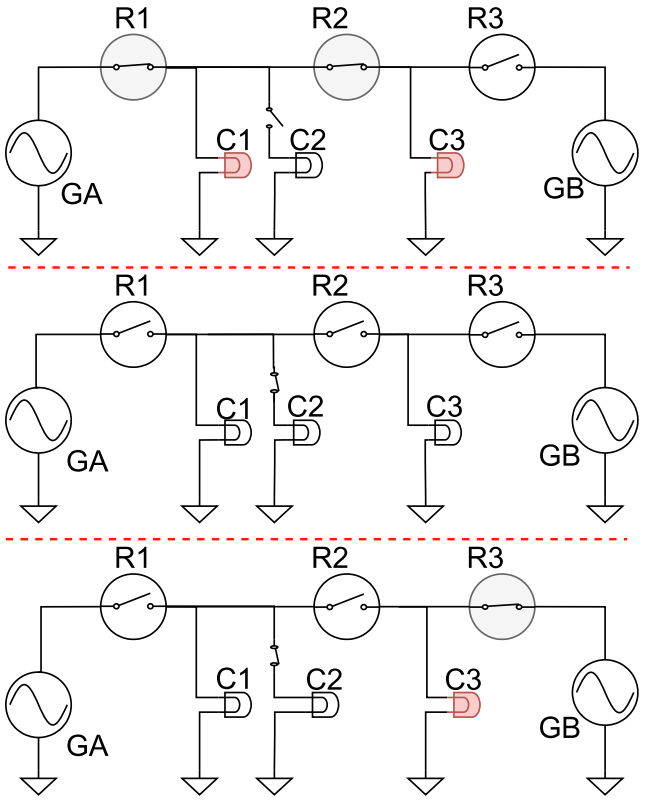

FIGURE 14. Illustration of restoration steps performed in three consecutive stages, namely, normal (top), fault isolation (middle), partially restored conditions (bottom).

multiple estimations of the latency. Process 1 was developed in C, and we used the clock_gettime function from the time.h header file with the parameter CLOCK_MONOTONIC. This way, it allows measuring the latency with improved accuracy.

Fig 13 shows the results of the measurements made with the setup described. In the top, we show the histogram of estimated latency and in the bottom plot we provide the measured latency for each realization. Most of them is below 65 μs (less than one sampling period 1/15360). The number of occurrences above 65 μs is only 38 out of 10790 (0.35%). These outliers are due to eventual interruptions the processor may face, as there are several software running simultaneously in the Linux environment. The worst case latency is less than 700 μs. It is worth to mention that there is no loss of samples in that case because the digital samples are stored on the UART buffer and processed later.

V. EVALUATION OF A RESTORATION PROCEDURE WITH SMART RECLOSERS

In this section we present an evaluation setup that has been built to assess the capability of the proposed system to test restoration procedures for power distribution systems. Figure 14 shows the setup, which is composed of three reclosers, R1, R2 and R3, three loads C1, C2 and C3, and two power sources, GA and GB. The reclosers are controlled by the proposed embedded system and have the capability of connecting/disconnecting two branches of the network through a controllable power switch and circuit breaker. The reclosers can, for instance, detect the presence/absence of voltage in a terminal branch and measure the current through its switching element, so, it can take actions in case of overcurrent events related to fault conditions.

Figure 14 shows the evaluation setup in a sequence of three different situations, namely, a normal condition shown at the top, a fault isolation condition shown at the middle, and a partially restored condition shown at the bottom. In the normal condition, reclosers R1 and R2 are responsible for managing the network block/section covering C1 and C3, respectively. Reclosers are constantly monitoring the circuit current to detect fault conditions, which must be cleared to protect the network equipment. In case of a fault event, simulated through the connection of load C2 by closing the switch near C2, the sensed current in R1 is higher than the configured threshold, causing the opening of the switching element of R1 to protect the system.

After this protection scheme, the agents running within reclosers R1, R2 and R3 update their states. As R1 opened its switch to protect the system, it informs this condition to R2. Knowing its upstream network section is in a faulted condition, R2 keeps its switch opened and locked to isolate the faulted section. Once the faulted section is isolated, R3 can cooperate with the others to support the restoration procedure. R3 is informed about the states of R1 and R2, as well as about the fact that the fault is isolated. Moreover, R3 receives from R1 a call for help. Since the faulted section is isolated and

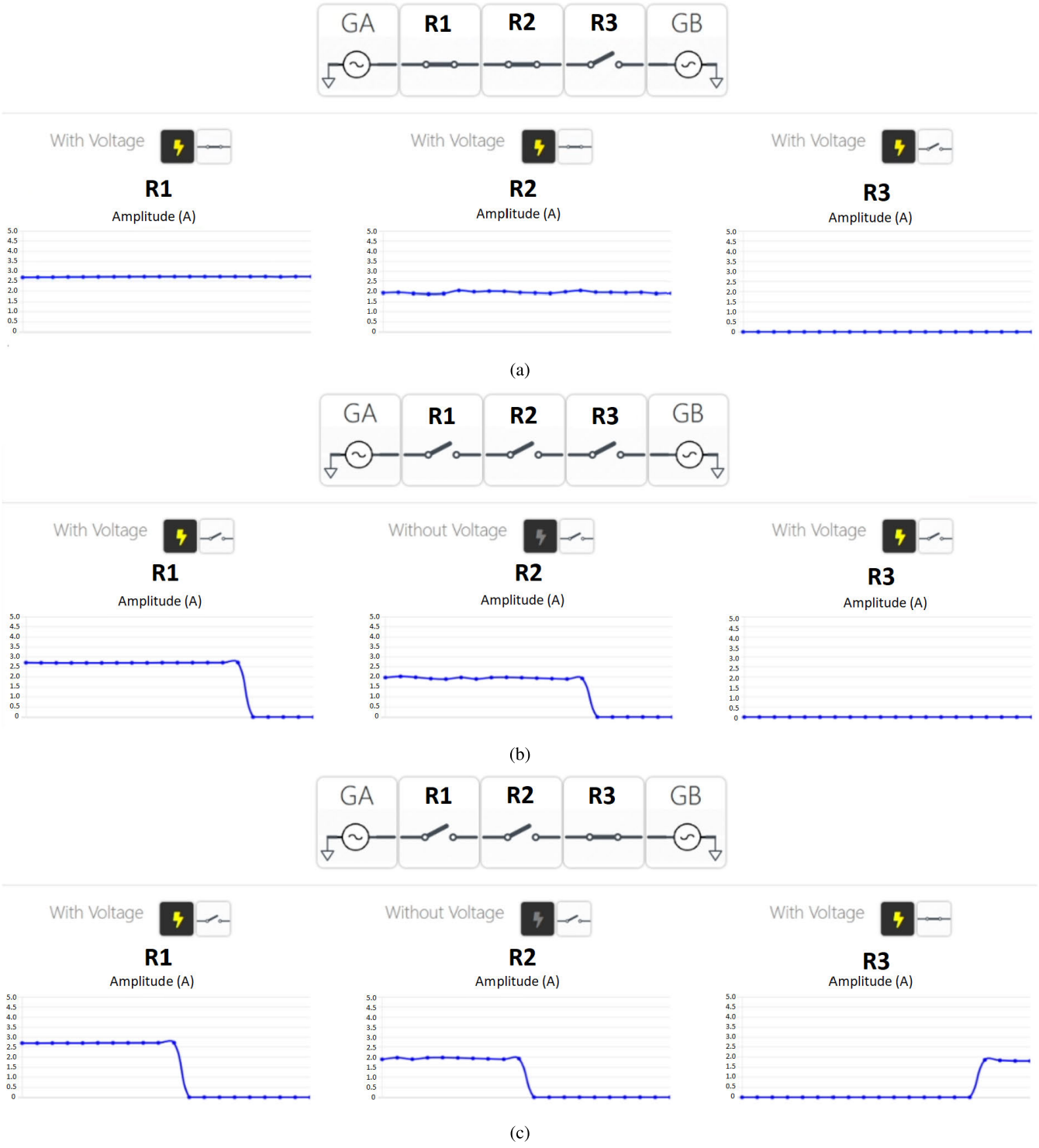

FIGURE 15. Screen captures of the dashboard implemented to the evaluation in the normal operation (a), the overload (b), and the temporary configuration (c) to restore the service to some customers.

it is known that GB has available capacity to supply C3, the switching element of R3 can be safely closed to restore the energy service to C3. This leads to the third situation, in which the faulted section is isolated and the service has been restored to part of the customers.

The actions assessed in this section were taken by Process 1 and Process 3 of Figure 1. The overcurrent was detected by Process 1 of R1, which readily opened its switch. The instances of Process 3 running in R1, R2 and R3 were informed about this decision. Process 3 in R1, which it is

more closely connected to where the decision has been taken, is firstly informed, followed by the other agents (instances of Process 3 in R2 and R3). All the actions were taken autonomously, i.e., without a central node monitoring the reclosers.

In practice, a central node would also be notified. For that, we implemented a web server that is also notified of the reclosers state. Moreover, this web server is also constantly querying the currents of the reclosers, which can be viewed by a client browser as a dashboard. Figure 15 shows screen captures of the dashboard in the three situations presented in Figure 14. Figure 15a shows the states of the switches in the normal condition, in which R1 and R2 are with their switches closed, and R3 with its switch open. Figure 15a shows the measured currents in R1 as approximately 2.5 A and in R2 as 2 A. Figure 15b shows all the switches open due to the fault condition, as well as the current levels in R1 and R2 falling to 0 A, illustrating the instant when R1 opened its switch. Figure 15c shows the partially restored condition, where the current level in C3 is increased, as R3 closed its switch.

VI. CONCLUSION

This paper presented an evaluation of an embedded system devoted to monitoring and handling faults in power distribution systems. We considered the concept of multi-agent systems (MAS) is deployed in this context, which is evaluated in some recent works. MAS are capable of handling problems by taking autonomous actions or by interacting with other agents. Thus, they could be able to locate and isolate faults in power distribution systems more effectively. However, several aspects of the real-world need to be evaluated before putting such innovative concepts in production plants.

In this context, the main contribution of this paper is the proposal of a novel hardware and software approach to monitor signals in real-time, which is part of the features needed to implement MAS in power distribution systems. The paper described the development of the SBC-based DAQ embedded system used in the evaluations, which has the capability of communicating in a long-range with the 6TiSCH over IEEE 802.15.4g technology. The target application is to test multi-agent restoration procedures based on smart reclosers, benefiting by the integration of a SBC and a DAQ, achieving real-time and low-latency sampling of electrical waveforms as well as computational capability to perform calculations in real-time. Moreover, the adopted SBC is the off-the-shelf Raspberry Pi 3b+, which is compatible with Linux and allows reusing several available applications and protocols. It can lead to smaller development times. We presented in-depth details regarding its development, comprising the hardware development, the low-level software, which interfaces to the hardware, and details of the high-level applications running at the SBC. We also discussed the approaches integrated into the hardware and software to allow the synergy between the general-purpose Linux OS and the real-time processing with very low sample loss.

The embedded system has been evaluated in terms of the quality of the sampled signals and latency. For the quality of the signals, we considered the error from the sampled waveform in relation to another synthetic perfect waveform. In this evaluation, we showed errors in the order of 1%. In another evaluation, we presented the THD generated in the conditioning and sampling circuitry, which is in the range of 0.5% and 0.05%, depending on the amplitude of the input signal. These values of THD are much smaller than the recommended upper bound of 5% of the 50/60 Hz waveform, which indicates the THD of the circuits will not impact the measurement of this parameter in the signal of interest. In the evaluations, it is also included an evaluation of the latency of the circuitry, which should be as low as possible, preferably in the order of sub-milliseconds to allow detecting and analyzing phenomena that happen in case of a fault, such as traveling waves. The paper also presented an example application of an Agent-based restoration procedures for power distribution systems are tested, illustrating the applicability of the proposed embedded system to autonomously handle faults, communicate their actions to other agents, and cooperatively restore service to the higher number of clients as possible.

An open topic for investigation is deploying the developed embedded system in a real or realistic plant. This deployment requires adoption of current and/or voltage converters to drop voltage levels from transmission line to the range of −5 V to 5 V. Furthermore, it requires emulation of distinct types of faults. With such a setup it is possible to investigate algorithms and techniques to detect, classify, and extract parameter and insights to help improving the quality of service or automatic fault handling with the agents. Another future research direction is related to investigate the performance of other SBCs or platforms, such as FPGAs, as real time data acquisition system, including the ones that have programmable real-time unit integrated on the SoC, in order to process the real time events of the ADC. An improved platform could have, for example, GPS for synchronized sampling, as it was evaluated in related works. In these future investigations, it is possible to evaluate and propose optimizations in relation to power consumption, sleep states, cost of different platforms, and other evaluations. Investigations with different platforms is already possible due to the modular construction of the proposed system, which allow changing the Raspberry Pi by other electrically compatible one.

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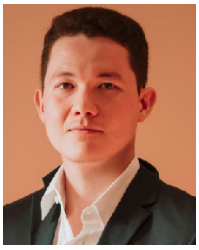

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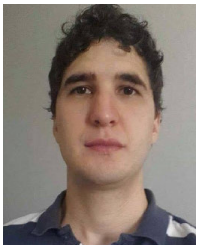

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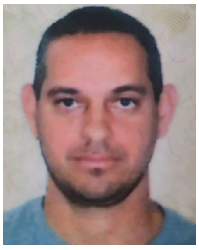

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