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RESEARCH ARTICLE

Effective Current-Driven Memory Operations for Low-Power ReRAM Applications

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ABSTRACT Resistive switching (RS) devices are electronic components which exhibit a resistive state that can be adjusted to different nonvolatile levels via electrical stressing, fueling the development of future resistive memories (ReRAM) and enabling innovative solutions for several applications. Most works so far have used voltage-based driving schemes for both WRITE and READ operations. However, results from current-driven WRITE operations have shown high uniformity in switching performance, and thus constitute a valid alternative to consider, but current-driven READ operations have rarely been explored. In this context, here we tested a current-based READ/WRITE memory driving scheme on commercial self-directed channel (SDC) devices, while operating constantly at low current levels between tenths of nA and 1.5 uA. We propose a novel method to carry out efficient READ operations exploiting the transient response of the voltage on the current-driven ReRAM memory cells. For READ operations performed at 100 nA, we calculated the cumulative probability distribution of the standard deviation of the measured voltage (σ_V) on the devices and we observed a ratio $\sigma_{V-HRS}/\sigma_{V-LRS} \sim 10\times$. Moreover, the HRS and LRS states were distinguishable in all the tested devices with less than 0.5% error. Finally, the calculated energy consumption ($E_{SET} \approx 10$ nJ, $E_{RESET} \approx 30$ nJ, and E_{READ} between 80-400 pJ) was competitive even when the duration of the READ/WRITE current pulses was suboptimal in the millisecond range. Therefore, the presented results validate the promising characteristics and the power-efficiency of the proposed READ method for current-driven ReRAM circuits and applications.

INDEX TERMS Current driver, electrochemical metallization memory, knowm, memristor, resistive RAM (ReRAM), resistive switching, self-directed channel memristors, voltage-controlled current source.

I. INTRODUCTION

During the last two decades, within a constant quest for novel and low-power solutions in the non-volatile memory regime, among different emerging technologies, the resistive switching (RS) device technology has been actively explored [1]. RS devices are also termed memristors and/or memristive devices ever since such RS behavior was linked to the theory of the fourth fundamental circuit element posed by Leon Chua in the early '70s [2].

Different terminologies have been frequently used within the research community to denote resistive memory devices, commonly known as resistive random-access memory (ReRAM). One of the most recognized classifications is based on the underlying working principle [3]. As far as redox-based devices are concerned, there are two main types, namely the metal-ion (M-ion) based devices, generally known as electrochemical metallization memories (ECM),

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and the valence change memories (VCMs) [4], [5]. Among the ECM devices we find the conductive bridge RAM (CBRAM) and the self-directed channel (SDC) devices [6]. Both CBRAM and SDC devices typically use chalcogenide materials as the active layer and an easily oxidizable metal (e.g. Cu or Ag) to change the device conductivity. However, among several other differences, the CBRAM devices change their resistance through the formation and dissolution of a conductive filament [7]. On the other hand, the SDC devices use a metal-catalyzed reaction within the active layer to generate conductive channels that contain Ag agglomeration sites. Such Ag ion transport routes are channels with varying concentrations of Ag at the Ag agglomeration sites. So, the device resistance depends on the concentration of Ag at a given agglomeration site, and the distance between the agglomeration sites [6].

Several companies around the world [8], [9] are pushing forward the ReRAM nanofabrication and the commercialization of innovative products, targeting advanced (neuromorphic [10]) computation and hardware security applications [11], [12]. ReRAM devices exhibit a resistive state that can be adjusted to several nonvolatile levels via electrical stressing [13]. In ReRAM arrays, the data stored in memory cells are represented by resistance; logic '0' by a high resistive state (HRS) and logic '1' by a low resistive state (LRS), or vice versa. In case of bipolar ReRAM devices, one voltage polarity is required to switch the device from HRS to LRS (SET process), and the opposite polarity is required to change the device from LRS to HRS (RESET process) [14].

Standard WRITE/READ operations in ReRAM memories have been normally performed using voltage-based schemes [15], [16]. For instance, a single voltage pulse of a fixed duration is used for the WRITE operations (SET and RESET). One of the main issues with fixed voltage pulse input is the behavioral variability [17], [18]. ReRAM devices suffer from intrinsic temporal (cycle-to-cycle) variations that are attributed to the stochastic nature of the resistive switching phenomenon and result in wide distributions of HRS and LRS values. Further issues with such driving technique involve the control over the flowing current through the device and the excessive energy consumption as the current keeps flowing while the voltage across it is kept still even after the switching has already occurred [19], [20]. Additionally, in memory READ operations the current can also be relatively high for devices that reach very low LRS values.

In this context, progressive feedback-WRITE schemes have been proposed which use READ and WRITE pulses in an alternate fashion to periodically verify that switching has occurred [21], [22], and present a time-accuracy tradeoff. Optimized WRITE voltage pulse shapes have been used in [23] to minimize the current overshoot in voltage-based memory operations and thus to improve the endurance and the variability of the devices, whereas current limitation (current compliance) has been used basically for device protection and for multi-level resistance tuning through controlled SET operations [24]. Analog applications exploit such progressive conductance increase, achieved with increasing the compliance current level, as in the case of synaptic electronics [25]. The dilemma of whether voltage driving or current driving is more suitable for RS devices still holds today [26]. Only few works have explored driving schemes based exclusively on current pulse inputs, probably because direct current injection, unless fine-controlled, could potentially be a source of irreversible damage for RS devices, like in the case of nanowires which can suffer damages by undesired current fluctuations [27].

Nevertheless, results on RS device characterization, originating from current-driven instead of voltage-driven methodologies [28], [29], have revealed promising performance characteristics for the devices under test [30]. More specifically, results in [31] demonstrate that current is the dominant driving force for RESET operations and that the switching event is significant only above a certain current threshold. Also, authors in [26] compared the performance of $Cu/HfO_2/Pt$ devices using current and voltage sweeping. Better uniformity and a higher HRS-to-LRS resistance window were achieved with current sweeping. In search of effective approaches to control the switching behavior and to minimize the variation of critical switching parameters, authors in [32] observed abrupt SET but gradual RESET while using voltage signals, whereas gradual SET and sharp RESET was achieved with current pulses. Likewise, authors in [33] observed a reliable control of the LRS resistance through gradual current sweeping on TaO_x-based devices. Furthermore, the possibility to control intermediate conductance levels in HfO_2-based devices was explored in [28] using current pulses. Results showed that, unlike voltage pulses, the consecutive current pulses do not produce an accumulative response in the device resistance, and that gradual RESET cannot be obtained. In addition, novel topologies for dynamic and strict control of both WRITE and READ currents have been recently proposed towards more energy efficient ReRAM circuit architectures [34].

Following such recent trends in current-based ReRAM operation, in this work we analyzed the performance of ReRAM devices under both READ and WRITE operations using a very low current-based scheme. For this reason, unlike other custom circuits for current control [28], here we used a circuit which makes possible the fine control of currents ranging between tenths of nA and 1.5 uA [29], [35]. This circuit was successfully used in the past for current-based characterization of nanowires [36], [37], [38] where stable current pulses in the pico-/nano-ampere range were required.

More specifically, our measurements were performed on bipolar SDC devices, commercialized by *Knowm Inc*. [39], [40]. Since the switching response of ReRAM devices depends on the recent history of applied stimuli, instead of applying alternating SET and RESET pulses, we rather used a sequence of current pulses whose amplitude varied randomly within the full current scale, to assess

whether the switching performance of the devices remained coherent. The results demonstrated a stable switching behavior at such low current levels of operation, revealing levels of current that could serve exclusively for READ operations. In this direction, a statistical analysis on the time-evolution of the measured voltage on the current-driven devices led us to devise a novel method to carry out efficient and low-power current-based READ operations. For READ operations performed at 100 nA, we calculated the cumulative probability distribution of the standard deviation of the measured voltage (σ_V), and observed a ratio $\sigma_{V-HRS}/\sigma_{V-LRS} \sim 10\times$. Using the proposed method, the HRS and LRS states were distinguishable with less than 0.5% error performance in all the tested devices. Moreover, we integrated the instantaneous power on the devices over time (without considering the consumption in the driving circuitry) and calculated the energy consumption as low as: $E_{SET} \approx 10$ nJ, $E_{RESET} \approx 30$ nJ, and E_{READ} between 80-400 pJ, which is competitive even though the applied current pulse duration was suboptimal in the millisecond range. Therefore, regarding the dilemma of whether voltage driving or current driving is more suitable for RS devices, our results demonstrate that the current-based driving approach emerges as a feasible solution, not only to comply with low energy consumption requirements in ReRAM applications, but also to allow for unconventional READ methods for binary information encoded in HRS and LRS resistance values.

The rest of the paper is organized as follows: Section II describes the experimental setup and the RS devices under test. Section III presents results from the forming and cycling SET-RESET performance of the devices under periodic stimuli. Section IV analyzes the switching performance under nonperiodic current pulse input, whose results lead to the formulation of a novel current-based READ method, presented, and verified in Section V. Finally, Section VI presents the analysis of the current-based driving approach from an energy-consumption point of view, and Section VII concludes this work.

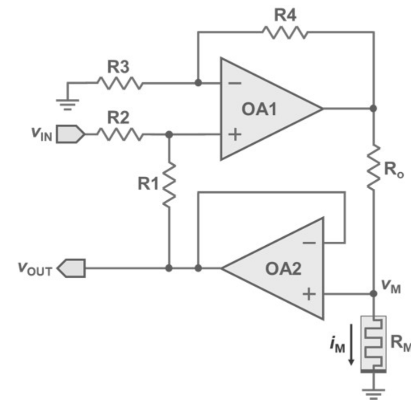
II. MATERIALS AND METHODS

A. EQUIPMENT

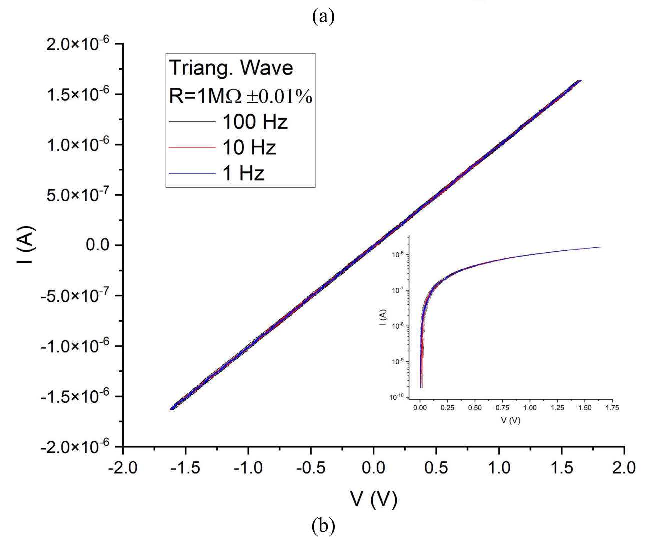
For the current-driven characterization of RS devices we used a custom circuit of a voltage-controlled current source, shown in Fig. 1(a). It consists of two operational amplifiers: the OA_1 in summing amplifier configuration and OA_2 as voltage follower, ensuring a constant current through the device under test, while allowing to monitor the voltage at its terminals $V_M = V_{OUT}$. The current I_M depends on the control voltage V_{IN}, on the ratio of the resistors R_2/R_1 and on the value of resistor R_o, as described in 1.

$$I_M = V_{IN}/[R_0(R_2/R_1)] \tag{1}$$

When the resistance R_M of the RS device changes dynamically, so does the output voltage V_{OUT}, and such change is reflected in the noninverting input of OA_1 which reacts in a way to maintain a stable current I_M independent of R_M.



(a)



(b)

FIGURE 1. (a) Schematic of the custom circuit of a voltage-controlled current source. R_M represents the RS device under test (DUT). Adapted from [29]. (b) Plot showing the current through a 1 MΩ resistor with tolerance ±0.01%, used as DUT, while varying the control voltage at different frequencies up to 100 Hz. The inset shows a semi-log plot of the first quadrant ($i > 0$, $v > 0$) of the main figure.

To this end, the following equation must hold: $R_1R_3 - R_2R_4 = 0$, so the values of the resistors in our circuit implementation were selected as $R_1 = 3.3$ kΩ, $R_2 = 33$ kΩ, $R_3 = 3$ kΩ, $R_4 = 300$ Ω and $R_o = 303$ kΩ, to make possible the fine control of low levels of current from tenths of nA up to 1.5 uA. Different combinations of resistor values can be used according to this relation. High resistor values should be avoided since they could affect the performance of the circuit. Note also that, unless this relation holds, then for different R_M values, the current will vary, which is not desirable. Considering a 1% tolerance for the resistor values, we simulated in LTSpice the worst-case scenarios that maximize the difference between R_1R_3 and R_2R_4. The results showed that the output current varied only by 1.5% from the expected value, which demonstrates the robustness of the proposed topology in finely controlling the current through the device under test.

We implemented the circuit in a printed circuit board (PCB) with ±9 V supply voltage. We used the OP482 operational amplifiers due to their high speed, high slew rate,

and low input bias current and voltage. The generation of the V_{IN} control signal and the measurements of the V_{OUT} voltage were carried out using the function generator and the digital oscilloscope of the Digilent ADP3450 instrument. All the measurements were computer-controlled and were carried out at room temperature, considering natural variation of laboratory conditions. Variability was properly accounted for in our experiments by repeating the measurements on different devices of the same technology. The circuit was calibrated using a stable 1 MΩ Caddock USF340 resistor with ±0.01% tolerance and 5 ppm/°C temperature coefficient. Circuit response for V_{IN} frequencies up to 100 Hz is shown in Fig. 1(b).

B. RESISTIVE SWITCHING DEVICES UNDER TEST

The devices under test were BS-AF-W discrete self-directed-channel (SDC) bipolar resistive switching (RS) devices with tungsten (W) as dopant on a chalcogenide material [6], [39] developed and commercialized in 16-pin ceramic DIP packages by *Knowm Inc*. [40]. Such SDC devices constitute an ion-conducting device type, a sub-class of electrochemical metallization (ECM) devices which, in response to an applied voltage, uses a metal-catalyzed reaction within the device active layer to generate conductive channels (Ag ion transport routes) that contain Ag agglomeration sites, permanent under similar operating conditions. SDC devices are distinct from Conductive Bridge RAM (CBRAM) technology and represent their own class of metal-ion RS devices.

III. DEVICE PREPARATION: CURRENT-BASED FORMING AND SET-RESET CYCLING

A key aspect in ReRAM device operation is the initial stressing of the device, in which it transitions from a pristine to an operational state. This process is commonly referred to as ''electroforming'' or ''forming'' and can affect fundamental parameters such as the SET-RESET cycling repeatability and multi-level switching response of the devices [41]. Therefore, different methods to carry out this task have been explored [14], [42], [43]. In voltage-based experimental setups, forming is typically carried out using a voltage ramp that might reach much higher voltages than the nominal operating voltages for SET/RESET. Thus, a compliance current is set-up for device protection. However, with a current-based ReRAM driver, the forming stage is not a complex process, as we demonstrate next.

The pristine SDC RS devices where directly submitted to a sequence of positive current pulses of Gaussian shape [44] with +1.5 uA amplitude and full width half maximum (FWHM) of 10 ms. By observing the results shown in Fig. 2(a) we notice that within the very first few cycles the conductive channel was formed with a resulting gradual decrease in the measured voltage drop on the device. Afterwards, any further applied current pulses do not show an accumulative behavior, as confirmed in the current-voltage (i-v) representation of the data in Fig. 2(b),where the curves overlap after the device has reached a certain resistive value

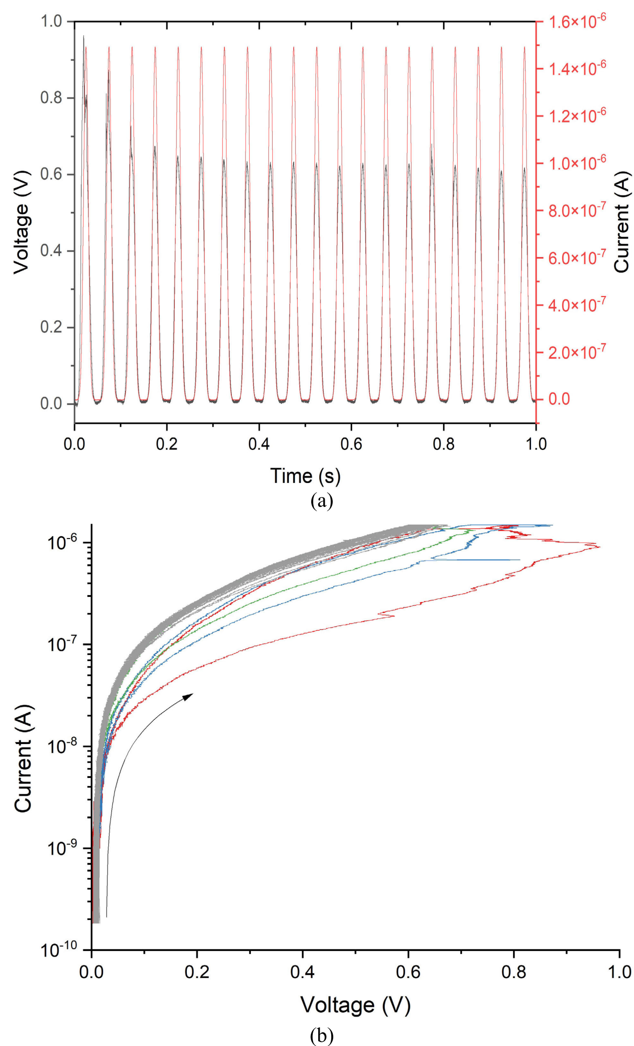


FIGURE 2. (a) A sequence of 20 current pulses of Gaussian shape (red curve) with a FWHM of 10 ms and +1.5 uA amplitude, along with the measured voltage response on the device (black curve). (b) Current-voltage (i-v) plot of the data in (a). The voltage responses for the 1st, 2nd and 3rd current pulse are highlighted in red, blue, and green color, respectively. The voltage responses for the remaining current pulses are all shown in light gray color.

and it does not become more conductive with the subsequent current pulses. Such results are in accordance with relevant observations in [28]. Therefore, a current-driven characterization strategy for RS devices practically eliminates the risks and complexity of the forming process. Particularly for the SDC devices, the incorporation of Ag ions into the chalcogenide Ge_2Se_3 layer during the first forming attempt, generates permanent conductive channels that contain Ag agglomeration sites and the amount of Ag within the channels determines the resistance of the device.

Next, the devices were submitted to a sequence of 1000 SET-RESET cycles using pulses of Gaussian shape, ±1.5 uA amplitude and a FWHM of 10 ms. The results in Fig. 3(a) correspond to the time-evolution of the applied current and the measured output voltage, whereas in

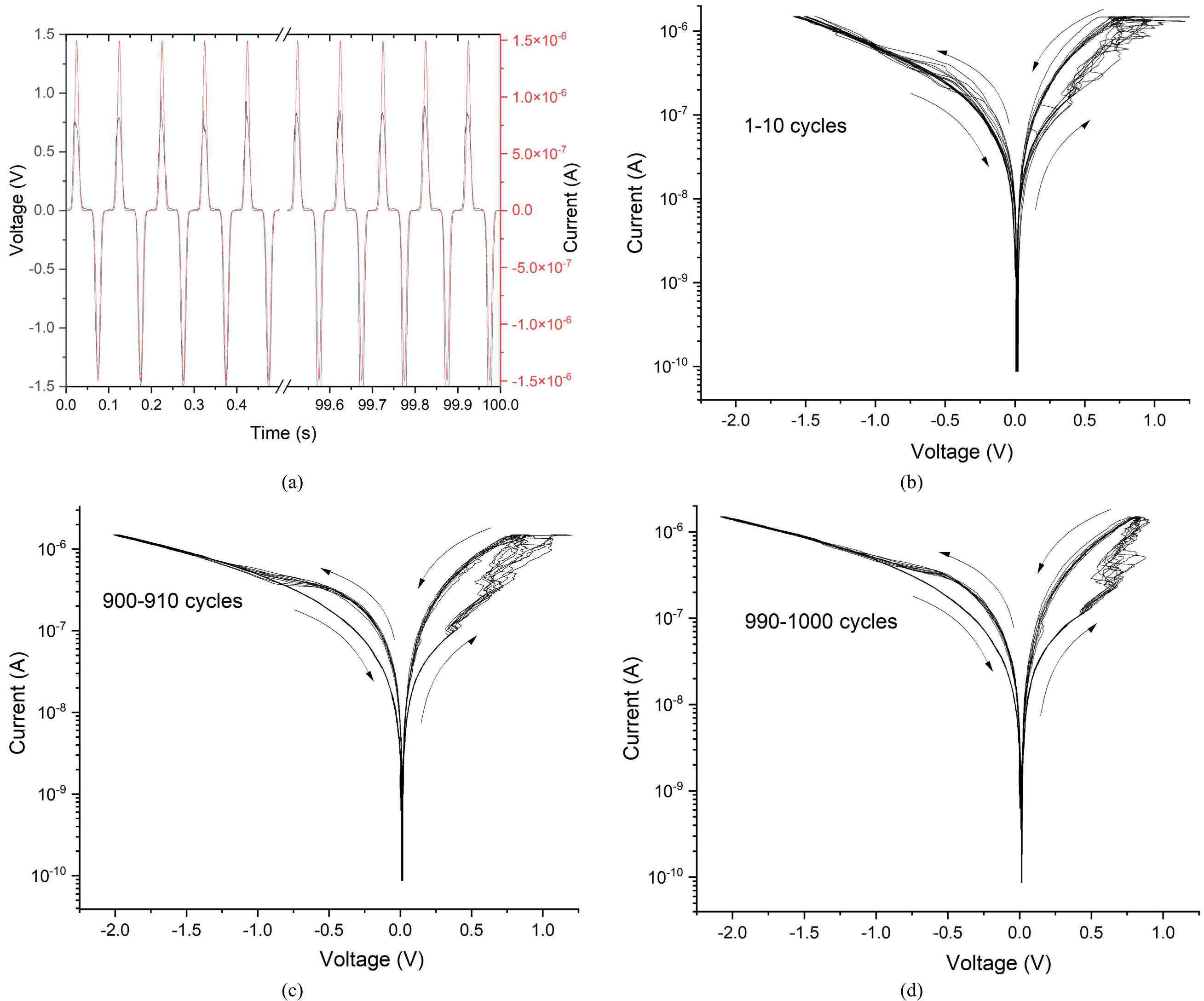


FIGURE 3. (a) Part of a sequence of 1000 SET-RESET cycles using current pulses of Gaussian shape and ±1.5 uA amplitude (red curve) with the voltage response on the device (black curve). (b)-(d) The semi-log representation of the "absolute current" – "voltage" data shown in (a) for different parts of the pulse sequence, as specified in the legend of every figure.

Fig. 3(b)-(d) we see the *i*-*v* characteristic for a certain number of cycles at different moments of the experiment. The resistive levels are in accordance with the device´s manufacturer information for WRITE operations with current levels in the microampere (uA) range. We observe a higher variability during the first cycles which later decreases progressively towards a stable cycling performance, as shown in the *i*-*v* characteristic for the last switching cycles in Fig. 3(d). Temporal variability is an important issue since it can affect the Bit Error Ratio (BER) metric in ReRAM modules; i.e., the percentage of unsuccessful WRITE operations out of the total amount of memory WRITE events, as defined in [45].

A closer look at the switching characteristics of the devices tells us that the assessment of the output voltage to perform READ operations to distinguish HRS from LRS levels (V_{LRS} and V_{HRS} output values), could be done at low input currents in the range of a few hundreds of nA. For 100 nA positive current the output voltage window is larger than 200 mV after 900 SET-RESET cycles. Thus, besides operating at low current levels and in the presence of variability, the results demonstrate a gradually achieved stable and repeatable cycling behavior, which complies with the desired RS performance for memory applications.

IV. CYCLING PERFORMANCE UNDER NONPERIODIC INPUT CURRENT PULSES

Once stable cycling performance was verified, the devices were tested in typical memory cell driving conditions using rectangular current pulses. It is common in the literature to find analyses of cycling behavior for applied input signals that consist of periodic SET-RESET sequences. Such a process applies also for the characterization of endurance

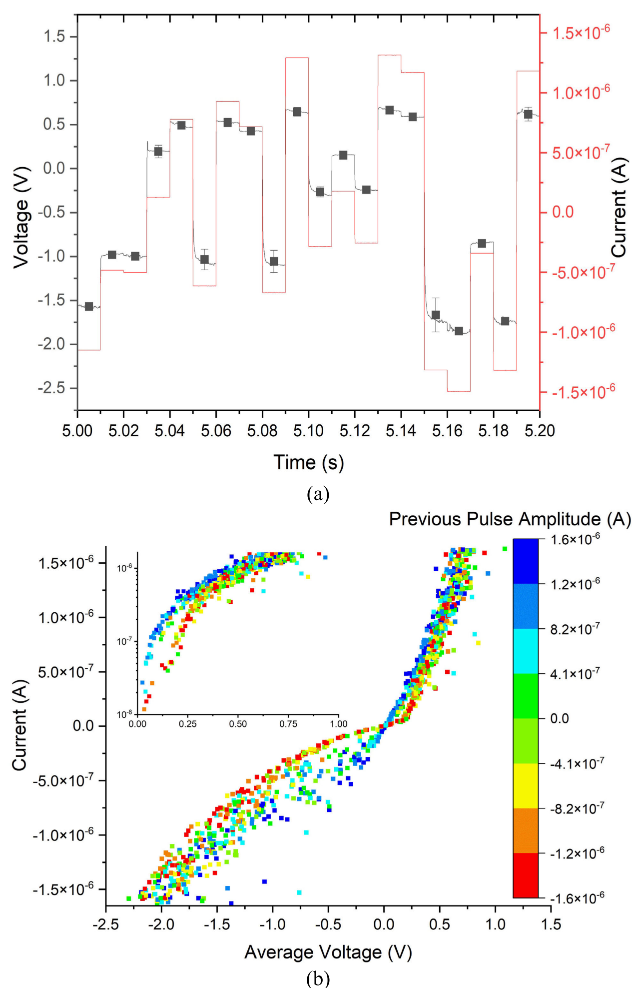


FIGURE 4. (a). Part of sequence of one thousand 10-ms wide current pulses (red curve) using randomly selected amplitudes within the full scale of ±1.5 uA. Mean values and standard deviation (SD) of the output voltage (black curve) for each pulse is depicted through solid squares and error bars, respectively. (b) The average voltage for every current value of (a) is shown in the *i-v* plane. The inset shows a semi-log plot of the first quadrant (*i* >0, *v* >0) of the main figure. Color code stands for the current amplitude of the pulse that was applied immediately before the last pulse.

of ReRAM devices [46]. However, since the switching response of ReRAM devices depends on the recent history of applied stimuli, in our analysis we rather employed a random sequence of input current pulses using amplitudes within the full current scale of ±1.5 uA, to assess whether the switching performance remained coherent. We present in Fig. 4(a) a timestamp of the experiment with a sample of the applied square current pulses, each being 10-ms wide and with a pseudo-randomly selected amplitude. In the same plot we show the mean values and the standard deviation (error bars) of the measured output voltage response. We applied a total of 1000 current pulses and in Fig. 4(b) we observe that the average voltage for every current value, when plotted in the *i*-*v* plane, yields a scattered hysteresis loop.

Owing to the memory property of RS devices, the position of each *i*-*v* data point in this plot contains information about the recent history of pulses that the device has experienced. In practice, for periodic SET-RESET input sequences, this history is identified by the immediately previous data point, which allows evaluating the posterior effect of the last applied input pulse (e.g., a device previously in HRS and currently found in LRS after a SET pulse validates a successful SET process). Here we follow a similar approach to analyze our results by looking every time at the last pair of applied current pulses. For instance, if we focus on the first quadrant of the *i*-*v* plot in Fig. 4(b) ($i > 0$, $v > 0$) we observe that the blueish data points that are mostly gathered on the far-left side, correspond to pulses which immediately followed a previously applied high positive current (SET). On the other hand, the reddish points which correspond to pulses that immediately followed a previously applied high negative current (RESET), are mostly found on the far-right side. Such differentiation corresponds to LRS and HRS levels, respectively, and indicates the memory capacity of the devices, which remains coherent for such nonperiodic input stimuli. Moreover, as observed in the inset of Fig. 4(b), the voltage difference between blueish and reddish data points is maximum around 100 nA, so such level of current could be used to assess the voltage on the devices under test for READ purposes.

Moreover, we observed certain patterns in the measured voltage on the devices that motivated us to perform further statistical analyses. More specifically, we noticed that opposed consecutive memory WRITE operations (i.e., a SET after a RESET, or vice versa) induced a ''tail'' in the transient response of the voltage on the current-driven RS devices. Processing of the data revealed a notably different standard deviation σ_V whenever there was a sequence of opposed memory WRITE operations. The σ_V is reflected in the error bars of Fig. 4(a) and the corresponding transient voltage response that causes this can be certainly detected at circuit level.

As a matter of fact, we show in Fig. 5 the standard deviation σ_V of the measured voltage during 1000 current pulses, presented as a function of the current pulse amplitude. The green data points correspond to pulses that immediately followed a previously applied low current pulse which did not induce any significant change in the resistive state of the device. Likewise, the blue data points correspond to pulses that immediately followed a previously applied high positive current (SET), whereas the red data points correspond to pulses that immediately followed a previously applied high negative current (RESET). At first glance, we notice that the blueish data points are clearly separated from the reddish data points. Additionally, the results show that such separation is wider for a low positive input current.

V. A NOVEL READ SCHEME USING THE VOLTAGE RESPONSE ON CURRENT-DRIVEN RERAM CELLS

The findings described in the previous section could be further exploited in unconventional low-power ReRAM memory

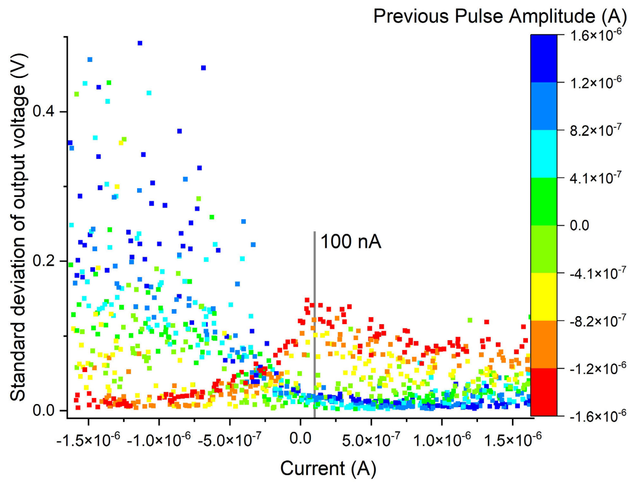


FIGURE 5. The standard deviation of the output voltage σ_V for a sequence of one thousand 10-ms wide current pulses of randomly selected amplitudes within the full scale of ±1.5 uA, shown as a function of the current pulse amplitude. Color code shows the current amplitude of the pulse that was applied immediately before the last pulse.

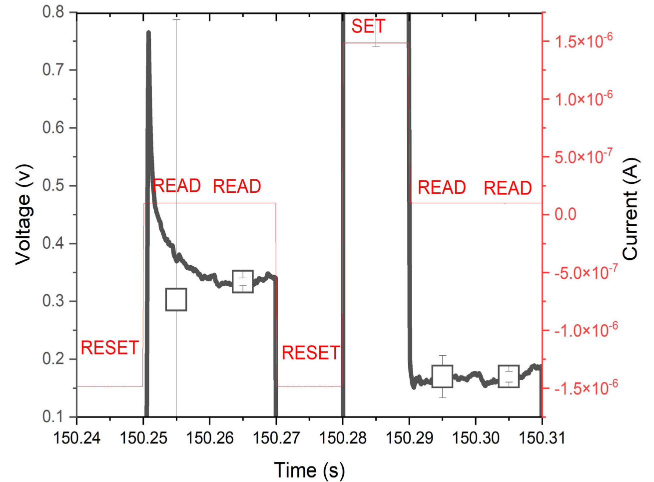


FIGURE 6. Part of a random sequence of 32768 (2^{15}) 10-ms wide current pulses (red curve) using +1.5 uA for SET, −1.5 uA for RESET, and +100 nA for READ operations. Mean values and standard deviation of the output voltage (black curve), for each applied current pulse, is depicted through blank squares and error bars, respectively.

READ schemes. To explore such possibilities, we performed similar measurements with a pseudo-random sequence of current pulses, this time using only three possible pulse amplitudes: +1.5 uA for SET, -1.5 uA for RESET, and +100 nA for READ operations, to emulate typical operational conditions for ReRAM memory cells. We tested the switching performance of the device for a sequence of 32768 (2^{15}) random SET/RESET/READ 10-ms wide current pulses. We show in Fig. 6 a short timestamp of the experiment where it can be observed that a READ pulse, applied after RESET, produces a characteristic transient response in the resulting output voltage, not observed when a READ pulse is applied after SET. In the plot we show the mean values and the standard deviation of the measured output voltage (σ_V) for READ operations that occurred after a previous SET or RESET pulse. Notice that, due to the large number of applied pulses, no pulse separation was considered for convenience, thus consecutive READ events appear as a single wider current pulse.

Based on this evidence, we calculated the cumulative probability distribution of σ_V for READ operations after a previous SET or RESET event. In the results presented in Fig. 7 we notice a ratio $\sigma_{V-HRS}/\sigma_{V-LRS} \sim 10\times$. We repeated the experiment on five different SDC devices from the same DIP package to confirm there was no significant impact of device-to-device variability on the effectiveness of the proposed memory READ method. All devices went through the same forming process and the obtained distributions were always distinguishable in the whole range with less than 0.5% error performance. Considering the very low WRITE/READ currents used in this work, such findings are competitive compared to data reported in a recent study [47] where Hirtzlin et al. presented raw BER values from HfO_2-based kilobit 1T1R ReRAM arrays, integrated in the backend-of-line of

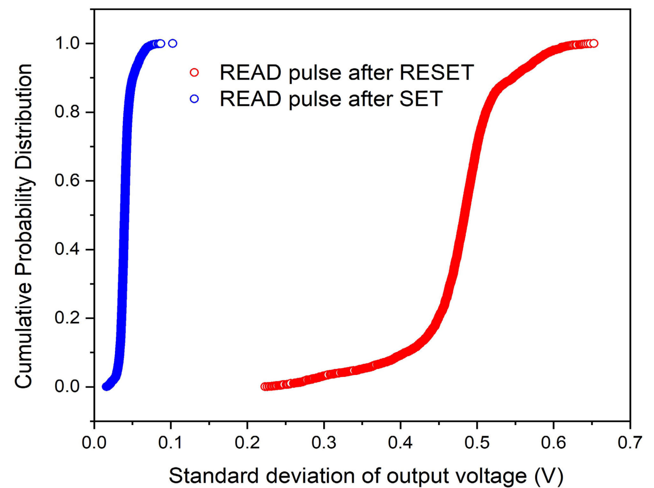


FIGURE 7. The cumulative probability distribution of the standard deviation of the output voltage response. (σ_V) for READ operations that occurred after a previous SET or RESET operation, within a random sequence of 32768 (2^{15}) 10-ms wide current pulses using +1.5 uA for SET, −1.5 uA for RESET, and +100 nA for READ operations.

a full CMOS process. For 100-ns WRITE voltage pulses, applying a 20 uA compliance current led to BER values up to 3.3%. Using $\sigma_V = 0.1$ V as a common threshold to distinguish HRS from LRS, we assessed the average BER in the proposed READ scheme and was found 0.189% with a standard deviation (SD) of 0.221%. Table 1 resumes our calculations for all the different tested devices.

VI. ENERGY CONSUMPTION IN CURRENT-DRIVEN MEMORY OPERATIONS

For the memory operations we integrated the instantaneous power on the RS devices over time (without considering the consumption in the driving circuitry). Besides the long

TABLE 1. Bit Error Ratio (BER) using $\sigma_V = 0.1$ V as a HRS-LRS threshold.

Device	BER(%)
A	0.430
B	0.028
C	0.057
D	0.430
E	0.027
Mean ± SD	**0.189 ± 0.221**

pulse-width, which was in the millisecond range due to limitations of the experimental setup, the energy consumption was calculated as low as $\approx$ 10 nJ for SET, $\approx$ 30 nJ for RESET and between 80-400 pJ for READ operations. The reason why the reported READ energy consumption varies is because of the dynamic nature of the READ process. As shown in Fig. 6, the difference in the resistance of the device to be read causes a much different transient response of the voltage drop on its terminals, while current is kept still at 100 nA. According to the model for the total energy consumed by a ReRAM cell during SET/RESET operations, proposed in [19], there are two components to consider: a Joule heating component E_{Joule} which corresponds to the energy dissipated in the time-varying resistance of the device, and a fixed component E_{RS}, which is principally related to the internal structural modifications in the device implied by the RS event. For short pulsed excitations, the total energy required for SET/RESET is dominated by E_{RS} whereas E_{Joule} is minimized.

The abovementioned numbers of 10 nJ for SET and 30 nJ for RESET energy are in line with those reported in [19] for voltage-based measurements on the same SDC RS devices. In that work, Gomez et al. reported on average 13 nJ for SET and 60 nJ for RESET, while considering a time-to-SET/RESET of $\approx$ 1 ms. However, our energy calculations considered not only the minimum energy required to trigger a SET/RESET, but instead the total energy consumed during the applied current pulse (i.e., during 10 ms). This includes the extra energy consumed as the current keeps flowing through the device after the RS has occurred. So, we believe such results are competitive and highlight the potential of current-based against voltage-based driving schemes. Moreover, in our measurements we observed that the RS event in all WRITE operations occurred approximately in the first 10% of the duration of the applied pulse. Therefore, we estimate that the real E_{RS} energy in our proposed scheme could probably be up to an order of magnitude lower than reported here, with an optimized design of the current driver. Moreover, current-driven memory operations could lead to much lower power consumption with nanodevices that respond faster to the applied stimuli [20], [48].

On the other hand, due to the much higher currents that resulted from the voltage pulses applied during memory operations in [19], the voltage-driven SDC devices demonstrated much lower HRS and LRS resistance values, compared to the resistance range observed in our measurements. This could eventually affect the endurance of the devices in practical ReRAM architectures, and therefore this constitutes another reason why current-based driving schemes should be further explored for ReRAM applications.

VII. CONCLUSION

Through the characterization of a sub-class of electrochemical metallization memory (ECM) devices commercialized by *Knowm Inc.*, this work demonstrated the feasibility of current-driven ReRAM operations via fine control of current levels in the nA range. Besides operating constantly at low current levels and in the presence of variability, the presented results demonstrated a gradually achieved stable and repeatable cycling performance, with the memory capacity of the devices remaining coherent for both periodic and nonperiodic stimuli. Furthermore, studying the cumulative probability distribution of the standard deviation of the output voltage (σ_V) for READ operations led us to propose a novel READ scheme for ReRAM modules based on monitoring the transient response of the voltage on current-driven ReRAM cells. With a ratio of $\sigma_{V-HRS}/\sigma_{V-LRS} \sim 10\times$ and the energy consumption for READ operations calculated between 80-400 pJ, our results show that such method allows carrying out both efficient and low-power READ operations. Everything considered, the current-based ReRAM driving approach emerges as a feasible solution not only to comply with low energy consumption requirements in emerging ReRAM applications, but also to allow for unconventional READ methods for binary information encoded in the HRS and LRS resistance levels of ReRAM cells.

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