IEEE Access
Multidisciplinary ⋮ Rapid Review ⋮ Open Access Journal

Received 7 April 2023, accepted 7 May 2023, date of publication 12 May 2023, date of current version 18 May 2023.

Digital Object Identifier 10.1109/ACCESS.2023.3275751

RESEARCH ARTICLE

Optimization and Design Considerations of GaN-Based Multi-Level TP PFC Converters

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This work was supported in part by the H2020-MSCA-IF-2020 under Project 101031029, and in part by the 2232 International Fellowship for Outstanding Researchers Program of the Scientific and Technological Research Council of Turkey (TUBITAK) under Project 118C374.

ABSTRACT Latest developments in low voltage wide-bandgap semiconductor technology have increased the popularity of single-phase multi-level (ML) totem pole (TP) power-factor correction (PFC) converters. Phase shifted flying capacitor based power stages offer several advantages, such as higher input current ripple frequency, smaller size inductor and differential mode (DM) filter, and usage of low voltage Gallium Nitride (GaN) devices with better figure-of-merit. Even though it has been proven that ML TP PFC converters have good power density and efficiency, the determination of optimal voltage levels and switching frequency requires a system-level optimization. This paper proposes an optimization framework for ML TP PFC converters, taking the power stage, thermal, DM filter, and magnetic designs, as well as practical design considerations, into account to determine the voltage-levels and switching frequency that minimize the power losses, cost and volume of the total system. To process output power of 3700W, the optimization tool suggests using a 4-Level GaN TP PFC topology switched at 45 kHz. The outcome of the tool has been compared with other fixed inductor current ripple designs, as well as optimized designs for 3-Level and 5-Level TP PFC converters in terms of cost, volume, and power losses. In accordance with the optimization results, a prototype of a 4L TP PFC rated at 3700 W is designed, which achieves a peak efficiency of 99.6% at 1 kW and >99.1% efficiency under the full power range.

INDEX TERMS Ac/dc conversion, multi-level, optimization, power factor correction, totem-pole.

I. INTRODUCTION

Multi-level (ML) converters have been initially introduced for high voltage applications such as solid-state-transformers, high voltage inverters, etc [1], [2], [3], [4], [5]. With the recent advances in Gallium Nitride (GaN) power devices, some studies have proposed designs with ML configurations to achieve high power density single-phase totem pole (TP) power factor correction (PFC) converters using low voltage GaN FETs with better figure-of-merit [6], [7], [8], [9], [10], [11], [12], [13], [14], [15], [16], [17], [18], [19]. For a single-phase N-level TP PFC, there are N-1 half-bridge circuits and N-2 flying capacitor stacks in parallel with them as illustrated in Fig. 1. FETs connected in complementary pairs are driven with a phase shift of 360/(N-1) with respect to other half-bridges. Phase-shifted PWM control method shifts the input current ripple frequency to N-1 times the switching frequency (f_{sw}) [7]. Thanks to the increased input current ripple frequency and decreased switching voltage levels, the total volume of both electromagnetic interference (EMI) filter and PFC inductor is significantly reduced [8].

In recent literature, several single-phase ML TP PFC converters have been proposed utilizing either low voltage Silicon (Si) Si FETs or GaN FETs. In [9], a 3-level (3L) TP PFC converter is designed with low reverse recovery Si FETs. In a 3L TP PFC configuration, each device is exposed to half of the output DC voltage, which necessitates using power devices with voltage ratings of 250-300V. However,

The associate editor coordinating the review of this manuscript and approving it for publication was Jahangir Hossain.

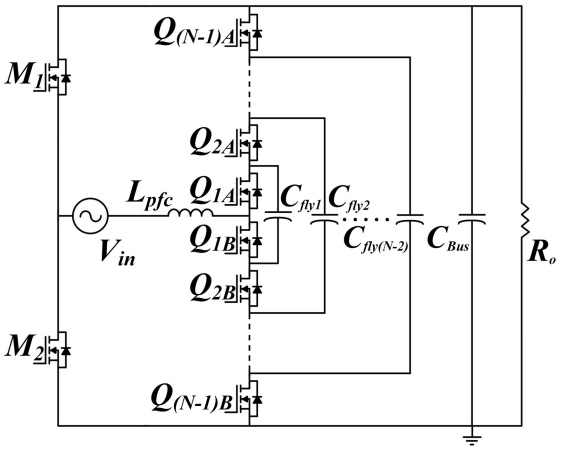

FIGURE 1. Generalized schematic of ML TP PFC converters.

there are no commercially available power device with such voltage ratings. Due to this reason, two 150V Si FETs are connected in series to make a 300V device, resulting in additional complexity in layout and gating schemes to ensure that the series connected FETs share the voltage equally. To overcome the voltage imbalance issue among the series connected power devices, a 4-level (4L) configuration, where each power device is exposed to 1/3 of the DC bus voltage, has been considered as an alternative [11], [12], [13]. There are numerous suitable FETs available in commercial markets with voltage ratings ranging from 150V to 200V [20].

Many published studies on single-phase ML TP PFC converters have demonstrated high-power-density prototypes [11], [12], [13], [14], [15], [16], [17], [18], [19]. Nevertheless, these prototypes are not fully optimized. For instance, f_{sw} is selected only based on PFC inductance volume and overall FET losses without considering the generated differential-mode (DM) noise. This approach simply ignores the f_{sw} impact on the size of the EMI filter and thermal components such as heatsinks, thus significantly increasing the overall volume of the converter. In [11], a very compact 7-level (7L) TP PFC converter design is presented. The reasons for selecting a 7L topology are summarized as follows: decreased input current ripple magnitude, decreased PFC inductor volume, commercially available transistor voltage ratings, and increased power density. However, the f_{sw} is selected as 150 kHz, which would cause side-band harmonics of the common-mode (CM) noise to appear right after 150kHz in the EMI spectrum.

In most cases, TP PFC converters are designed with a straightforward fixed current-ripple magnitude approach, as in [14]. In this approach, a f_{sw} of 33 kHz, 45 kHz, or 67 kHz is first selected, ensuring a thermally stable design for high-frequency FETs under a defined cooling effort. Next, a maximum input inductor current ripple, i.e. 20%, is defined as a design criterion. The EMI filter is mostly experimentally tuned to compensate for the remaining differential mode noise. However, the design process of ML TP PFC converters is complicated and includes complex trade-off points [8]. Therefore, a system level design and optimization approach is necessary to obtain an optimum design and fully utilize the benefits of ML converters. One of the few optimization approaches to TP PFC design is presented in [10]. In this study, the PFC inductor is optimized by sweeping input current ripple magnitude and f_{sw}. However, this approach may result in a sub-optimal design, as the EMI filter, FET losses, and heatsink volumes are not included in the framework. Moreover, it is crucial to use a fair drive strength comparison method when comparing FETs with different sizes and technologies, as well as taking into account package-related parasitics.

The design trade-offs among ML candidate topologies remain unaddressed without a holistic optimization model. This paper proposes a system-level optimization framework for ML TP PFC converters to determine the optimal number of voltage levels, f_{sw}, and all other design parameters based on given design specifications. The proposed design tool can provide the optimal solution among the design space of ML converters and is used to compare the best designs of each N-level converter. A 3700W ML TP PFC has been optimized with the proposed tool and prototyped to validate the results of the algorithm.

II. OPTIMIZATION FRAMEWORK

The proposed optimization algorithm includes three major loops; the outermost loop sweeps through N-levels up to 5-level (5L), the middle loop sweeps the PFC boost inductance (L), and the innermost loop sweeps the f_{sw}. In the inner loop, the current ripple envelope is extracted for each L - f_{sw} pair, and an EMI filter is designed based on the required attenuation for the filter. For the same L - f_{sw} pair, the optimal local best FET selections and corresponding heatsink volumes are determined through the developed gate drive strength model, taking the package parasitics as well as thermal resistances of the package and PCB into account [26]. In parallel, multiple PFC inductors are designed for the given L - f_{sw} pair using every feasible core in the database. A local penalty function is applied to each sub-models, and the local best designs are stored. At the last step, a cost function with assigned weights to the total cost, power loss, and volume is applied to the design space, and the optimum design is determined. The flow-chart of the proposed optimization framework is illustrated in Fig. 2.

A. DIFFERENTIAL MODE FILTER

The overall EMI filter design algorithm is illustrated in Fig. 3. Firstly, the algorithm calculates both the input current ripple envelope and the resulting DM noise at the multiples of the effective current ripple frequency using the Fourier coefficient expansion method as proposed in [27]. Then, the required filter attenuation is calculated for the first DM harmonic in the EMI spectrum. Lastly, the DM inductance (L_f) is swept, and candidate DM filters are designed with all

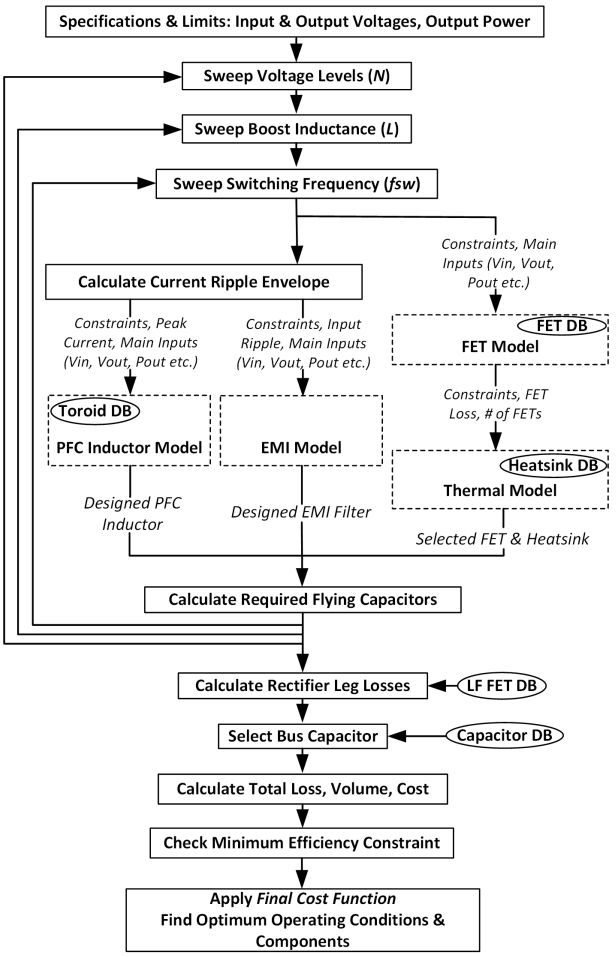

FIGURE 2. The overall flow-chart of the proposed optimization framework.

L_f & C_f pairs until the algorithm selects the one with the minimum total volume.

In PFC converters, the DM noise is determined by the magnitude and frequency of the input current ripple [28]. Both quantities are a function of the number of voltage levels in ML TP PFC converters. A higher number of voltage levels increases the input current ripple frequency and decreases the magnitude of it, which in turn decreases the total volume of PFC inductor and DM filter. Example input current ripple envelopes for 3L, 4L, and 5L TP PFC converters having the same input inductance are illustrated in Fig. 4. The switching frequencies are selected as 33 kHz, 45 kHz, and 67 kHz. This is because the major DM harmonic appearing in the EMI spectrum tends to be lower at these switching frequencies as the effective input current is shifted to N-1 times the switching frequency. As seen in Fig. 4, the volume of the DM filter is discontinuous when the effective input frequency is below 150 kHz. Furthermore, the shift in the gradient color from red to green illustrates the amplitudes of the current ripple envelopes when larger input inductances are used. This introduces another design trade-off between DM filter size and input inductance, as DM noise is a discontinuous function of the switching frequency.

B. PFC BOOST INDUCTOR

The flow-chart of the PFC inductor design sub-module is given in Fig. 5. The PFC inductor cores are required to have high saturation flux density and soft-saturation characteristics. Considering these factors, as well as the low magnitude current ripple envelope shown in Fig. 4, ungapped toroid cores are preferred. As a first step, the number of turns, N, required for the given L is found by

$$N = \sqrt{\frac{L}{Al}} \tag{1}$$

where, Al represents the inductance per square turn. The maximum magnetic flux density, B_{max}, is calculated to check if operating flux density is less than a percentage of saturation flux density, B_{sat}. Here, the constraint is set to $B_{max} \leq 0.7\ B_{sat}$. B_{max} is expressed as

$$B_{max} = \frac{I_{in_{max}} L}{N A e_{core}} \tag{2}$$

where Ae_{core} stands for the total cross-section area of magnetic core. The optimization routine also designs inductors with stacked cores to obtain the required core cross-sectional area if a single core is not enough. For single and two stack core options, the maximum winding radius, r_{max}, that can fit in the 80% of the inner circumference and utilizing 50% window area is calculated. The maximum number of winding layers is limited to 2, which limits the intra-winding parasitic capacitances [32]. To satisfy the thermal limits and reduce the copper related losses, a current density limit of 4 A/mm^2 is also used. After calculating the maximum copper wire radius, the closest commercially available winding radius in terms of AWG is selected. The total copper losses caused by both the DC (R_{DC}) and AC (R_{AC}) resistances of windings are calculated by

$$P_{copper} = I^2_{in_{RMS}} R_{DC} + I^2_{ripple_{RMS}} R_{AC} \tag{3}$$

where, $I_{ripple_{RMS}}$ is the rms value of the current ripple on the inductor. The DC resistance is

$$R_{DC} = \frac{l_{wire}\rho_{copper}}{\pi r^2_{wire}} \tag{4}$$

where, l_{wire} is the length of the wire and ρ_{copper} is the resistivity of the copper as a function of temperature.

$$\rho_{copper}(T) = 1.7210^{-8}[1 + 0.00393(T_o - T_a)] \tag{5}$$

The skin effect on AC resistance in relationship with the proximity effect of a single-layer winding can be expressed as in [29]

$$R_{AC} = R_{DC}\left[1 + \frac{(\frac{r_{wire}}{skindepth})^4}{48 + 0.8(\frac{r_{wire}}{skindepth})^4}\right] \tag{6}$$

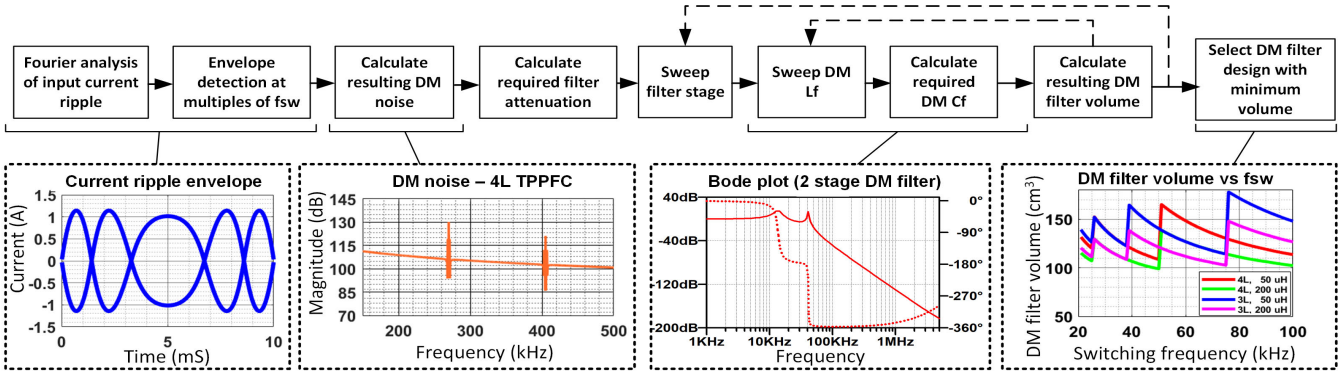

FIGURE 3. The local optimization flow-chart of the EMI model.

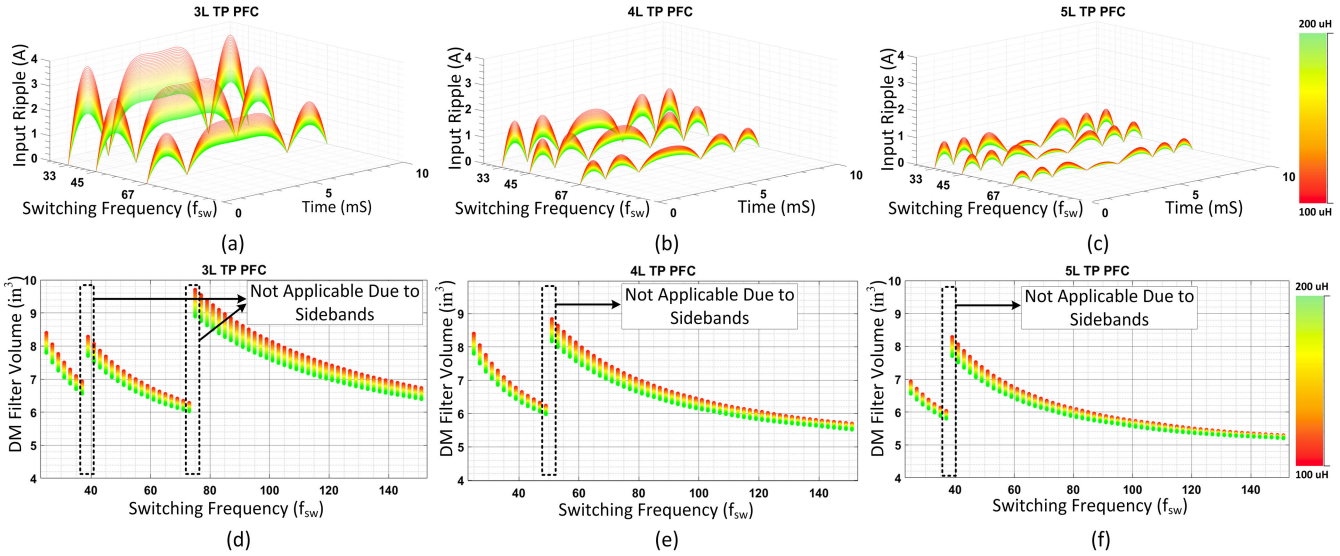

FIGURE 4. Input current ripple waveform, switching frequency and PFC inductance relation of (a) 3L, (b) 4L and (c) 5L TP PFC converters, Input current ripple and DM filter volume comparison of (d) 3L, (e) 4L and (f) 5L TP PFC converters.

The Steinmetz' loss equation [29] is used to estimate the core losses as

$$P_{core} = \frac{1}{0.5T_{in}} \int_{t=0}^{t=0.5T_{in}} k f_{eff}^{a} \Delta B(t)^{b} dt \tag{7}$$

where,

$$\Delta B(t) = \frac{L I_{ripple(t)}}{2NAe_{core}} \tag{8}$$

Here in Eq. (7), f_{eff} stands for the effective input current ripple frequency, which equals $N-1$ times of the switching frequency in ML TPPFC converters. After calculating the total losses and using thermal resistance of the core under convection cooling, cores with temperatures rising above $80^{o}C$ are not stored as a solution.

C. FLYING CAPACITORS

The flying capacitors carry a portion of the output power with respect to the time-varying duty cycle. Moreover, the energy holding capacity in each flying capacitor stack is different, as they are connected to different voltage nodes. Therefore, the flying capacitors connected to the low voltage node need higher capacitances compared to the ones connected to the higher voltage nodes. These capacitors have to be high enough to keep required individual voltage stable while providing energy to output. For that reason, the voltage ripple on flying capacitors affect the switch node voltage and input current ripple directly. Therefore, main design consideration for flying capacitors must be the maximum voltage ripple over them. It is possible to calculate minimum required flying capacitor value to limit voltage ripple over them with Eq. (9) [34].

$$C_{flymin} > \frac{i_{Lmax}}{f_{sw}(N-1)\Delta V_{C_{fly}}} \tag{9}$$

where, C_{flymin} is the minimum required value of the flying capacitor, N is the voltage level of ML TPPFC, i_{Lmax} is the maximum average current of the worst-case and $\Delta V_{C_{fly}}$ is the maximum amplitude of allowed voltage ripple over the flying

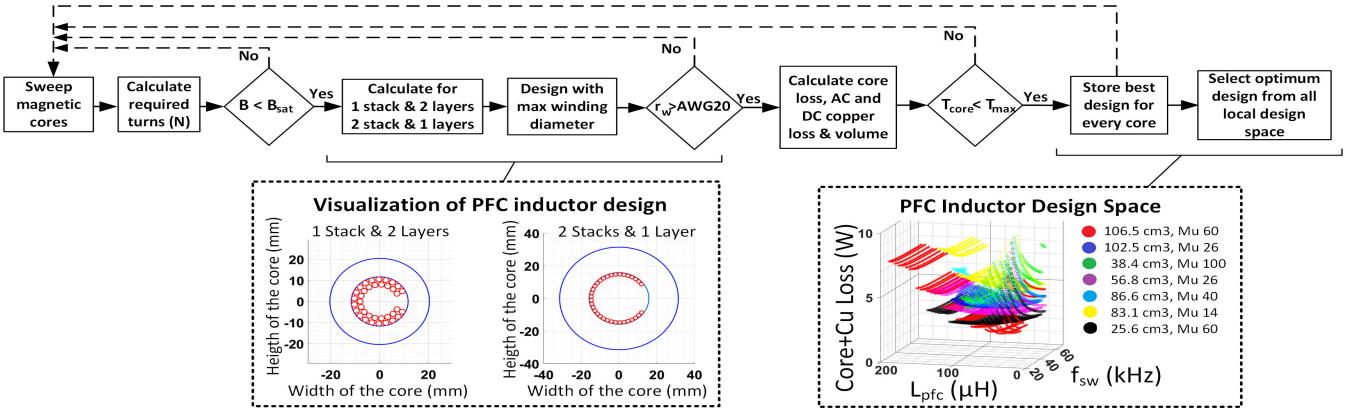

FIGURE 5. The local flow-chart of the PFC inductor design algorithm.

capacitors. On the other hand, it is suggested to double the resulting required flying capacitor value for ceramic capacitors due to roll off phenomenon. Using a value smaller than the required capacitor value may result in low frequency noise in current ripple and devastation of the high-frequency line (HF) FETs.

D. SELECTION OF FETs

The dissipated power on the HF FETs affects the overall efficiency and increases the required heatsink volume. Therefore, another local cost function, which is a product of power loss and heatsink volume, is used to select the optimal FET and heatsink pair. Calculating the conduction losses considering the temperature dependent on-state-resistance is straightforward [24]. On the other hand, switching loss calculation of a FET involves several components such as output charge losses (P_{Qoss}), reverse-recovery losses (P_{Qrr}), turn-off losses (P_{off}), body-diode or 3^{rd} quadrant losses during dead-time (P_{DT}), I-V overlap losses during turn-on (P_{IV}), and gate drive losses (P_{gate}).

$$P_{sw} = P_{Q_{oss}} + P_{gate} + P_{off} + P_{IV} + P_{DT} \tag{10}$$

Among these loss components, the P_{Qrr} includes the P_{Qoss}, and P_{Qoss} is only considered when P_{Qrr} is absent, such as in GaN FETs, and expressed as

$$P_{Q_{oss}} = V_d Q_{oss} f_{sw} \tag{11}$$

I-V overlap power losses directly depend on the turn-on speed of the FET. GaN FETs come in low inductance packages, making the common-source inductance as well as the loop inductance low. Low common-source inductance allows for faster turn-on, while helping with the self-turn issue when it is in the range of 50-200 pH. Similarly, low loop inductance enables faster turn on, which reduces the I-V overlap losses. The remaining energy in the loop inductance starts resonating with the output capacitance of the FET and cause a voltage overshoot. Therefore, fast turn-on speed necessitates a low loop inductance. Estimating the necessary gate drive strength for different FETs that would cause a similar voltage overshoot requires a complex relationship between parasitic capacitances of the FET, transconductance, gate resistance, gate loop inductance, common-source inductance and power loop inductance. In [26], a simplified gate drive strength comparison method is presented. In this method, the drain voltage transition speed, dV/dt, for a given maximum voltage overshoot can be estimated by simplifying the complex relationship by conducting a simple SPICE simulation. This approach allows comparing various FETs in a fair manner considering layout, package parasitics, as well as electrical properties of FETs. After determining the gate drive resistance and package inductance, total switching loss caused by HF FETs (P_{sw}) can be calculated with the equations given in Eqs (11)-(15) [8].

The power loss due to drain voltage and current cross-over during the turn-on instant of HF FETs are named as P_{IV} and calculated as in Eq. (12).

$$P_{IV} = V_d I_d \frac{(t_{fv} + t_{ri})}{2} f_{sw} \tag{12}$$

where t_{fv} and t_{ri} are the fall time of drain-source voltage (V_d) and rise time of drain-source current (I_d). Similar to I-V losses, voltage and current overlaps in every turn-off instant of the FETs, too. Additional switching loss caused by the turn-off instant of the FETs is calculated as

$$P_{off} = V_d I_d \frac{(t_{fi} + t_{rv})}{4} f_{sw} \tag{13}$$

where t_{fi} and t_{rv} are the fall time of drain-source current (I_d) and rise time of drain-source voltage (V_d). The required gate charge to turn a FET on is annotated as Q_{gate} and causes additional power loss named P_{gate} in every switching cycle.

$$P_{gate} = V_{gate} Q_{gate} f_{sw} \tag{14}$$

where V_{gate} is the gate drive voltage of the HF FETs. Lastly, 3^{rd} quandrant loss caused during dead-time, T_{DT} is calculated as

$$P_{DT} = V_{sd(I_d)} I_d T_{DT} f_{sw} \tag{15}$$

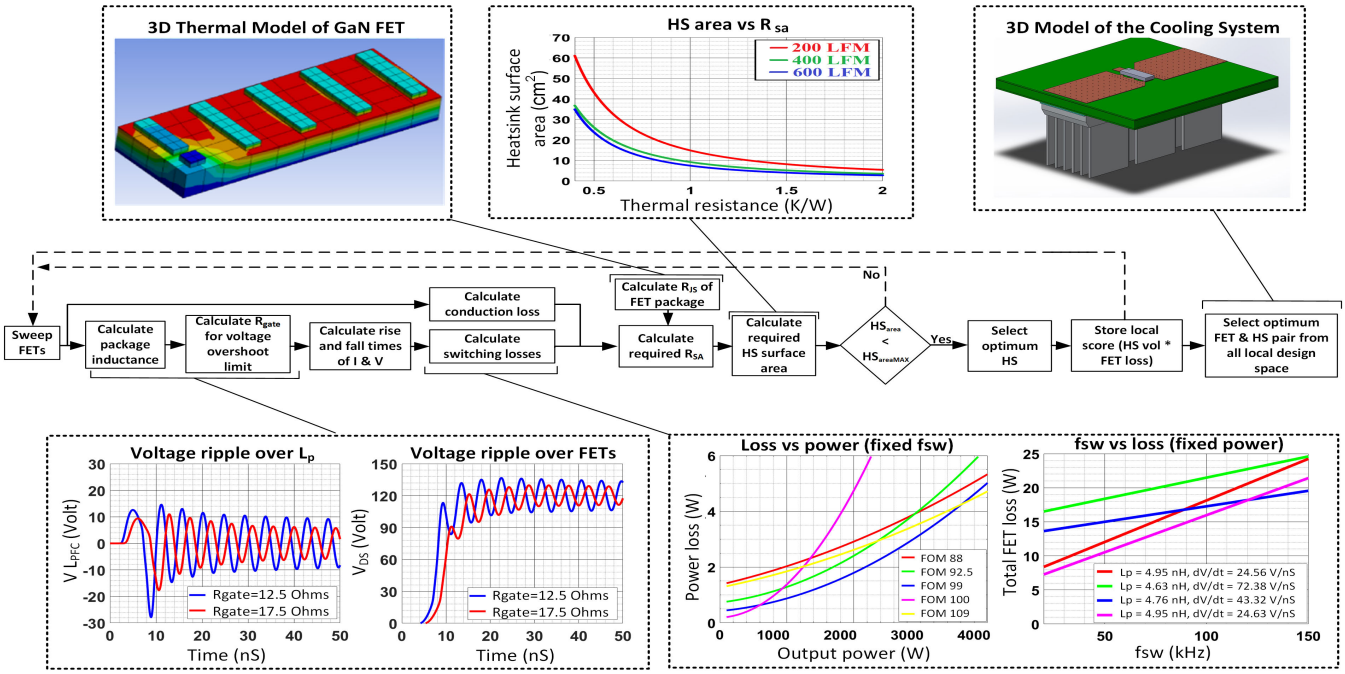

FIGURE 6. The local flow-chart of the FET and heatsink selection algorithm.

where V_{sd} is the reverse conduction voltage drop of the HF FET. The total FET loss can be calculated with the summation of P_{sw} and P_{cond} as in Eq. (16).

$$P_{FET} = P_{sw} + P_{cond} \tag{16}$$

To visualize the importance of HF FET selection, four different 200V GaN FETs are selected. Two subfigures given in Fig. 6 show the comparison of selected GaN FETs with different parasitic inductance (L_p) and figure-of-merit values with respect to output power and switching frequency. dV/dt values shown on the graph are determined by gate drive strength method [26]. Figure-of-merit values on the figure are calculated by the multiplication of R_{dson} and Q_{gate} values of the FETs.

E. SELECTION OF HEATSINKS

The junction-to-sink thermal resistance (R_{js}) are calculated using dimensions of FET packages and spreading thermal resistance calculation method presented in [31]. Once R_{js} is known, the required sink-to-ambient thermal resistance of the heatsink (R_{sa}) is calculated using Eq. (17).

$$R_{sa} = \frac{T_{max} - T_{ambient}}{P_{FET}} - R_{js} \tag{17}$$

where T_{max} and $T_{ambient}$ are the application specific parameters that are defined as 110^oC and 50^oC in this study, respectively. Selecting a heatsink with a lower thermal resistance than calculated R_{sa} ensures a proper cooling for FETs.

III. 3L - 4L - 5L TP PFC DESIGN COMPARISON

Increasing the voltage level of a ML TP PFC brings several advantages in terms of FET drive performance. As a rule of thumb, FETs with low drain-source voltage ratings exhibit better figure-of-merit, allowing the use faster FETs in the TP PFC converter with higher voltage levels. However, it is essential to note that this only holds true for switch-by-switch comparison. On the other hand, each added voltage level introduces two more FETs to the main power line, which increase the conduction loss of HF FETs, particularly for mid-to-high power converters. This creates another trade-off point from a thermal perspective.

In a ML TP PFC converter, the size of the DM filter is indeed directly related to the magnitude and frequency of the input current ripple. Increasing the voltage level of the converter raises the input current ripple frequency, which in turn, reduces the total volume of the PFC inductor and DM filter. As a result, the main DM noise harmonic can be shifted to just before the 150 kHz band by decreasing the switching frequency to lower values and increasing the voltage levels of the converter. However, the size of the PFC inductor still depends on the magnitude and frequency of the input current ripple. This complex trade-off between the size of the DM filter and the PFC inductor designs stems from the fact that the DM filter size has a discrete relationship with the switching frequency, and conducted EMI measurements start from 150 kHz. The optimal size of the DM filter and PFC inductor is influenced by the voltage level, switching frequency, and input current ripple, as well as the desired level of efficiency and power density.

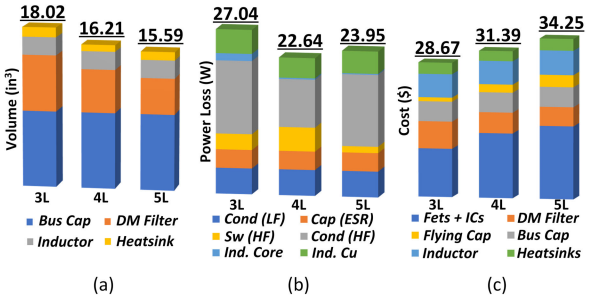

FIGURE 7. **Comparison of 3L, 4L and 5L TP PFC converters, (a) volume, (b) power loss, (c) cost.**

In this study, a system-level optimization framework has been developed to address the design trade-offs and identify the optimal topology and design parameters for ML TP PFC converters. The optimization process considered volume, power loss, and cost, with assigned weighting coefficients of 0.6, 0.2, and 0.2, respectively. Key design criteria included a minimum efficiency limit of 98.5%, thermal limits for both the FETs and PFC inductor core capped at 110 °C, a current density limit of 4 A/mm^2 for the PFC inductor and EMI filter windings, and a maximum allowable voltage overshoot on the HF FETs restricted to 10% using the previously developed gate drive strength method. With these limits and criteria, the optimization framework determined the optimum designs for 3L, 4L, and 5L TP PFC converters.

The total volume, total loss and total cost of these optimum designs are illustrated in Fig. 7 (a), Fig. 7 (b) and Fig. 7 (c), respectively. The results showed that the 5L TP PFC converter had the smallest volume, while the 4L TP PFC converter exhibited the lowest total power loss. However, it is important to note that increasing the voltage level of the converter also increases the cost of additional circuitry, flying capacitors, and controller requirements. After optimization, the 4L TP PFC converter outperformed the 3L TP PFC converter by a significant margin, while the difference between the 5L and 4L TP PFC converters was less pronounced. Consequently, the optimization algorithm selected the 4L TP PFC converter as the optimal ML TP PFC converter for the 3.7 kW output power condition.

IV. COMPARISON OF DIFFERENT 4L TP PFC DESIGNS

In this section, four different 3.7 kW 4L TP PFC converters are designed with two different approaches: fixed input current ripple magnitude and system-level optimization. The selection of the maximum input current ripple when designing a TP PFC converter is a method frequently used by many designers.

Fig. 8 illustrates a comparison between the fixed current ripple and system-level optimized results. The amplitude of the input current ripple is held constant at 3 Amps corresponding to a maximum inductor current ripple of 12.5%. Different combinations of switching frequency and PFC inductance are used, namely 20 kHz-184 μH, 33 kHz-112 μH, 45 kHz-84 μH and 67 kHz-55 μH. On the other hand, the proposed system-level optimization method suggested alternative pairs of 20 kHz-122 μH, 33 kHz-138 μH, 45 kHz-108 μH, and 67 kHz-138 μH under weighting coefficients 0.6 for volume, 0.2 for power loss, and 0.2 for cost. Fig. 9 (a) illustrates the volume improvements achieved using the system-level optimization approach in comparison to the fixed current ripple approach for four different designs. Total volume improvement for 33 kHz (-2.01%) and 45 kHz (-2.64%) designs are not as significant when compared to 20 kHz (-23.34%) and 67 kHz (-7.96%). The main reason behind this difference is the optimized input current ripple amplitude, which are 4.55 A, 2.44 A, 2.29 A, and 1.20 A for 20 kHz, 33 kHz, 45 kHz and 67 kHz, respectively. It is evident that the resulting optimum input current ripple magnitudes are very close to fixed approach (3 Amps) for the 33 kHz and 45 kHz designs. As a result, the decrease in total volume for these two cases is less substantial than the others. In summary, the optimization framework has successfully reduced the total converter volume at the expense of a slight increase in total power loss, leading to higher power density levels.

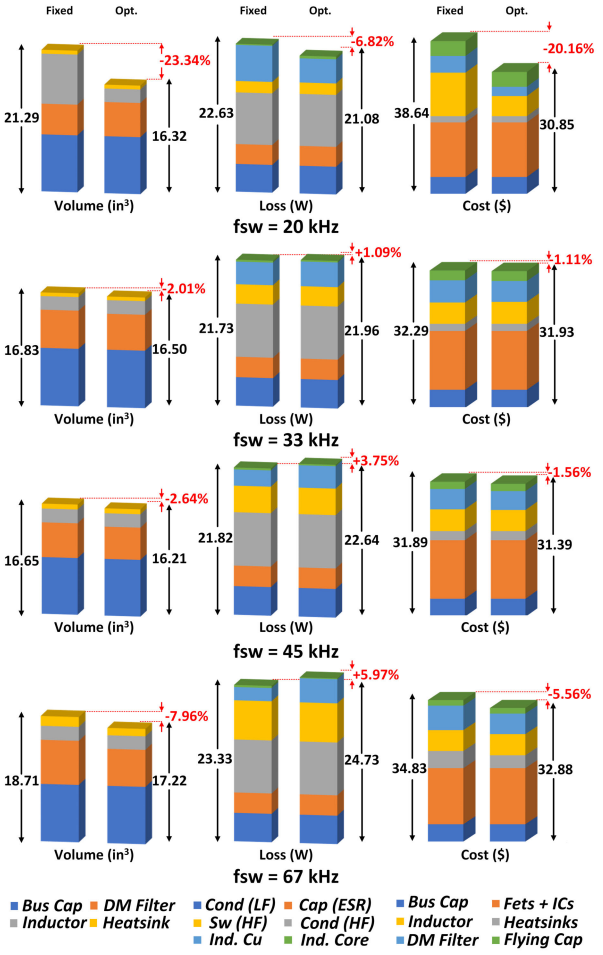

FIGURE 8. **The comparison of optimized and non-optimized 4L TP PFC converters.**

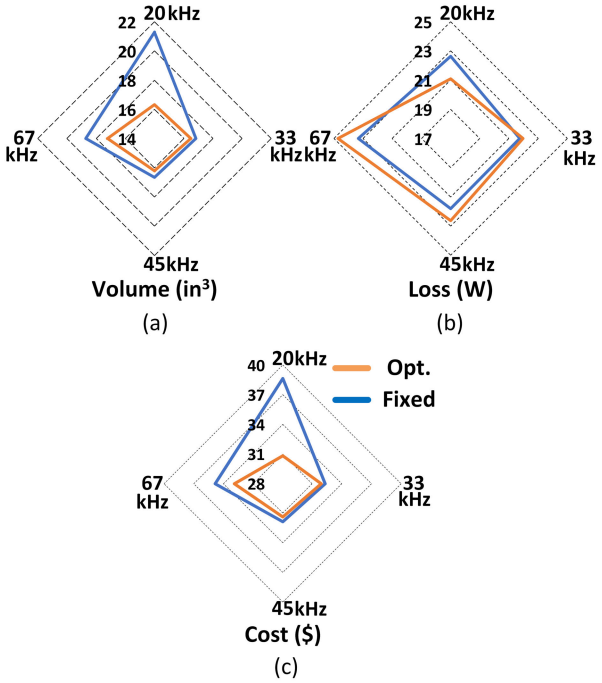

FIGURE 9. The performance metric comparison of the optimized and non-optimized 4L TP PFC converters; (a) volume, (b) loss, (c) cost.

V. PRACTICAL DESIGN CONSIDERATIONS

Designing a high-frequency GaN power stage for ML TP PFC converters can be challenging, with several key design considerations to ensure efficient and reliable operation. Here are some essential practical design considerations:

- Minimize loop inductances: GaN FETs have minimal package inductance, so it is crucial to minimize gate loop, power loop, and bootstrap loop inductances in the PCB layout. This helps in reducing voltage overshoots, ringing, and EMI, as well as improving efficiency and switch performance.
- Cascaded bootstrap scheme: To minimize costs, a cascaded bootstrap scheme can be employed. This approach involves using bootstrap capacitors to create isolated power supplies for the gate drivers of the GaN FETs. The bootstrap capacitors are charged from a single power supply, reducing the need for multiple isolated power supplies and thereby lowering the overall system cost.
- Thermal management: GaN FETs can generate significant heat at high frequencies, so it is essential to design an effective thermal management system. This may include using appropriate heat sinks, thermal vias, and thermally conductive materials to dissipate heat efficiently.

A. DESIGN OF THE GATE DRIVE LOOP

GaN FETs are designed with low pin inductances to enable fast switching and to prevent voltage ringings that may occur between gate-to-source and drain-to-source. To fully realize the benefits of GaN FETs, it is crucial to optimize the PCB layout to minimize the gate loop inductance. Otherwise, the low threshold voltage of GaN FETs makes them susceptible to gate ringing caused by improper design of the gate-source loop. To address this issue, the shortest possible gate-to-source path is implemented with a separated source tab as Kelvin connection on the first internal PCB layer. Using Eq. (18), the gate-to-source inductance is calculated as 4.14 nH with a similar approach presented in [33].

$$L_{loop} = \frac{l}{500}\left[\ln\frac{2l}{wt} + 0.2235\frac{w+t}{l} + 0.5\right] \qquad (18)$$

where l, w, and t represent the length, width, and thickness of the PCB route, respectively. Designed gate drive loop is shown in Fig. 10. This Kelvin connection of the gate drive loop ground helps eliminate the common-source inductance, preventing self-turn on issues when FETs are switched on and off at high speeds.

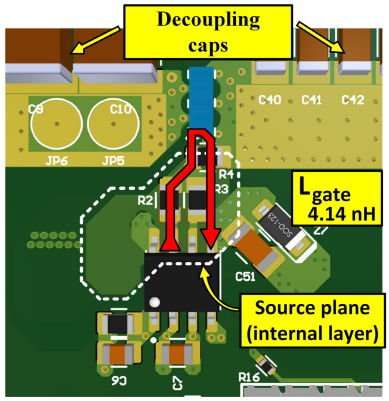

FIGURE 10. The gate-source loop of the gate drive circuit.

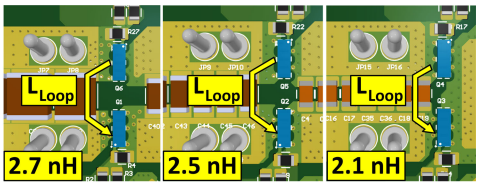

FIGURE 11. The power loop of half-bridges.

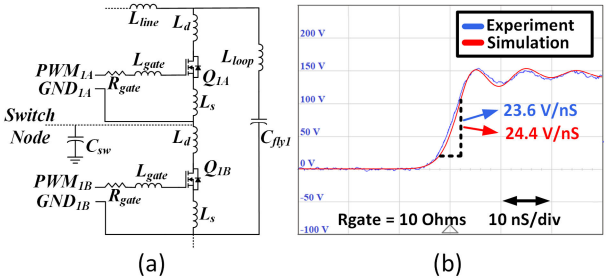

FIGURE 12. Turn on transient; (a) gate drive parasitics, (b) drain-source voltage waveform.

B. DESIGN OF THE POWER LOOP

The ringing that occurs between the drain and source pins of a FET is influenced by various factors, including the output

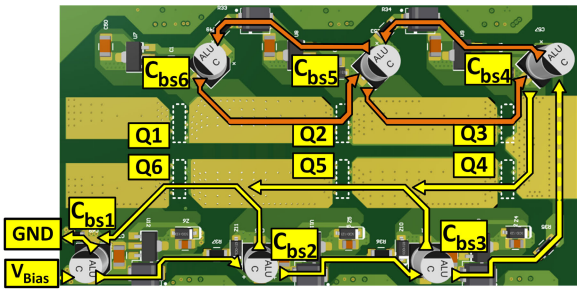

FIGURE 13. The current paths of bootstrap circuits.

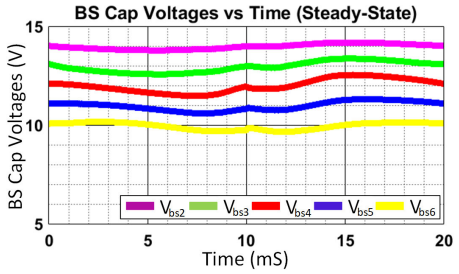

FIGURE 14. The voltage swings of the bootstrap capacitors in one input cycle (steady-state).

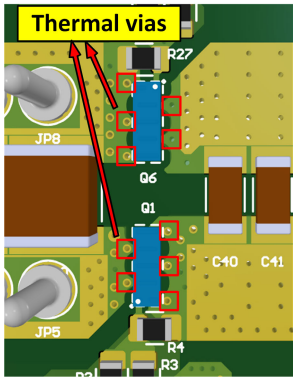

FIGURE 15. The placement of thermal vias.

capacitance (C_{oss}), drain and source inductances of the FET package (L_d & L_s), gate drive resistance (R_{gate}), load current (I_d), and reverse transfer capacitance of the FET (C_{rss}) [24]. When GaN FETs are turned on and off at high speeds, the energy stored in the power loop inductance is not dissipated and instead initiates oscillations with the C_{oss} of the GaN FETs, resulting in voltage fluctuations. To effectively switch on the low gate charge GaN FETs and avoid excessive drain-source voltages, it is crucial to minimize the power loop inductance. To achieve this, decoupling capacitors must be positioned as close as possible to the GaN FETs. In ML TPPFC topologies, the decoupling capacitors are arranged in parallel with flying capacitors. However, the placement of decoupling capacitors is more critical than that of the flying capacitors.

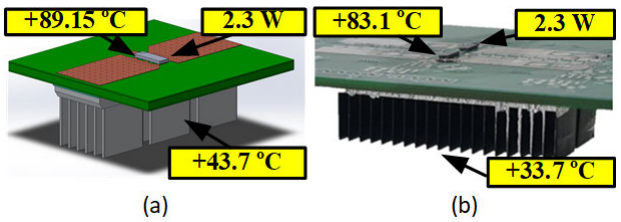

FIGURE 16. The thermal performance evaluation of the GaN power stage; (a) simulation results, (b) experimental results.

Efforts have been made in this design to reduce the length of the shortest path between the GaN FET pins and the nearest decoupling capacitor. This was achieved using decoupling capacitors with smaller packages placed in parallel with half-bridge FETs. The smaller packages in parallel helps to increase the width and reduce the inductance of the capacitors. In this design, the power loops of three half-bridges are reduced to a range of 2.1nF and 2.7nF as seen from Fig. 11. This wider path helps dissipate the heat produced by the FETs more easily and keeps the drain-source voltage ringing under 10%. Fig. 12.(a) shows the simplified gate drive and power loop schematics, while Fig. 12.(b) shows the comparison of simulated and experimentally tested drain-source voltage overshoot over the HF FETs. Apart from loop and package related parasitic inductances, there are some parasitic capacitances affecting turn-on and turn-off transients, which are switch node capacitance (C_{sw}) and parasitic capacitance between windings of PFC inductor. As can be seen from the results, special efforts given to reduce parasitic inductance limited the maximum voltage overshoot seen between the drain and source pins of HF FETs and reached 23.6 V/nS turn-on speed with the designed board. This demonstrates that the careful design and attention to parasitic elements, both inductive and capacitive, has led to improved performance in terms of switching speed and reduced voltage overshoot.

C. BOOTSTRAP CIRCUIT

Isolated power supply-based drive solutions can be expensive and cumbersome due to the increased number of HF FETs required. As a result, a well-designed bootstrap circuit offers a more cost-effective alternative for ML TP PFC designs [22], [23].

Steady-state voltages of bootstrap capacitors in a 4L TP PFC converter differ from the pre-charge voltage values. Although the average voltages across bootstrap capacitors will be equal to the steady-state values, it is important to consider the low-frequency oscillations that follow the shape of the duty function. For this reason, the steady-state voltage values of the bootstrap capacitor at the top (C_{bs6}), and the one connected to the switch node (C_{bs4}) are the most crucial for the safe operation of a 4L TP PFC. Designed bootstrap loop can be seen in Fig. 13 and Eq. (19) can be used to determine the required minimum DC bias voltage for an N level TPPFC converter.

$$V_{Bias_{ave}} > V_{gate} + [2(N-1)]V_{diode} \tag{19}$$

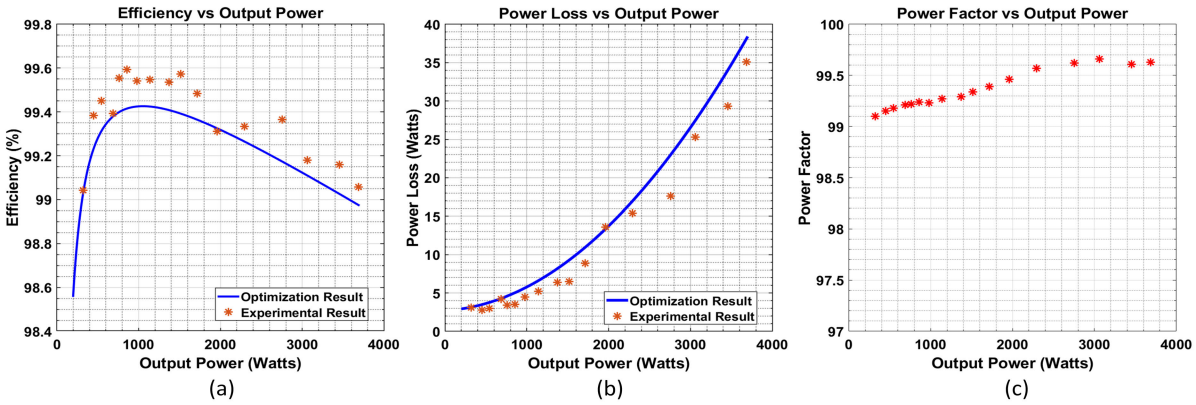

FIGURE 17. The comparison of the experimental and optimization framework results of the optimum 4L TP PFC converter; (a) efficiency (b) power loss (c) power factor.

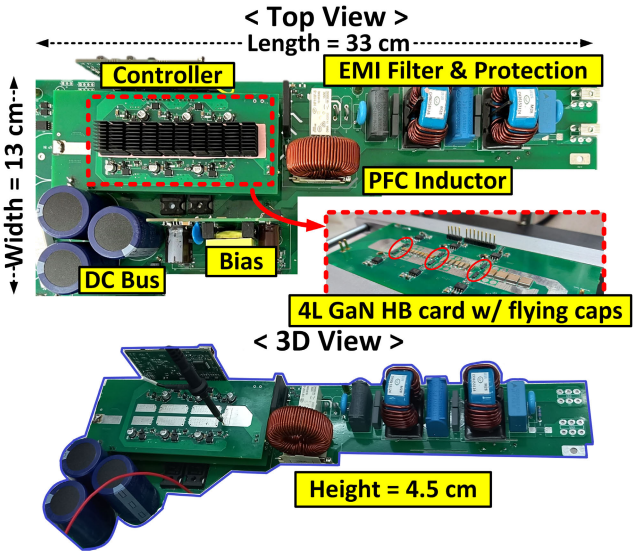

FIGURE 18. The designed 4L TP PFC converter prototype.

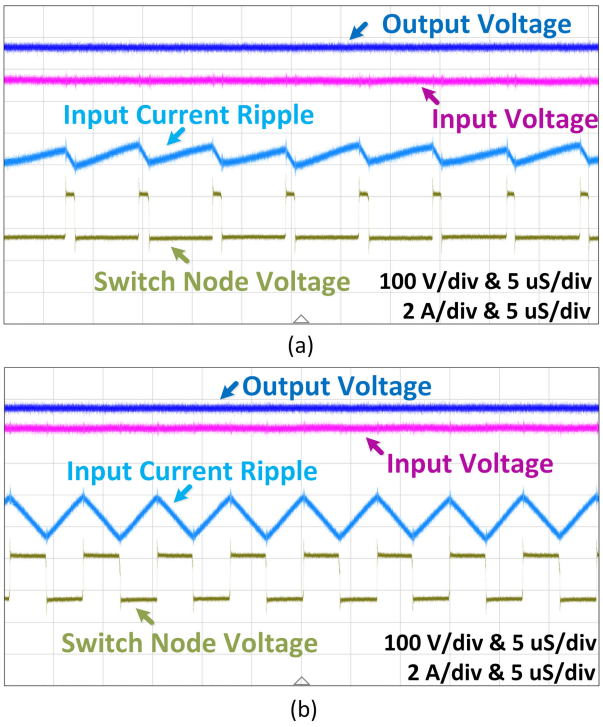

FIGURE 19. The current ripple within a switching cycle; (a) duty = 0.8, (b) duty = 0.5.

where V_{diode} is the forward voltage drop of bootstrap diodes, $V_{Biasave}$ is the minimum required DC voltage supply, and V_{gate} is the gate drive voltage of HF FET. In practical applications, low-frequency ripples caused by duty ratio variations during AC line cycle can jeopardize the secure charge-discharge process of bootstrap capacitors as shown in Fig. 14. Therefore, determining the minimum required bootstrap capacitance is a crucial aspect of the design process. A bootstrap capacitor in ML TPPFC converters has to provide necessary charge to its corresponding driver (p) while feeding upper switches ($p+1$ to q). To secure bootstrap operation, necessary calculations for minimum required bootstrap capacitor value has to be done considering worst case scenario ($D = 1$). During the time (ΔT_p) that p^{th} bootstrap capacitor feeds upper switches, it needs not only to keep minimum required voltage level for its corresponding driver, but also compensate voltage drop over the FETs in the longest boostrap loop. Notating the bottom capacitor as 1 and topmost capacitor as q, and calculated capacitor as p, required minimum capacitance value for p^{th} FET driver can be calculated as given in Eq. (20) [23].

$$C_{bs_p} > \frac{(i_p + (\Sigma_{k=p+1}^{q} i_k))\Delta T_p}{(V_{bs} - (p-1)V_{diode}) - (V_{bs_{min}} + (q-(p+1)V_{FET}))} \tag{20}$$

where V_{bs} is the power supply voltage, V_{diode} is the voltage drop of a bootstrap diode, $V_{bs_{min}}$ is the minimum voltage that has to be stored in the topmost bootstrap capacitor

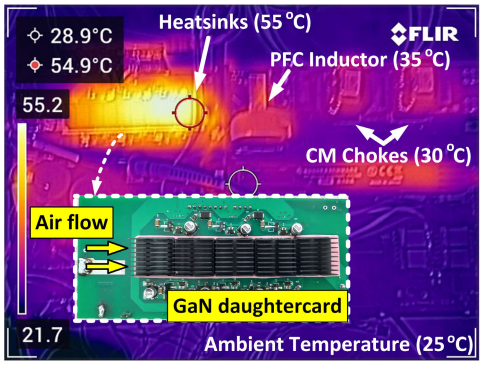

FIGURE 20. The thermal image of the converter when the output power is 3.7 kW.

(n^{th} capacitor) and V_{FET} is the forward voltage drop of a FET in the bootstrap loop.

D. THERMAL CONSIDERATIONS

In earlier sections, the importance of minimizing loop inductances for the secure operation of FETs has been discussed. However, there is a trade-off point between package inductance and thermal resistance of the package. FETs with smaller packages are expected to have higher thermal resistances. As a result, while efforts are made to reduce package inductance, there is a considerable increase in the thermal resistance of the FETs. To ensure proper cooling, the thermal resistance of the PCB must also be reduced. Fig. 15 illustrates PCB vias, indicated by red boxes, which are intentionally implemented to dissipate the heat generated to a heatsink located on the other side of the PCB. To verify the thermal model used in the optimization framework and test the thermal performance of the power stage with the determined bottom-side cooling system, a solid-state 3D model of the FET and resultant per half-bridge scaled-down heatsink is created using finite-element-analysis tool, as shown in Fig. 16. The junction-to-sink thermal resistance of the designed board was calculated as $19,76^oC/W$ with the help of simulations. Subsequently, HF FETs were mounted on the manufactured power stage board and forced to dissipate 2.3 W of power per half-bridge, which is the dissipated power per half-bridge provided by the proposed optimization tool. The experimental results have shown that the junction-to-sink thermal resistance of the designed board is $21.47^oC/W$, which is very close to the simulated value. The temperature difference between simulations and experiments is caused by the size difference of heatsinks. The heatsink used in experiments is for three half-bridges of a 4L TP PFC converter, whereas the simulated ones uses a scaled-down heatsink per half-bridge.

VI. THE OPTIMAL 4L TP PFC DESIGN

The proposed algorithm was used to identify the optimum design from a pool of 32, 000 created designs. A 4L TP PFC topology with 108 μH PFC inductance and 45 kHz switching

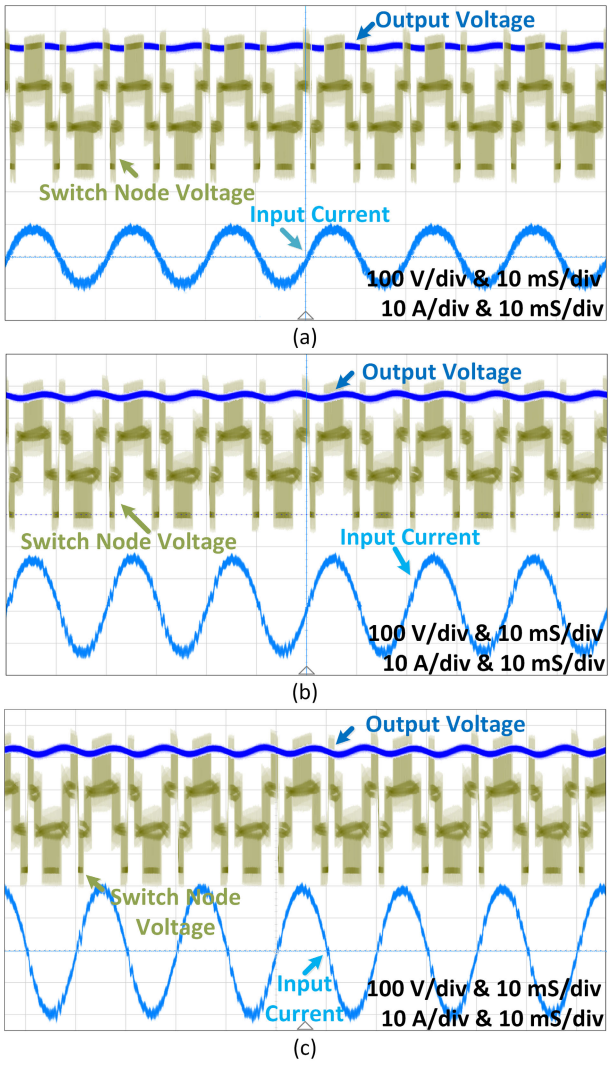

FIGURE 21. The experimental waveforms taken at different output power conditions; (a) 1.4 kW, (b) 2.5 kW, (c) 3.7 kW.

frequency was determined as the most favorable design. The selected components and operating conditions are presented in Table 1. The GaN power stage and flying capacitors are manufactured as daughter cards and mounted on the main board. The converter designed in this study achieved a peak efficiency of 99.6% at around 1 kW, and maintained an efficiency above 99% up to full load, as depicted in Fig. 17 (a). The accuracy of the algorithm was experimentally verified by comparing the estimated power losses with the measured values, as illustrated in Fig. 17 (b). As it can be seen from Fig. 17 (b), the optimization framework calculates the expected power loss and efficiency with some error. It should be noted that the power losses of the bias circuit were not included in either the experimental or optimization results. The DC resistance of the relay was also determined and added to the optimization framework as 20 mΩ. Additionally, the power losses of the PCB lines and power connectors were calculated to be 1.3 W and added to the optimization results as

TABLE 1. Details of the optimum design.

Design parameter	Value/component
Switching frequency	45 kHz
PFC inductance	108 μH
High-frequency FETs	6 x EPC2215
Low-frequency (rectifier) FETs	4 x FCH029N65S3
PFC inductor details	1 core stack (KM 0059083A2) 2 layers (AWG 10, 37 turns)
Bus capacitors	3 x 470 μF
Flying capacitors	2 x 22 μF
Heatsinks	5 x UB1912

a constant value. The achieved power factor is above 0.99 as seen from Fig. 17 (c). Designed 3.7 kW 4L TPPFC converter prototype can be seen in Fig. 18.

Fig. 19 shows the input current ripple and its relationship with the duty ratio of the HF FETs within a switching cycle. Despite the use of a 108 μH inductor with a switching frequency of 45 kHz, the input current ripple remains low due to the 135 kHz effective frequency seen by the inductor. The thermal testing was conducted at 3.7 kW operation with 400 LFM cooling, and the resulting thermal distribution is presented in Fig. 20. As can be seen from the Fig. 20, the converter is thermally safe and stable at full load operation. Lastly, the waveforms for three different output power levels of the designed 4L TP PFC are also presented in Fig. 21.

VII. CONCLUSION

This paper proposed an optimization framework for ML TP PFC converters to tackle the complexity of the design process involving numerous parameters and complex trade-offs between components. To create framework, PFC inductor, high-frequency line FETs, heatsink, bus capacitor, flying capacitor, low-frequency rectifying FETs and EMI filter design and selection algorithms are developed one-by-one. Then, electrical, magnetic, thermal, geometric and economical properties of hundreds of components are stored in the created databases. After all, the proposed framework is used for 3L, 4L and 5L TP PFC topologies with switching frequencies ranging from 25 kHz to 135 kHz and PFC inductance values between 20 μH and 400 μH. The local cost function considers total volume, total loss and total cost as constraints with weights of 0.6 for volume, 0.2 for efficiency and 0.2 for cost to ensure high power density.

The 4L TP PFC converter with 108 μH PFC inductance and 45 kHz switching frequency is found to be optimal for the chosen cost function, resulting in an efficiency of 99.6% at quarter load and 99.1% at full load with an input power factor above 0.99 in all operating intervals. The power density is calculated as 67 W/in^3. Experimental results confirm the success of the system level optimization approach, showing good agreement between the calculated and measured results. Overall, the proposed framework offers additional benefits, enabling the optimization of cost, efficiency, volume, and power density simultaneously based on the desired cost function.

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