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RESEARCH ARTICLE

Long-Range Pulse Interactions in Unclocked FPGAs

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ABSTRACT Evidence of long-range interactions between logic transitions in unclocked FPGA circuits is reported. The relative positions of pulses traveling in digital feedback loops are observed to dynamically interact and move to equal spacing over long timescales. We confirm the presence of this interaction over different FPGA supply voltages and hypothesize the pulse interactions are due to current draw in the power distribution network of the FPGA. This pulse interaction effect is observed for different FPGA families and manufacturers, including Altera and Xilinx, and has been tested using both look-up table (LUT) and carry chain (CC) logic to realize the feedback delays.

INDEX TERMS Asynchronous circuits, feedback circuits, field-programmable gate arrays, pulse circuits, pulse interactions, non-blocking delay lines, oscillators, network dynamics, transient analysis.

I. INTRODUCTION

Technologies that use unclocked or asynchronous logic designs in Field-Programmable Gate Arrays (FPGAs) to realize software-defined delays are prevalent throughout the engineering literature. Recent applications include time-to-digital converters (TDCs) [1], [2], physically unclonable functions (PUFs) [3], [4], [5], [6], [7], true random number generators (TRNGs) [8], [9], [10], [11], and reservoir computers [12], [13], [14]. In many of these designs, cascaded logic elements (often an even number of inverters or NOT-gates [15], [16]) are used to approximate ideal delays for logic levels and switching times. However, as software-defined delays in FPGAs continue to be used in designs, it is important to explore and understand non-ideal behaviors, particularly those that may occur on unexpected timescales.

In this paper, we use a FPGA design comprising an unclocked delay line with feedback to demonstrate an unanticipated effect: voltage transitions of injected nanosecond pulses can weakly interact across timescales that are on the order of hundreds of nanoseconds to microseconds. In other words, within a feedback loop configuration, long-range interactions (i.e. coupling) is present between the voltage pulses. This coupling causes pulses to repel one another with a "force" that is inversely proportional to their separation distance. A conceptual illustration of the pulse interactions is shown in Fig. 1a with two pulses traveling in a closed feedback loop. With each cycle around the loop, pulses separate until a steady-state of approximately equal pulse spacing is eventually realized, a phenomenon we refer to as *pulse timing equalization* (PTE).

Interactions between pulses in feedback loops that result in PTE have been previously reported in both electronic and optical systems. Micro-pipeline rings [17], self-timed ring oscillators [18], [19], and collective pulse oscillators [20] include feedback for active jitter suppression. In these fully-electronic systems, voltage pulses and feedback times are on similar timescales, and PTE can be achieved with a relatively short number of round trips in the feedback loops ($<$50 to 500). In contrast, optical feedback systems can have long range pulse interactions, where there is a large separation in timescales between pulse timing and the feedback delay times [21], [22]; these long-range interactions are a weaker coupling, and PTE manifests after thousands of cycles in a feedback loop.

Here, we demonstrate that a similar long-range interaction occurs in FPGAs such that it requires $\sim$5, 000 cycles of the feedback loop to observe PTE. For example, in Fig. 1b, we

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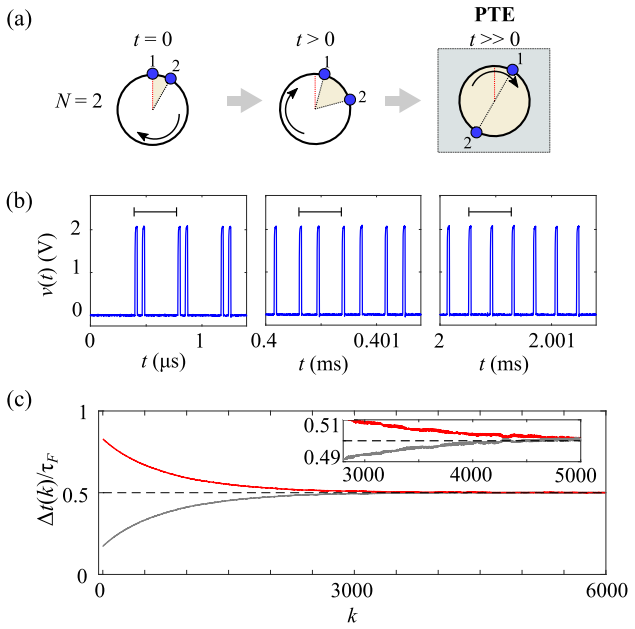

FIGURE 1. (a) Conceptual illustrations of the relative pulse positions for $N = 2$ pulses traveling in a FPGA feedback loop. Snapshots of the relative pulse positions are shown for the initial state at $t = 0$, a relatively short time into future $t > 0$, and a relatively long time in the future $t \gg 0$ where pulse timing equalization (PTE) is achieved. (b) Measured output voltage $v(t)$ from the feedback loop with horizontal bars to indicate an approximate round trip time, and (c) inter-pulse spacings $\Delta t(k)/\tau_F$ as a function of the number of pulse cycles k with a dashed line at $1/N$ for $N = 2$ pulses. Color traces are used for a visual aid to follow the interpulse spacings in the insets.

plot the observed output pulses from an unclocked feedback loop in an Artix 7 FPGA after two pulses of widths $\tau_W \sim 22$ns are injected (experimental details are presented later). The pulses are shown at $t = 0$ with a small separation (∼60ns between rise times) that grows by $t = 0.4$ms and eventually reaches a stable state with equal spacing by $t = 2$ms.

We measure the times between successive rising edges Δt as a function of the number of cycles k in the loop and normalize them using the feedback loop delay time $\tau_F \sim 0.39\ \mu$s. The observed results are shown in Fig. 1c. The PTE steady-state is represented by a $\Delta t/\tau_F = 1/N$, where N is the number of pulses (For reference, the $N = 1$ case is presented in the Appendix). Note, the acceleration of the pulses as they move away from one another (i.e., the magnitude of the slopes for the $\Delta t/\tau_F$ curves) decreases over time, indicating that pulses repel each other less when they are further apart. The initial movement of each pulse through the feedback loop is ∼200 ps per revolution, and this value decreases exponentially with each cycle.

After the PTE state is achieved, jitter in the inter-pulse spacing is present with a maximum observed amplitude of approximately 2ns (that can be traced to noise and fluctuations in the power supply of the FPGA and, to the best of our knowledge, are not a major contributing factor to the dynamics). Lastly in Fig, 1c, we note that the pulse separations equalize after approximately after $k = 5,000$, which corresponds to a timescale of $5,000\tau_F \sim 1.9$ms. This is evidence of both long-range interactions and a surprisingly long transient given the fast timescales normally associated with unclocked FPGAs.

In the remainder of this work, we first present details of our experimental setup. We next demonstrate long-range interactions and timing equalization for initializations containing both three and four pulses. We then investigate the effect of the FPGA supply voltage on the pulse interactions. Lastly, we discuss the additional configurations that have been and will need to be explored to better understand this phenomenon and place these results in the boarder context of the literature.

II. EXPERIMENTAL SETUP

A schematic of the unclocked FPGA feedback loop is shown in Fig. 2a. In the figure, a delay block is composed of cascaded copies of unclocked logic elements to realize the feedback delay time τ_F. In this example, the logic elements are an even number of NOT-gates that are realized in the FPGA using 1,260 Look Up Tables (LUTs). An OR-gate is then used as the injection point for initial pulses of equal widths τ_W in different initial patterns, which then drive an unclocked pulse repeater (PR) structure. The PR replicates input pulses upon incident rising edges and preserves τW while allowing the inter-pulse spacings Δt to change (Pulse width preservation is necessary because an imbalance in the rise and fall times of FPGA logic elements can cause pulses circulating in unclocked feedback loops to collapse [23]). An AND-gate in the feedback path is used with a voltage sw to open and close the feedback loop with a switch. The switch is opened to ensure there are no transitions in the loop, and then it is closed prior to injecting pulses. Details of the PR and pulse initialization are in the Appendix.

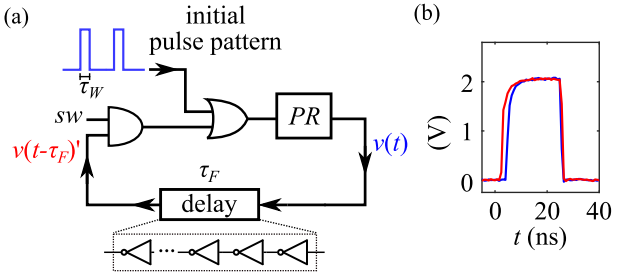

FIGURE 2. (a) Experimental setup for studying long-range interactions between pulses in an unclocked FPGA delay line. (b) Measured $v(t)$ as $v(t - \tau_F)'$ [blue and red, respectively] for a pulse that travels through the digital feedback delay.

In our experiments, an oscilloscope measures the time evolution of the output of the PR structure $v(t)$ as well as the delayed version of $v(t)$. In Fig. 2a, we label this delayed version of $v(t)$ as $v(t - \tau_F)'$, where in an ideal case the two voltages are identical except for a delay. However, for injected pulses, we note that the digital feedback induces a slight pulse lengthening in $v(t - \tau_F'$. Direct measurements of $v(t)$ and $v(t - \tau_F)'$ are plotted in Fig. 2b. Experiments were conducted

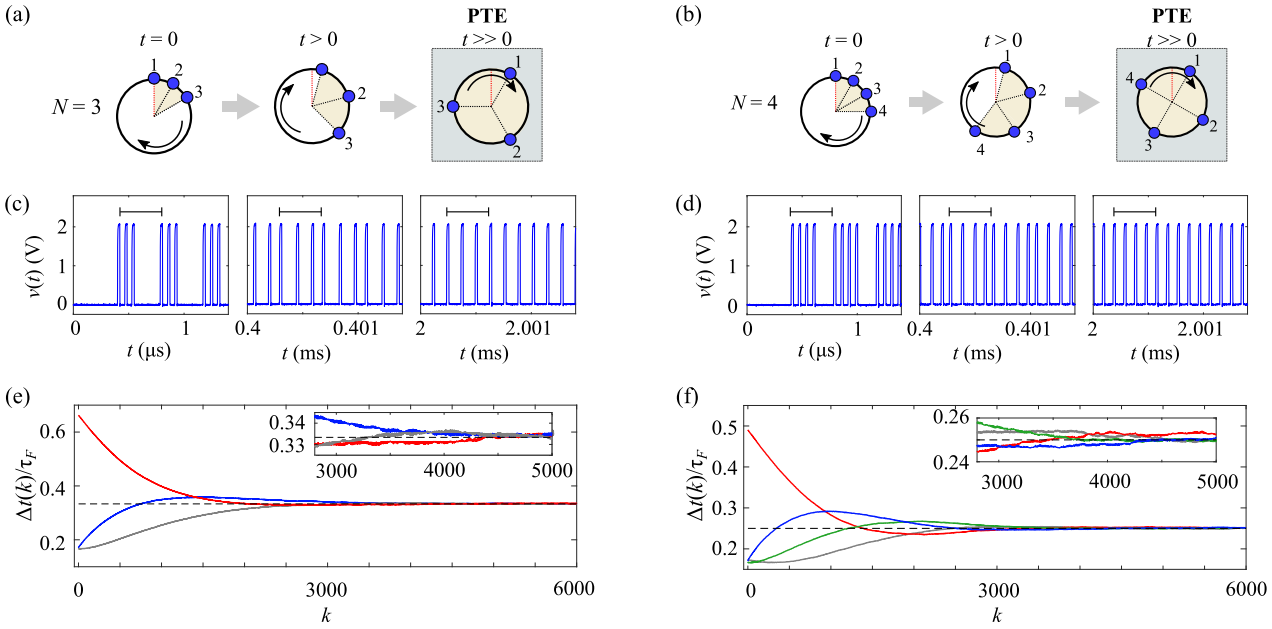

FIGURE 3. (a)–(b) Conceptual illustrations of pulses in the FPGA feedback loops, where blue circles represent $N = 3$ or $N = 4$ pulses at $t = 0$, $t > 0$, and with PTE achieved after $t \gg 0$. (c)–(d) FPGA results for $N = 3$ and $N = 4$ initial pulse patterns. (e)–(f) Corresponding $\Delta t(k)/\tau_F$ curves with dashed reference lines at $1/N$. Color traces are used for a visual aid to follow the interpulse spacings in the insets.

using an Artix 7 on the NewAE CW305 FPGA development board. Time series are collected using a Tektronix 6 Series Mixed Signal Oscilloscope with 4 GHz of analog bandwidth and recorded for 10ms with a sampling rate of 1.25 GSa/s. Details of the PR logic structure and pulse patterns of widths τ_W are provided in the Appendix.

III. PULSE INTERACTION RESULTS

Using this experimental setup, we initialize the system with different pulse width configurations. In 3a-b, we show conceptual depictions for $N = 3$ and $N = 4$ and plot the resulting $v(t)$ from injecting the different pulse configurations in Fig. 3c-f (Note, $v(t - \tau_F)'$ is omitted because it is quantitatively similar to Fig. 2b). For each case, time series snapshots are shown at $t \sim 0$, $t = 0.4$ms, and $t \sim 2$ms. Similar to the $N = 2$ case, transients last for $\sim 5,000$ round trips of the feedback loop before PTE is observed. However, in these cases, the slopes of some of the $\Delta t/\tau_F$ curves are non-monotonic as they eventually approach a slope of zero, indicating that the interaction is slightly more complex than the $N = 2$ case. Regardless, each case demonstrates that the transients of the dynamics depend on the initial spacing, and that the pulse spacings undergo nontrivial dynamics before arriving at the $1/N$ steady state.

To explore a possible explanation for the pulse interactions, we investigate the effect of a changing supply voltage for the FPGA. For this study, we leverage a unique aspect of the selected FPGA development board (NewAE CW305): the DC supply voltage V_{cc} of the FPGA can be provided from an external source. This allows us to investigate the impact of changing the FPGA supply voltage to the observed long-range interactions and PTE. Note, $V_{cc} = 1.0$ V is used for the experiments conducted in Fig. 1 and Fig. 3. For the purposes of testing different values of V_{cc}, we focus on the interaction of only two pulses. For each value of V_{cc}, we reset the system, inject pulses, and record the transient behaviors.

Test results over a selected range of supply voltages V_{cc} are shown in Fig. 4a. In the figure, we first plot the observed pulse widths $\tau_W(V_{cc})$ and the feedback delay $\tau_W(V_{cc})$ as a function of supply voltage. As expected, for lower values of V_{cc}, the FPGA runs slower (propagation times through unclocked logic elements increase with decreasing supply voltage). This effect causes all delay elements, including those used to generate the pulses, to change with V_{cc}.

Fig. 4b shows the measured $N = 2$ inter-pulse spacings $\tau_W(V_{cc})$ for each value of V_{cc}. Interestingly, the length of the transient to achieve PTE depends on the supply voltage; a higher supply voltage requires more round trips to achieve the steady state. This indicates a possible dependency on τ_W and τ_F for the amount of interaction (i.e., coupling strength) that occurs between two pulses as they move around the feedback loop; future investigations will examine this relationship systematically.

IV. ALTERNATIVE EXPERIMENTAL SETUPS

Given there are many different FPGA technologies and alternative delay elements (e.g., carry chains), we provide additional experimental results in Appendices C and D.

In particular, we replace the inverter feedback delay in Fig. 2a with set of cascaded carry chains (CCs) in the Artix 7

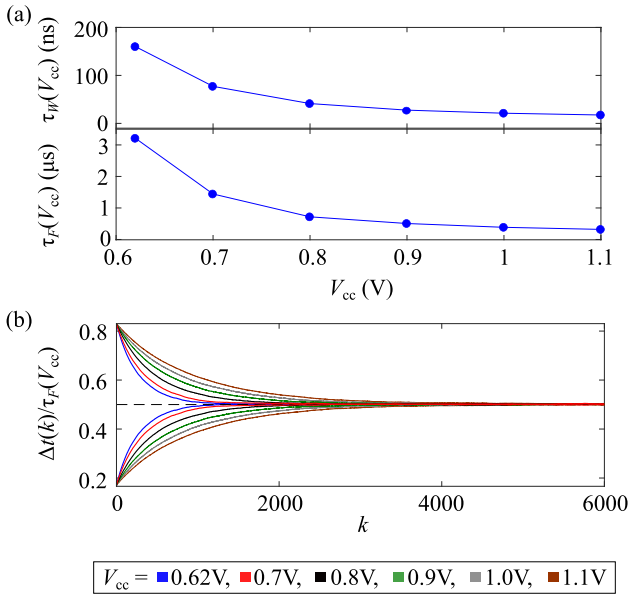

FIGURE 4. **(a) Observed pulse width τ_W from the PR and feedback delay time τ_F as a function of the supply voltage V_{cc}. (b) Scaled inter-pulse spacing $\Delta t/\tau_F$ for each of the supply voltage in the $N = 2$ case.**

on the NewAE CW305 FPGA development board. Featured in Appendix C, CC results indicate long range interactions and quantitatively similar PTE for the $N = 2$, $N = 3$ and $N = 4$ cases. To highlight the robustness of these results, Appendix C also includes two additional sets of data: (1) repeated PTE in CCs for the $N = 2$ and $N = 4$ cases from the same initialization conditions, and (2) alternative initial pulse spacing in the $N = 3$ case.

In addition, using a Cyclone V FPGA we provide two sets of data that demonstrate quantitatively similar PTE for the $N = 2$, 3, and 4 cases. The two data sets correspond to experiments that use different sizes of the feedback loop and pulse widths (i.e., different parameter scalings). Details of the experimental setup are provided in Appendix D. This shows it is possible to see the long-range interactions in both Intel and Xilinx chips and that the PTE can be observed using feedback loops of different sizes.

Lastly, as a control, we have also performed experiments using a 500-foot external, RG58 coaxial cable as the feedback delay (to match the $\sim$ 0.39's LUT delay in Fig. 2a) and do not observe these interactions; instead, we observe that pulses are not repelled in the coaxial cable and can collide.

V. DISCUSSION AND FUTURE WORK

One important future direction involves modeling the long-range interactions reported here. Modeling efforts will greatly enhance our understanding of this phenomenon, but we acknowledge the difficulty involved with modeling the nuances of the pulse-to-pulse interactions across all parameter regimes (pulse widths, supply voltages, LUTs vs. CCs, etc.) and compiler settings; the compilers (Vivado and Quartus) placed the designs used in all our data collection.

As we continue our future investigations, individualized models may be necessary for each delay type, compiler placement of the logic, and chip technology, particularly because each chip may have a different configuration of its power distribution network across LUTs and CCs. Rather than withhold these results until a fully comprehensive model is developed that can predict the observed dynamics in each of the observed experiments, we choose to report the experimental observations now to motivate future research among FPGA designers and the dynamics community. Additional studies into the pulse widths, pulse width intervals, and number of LUTs will be needed to fully vet the robustness of this phenomenon in FPGAs.

As an initial motivation for future modeling, we note that in both [20] and [24] there exists some type of pulse coupling model such that the time for a pulse going around a loop depends on the interval between it and the preceding pulse in the delay. These types of models require a mechanism for altering the time of a pulse around the feedback loop. In addition, there are well-documented cases of voltage drops occurring in power distribution networks of FPGAs due to asynchronous switching that results in increased propagation delays of logic elements [25], [26], [27]. While these are typically transient effects, they provide a direction for continuing our investigations into probing and modeling these long-range interactions. In our system, we know from Fig. 4 that the FPGA supply voltage can impact the time for a pulse to travel around the feedback loop. Thus, we can hypothesize that the long-range interactions are likely caused by small changes to the supply voltage of the FPGA (i.e. the power distribution network) that contains the delay as pulses circulate in the feedback loop.

We also note that various works in the literature inspired our interpretations of the observed PTE and will likely help guide the future modeling. For examine, the format of Fig. 1a and Fig. 3a-b is inspired by Kuramoto phase oscillators. Similar pictures have been used to represent these oscillators, where a circle is a revolution of 2π and numbered points are the phases of oscillators. Reference [28] even shows nearest-neighbor coupling with phases becoming equally spaced over 2π after a transient.

In addition, PTE in FPGAs is an emergent behavior from interacting elements, a property often associated with biological systems or networks. Genetic networks are often considered systems with asynchronous switching, and studies have examined models for genetic feedback loops that support stable pulses [29]. In addition, cellular phenomenon such as molecular time sharing, single-file dynamics, and spiking in excitable cells with delayed feedback have all been reported to show a similar balanced timing through coupled interactions [30], [31], [32]. We hope this work provides a new method for studying and engineering emergent behaviors.

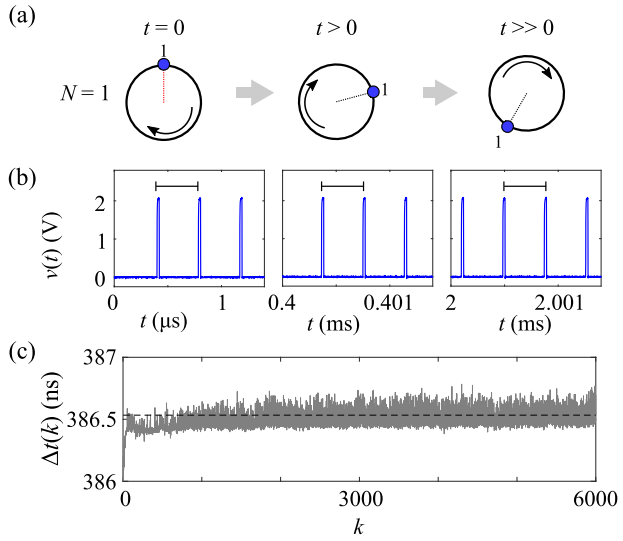

FIGURE 5. $N = 1$ case at $V_{cc} = 1.0$V. (a) Conceptual diagram of a single pulse cycling in the feedback loop. (b) Time evolution of the voltage pulse cycling in the experimental feedback loop. (c) Unscaled measurement of the inter-pulse spacing Δt as a function of the cycle number k.

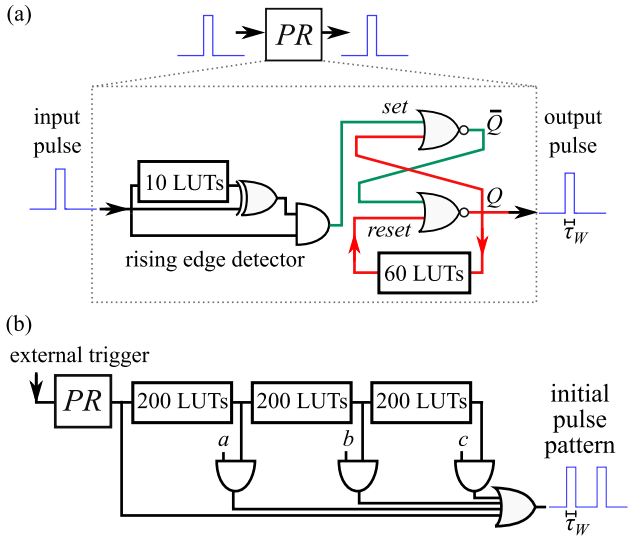

FIGURE 6. (a) Pulse Repeater (PR) structure that uses a rising edge detector and a Set-Reset (SR) latch with feedback to produce pulses of width τ_W. (b) Pulse initialization structure that uses a trigger, the PR, and a tapped delay line with AND-gates that serve as switches with switching voltages a, b, and c.

Lastly, we place our results within the context of other unclocked FPGA systems that have been engineered to study dynamics-related phenomena. In the past decade, there has been a growth of scientific experiments that use unclocked FPGAs as a platform for studying network science. These include studies of Boolean chaos [33], pulse coupled systems and synchronization [34], chimera states in phase oscillators [35], super transients in ring oscillators [24], as well as other mechanisms that can lead to coupling of transition times in FPGAs [36]. While each of these studies is not focused on FPGA design principles, they provide new insight into

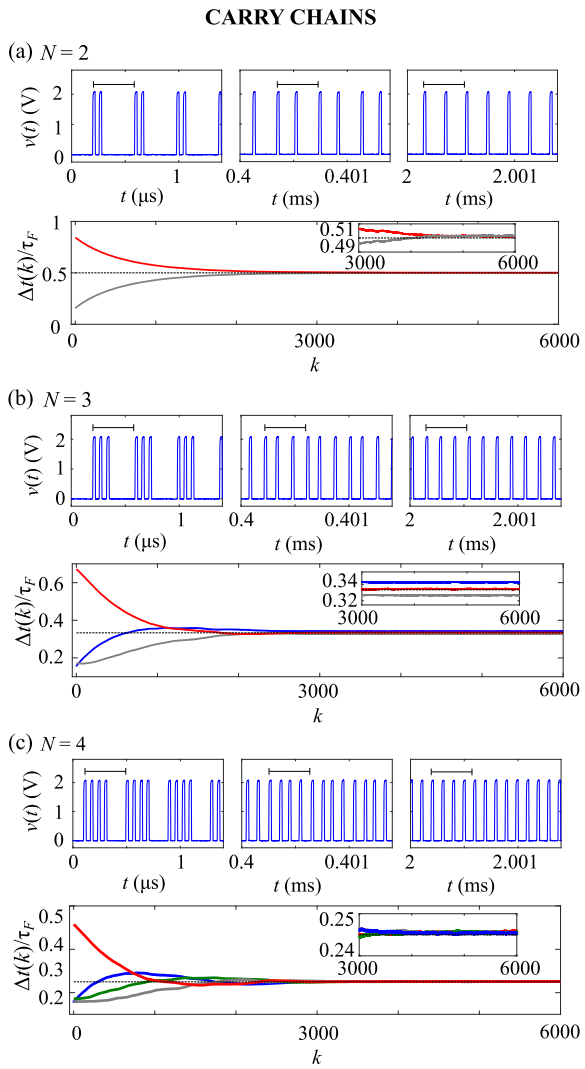

FIGURE 7. Artix 7 Carry chain experiments for the (a) $N = 2$, (b) $N = 3$, and (c) $N = 4$ cases using CCs in the feedback delay loop.

non-ideal FPGA properties that can be quantified using dynamics, similar to the observed PTE transients.

VI. CONCLUSION

In summary, we report experimental evidence of long-range interactions between FPGA logic transitions in asynchronous delays. Overall, these interactions appear to have microscopic impacts on pulse spacing during a single transit through an unclocked delay line. However, in a feedback loop configuration, the interactions lead to transients with timescales that are orders of magnitude greater than those normally associated with unclocked FPGAs and cause nontrivial, macroscopic changes to the timing of logic transitions. The behaviors presented appear generalizable and should be noted as a potential contributor in all unclocked delays. This is particularly important for technologies that leverage unclocked feedback

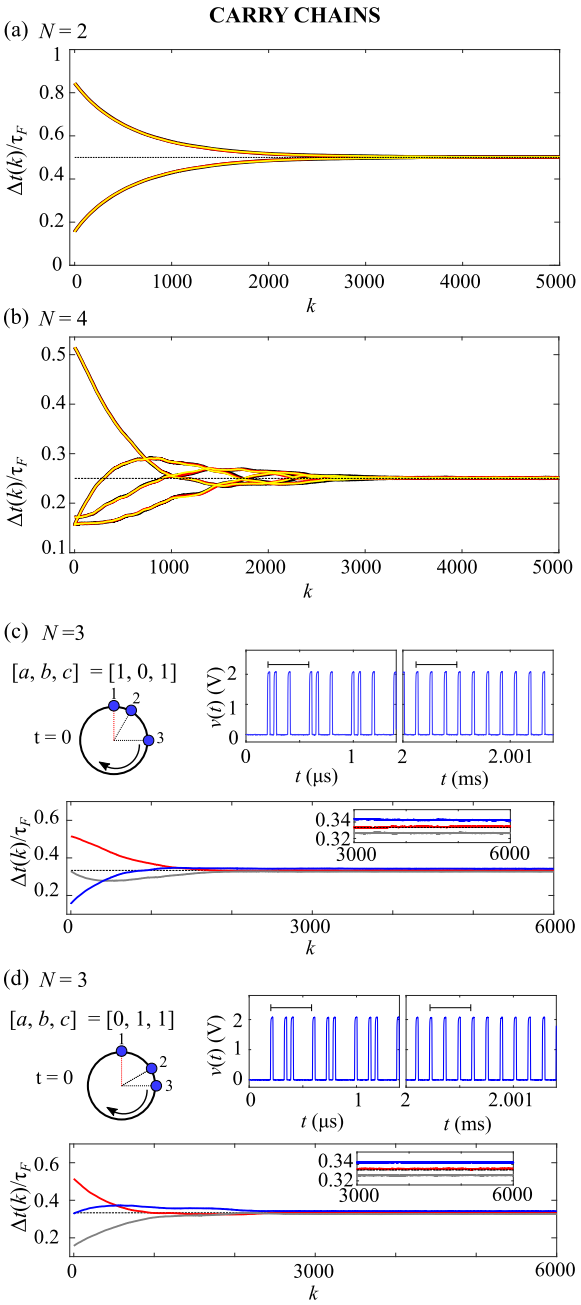

FIGURE 8. Repeated carry chain results for (a) $N = 2$ and (b) $N = 4$ cases. Black, red, and yellow traces each represent separate PTE transients from the same initial conditions. Alternative $N = 3$ initial pulse spacing setups for carry chain feedback using (c) $[a, b, c] = [1, 0, 1]$ and (d) $[a, b, c] = [0, 1, 1]$.

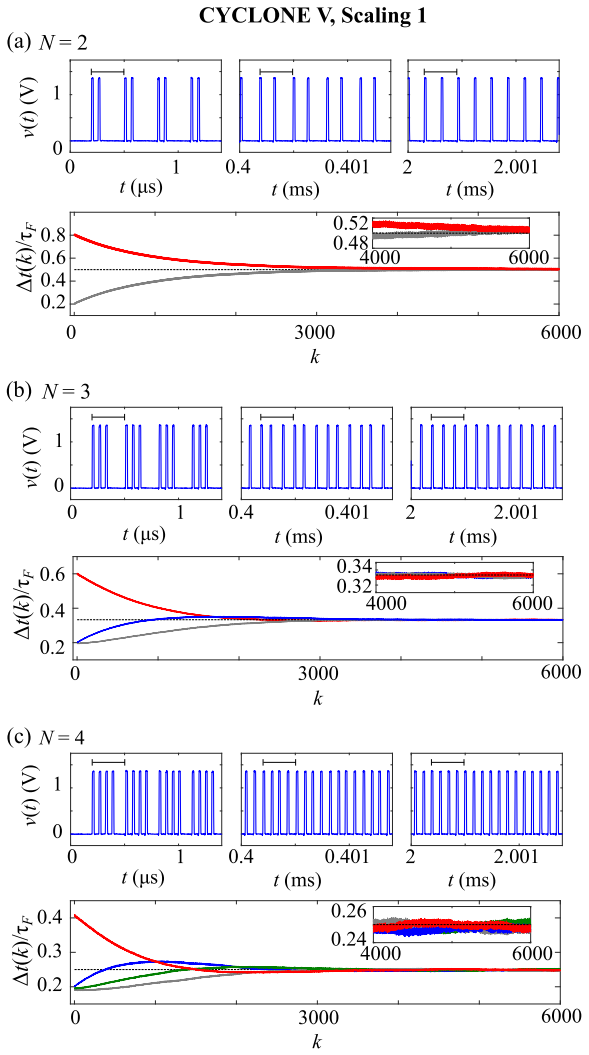

FIGURE 9. Cyclone V experiments using Scaling 1 for the (a) $N = 2$, (b) $N = 3$, and (c) $N = 4$ cases using 1,260 LUTs in the feedback delay loop.

loops in FPGAs and may assume that logic transitions do not interact over long timescales.

APPENDIX A
SINGLE PULSE CASE

For completeness, we show the $N = 1$ pulse initiation in Fig. 5. In the figure, the inter-pulse spacing is approximately constant. Figure 5c highlights this with an unscaled representation of Δt. A minor transient is present in the feedback time, which is likely due to settling of the FPGA supply voltage once a pulse is injected in the feedback loop.

APPENDIX B
PULSE REPEATER

Details of the experimental pulse repeater (PR) and pulse initialization structure are shown in Fig. 6. The PR in Fig. 6a first uses unclocked logic and LUTs to create a rising edge detector that outputs a short pulse (∼3ns) upon an input pulse (>10ns). The output of the rising edge detector then triggers an unclocked set-reset (SR) latch with delayed feedback between the output and the reset. The delayed feedback is realized using 60 LUTs, which produces the pulses of width $\tau_W \sim 22$ns used in all of the experimental results presented in this manuscript.

The on-chip, pulse initialize structure that allows us to change between $N = 1, 2, 3$, and 4 is shown in Fig. 6b.

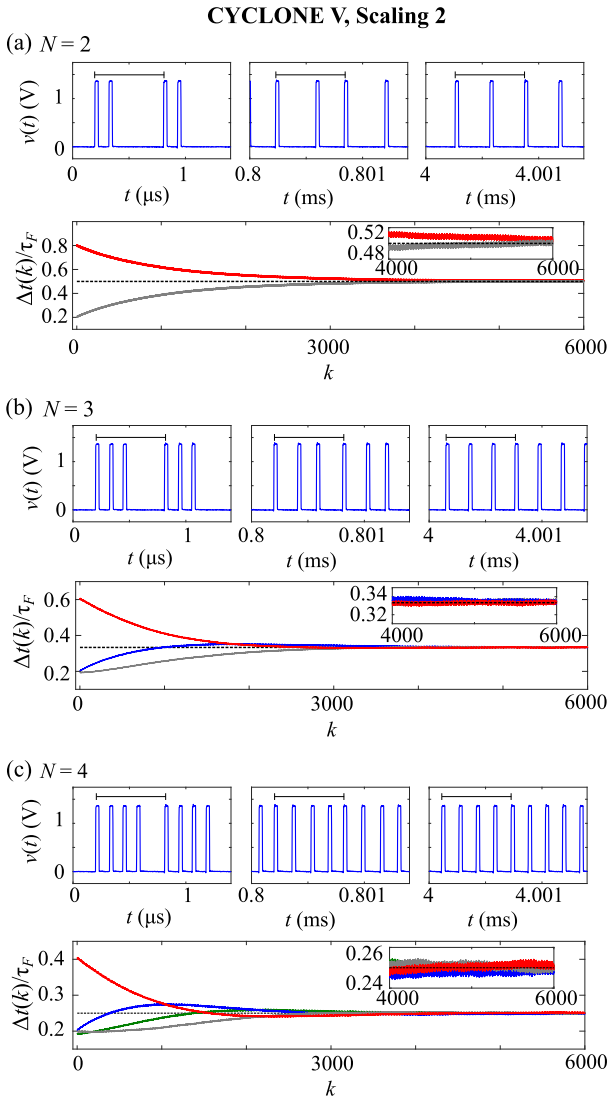

FIGURE 10. Cyclone V experiments using Scaling 2 for the (a) $N = 2$, (b) $N = 3$, and (c) $N = 4$ cases using 2,520 LUTs in the feedback delay loop, which is doubled compared to Scaling 1. Pulse widths and initial pulse spacing are also doubled compared to Scaling 1.

The initialization uses an external trigger (e.g. a debounced button) and a copy of the PR in order to launch a pulse of width τ_W down a tapped delay line, where the spacing of the taps is 200 LUTs or ∼60ns. At each tap, an AND-gate serves as a switch to control the number of pulses that accumulate at the output of final OR-gate.

APPENDIX C
CARRY CHAIN RESULTS

Carry chains (CCs) are dedicated logic structures in FPGAs meant for arithmetic and can be cascaded to form unclocked delay lines. Experiments using CCs substituted for the feedback delay in 2a were conducted using the Artix 7 on the NewAE CW305 FPGA. The CC feedback delay uses 20,000 CCs to realize a feedback delay of $\tau_F \sim 390$ns. To isolate the CC feedback delay, we continued to use the same number of LUTs in the pulse-repeater and pulse initialization structures such that $\tau_W \sim 22$ns and the initial pulse spacing is still around 60ns. Outputs for the $N = 2$, 3, and 4 cases are shown in Fig. 7. We note that long range interactions and PTE are present in all cases, where the $N = 3$ case settles with a small visible offset; this offset is approximately two orders of magnitude smaller than the overall pulse-spacing changes that are observed during the PTE transient.

Next, for each of the $N = 2$ and $N = 4$ cases, we repeat the data collection procedures three times in order to examine the robustness of the PTE phenomenon. Results of these repeated experiments are plotted on top of one another in Fig. 8a-b. This highlights the robustness of the PTE transient trajectories and timescales.

Lastly, we leverage the flexibility of the pulse initialization structure in Fig. 6b to create alternative $N = 3$ initial states. Two separate $N = 3$ initial pulse spacing setups were tested using $[a, b, c]$ equal to [1, 0, 1], and [0, 1, 1]. Results using these initial states for CC delay experimental setups are shown in 8c-d. Again, these results highlight the robustness of PTE and its timescales.

APPENDIX D
CYCLONE V RESULTS

Experiments using the setup in Fig. 2a were also conducted using a Cyclone V GX Starter Kit (5CGXFC5C6F27C7). The same number of LUTs is used in the pulse-repeater, pulse initialization, and feedback delay loop; we call this set of parameters 'Scaling 1'. Outputs for the $N = 2$, 3, and 4 cases using Scaling 1 are shown in Fig. 9, where $\tau_W \sim 22$ns, the initial pulse spacing is around 60ns, and $\tau_F \sim 390$ns. In all three cases, we observe PTE as the equilibrium state after approximately 5,000 cycles of the feedback loop.

Next, we leverage the simplicity of the experimental setup that uses only Verilog HDL and include a scaling parameter to double the number of LUTs used across the entire experimental system; this new scaling, deemed 'Scaling 2', causes a factor of two increase in the feedback loop delay as well as the pulse widths and pulse width spacing in the pulse initialization and pulse repeater structures. Results from this change in scaling are shown in Fig. 10, where long-range interactions between pulses and PTE are observed over a similar number of cycles.

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