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RESEARCH ARTICLE

CMOS Noise Analysis and Simulation From Low Frequency and Baseband to RF and Millimeter Wave

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ABSTRACT Generic guidelines for noise simulation of CMOS integrated circuits and advanced noise signal integrity analyses, were addressed in this work. The provided noise simulation guidelines are referring to a wide application spectrum, from baseband designs to high frequency RF/mmWave applications. Linear, periodic state and non-linear circuits, were used to categorize the noise simulation guidelines to the respective topology in which they can be applied. In addition, thermal, flicker and gate induced noise, were addressed, and classified with respect to the application field. Three test case vehicles were designed, each vehicle corresponds to a linear, periodic state or non-linear circuit topology. As a linear vehicle, an Operational Transconductance Amplifier (OTA) was designed, as a periodic state vehicle, a Voltage Controlled Oscillator (VCO) was designed while as a non-linear vehicle, a DC-to-DC Boost Converter was designed. Small-signal and large-signal noise analyses were benchmarked in terms of simulation time, compatibility and obtained accuracy. As small-signal analyses, AC noise, PNOISE and ENVLP analyses were performed, whereas as large-signal analyses, direct time domain (TRAN), PSS and QPSS analyses were performed in the respective topologies. Furthermore, using as a victim the VCO test case circuit, noise interference due to mutual coupling (mixing interference) was thoroughly addressed and simulation compatibility check was presented. Finally, noise simulation guidelines were efficiently summarized and categorized with respect to the circuit type and the application field.

INDEX TERMS Integrated circuits, noise simulation, signal integrity, linear circuits, periodic state circuits, non-linear circuits, noise simulation guidelines.

I. INTRODUCTION

Semiconductor technology is one of the most fast-paced developing aspects in the industry plane. From chips targeted to low frequency applications to advanced SoC designs operating in the RF/mmWave spectrum in mobile communication products, transistor noise is of high importance and must be addressed at the early stages of the design cycle procedure.

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Noise in general is generating by the chaotic and random movement of the device electrons. This random movement is caused by temperature fluctuations, hole and electron diffusion through a potential barrier and the indeterministic hole-electron recombination [1]. The above noise-generating phenomena are inevitably present when dealing with materials with semiconductor properties. The Signal-to-Noise ratio is of a grave importance in transceivers in RF/mmWave applications while data losses due to noise (Bit Error Rate – BER) can be observed in large electronic systems and mobile communication applications [2], [3], [4].

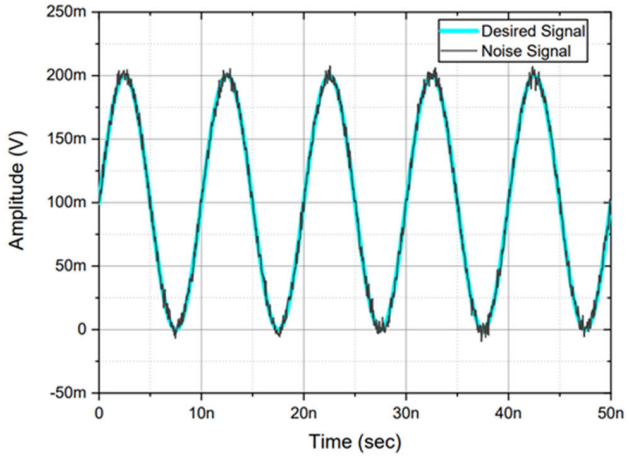

FIGURE 1. Desired signal and noise signal representation in the direct time domain.

In CMOS planar processes, the device noise must be thoroughly addressed to be able to accurately simulate the noise behavior of a design or even a full chip. Depending on the application field, the need of addressing all of the possible noise sources, is inefficient and redundant. Thus, it is wise to classify the noise sources of the circuit with respect to the operating frequency. This noise classification offers a more efficient time-wise and straight-forward noise analysis and simulation flow.

Integrated circuits can be categorized into three major categories, linear, periodic state, and non-linear topologies. Linear circuits, such as Operational Amplifiers (OpAmps), Low Noise Amplifiers (LNAs), Filters, etc., have a stationary DC operating point for biasing and it should be unaffected due to noise fluctuations. Periodic state circuits, such as Voltage-Controlled Oscillators (VCOs), Ring Oscillators, Mixers, etc., have a steady periodic state which indicates a steady oscillation frequency. Non-linear circuits, such as DC-to-DC converters, Sigma-Delta Modulators, ADCs, etc., have neither a stationary DC operating point, like linear circuit topologies, nor a steady periodic state, like periodic state circuit topologies.

Several works that have been so far presented, are including noise simulation results of the respective circuit under test. Most of them are addressing a single circuit topology, either a linear topology [5], [6], or a periodic state topology [7], [8], or even a non-linear topology [9], [10], thus limiting the noise simulation analyses that can be performed. The proposed work provides full noise simulation guidelines for all possible circuit categories while addressing all dominant noise sources of the circuit by having only the operating frequency as a parameter. Hence, the provided noise simulation guidelines are easily scalable circuit-wise and application-wise whereas they are difficult to find in the literature in such a concrete way.

II. CMOS NOISE SIMULATION

The commercial noise analysis tools commonly use the small-signal approximation and linearize the circuit equations to assess the noise behavior of the device. This linearization is valid only under the assumptions of a stationary operating point or a steady periodic state of the circuit under test. In addition, the small-signal approximation assumes that the device noise is a small perturbation added to the desired signal and thus, neither the operating point nor the periodic steady state are affected. Limitations and inaccurate results arise when large noise signals must be addressed which cannot be assumed as a small disturbance added to the desired signal.

A grave challenge of solving probability distributions of the circuit parameters arises when random noise sources were added into the circuit netlist. Gaussian probability distribution of the random circuit variables can be assumed to simplify the challenge and thus, allowing a circuit equation approximation using lower order distribution moments. Monte Carlo approach proved to be a practical method for solving direct time domain noise analysis equations [11], [12]. The desired signal as well as the random noise injection into the transient signal are depicted in Fig. 1. To be able to capture accurately the injected noise in the transient signal, the simulation time step should be aggressively decreased as to cover all the noise bandwidth, which typically is larger than the bandwidth of the circuit under test. Hence, due to the need of small simulation time steps, transient noise analysis is a rather time-consuming simulation compared to small-signal analysis methods.

Due to its nature and definition, transient noise analysis can be applied to any kind of baseband or RF/mmWave circuitry. When circuit classification is not applied, transient noise analysis is inefficient time-wise for the noise verification of a system. When an optimum classification of a circuit is applied, i.e. a stable DC operating point or a steady periodic state, small-signal analyses can be performed as to obtain accurate noise simulation results in a more time-conservative way.

In DC biased circuits with stationary operating points, AC noise small-signal analysis can be performed and accurate results in terms of noise behavior can be obtained. In linear circuits operating at the RF/mmWave frequency spectrum, S-parameter noise analysis can be performed to capture the noise behavior of the RF/mmWave circuit topologies. In periodic circuit topologies, a large-signal PSS analysis followed by a small-signal PNOISE analysis can be executed as to extract the noise figure of a circuit. In non-linear topologies, no other noise simulation alternative besides the transient noise, can be provided, thus noise simulation becomes a time-consuming procedure.

A. DIRECT TIME DOMAIN NOISE SIGNAL GENERATION

In the direct time domain noise analysis, the noise n(t) and the signal u(t) are lumped together, synthesizing the transient

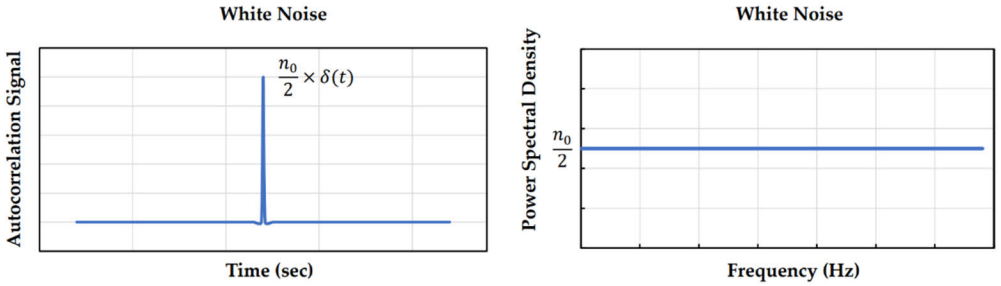

FIGURE 2. Autocorrelation function and the respective power spectral density (PSD) of white noise sources.

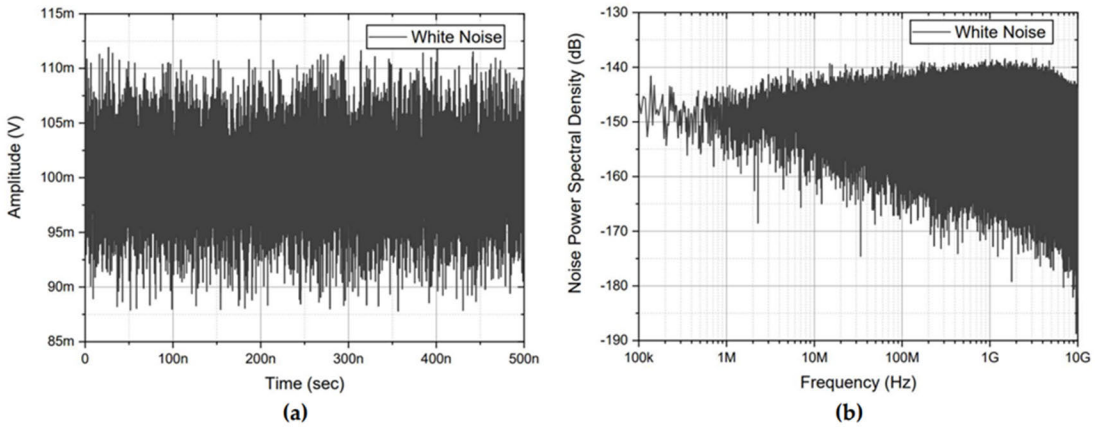

FIGURE 3. White noise sources (a) transient signal and (b) power spectral density.

noise signal. Therefore, the composed noise signal $u_n(t)$ can be defined as,

$$u_n(t) = u(t) + n(t) \tag{1}$$

The transient noise and the small-signal AC noise validation comes from the need of the autocorrelation function of the noise signal and its Fourier transform [2], [13], [14]. The autocorrelation of one noise source can be found by integrating over time as,

$$n^2(t) = \lim_{T\to\infty}\left(\frac{1}{2T}\right)\int_{-T}^{T} n(t) \times n(t-\tau)dt \tag{2}$$

The power spectral density of the noise n(t) can be calculated by performing a Fourier transform of the noise autocorrelation function. For white noise sources, the power spectral density is constant across all frequency spectrum. Hence, from a mathematical point of view, the autocorrelation function of a white noise source is a delta function $\delta(t)$, as illustrated in Fig. 2. A real white noise signal was generated and simulated using a noisy resistor as to derive its power spectral density (PSD), depicted in Fig. 3. The derived behavior of the real white noise source PSD depicted in Fig. 3b, is in great agreement with the ideal white noise PSD derived from the autocorrelation function of the white noise source, illustrated in Fig. 2.

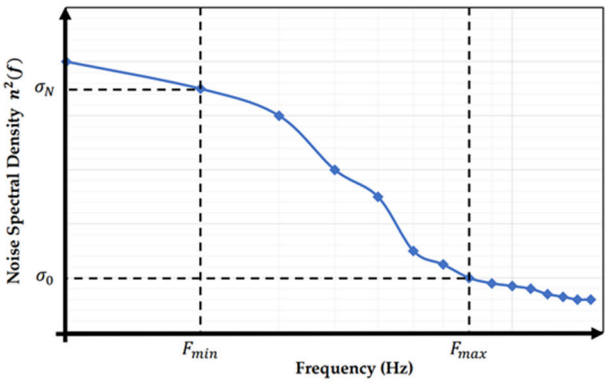

FIGURE 4. Power spectral density (PSD) of colored noise superposed by white noise sources.

B. FREQUENCY DOMAIN NOISE SIGNAL GENERATION

Small-signal noise analyses are usually performed in the frequency domain rather than in direct time domain. Hence, the need of generating frequency dependent noise signals arises. As to be able to generate frequency dependent noise signals in the time domain, an extension of white noise signal approach must be introduced. Noise signals were synthesized using step functions that devide the frequency spectrum into discrete frequency steps.

$$f_k = 2^{-k} \times F_{max}, \quad k = 0, 1, 2, \ldots, N \tag{3}$$

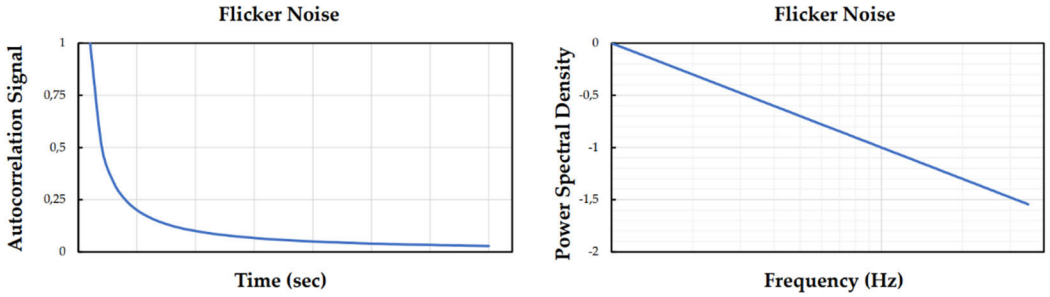

FIGURE 5. Autocorrelation function and the respective power spectral density (PSD) of flicker noise.

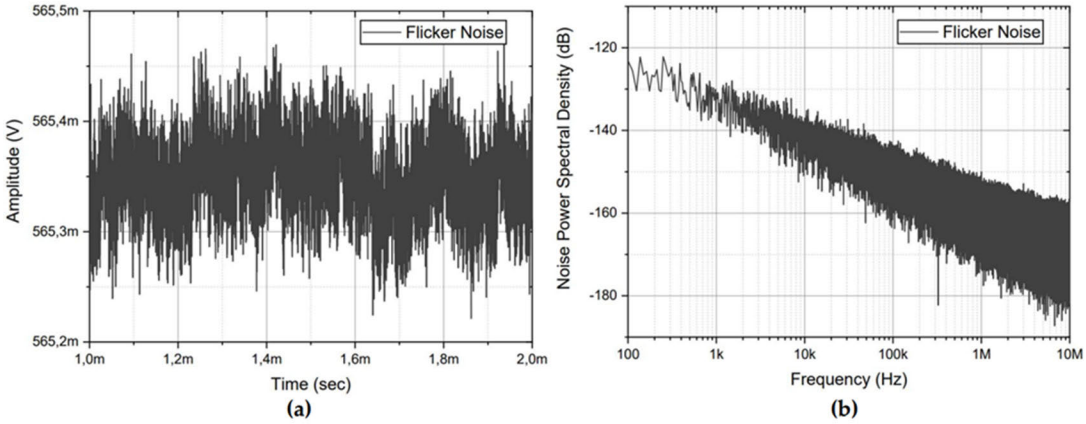

FIGURE 6. Flicker (1/f) noise (a) transient signal and (b) power spectral density.

According to (3), $f_0 = F_{max}$ and $f_N = F_{min}$ are the maximum and minimum frequencies of the desired spectrum, respectively. The power spectral density of a frequency-dependent noise signal can be graphically illustrated in Fig. 4.

Flicker noise is a frequency-dependent noise source and the autocorrelation function of the flicker noise must be calculated in order to derive its power spectral density. The autocorrelation function of the flicker noise is a *1/f* function, and its power spectral density is depicted in Fig. 5. The flicker noise, according to its PSD, is dominant at low frequencies whereas its noise contribution is negligible at high frequencies. A simple testbench with a MOSFET device operating in the saturation region, was designed as to generate and simulate the flicker noise behavior. The transient flicker noise signal and the flicker noise power spectral density, were illustrated in Fig. 6. As expected, the behavior of the real flicker noise PSD depicted in Fig. 6b, is in great agreement with the ideal flicker noise PSD derived from the *1/f* autocorrelation function of the flicker noise source, illustrated in Fig. 5.

A typical device noise spectrum consists of white and frequency-dependent noise sources. Thermal noise is a white noise source in which the power spectral density is flat across all frequencies. Flicker *(1/f)* noise is a frequency-dependent noise source, and its power spectral density is depicted in Fig. 6b. The typical device noise spectrum, with thermal and flicker noise, is illustrated in Fig. 7. A flat noise behavior was

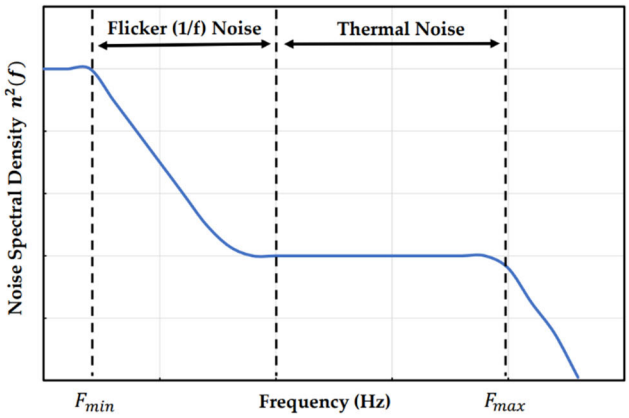

FIGURE 7. Typical device noise spectral density with thermal and flicker noise contributions.

simulated for frequencies lower than the F_{min} value, while for frequencies higher than the F_{max} value, noise spectrum was simulated as a declining function of frequency. Practically, there is no need to set the F_{max} value higher than the circuit's bandwidth because any noise will be suppressed by the circuit anyway.

The RF MOSFET devices are modeled using an RF macro model in which the gate impedance network is taken into consideration. Gate current, at frequencies in the RF/mmWave

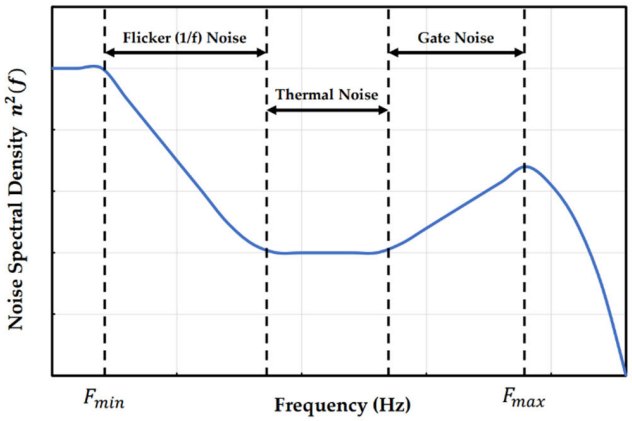

FIGURE 8. RF device noise spectral density with thermal, flicker and gate induced noise contributions.

spectrum, has a non-zero value and cannot be neglected. Thus, gate induced noise was introduced to the noise spectrum, as illustrated in Fig. 8. Contrary to flicker and thermal noise, gate induced noise is increasing with frequency and, in RF/mmWave applications, gate induced noise is dominating.

C. MULTIPLE TIME SCALE SIGNAL INTEGRITY ANALYSIS

Noise and signal integrity simulation challenges arise when the designed circuit is operating in multiple time scales, i.e. Amplitude and Phase Modulation (AM and PM) topologies, mixing topologies, etc. The term ''multiple time scale operating topologies'' refers to circuits whose output frequency spectrum consists of multiple frequencies. When these topologies need to be simulated in terms of noise and signal integrity, the standard large-signal and small-signal analyses are not applicable and advanced analyses should be introduced. However, direct time domain noise analysis is always applicable but with a time-consuming cost. The simulation time is the driving factor that led to more advanced simulation analyses introduced to the industry standard simulator. Two of the most practical and efficient noise and signal integrity simulation analyses are the Quasi-Periodic Steady-State (QPSS) and the Envelope Following (ENVLP) analysis. The QPSS analysis is a large-signal analysis whereas the envelope following analysis is a small-signal analysis.

The Quasi-Periodic Steady-State (QPSS) analysis can handle multiple fundamental frequencies of circuits topologies that operate in multiple time scales. The QPSS analysis, contrary to the PSS analysis, can efficiently compute the complex frequency spectrum of multiple time scale topologies whereas the PSS analysis cannot resolve accurately more than one closely spaced or incommensurate fundamental frequencies [15]. Frequency responses of several moderate signals combined to a strongly non-linear tone, such as a local oscillator or a clock signal, can be easily provided by the QPSS analysis in a non-time-consuming manner. The QPSS analysis assumes that the circuit under test is responding in a strongly non-linear fashion to the large signal tone while moderate tones have a weakly non-linear response. A comparison between Periodic Steady-State (PSS) analysis and Quasi-Periodic Steady-State (QPSS) analysis, is illustrated in Fig. 9. PSS analysis cannot resolve both F_1 and F_2 frequencies of the input spectrum and only the F_1 frequency is present at the output spectrum. The QPSS analysis can easily resolve both F_1 and F_2 frequencies of the input spectrum while their harmonics were also derived in the output spectrum.

The Envelope following analysis (ENVLP) is a small-signal analysis and it was introduced for simulation of the envelope transient response of multi-frequency (multiple time scale) signals. The envelope analysis is capable of accurately modeling and estimating the frequency translation effects in time-varying RF/mmWave topologies used in mobile communication applications [15], [16]. Modulation schemes and intermodulation noise can be resolved using the envelope following analysis in a time-conservative manner. In mixing or Amplitude and Phase Modulation (AM and PM) schemes, the desired information has a frequency orders of magnitude smaller than the clocked high-frequency signal used for down conversion (mixers) or transmission (AM/PM modulation).

For example, in a mixing topology, if the RF signal has a frequency of 990 MHz and the local oscillator signal (LO) has a frequency of 1GHz, the down converted IF signal (desired information) has a frequency of 10 MHz. The desired time interval needed for simulating a 10 MHz signal efficiently, is in order of microseconds to a few hundreds of nanoseconds. Due to the RF and LO high-frequency signals, the simulation time interval (or frequency window, as illustrated in Fig. 10) must be in orders of nanoseconds to a few hundreds of picoseconds, accordingly. Thus, the time interval (frequency window), using transient analysis, is increased aggressively, resulting in inaccurate and time-consuming simulations. Hence, the Envelope following analysis (ENVLP) was introduced to solve this time-consuming simulation problem when topologies with multiple fundamental frequencies, orders of magnitude apart, need to be simulated.

The Envelope following analysis provides an efficient way to simulate the modulation or intermodulation schemes without compromising the accuracy in a reasonably fast way. In each high-frequency clock cycle, the circuit behavior can be considered as similar, but not identical, to its behavior of the previous and following clock cycles [15]. This property provides the simulation time and accuracy advantages to the envelope following analysis compared to direct time domain one. The small-signal envelope analysis should be followed by a large-signal analysis, such as PSS or QPSS analysis, as to be able to calculate the time-varying large-signal operating point.

The envelope following algorithm assumes that the envelope behavior of a clock-driven circuit with a known clock period T, which is much smaller than the simulation time interval, can be calculated by sampling the state of the circuit

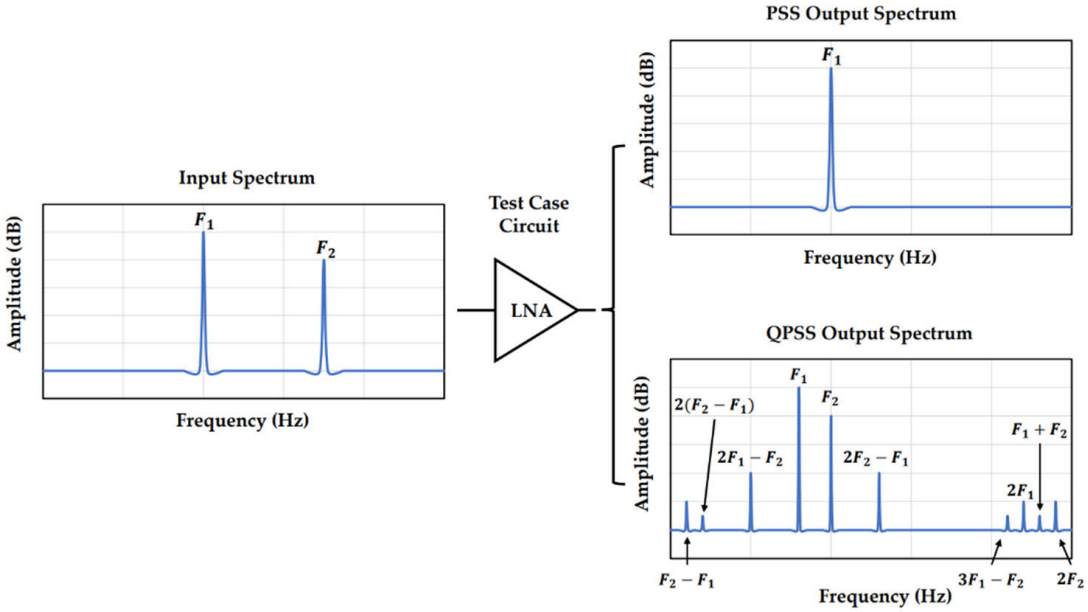

FIGURE 9. Information comparison from PSS and QPSS analyses.

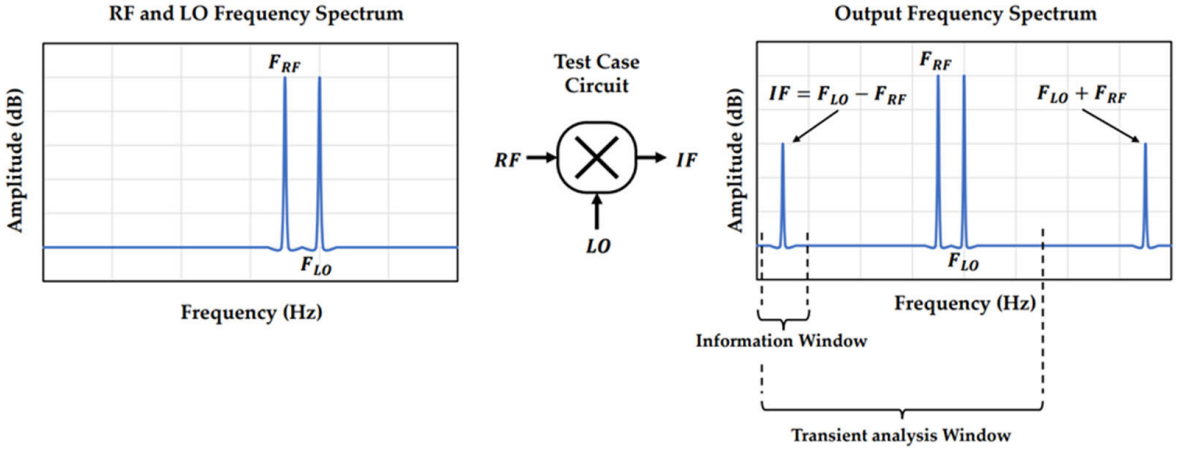

FIGURE 10. Comparison between the desired information window and transient analysis window.

at the beginning of each clock period [16]. This assumption is valid if the circuit behavior is not changing rapidly in between each envelope sample interval. Hence, a continuous function can be defined as to interpolate the envelope's data formed by sampling the circuit behavior at each time interval. This sampling algorithm is illustrated graphically in Fig. 11a while the envelope waveform, after interpolating the sampling data, is depicted in Fig. 11b.

III. MOSFET NOISE SOURCES

According to the application of interest, the noise sources which contribute to the overall noise of the device vary. The driving factor who defines the dominant noise sources of the circuit is the operating frequency. In low frequency and audio applications, flicker *(1/f)* noise is dominant while the noise contribution from the rest of the noise sources of the circuit can be neglected. From the opposite side of the frequency spectrum, in RF/mmWave circuits targeted to mobile communication applications, gate induced noise is the most dominant noise source whereas flicker noise contribution is negligible. Hence, the noise sources of the MOSFET devices must be thoroughly addressed and categorized according to the application field of interest. This noise source categorization can lead to efficient and accurate noise estimation and design cycle speedup in terms of noise optimization.

In standard CMOS processes, the noise contribution in integrated circuits is from thermal noise, flicker *(1/f)* noise and gate induced noise sources. Shot noise, generation/recombination noise and "popcorn" noise [17] are also present but their noise contribution, compared to thermal, flicker and gate induced noise, can be neglected. To properly monitor the gate induced noise, RF compact models for the

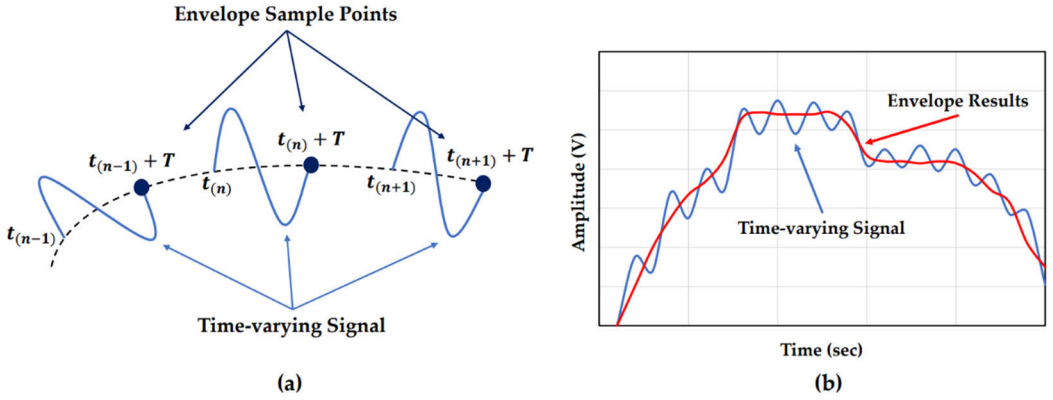

FIGURE 11. (a) Envelope following integration algorithm and (b) envelope waveform interpolated results.

MOSFET devices should be introduced. These RF models take into consideration the gate impedance network and a non-zero gate current flow can be observed at high operating frequencies. This gate current induces noise into the MOSFET channel, and it must be considered as to achieve accurate noise behavior extraction.

A. THERMAL NOISE

Thermal noise is a white noise source, and its generation is caused by the random movement of the electrons due to their thermal energy [18], [19], [20]. Due to the white noise nature of thermal noise, its power spectral density is relatively flat across the frequency spectrum. An external factor which increases the thermal noise of the device or circuit, is the temperature. High temperatures lead to an increase of the thermal energy of the electrons which also leads to a significant increase of the random movement of the electrons into the silicon. The thermal noise drain current, according to [21], can be calculated using the equation below,

$$\overline{I_d^2} = 4kT\Delta f \times \frac{\mu_{eff}}{L_{eff}^2} \times |Q_{inv}| \tag{4}$$

where μ_{eff} is the effective carrier mobility, L_{eff} is the effective channel length of the MOSFET device and the Q_{inv} (in coulombs) is the charge of the channel in the strong inversion region. For long channel transistors, (4) can be written as [21] and [22],

$$\bar{I_d^2} = \begin{cases} 4kT\Delta f \times \gamma\,(g_m + g_{mb}) & saturatin\ region \\ 4kT\Delta f \times g_d & linear\ region \end{cases} \tag{5}$$

where the g_m is the device transconductance, the g_{mb} is the substrate transconductance (when the device experience body effect) and the g_d is the drain transconductance (when the device operates in the linear region). The γ coefficient is calculated as $\gamma = 2/3$, for long-channel MOSFET devices whereas, for short-channel devices, the γ coefficient was found to be larger [23]. According to (5), the thermal noise, in long-channel MOSFETs operating in the saturation region, can be calculated using the formula below,

$$\frac{\overline{I_{th}^2}}{\Delta f} = \frac{8}{3} \times kTg_m \tag{6}$$

For the simulation of the thermal noise behavior described by (6), a simple test case circuit topology should be designed in a such a way that, it strongly exhibits the thermal noise characteristics. The selected topology in which, with a proper setup, the thermal noise is dominant, is depicted in Fig. 12. In this topology, a MOSFET device was biased above its threshold voltage, using a V_{gs} DC voltage source while, across the source and drain terminal of the MOSFET, an ideal zero-value DC current source was applied. The zero-value DC current source across the source and drain terminals, set the V_{ds} voltage to 0 V. Using this configuration, the MOSFET is biased in the strong inversion region, dominating by thermal noise. This test case topology was designed using a 65 nm planar CMOS process, and the RF device model from the respective design kit, was used.

For the simulation of thermal noise in the topology depicted in Fig. 12, two noise simulation analyses are applicable, the direct time domain noise analysis (TRAN Noise) and the AC Noise analysis. The AC Noise analysis can be performed because the test case topology has a steady DC operating point, provided by the V_{gs} voltage source. The power spectral density (PSD) of the thermal noise, using both transient noise and AC Noise analysis, is illustrated in Fig. 13. As expected, due to its white noise source nature, thermal noise power spectral density was simulated flat across the frequency spectrum. Thus, regardless of the operating frequency, thermal noise contribution has a non-zero value. The AC noise led to a significant noise simulation speedup advantage while the results are in great agreement with the results provided by the large-signal transient noise analysis.

B. FLICKER (1/f) NOISE

Flicker or *(1/f)* noise, is a frequency-dependent noise source and it can be observed in a kind of baseband circuitry. To be able to accurately simulate the flicker noise behavior,

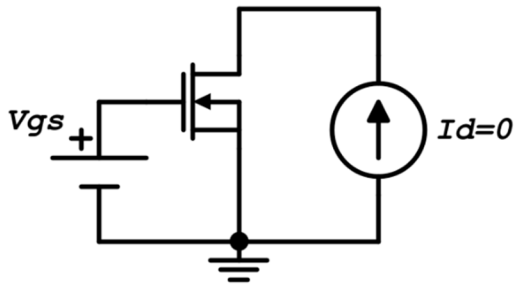

FIGURE 12. Test case topology for thermal noise simulation.

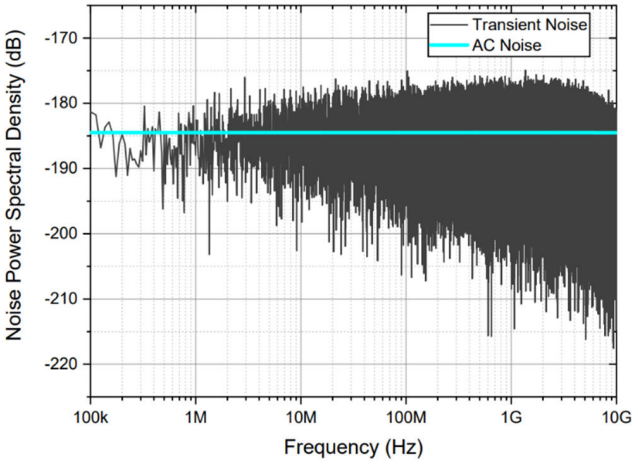

FIGURE 13. Noise Power Spectral Density (PSD) of the thermal noise using Transient noise and AC noise analysis.

a baseband circuit, operating at low frequencies, should be used. Despite the universal presence of the flicker noise in all types of materials or devices with semiconductor properties, its precise origin is difficult to interpret [21]. The flicker *(1/f)* noise can be described by the equation below [21] and [22],

$$V_f^2(f) = K_f \times \left(\frac{1}{C_{ox}^2 \times (WL) \times f} \right) \tag{7}$$

where K_f is the flicker noise coefficient, C_{ox} is the MOSFET gate capacitance per unit area, W and L are the width and length of the MOSFET channel respectively and f is the frequency of operation. According to (7), for the same device, the flicker noise is dominant when the frequency of operation is low. With the increase of the frequency, the flicker noise decreases until a point in which its noise contribution is below the thermal noise floor and thus, it can be neglected. In addition, for the same operating frequency, the flicker noise can be decreased by increasing the sizing of the active devices, i.e. the width and length of the transistors. Since the carrier mobility in PMOS devices is lower than the NMOS ones, the size of a PMOS device in a design, is usually larger than the NMOS. This results in lower flicker noise floor of the PMOS compared to the NMOS device.

To assess and simulate the flicker noise behavior of a circuit, a simple test case circuit was designed in such a way that it strongly exhibits the flicker noise characteristics. The

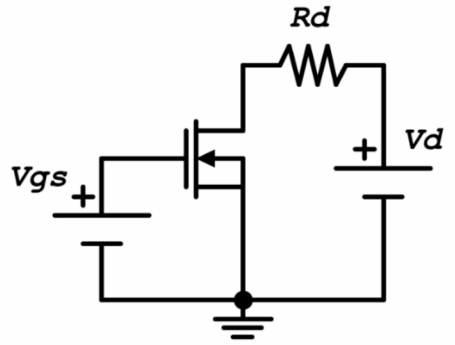

FIGURE 14. Test case topology for flicker (1/f) noise simulation.

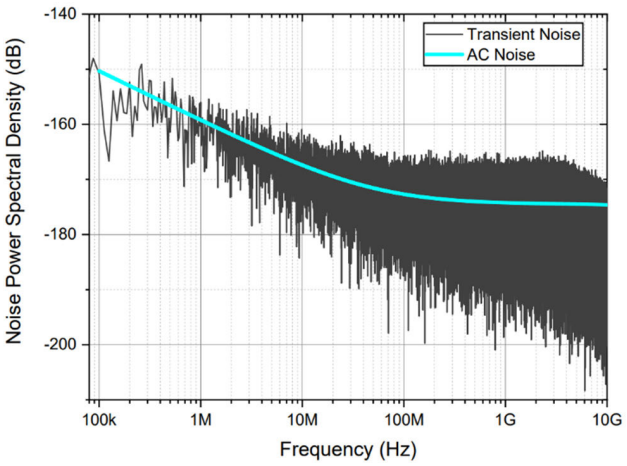

FIGURE 15. Noise Power Spectral Density (PSD) of the flicker noise using Transient noise and AC noise analysis.

designed circuit topology with strong flicker noise contribution, is depicted in Fig. 14. The respective topology was designed using a 65 nm CMOS process and again, the RF MOSFET models of the specific design kit, were used. The MOSFET is biased above its threshold region, using a V_{gs} DC voltage source with a value of 700 mV while, a V_d DC voltage source with a value of 1.2 V was introduced to the circuit as to provide a DC bias current to the device. This DC current indicates the flicker noise characteristics of the output noise spectrum of the circuit. In this topology configuration, the MOSFET is biased in the strong inversion region while flicker noise is the dominant noise source of the circuit.

For the simulation of the flicker noise, using the test case topology depicted in Fig. 14, direct time domain noise analysis (TRAN Noise) and AC Noise analysis are capable of capturing the flicker noise behavior. The small-signal AC noise analysis is applicable because the test case circuit has a steady DC operating point and thus, the circuit equations can be linearized around this point of interest. The power spectral density (PSD) of the flicker noise, using both transient noise and AC noise analysis, is illustrated in Fig. 15. The expected flicker noise behavior was simulated while, high flicker noise contribution at low operating frequencies, was accurately captured. Furthermore, the AC noise simulation led to a

significant noise simulation speedup advantage compared to the results provided by transient noise analysis. In addition, this noise simulation speedup did not compromise the accuracy of the AC noise results while, both noise simulation results are in great agreement, as graphically illustrated in Fig. 15.

C. GATE INDUCED NOISE

In circuit designs operating in the RF/mmWave frequency spectrum, the gate induced noise has a significant contribution to the total noise of the circuit and must be thoroughly addressed. Flicker noise, in these high-frequency topologies, is insignificant and only thermal and gate induced noise contributions are present in the output noise power spectral density. At low frequencies (according to the RF/mmWave standards), the thermal noise floor is higher than the gate noise floor and thus, thermal noise is the dominant noise source of the topology. Increasing the frequency of operation, the gate induced noise is increasing while the thermal noise level is unaffected. Inevitably, at high frequencies, the gate induced noise level surpasses the thermal noise floor and the gate induced noise dominates.

The gate induced noise is caused by the fluctuations of the channel charges due to equal and opposite fluctuations of the gate charges [21]. This charges fluctuations at the gate electrode and the device channel, resulting in a current fluctuation at the gate. This induced gate current noise must be taken into consideration when the gate coupling, due to high frequency operation, becomes significant. The gate induced current noise, can be described, according to [21], by the equation below,

$$\overline{I_g^2} = 4kT\Delta f \times \frac{4C_{gs}^2}{15g_m} \times \omega^2 \tag{8}$$

where k is the Boltzmann coefficient, T is the temperature, g_m is the device transconductance, C_{gs} is the gate-source parasitic capacitance and ω is the frequency.

The gate induced noise behavior can be derived if the gate impedance network is considered and modeled properly. The equivalent RC network and the lumped model of the gate impedance network are illustrated in Fig. 16. At high frequencies, the gate parasitic capacitances are coupled with the device channel and induce noise current. The channel charge cannot be built-up instantaneously and thus, in the lumped equivalent gate impedance model, a resistance R_g was introduced in series with the parasitic capacitances C_{gs} and C_{ds} (Fig. 16b). This network or similar gate impedance networks are commonly used when simulating circuits with the standard BSIM4 or even the more advanced PSP MOSFET models [24], [25].

The gate induced noise was simulated using the circuit topology depicted in Fig. 17. In this topology, the MOSFET was biased in the saturation region by setting the V_g voltage equal to 600 mV while, the DC voltage V_d across the MOSFET device, was set to 1.2 V. The conversion of the gate current to voltage was performed using a noiseless resistor (typically 1 Ω) at the gate terminal of the device. The R_s is the source terminal resistance of the MOSFET and is usually set to a small value. The drain terminal was deliberately connected to a DC voltage source to drive all the drain current thermal noise and flicker noise to ground and thus, only the gate induced noise contribution will be present. By monitoring the gate current at high frequencies, the gate induced noise behavior can be simulated.

For validation purposes of the gate induced noise using the test case topology illustrated in Fig. 17, two noise simulation analysis were performed, the direct time domain noise analysis (TRAN Noise) and AC Noise analysis. Both analyses can capture the gate induced noise behavior accurately, but a time-consuming disadvantage can be imposed when performing a transient noise analysis instead of AC noise analysis. The power spectral density (PSD) of the gate induced noise, using both transient noise and AC noise analysis, is illustrated in Fig. 18. The gate induced noise behavior is the expected noise behavior according to (8) where, at high frequencies, the gate induced noise is significantly increasing.

TABLE 1. MOSFET sizing of the OTA test case vehicle.

MOSFET Device	Sizing W(μm)/L(μm)
Mn1 – Mn4	0.9/14
Mn5 – Mn6	1/14
Mn7	15/14
Mp1 – Mp8	1/0.9
Power supply voltages and biases	
VDD	1.8 V
VSS	-1.8 V
Vbias	-1.1 V

IV. NOISE SIMULATION TEST CASE VEHICLES

The integrated circuits can be categorized into three major circuit types, linear, periodic state and non-linear circuits. Linear and periodic state circuit topologies have a stationary DC operating point or a steady periodic state, respectively. Thus, the noise equations are linearized and solved around each operating point of interest. Non-linear circuit topologies have neither a stable DC operating point nor a steady periodic state. Hence, the noise equations cannot be solved using approximations around a steady point and they can only be solved in the direct time domain using large-signal analysis.

A. LINEAR CIRCUITS NOISE SIMULATION

An Operational Transconductance Amplifier (OTA) was designed as a linear circuit vehicle test case, using a 1.8V 180nm planar CMOS process. Operational Transconductance Amplifiers (OTAs) are most used in low frequency filter designs as integrator and differentiator blocks or as a passive component replacement emulator [26], [27], [28], [29]. The schematic and the physical layout design of the OTA are illustrated in Fig. 19a and 19b, respectively. The transistors sizing of the OTA design are provided in Table 1.

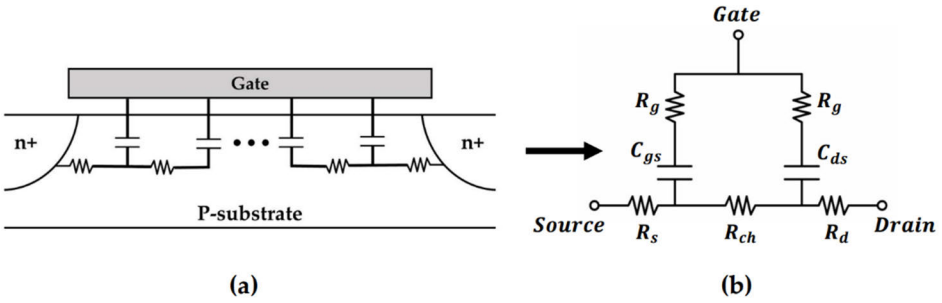

FIGURE 16. (a) Equivalent RC network and (b) lumped model of the gate impedance network.

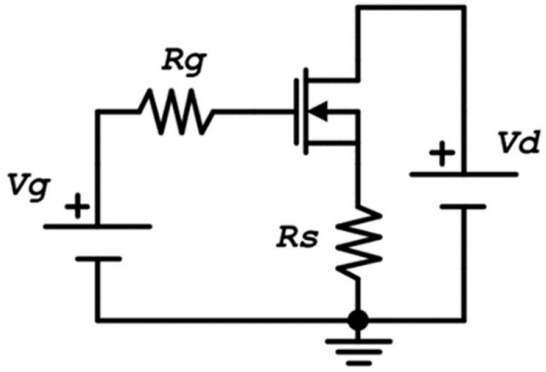

FIGURE 17. Test case topology for gate induced noise simulation.

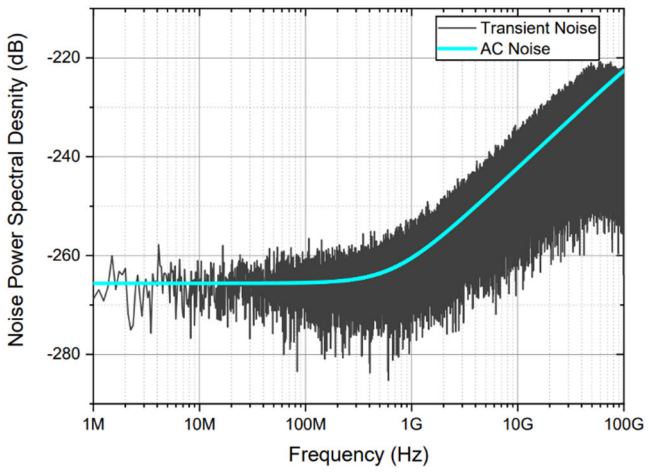

FIGURE 18. Noise Power Spectral Density (PSD) of the gate induced noise using Transient noise and AC noise analysis.

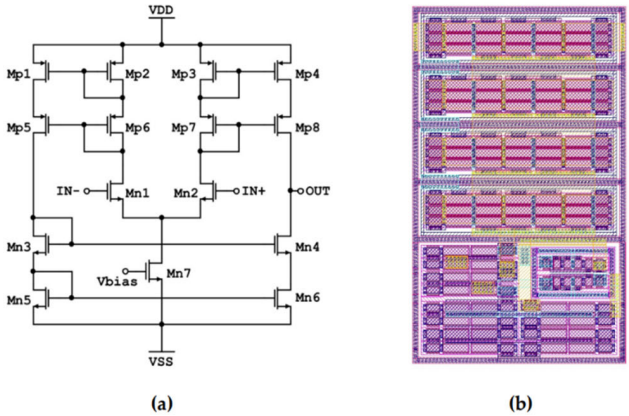

FIGURE 19. OTA test case vehicle (a) schematic and (b) physical layout design.

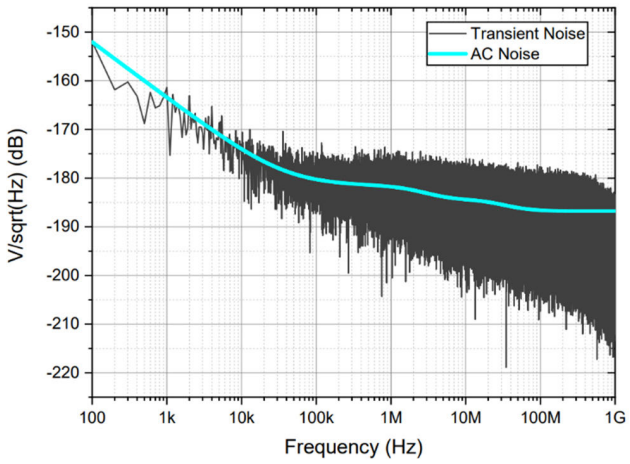

FIGURE 20. AC noise versus Transient noise PSD of the OTA test case vehicle.

The output transconductance of the OTA test case circuit was 4.8 μA/V with a common mode range (CM) of 800 mV. The OTA topology illustrated in Fig. 19a, was biased using a DC voltage of $V_{bias} = -1.1$ V. This bias voltage of the OTA forces all transistor devices in the design to operate in the saturation region. In addition, this bias voltage sets a stable DC operating point of the linear OTA topology and thus, AC noise small-signal analysis, in combination with a DC analysis, can be performed as to extract the noise behavior of the full OTA design.

The OTA test case vehicle is a linear topology with a stable DC operating point provided by the V_{bias} voltage. Thus, two simulation analyses, a large-signal DC analysis and a small-signal AC noise analysis, must be performed to adequately extract the noise behavior of the design. Transient noise analysis was also performed and a comparison with the AC noise results and the obtained accuracy, was derived. The

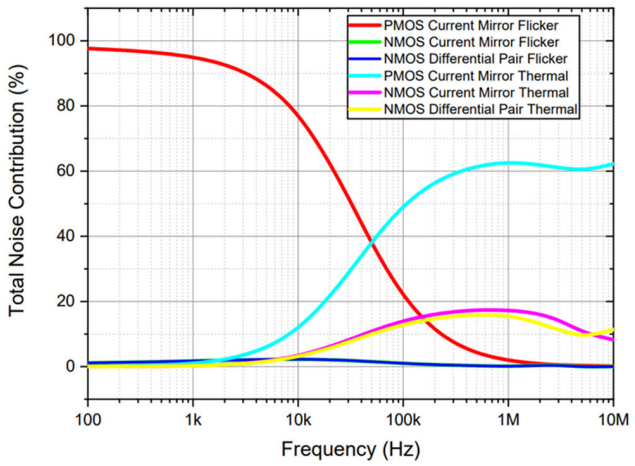

FIGURE 21. Total noise contribution per stage of the OTA test case vehicle.

noise PSD of the OTA design, for both transient noise and AC noise analysis, is depicted in Fig. 20. The AC noise analysis results agree with the transient noise analysis results while a noise simulation speedup by a factor of $\sim 10^3$ can be achieved, when performing AC noise instead of transient noise analysis.

The OTA design noise contribution per stage is illustrated in Fig. 21. At low frequencies, the flicker noise is dominant and at high frequencies, the thermal noise is dominant. The PMOS stage of the OTA test case vehicle is the main noise contributor to the overall noise of the vehicle. The NMOS stage along with the input differential stage, at low operating frequencies, have negligible noise contribution to the overall noise while, at high operating frequencies, their noise contribution cannot be neglected. The PMOS stage is the dominant noise contributor at all operating frequencies of the OTA design due to the small PMOS device sizing (compared to the NMOS devices, Table 1) which introduce high flicker noise (flicker noise is inversely proportional to W and L of the device, (13)) and high thermal noise due to high transconductance g_m (thermal noise is proportional to g_m of the device, (12)).

B. PERIODIC STATE CIRCUITS NOISE SIMULATION

In periodic state circuits or any kind of oscillator circuitry, phase noise should be performed as to extract the noise impact to the oscillation frequency of interest. In oscillators, the need to achieve very low phase noise and high oscillation frequency arises in the RF and mmWave applications. Ideal oscillator output signal and real oscillator output signal due to phase noise, are illustrated, both in the frequency domain, in Fig. 22. Phase noise or jitter noise is the period variations of a signal (in the time domain) resulting in a wider frequency spectrum at the oscillation frequency, i.e. more than one frequencies are present in the PSD window. The low phase noise performance of an oscillator is a critical metric in all of the RF transceiver chains and especially in the RF-to-IF mixer block because, high phase noise of the local oscillator

TABLE 2. MOSFET sizing and LC tank values of the VCO core test case vehicle.

MOSFET Device	Sizing W(μm)/L(μm)
Mp1 – Mn2	6/0.06
Mn1 – Mn2	14.4/0.06
Mn3	4.5/0.4
LC tank values	
L	943 pH
Q (@ 22 GHz)	11.2
SRF	39.9 GHz
C1 – C2	102.5 fF
Power supply voltages and biases	
VDD	1.2 V
VSS	0 V
Vbias	1.18 V

results in noise interference with the desired received signal (information signal).

Phase noise can be measured using two simulation approaches, the absolute and the relative frequency phase noise measurement. Phase noise measurement using an absolute frequency sweep is performed by sweeping the frequency of interest into a relatively large frequency window and measure the absolute phase noise of the circuit. This method can results in time-consuming simulations but it is useful when the upper and lower sidebands of the carrier is asymmetrical and thus, a full frequency spectrum sweep is needed. In most cases, when a steady state oscillator needs to be simulated, both the upper and lower sidebands of the carrier are symmetrical and thus, relative frequency phase noise measurement is the most optimum and efficient noise simulation.

Phase noise measurement using the relative frequency sweep is performed by sweeping the frequency of interest relative to the carrier frequency and measuring the phase noise using a 1 Hz window [30], as illustrated in Fig. 23. This phase noise measurement approach reduces the simulation time while the accuracy remains unaffected. This simulation approach assumes that the upper sideband and lower sideband of the carrier is symmetrical and thus, there is no need to sweep a wide frequency window. If the symmetrical sideband assumption is not valid, the relative phase noise simulation can be performed for each sideband independently but with simulation time impact. The exact carrier frequency, which is the reference frequency point of the phase noise simulation when performing a relative frequency sweep, is derived using a large-signal PSS analysis.

A Voltage Controlled Oscillator (VCO) with a power dissipation of 1 mW, was designed as a periodic state circuit vehicle, using a 1.2V 65 nm RFCMOS process. The VCO frequency can be tuned using a voltage control signal (Vbias in the schematic) while its tuning range extends from 19.7 GHz – 22 GHz. VCOs are most used in the RX/TX chains as a local oscillator signal due to their low phase noise. Other oscillator circuitry, such as ring oscillators, are way simple to design but with the cost of the high phase noise behavior [31], [32], [33].

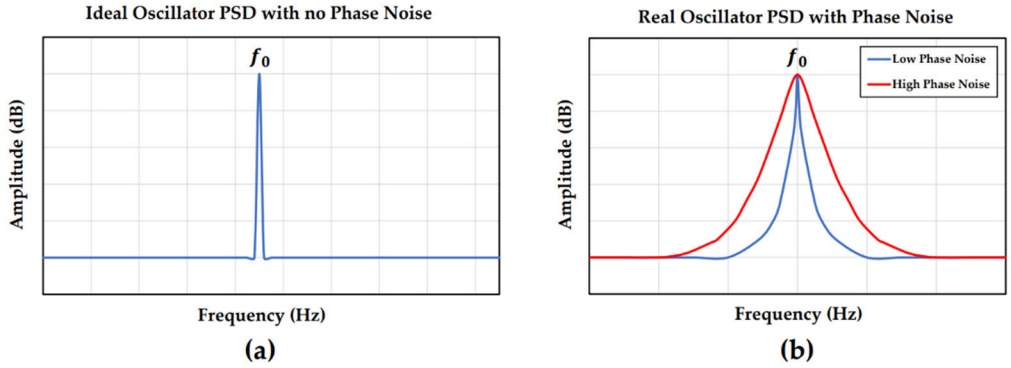

FIGURE 22. (a) Ideal oscillator PSD versus (b) real oscillator PSD and phase noise impact.

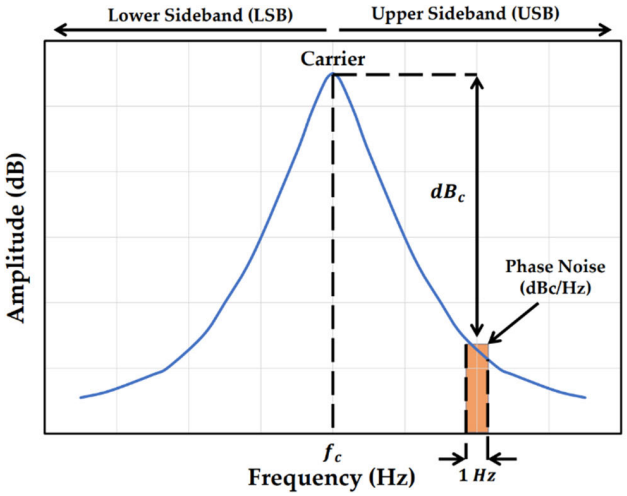

FIGURE 23. Phase noise measurement using relative frequency sweep.

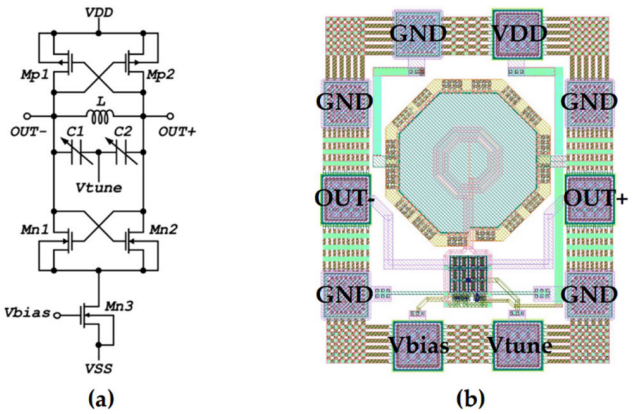

FIGURE 24. VCO test case vehicle (a) schematic and (b) physical layout design.

The schematic and the physical layout design of the VCO vehicle are illustrated in Fig. 24a and 24b, respectively. The transistors sizing of the VCO core, and the LC tank values, are provided in Table 2.

As a periodic state vehicle, the VCO topology has a steady periodic state and thus, phase noise (PNOISE) analysis can be performed to extract the phase noise behavior of the design. Along with the small-signal phase noise analysis, a large-signal PSS analysis must be performed as to extract the exact carrier oscillation frequency of the VCO which is the reference point for the phase noise analysis using relative frequency sweep with respect to the carrier. As mentioned above, the relative phase noise analysis can provide more explicit and more rapid simulation results than the absolute frequency sweep phase noise analysis. Transient noise analysis was also performed and used as the golden reference for the accuracy comparison of the phase noise analysis. The phase noise of the VCO design, for a carrier frequency of 22 GHz, using both transient noise and PNOISE analysis, is depicted in Fig. 25a and 25b, for relative and absolute frequency sweep, respectively. The PNOISE analysis results are in great agreement with the transient noise analysis results while PNOISE analysis achieved a noise simulation speedup by a factor of $\sim 10^2$ compared to the transient noise analysis.

Using the absolute frequency sweep for the phase noise extraction (Fig. 25b), the PNOISE results at the carrier frequency cannot agree with the transient noise results because, the transient noise analysis PSD includes both noise and signal whereas the PNOISE analysis includes only the noise component. The PNOISE results using a relative frequency sweep, are in great agreement with the results provided by the transient noise because, the phase noise is calculated at an offset frequency away from the carrier. This means that, the carrier signal is not considered for the phase noise calculation of the VCO core and only the carrier frequency (provided by the PSS analysis) is used as the reference frequency for the relative phase noise analysis. The phase noise results illustrated in Fig. 25a, using relative frequency sweep, are more valuable than those derived from an absolute frequency sweep because the carrier sidebands are symmetrical while the phase noise can be monitored at a specific frequency offset from the carrier.

C. NON-LINEAR CIRCUITS NOISE SIMULATION

In non-linear circuit topologies, the only applicable noise analysis is the transient noise because, the circuit under test

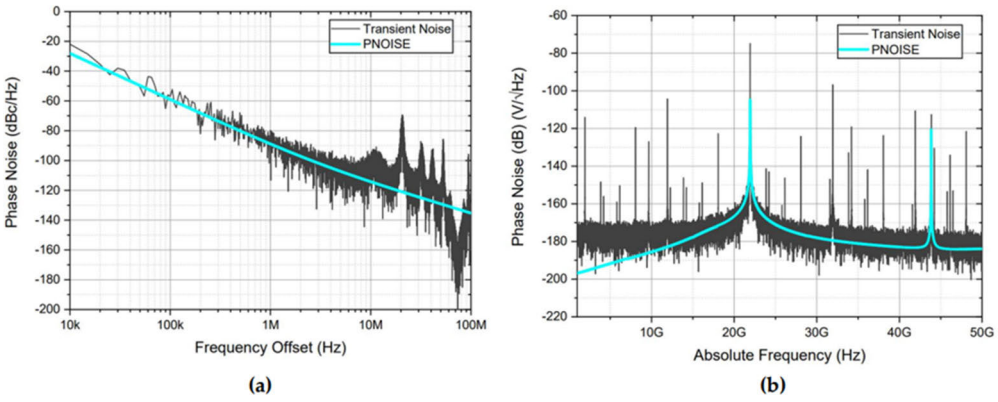

FIGURE 25. Phase noise versus Transient noise of the VCO core using (a) relative frequency sweep and (b) absolute frequency sweep.

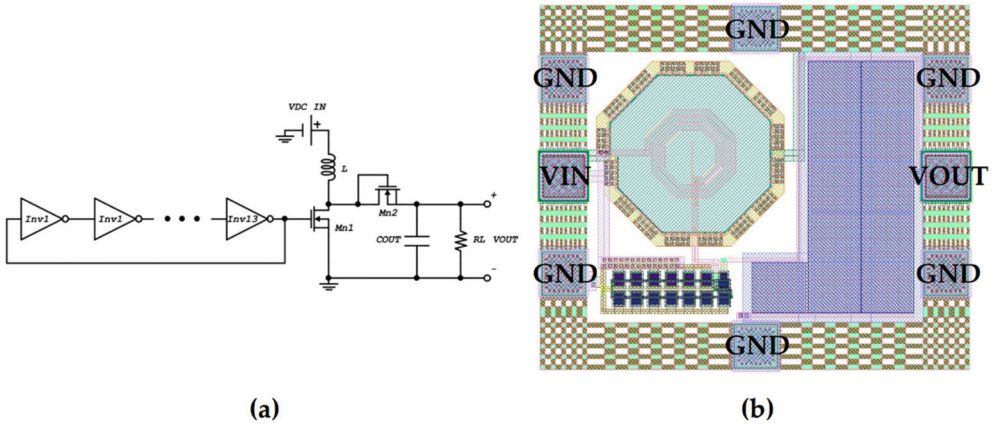

FIGURE 26. DC-to-DC boost converter test case vehicle (a) schematic and (b) physical layout design.

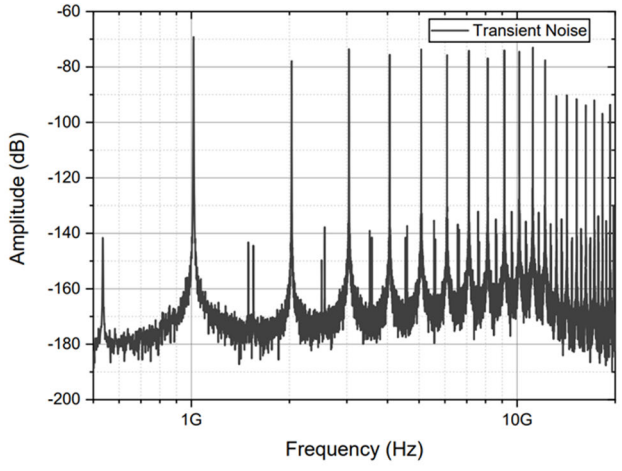

FIGURE 27. Transient noise of the DC-to-DC boost converter test case vehicle.

has neither a stable DC operating point nor a steady periodic state. Hence, none of the above small-signal noise simulation analyses can be applied and thus, no further noise simulation speedup can be achieved when simulating non-linear topologies. In addition, due to the incapability of performing small-signal noise simulation analyses, noise summary of the overall topology cannot be derived.

A DC-to-DC boost converter was designed as a non-linear circuit vehicle, using a 1.2 V 65 nm RFCMOS process. The designed DC-to-DC boost converter operates using a DC input voltage of 1.2 V and it can provide, to a 1 kΩ resistive output load, a DC output voltage of 2.5 V with a voltage ripple of 30 mV. A 13-stages ring oscillator circuit with a frequency of 1 GHz was used as a driving clock of the DC-to-DC boost converter circuit. The supply voltage of the ring oscillator is the same as the DC input voltage. This means that the oscillation frequency of the ring oscillator changes with the input DC voltage of the DC-to-DC boost converter. The 1 GHz oscillation frequency is derived using a 1.2 V DC input voltage. Integrated DC-to-DC boost/buck converters are most commonly used in many power management applications in which there is a need to generate voltages higher than the normal supply voltage or lower than the ground voltage [34], [35]. The schematic and the physical layout design of the DC-to-DC boost converter vehicle, are illustrated in Fig. 26a and 26b, respectively. The transistor sizing of both DC-to-DC boost converter core and ring oscillator block, are provided in Table 3.

TABLE 3. MOSFET sizing of the DC-to-DC boost converter test case vehicle.

MOSFET Device	Sizing W(μm)/L(μm)
Mp1	192/0.06
Mn2	120/0.06
Cout	34.2 pF
L	818 pH
13-stages Ring Oscillator	
Mn	60/0.22
Mp	120/0.22

The DC-to-DC boost converter operating point is not static and changes every half of the clock cycle of the ring oscillator signal. When the clock signal is high, the MOSFET switch (Mn1 in the schematic) is on and shorts the inductor terminal to ground. In this state, a DC current is flowing from the VDC IN to ground and the inductor is storing energy in the form of magnetic field. After half of the period of the ring oscillator signal, the clock is low and the MOSFET switch is off. In this state, the DC current flow stops and the inductor magnetic field collapses. This magnetic field collapse, pushes high amount of current to the output and charging the output capacitor to a specific voltage. The diode-connected MOSFET prevents the capacitor from discharging when the clock signal is high and the inductor is shorted to ground. At each cycle, the output capacitor is charging to a specific voltage while the output voltage is ramped up to the desired voltage level. The clock frequency and the inductor value (mostly the Q factor), are the main driving factors that determine the output voltage level. Higher frequency means more charging cycles and thus, higher output voltage while, higher Q means more energy stored than dissipated and thus, higher charging current when the magnetic field collapses.

Due to the nonlinear behavior of the DC-to-DC boost converter, the only applicable noise analysis is transient noise which is a time-consuming analysis and no alternative noise analysis, such as AC noise or PNOISE, can be performed. Furthermore, contrary to linear and periodic state vehicles, noise summary cannot be provided in non-linear topologies. The transient noise analysis result is illustrated in Fig. 27. The noise of the nonlinear DC-to-DC boost converter circuit is high at each clock cycle of the ring oscillator signal, i.e., output noise is high at every frequency step of 1 GHz (driving clock frequency).

D. NOISE INTEGRITY SIMULATIONS IN MULTIPLE TIME SCALE TOPOLOGIES

When digital and analog circuit blocks are integrated into the same silicon die, noise coupling interference can alter the performance of the noise-sensitive analog circuit blocks. High frequency operation and fast switching events from digital blocks or any other non-linear circuitry, are the main noise coupling aggressors if synthesized in the same substrate and designed using poor shielding in the physical layout level. This coupling noise originates mainly from the substrate coupling or from mutual coupling between routing lines or passive elements in the design block. When noise coupling is present, mixing interference can be observed which generates multi-frequency signals at the output spectrum. Hence, when a periodic state circuit is affected by noise coupling interference, multiple frequencies (intermodulation products) can be observed at the output spectrum and thus, multiple time scale simulation techniques should be performed as to accurately capture the noise coupling interference.

A noise integrity simulation scheme is set using the VCO core, designed in section IV-B, as the noise victim, with a carrier frequency of 22 GHz and a noise aggressor signal with a frequency of 1 GHz. The noise signal is derived using a technology-dependent s-parameter file (provided by a 2.5D EM simulator [36]) which describes the substrate isolation with respect to the frequency. The s-parameter file along with the 1 GHz noise signal were combined as to provide a noise signal from substrate coupling interference. This signal was injected into the common silicon substrate of the NMOS cross-coupled pair of the VCO core and the noise impact to the output frequency spectrum was simulated. The VCO output frequency spectrum, using standard and noise coupled simulations, is depicted in Fig. 28a and 28b, respectively.

From a simulation point of view, transient (TRAN), Envelope following analysis (ENVLP) and Quasi-Periodic Steady-State (QPSS) analysis are the only compatible simulation analyses that can capture the behavior of a circuit which operates in multiple time scales domains. The transient analysis and the QPSS analysis are large-signal analyses while the envelope following analysis is a small-signal analysis. The QPSS analysis is not capable of adequately capturing the noise signal at the output spectrum and only the intermodulation products and carrier frequencies can be monitored [37]. Transient (TRAN) and Envelope following analysis (ENVLP) are capable of adequately capturing the noise signal integrity at the output frequency spectrum of the VCO and they are only limited by the simulation time and the obtained accuracy. Envelope following analysis can provide noise integrity results way faster than performing transient analysis without significantly compromising the accuracy. The noise integrity simulation results, provided by transient analysis and envelope following analysis, are illustrated in Fig. 29. Using the envelope following analysis for noise integrity simulations, a speedup by a factor of $\sim$10 can be achieved with a $<$9% accuracy error (transient analysis CPU time $\sim$12.5 hours versus envelope analysis CPU time $\sim$1.3 hours).

V. NOISE SIMULATION GUIDELINES

The need to discretize and summarize the noise sources of a custom integrated circuit arises when it comes to rapid and accurate noise behavior extraction. Besides the categorization of the noise sources of a topology, the applicable noise simulation analyses should also be benchmarked time-wise and accuracy-wise. This categorization of the noise sources and noise simulation analyses can lead to accurate and rapid noise extraction without the time-consuming cost. Hence,

TABLE 4. Noise simulation guidelines for linear, periodic, non-linear and multiple time scale topologies.

Circuit Test Cases	Operating Point Large-Signal Analysis	Small-Signal Noise Integrity and Analysis		Noise Summary	Dominant Noise Sources		Noise Simulation Accuracy	Noise Simulation Speedup
Linear Circuits								
OpAmps, OTAs, Filters, LNAs, PAs	DC analysis	*Baseband*	*RF/mmWave*	✓	*Baseband*	*RF/mmWave*	*AC Noise / SP Noise*	
		AC Noise	SP Noise		Flicker Noise	Thermal Noise/ Gate Noise	High	$\times 10^3$
Periodic State Circuits								
VCOs, DCOs, Ring Oscillators	Periodic Steady-State analysis (PSS)	*Baseband & RF/mmWave*		✓	*Baseband*	*RF/mmWave*	*Relative frequency sweep PNOISE*	
		Phase Noise (PNOISE)			Thermal Noise	Gate Noise	High	$\times 10^2$
Non-Linear Circuits								
DC-to-DC Boost/Buck Converters, ADCs, Sigma-Delta Modulators	Transient analysis (TRAN)	*Baseband & RF/mmWave*		✗	*Baseband*	*RF/mmWave*	*Transient Noise*	
		Transient Noise (TRAN Noise)			Thermal Noise	Gate Noise	High	No speedup
Multiple Time Scale Topologies								
Mixers, Frequency Multipliers, Frequency Synthesizers, Mutual Coupling Topologies	Quasi-Periodic Steady-State analysis (QPSS)	*Baseband & RF/mmWave*		✗	*Baseband & RF/mmWave*		*Envelope Analysis*	
		Envelope Following Analysis (ENVLP)			*Noise Integrity Analysis: Noise signal is way above the noise level of the circuit (flicker, thermal, gate)*		Satisfactorily	$\times 10$

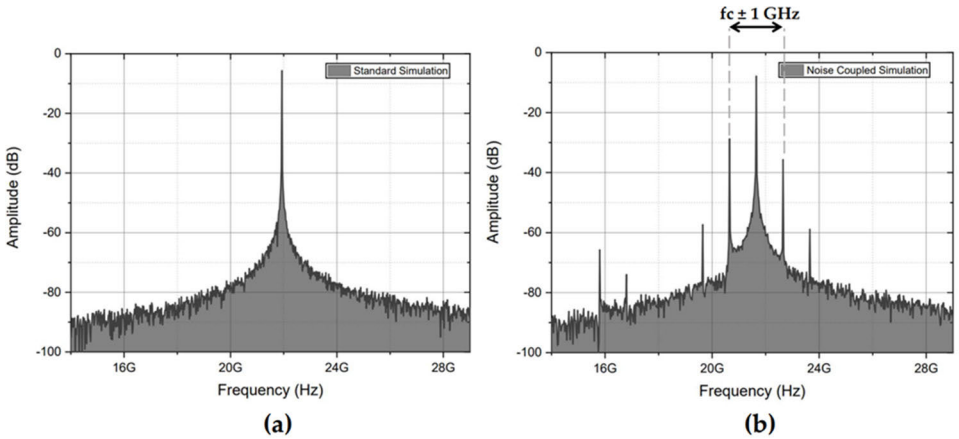

FIGURE 28. VCO output frequency spectrum using (a) standard simulation versus (b) noise coupled simulation.

providing a complete noise simulation guideline framework, the design cycle of a product could be significantly accelerated when the product noise optimization is a necessity. This design cycle speedup can be achieved only if the noise simulation guidelines are generic and can be applied in any topology regardless of the circuit type and the fabrication process. A full guide on noise simulation benchmarking according to each circuit type is provided in Table 4.

Linear, periodic, or non-linear circuit topologies indicate a specific variety of small-signal and large-signal analyses that can be executed for noise integrity verification. Each circuit type has a unique attribute which can provide all the applicable noise simulation analyses for rapid noise behavior extraction. Linear circuits have a stable DC operating point and thus, the AC noise analysis can be performed whereas, periodic state circuits have a steady periodic state and thus, PNOISE analysis can be performed. Non-linear topologies have none of the above attributes which is why the noise behavior extraction is forced to be simulated using only transient noise analysis. In topologies which operate in multiple time scales, more than one fundamental frequencies can be captured and analyzed. This frequency domain complexity forces the noise integrity simulation to be performed using advanced, multi-time scale domain analyses and hence, introducing the QPSS and ENVLP analysis into the simulation spectrum.

The two driving factors when simulating a test case topology noise-wise are the simulation time and the obtained accuracy. The transient noise analysis was used as the golden reference for the accuracy comparison between the noise analyses. Small-signal AC noise and PNOISE analyses were in great agreement with the transient noise results while high noise simulation accuracy and low simulation times were achieved. When simulating the noise integrity in multiple time scale topologies, the ENVLP analysis was proved to be quite accurate compared to the transient noise results while

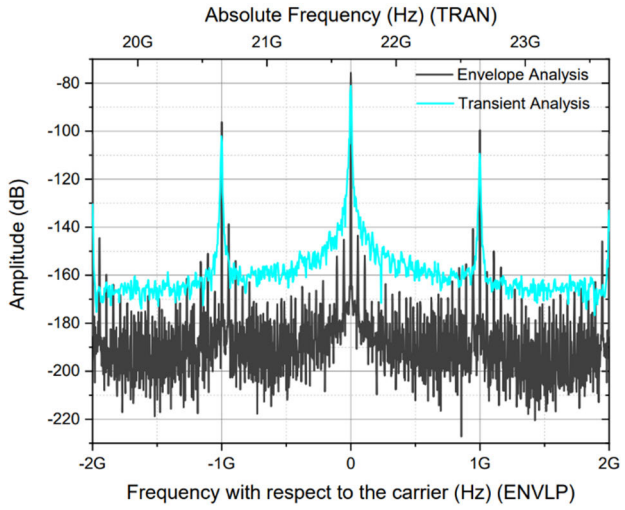

FIGURE 29. Envelope analysis versus Transient analysis of the noise coupled VCO vehicle.

a significant speedup regarding the noise integrity simulation using ENVLP analysis, was achieved.

Besides the discretization of the noise simulation analyses for each circuit type, the dominant noise sources in the respective topologies are a volatile noise parameter. In linear circuit topologies, operating in the low frequency spectrum, flicker noise is the most dominant noise source of the topology. In linear circuits that operate in the high frequency spectrum but not in the deep RF/mmWave frequency spectrum (UHF spectrum using IEEE band designation [38]), thermal noise is the dominant noise source while gate induced noise contribution cannot excel the thermal noise contribution. At the deep RF/mmWave spectrum, gate induced noise contribution is dominant and excels the overall thermal noise contribution. In periodic state circuits, when the oscillation frequency is low, thermal noise is the most dominant noise source in the topology. When the oscillation frequency is high, gate noise contribution overcomes the thermal noise contribution and results in jitter noise. In the same manner, in non-liner circuits which are driven by a high frequency switching signal, gate induced noise is dominant while thermal noise is dominating in topologies with low frequency switching events. In addition, due to unstable operating point, in non-linear circuits, flicker noise can be neglected.

VI. CONCLUSION

Noise simulation guidelines across three major circuit types, linear, periodic state, and non-linear circuits, were provided for fast and accurate noise integrity simulation. Among them, small-signal (AC noise, PNOISE and ENVLP) and large-signal (PSS, QPSS and TRAN) analyses were performed and compared with the transient noise analysis in terms of simulation time, compatibility and obtained accuracy. Three test case vehicles, a linear OTA circuit, a periodic state VCO circuit and a non-linear DC-to-DC boost converter circuit, were designed and simulated noise-wise. The provided noise simulation guidelines were used as to accurately derive the noise behavior across all three test case vehicles while, the obtained noise simulation results were compared to the transient simulation results as a sanity check and accuracy validation. The noise simulation guidelines provided by this work, allow the designer to accurately simulate the noise behavior of the circuit under test regardless of the type of the topology or the fabrication process, enabling a more rapid and efficient design cycle flow.

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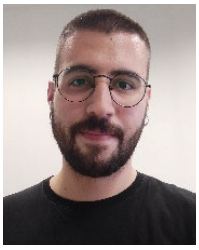

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