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SURVEY

Double-Dual DC-DC Conversion: A Survey of Contributions, Generalization, and Systematic Generation of New Topologies

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ABSTRACT The integration of renewable energy into the grid demands the development of increasingly more sophisticated power electronics configurations. This situation has motivated the current boom of new power converter topologies. Even though most of the recently proposed converters are scattered across the literature, some of them can be classified in a taxonomical fashion. This action permits studying their properties, generalizing principles, and generating new contributions with improved features—these are the general aims and overall research direction reported in this paper. In this work, we are devoted to generating a well-defined corpus of knowledge by characterizing an emerging family of DC-DC double dual converters. We show that the underlying principle of dualization can be fully enclosed within a systematic procedure and applied not only to classical DC-DC converters but also to any modern configuration. This contribution thus permits the diversification of new topologies that hold relevant features, such as low common-mode voltages and currents, high-voltage gains, and efficient harmonic mitigation—among other advantages that are oriented to renewable energy management. We thus demonstrate that systematic dualization leads to the development of new designs with enhanced features. Experimental results of new topologies are also presented to corroborate the proposed principles and advantages.

INDEX TERMS Power electronics, DC-DC power converters, double dual converters.

I. INTRODUCTION

Switching mode power supplies play a central role in many applications, representing an important part of all electronic equipment. The increasing energy consumption and the problems related to climate change make renewable energy sources of particular importance. Some renewable energy technologies, such as fuel cells and PV panels, require DC-DC converters to increase their output voltage and track the maximum power point of operation [1], [2].

Renewable energy imposes strict requirements for power conversion beyond the classical (second-order) family of DC-DC converters that encompasses the traditional buck, boost, and buck-boost converters [1], shown in Fig. 1.

The family of traditional fourth-order converters, such as the Cuk, Sepic, Zeta, etc. [1], shown in Fig. 2. In order to meet such strict specifications such as high-voltage gains and current-ripple mitigation, a recently proposed converter with two inductors and two capacitors, referred to as the double dual boost converter (DDBC), was introduced in [3] (see Fig. 3(d)). However, even though it has fourth energy storage components, the DDBC cannot be identified as a classical fourth-order converter (as those in Fig. 2) since its principle of

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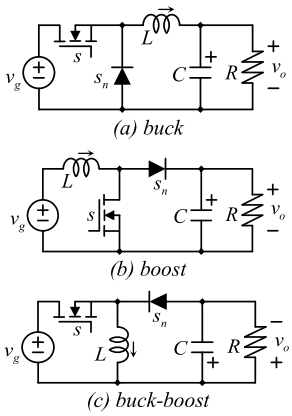

FIGURE 1. The basic family of DC-DC converters (a) buck, (b) boost, and (c) buck-boost topologies.

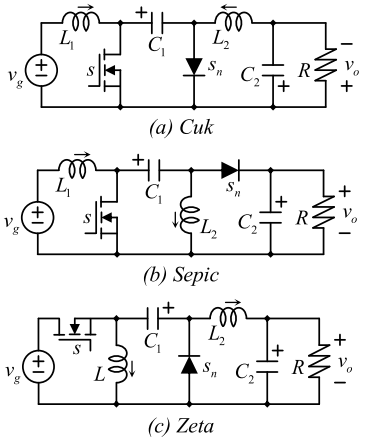

FIGURE 2. Fourth-order DC-DC converters (a) Cuk, (b) Sepic, and (c) Zeta.

operation varies considerably, and it contains two transistors. Furthermore, the DDBC structure consists of two switching stages, as shown in Fig. 3, by interleaving structures (in both the upper and lower switching stage) [3].

The DDBC has been competitive with respect to the classical Interleaved Boost Converter (IBC) [4]. It has advantages such as low input current ripple (similar to the IBC), large voltage gain (larger than the IBC), and modular structure. Therefore, several research works have recently dedicated a full analysis to this converter, which includes design and experimental verification [5], applications [6], [7], [8], [9], modeling and control [10], [11], [12], [13], [14], [15], [16], and modulation strategies with special purposes [17], [18], [19].

Note that the circuit in Fig. 3(d) shares a similar structure as the one proposed in [3] and later studied in [5], [6], [7], [8], [9], [10], [11], [12], [13], [14], [15], [16], [17], [18], and [19]. However, the circuit in Fig. 3(d) is drawn in a planar way, which does not affect the circuit's operation. In addition to DDBC, several topologies with the double dual interconnection have been recently introduced to the literature [20], [21], [22], [23], [24], [25], [26], [27], [28], [29], [30], [31], [32], [33], [34], [35], [36], [37], [38], [39], [40], [41], [42], [43], [44]; this includes, for example, the buck [20], the Cuk [23], the multilevel boost [29], Fly-Back [35], the combination of converter [36], [37], [38], inverted double dual boost [41].

We can hence consider double dual converters as an emerging family of topologies. The main advantage of the double dual circuits against non-double dual configurations is lower voltage stress in semiconductors and lower energy storage required to achieve a particular input and output switching ripple specification. At first sight, a couple of issues might discourage the use of double dual converters, e.g., the higher number of components and the fact that some transistors are not grounded. However, we can notice that the increment of component count is equivalent to the interleaving connection of the converter. Consequently, comparisons between double dual and classical converters must consider the interleaving feature. Then when weighted against the interleaved features, double dual converters have the same number of components compared to traditional solutions. Furthermore, the ungrounded connection of transistors is a common issue that has been successfully solved in other configurations, such as traditional synchronous rectified converters, in which bootstrap gate drivers have been used as a solution.

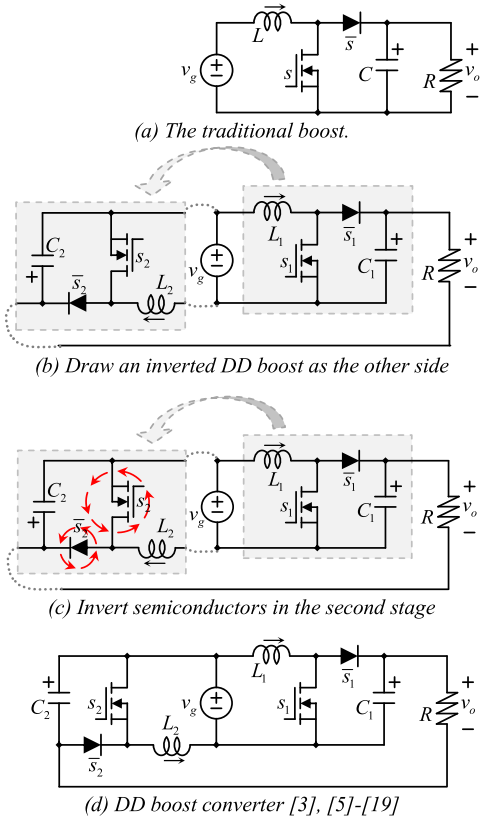

FIGURE 3. Derivation of the double dual boost converter.

This article explores the double dual boost converter initially introduced in [45] and other converters that can be characterized as part of the same family. As the main contribution

of this paper, we present a systematic procedure to obtain double dual (DD) converters out of any general modern topologies, which permits the exploitation of emerging features. A comparative evaluation is also presented based on the boost converter example to emphasize the advantages of the double dual connection. Finally, we also present a review of DD converters that have been recently introduced to the power electronics literature. In fact, among all the review papers that can be found in the literature, this is the first article that is devoted to identifying and generalizing double-dual topologies—including the generation of new configurations. Some DD converters share the advantage of getting low common-mode voltage at the output side, which is a benefit in renewable energy generation applications.

Experimental results with one of the topologies are presented to corroborate the principle of the proposition.

II. BASIC DOUBLE DUAL CONVERTERS

Double Dual (DD) topologies can be defined as converters with at least one upper and one lower switching stage (can be interleaved stages on both upper and lower sides). If the converter's input and output share a common ground, a double dual connection can be implemented. Fig. 4 shows a common-ground DC-DC converter with one power stage (PS_1). It is considered that both input ($+in_1$) and output ($+out_1$) have a positive voltage with respect to the converter ground (g_1).

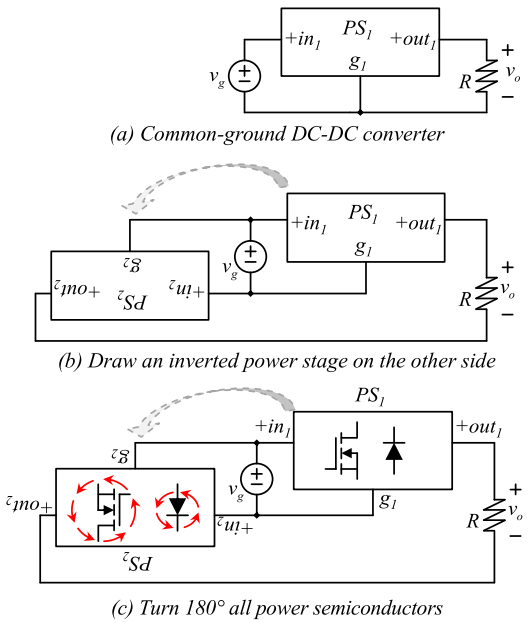

FIGURE 4. Derivation of the double dual boost converter.

The first step is to draw a second power stage, as shown in Fig. 4(b), but twisted 180° in a way that the positive side of the input voltage v_g is connected to the reference of the second power stage (g_2), and the reference of the input voltage is connected to the input ($+in_2$). That would mean the second power stage is connected to an input with inverted polarity. Then power semiconductors must be turned 180° inside the second power stage (PS_2) to prevent a short circuit. The inversion of the source polarity is a known procedure in DC-DC converters [1], [46].

We apply the proposed procedure to the boost converter (see Fig. 3(a)) to obtain its double dual version (see Fig. 3(d)). The first step is to add a second converter (drawn at the left), which is a copy of the original converter twisted in the counterclockwise direction at 180° (see Fig. 3(b)).

The second step is to invert semiconductors. Since the voltage polarity of the second stage is inverted, reversing the semiconductors makes their operation consistent with the new input voltage polarity, see Fig. 4(c). The DD boost converter is shown in Fig. 3(d).

The DD buck converter, recently studied in [20], provides the following advantages: (*i*) it can be used as an inverter, and (*ii*) it generates low common-mode voltage [20].

Following the previously described procedure, new double dual converters can be derived to complete the family of DC-DC DD converters. Fig. 5 shows the basic family of double dual converters. For example, the DD buck-boost converter shown in Fig. 5(c) has been derived following the described procedure.

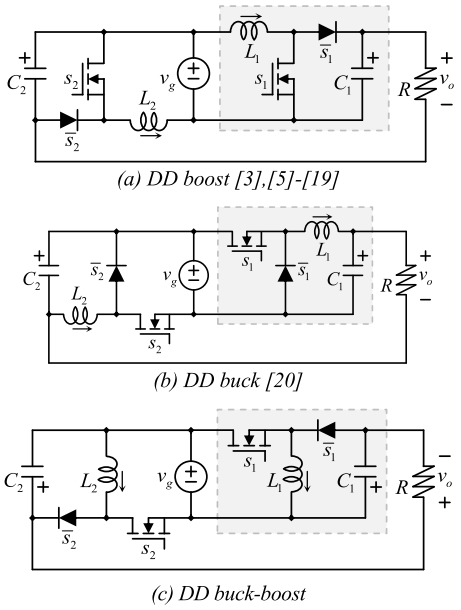

FIGURE 5. The basic family of DC-DC double dual converters.

III. ADVANTAGES OF A DOUBLE DUAL TOPOLOGY

Among the advantages of a double dual interconnection, we can focus on (*i*) the possibility of increasing the voltage gain without increasing the duty cycle. This influences the size of passive components, as will be explained (for instead, inductors due to a kind of interleaving operation). Another advantage reported in [20] is *(iii)* the reduction of common-mode voltage. Let us start with the first advantage:

In converters with discontinuous input current, the input current gets twice the switching frequency, which still helps reduce the size of EMI filters if necessary.

To demonstrate those advantages, let us consider a comparative evaluation with the boost converter (Fig. 6(a)), and the double dual boost (Fig. 6(c)), the interleaved (2-phases) topology (Fig. 6(b)) is also included since it is a very competitive topology and contains the same number of components than the double dual topology.

Consider a converter powered by a renewable energy source that must increase and regulate the voltage for a specific operating range. In renewable energy sources, the voltage depends on the current. Therefore, the behavior can be approximated in the following manner: the maximum power is obtained when the source current is 8.5A and 35V; as the current decreases, the voltage increases (linearly for the example) in a way that the minimum power point is obtained when the current is 1A while the voltage is 50V. Although this is only a design example, the parameters are similar to the H-300 FC stack from the horizon brand [21].

The converter must provide a well-regulated voltage of 200V suitable to feed an H-bridge inverter. The converter then must operate within a voltage gain of 4 to 5.71. Furthermore, there is an input current ripple constraint. The maximum allowable ripple is 0.85A (10% of the rated current) at the maximum power operating condition (when the current from the source is 8.5A). The switching frequency is 50kHz. Fig. 6 shows the topologies and the result of the exercise; the calculations will also be explained.

A. SOLUTION WITH THE TRADITIONAL BOOST CONVERTER

For the boost converter, the inductor is calculated considering the operating condition and the required input current ripple Δi_g as (1).

$$L_A = \frac{DV_g}{2f_S \Delta i_g}. \tag{1}$$

The duty cycle for a particular operating condition can be obtained from the voltage gain equation of the boost converter (2). In this case, the gain is *200/35=5.7143* (this applies to both the traditional and the interleaved boost converter).

$$G = \frac{V_o}{V_g} = \frac{1}{1-D} \Rightarrow D = \frac{G-1}{G}. \tag{2}$$

The inductor L_A which a traditional boost converter requires to comply with the input current ripple, is L_A=*339.71*μH (V_g=*35*, D=*0.8350*). Therefore, this inductor will drain a peak current of *9.35* A, the rated inductor current plus their current ripple at the rated current; this results in *14.8mJ* of stored energy in inductors; this is important since the size of inductors is related to their peak stored energy [1], [22].

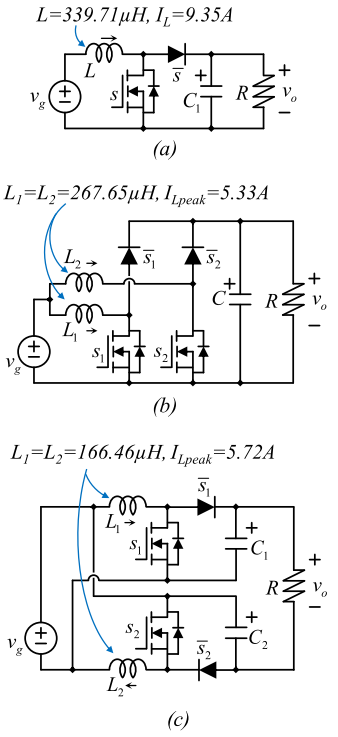

FIGURE 6. Topologies in the comparative evaluation.

B. SOLUTION WITH THE TWO-PHASE INTERLEAVED BOOST

In the case of the interleaved boost converter, inductors are calculated with the same equation, expressed as (3).

$$L_X = \left| \frac{(1-2D)\, V_g}{2f_S \Delta i_g} \right|. \tag{3}$$

The interleaved converter requires two equal inductors with the same inductance (3), but the dc input current is split among them. The inductance of the interleaved boost converter will be called L_B; it turns out to be L_B=*267.65*μH, and both inductors will drain a peak current of *5.3288A*.

Notice that the peak current is larger than half the peak current in the traditional boost inductor. This is because only the dc component of the input current is split among inductors. The peak current includes the DC component plus the current ripple.

The stored energy in both inductors is *7.6mJ*. Although the number of inductors is two, their combined size is smaller than the size of the inductor in a single-phase boost.

C. SOLUTION WITH THE DOUBLE DUAL BOOST

As mentioned before, inductors in the double dual boost are still calculated with (3), but the difference against the design in an interleaved boost lies in the duty cycle. It is different since the gain of converters is different.

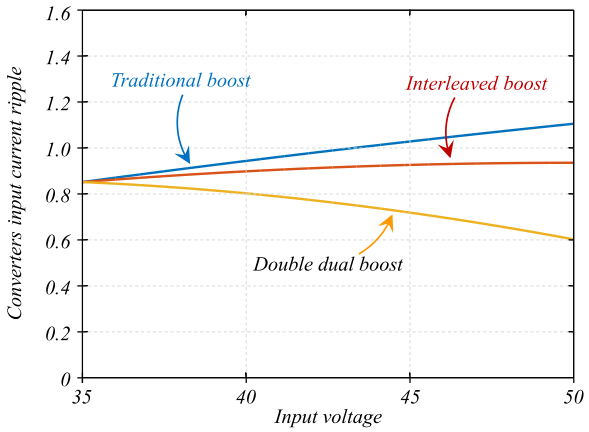

FIGURE 7. Input current ripple of all converters vs. the input voltage within the entire operating range.

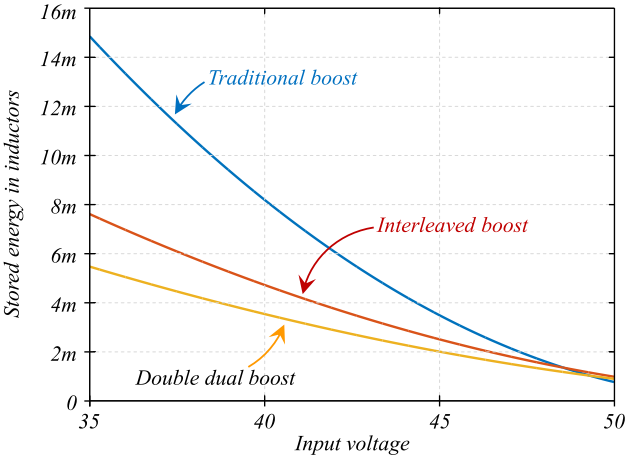

FIGURE 8. Stored energy in the inductors of converters under comparison.

The duty cycle for a particular operating condition can be obtained from the voltage gain equation as:

$$G = \frac{V_o}{V_g} = \frac{1+D}{1-D} \Rightarrow D = \frac{G-1}{G+1}. \tag{4}$$

The inductance of the double dual boost converter will be called L_C, and it turns out to be L_C=*166.46*μH; both inductors will drain a peak current of *5.7263A*.

The peak current is slightly larger (7.5% larger) than in the interleaved boost converter, but the required inductance is considerably smaller. This is because the stored energy in both inductors is *5.5mJ*, resulting in the exercise's smallest inductors.

Fig. 7 shows the input current ripple of all three topologies with the parameters shown in Fig. 6.

All converters have the same current ripple when the input voltage is 35V. This is expected since it was the design specification. Still, it can also be observed that the traditional and the interleaved boost have an increase in their input current ripple as the input voltage is decreasing, in contrast to the double dual boost in which the input current ripple decreases. This is because the input current ripple presents a compromise against the stored energy or the inductance in inductors; Fig. 8 shows the stored energy in inductors; their peak value is related to the size of the physical inductor [1], [22].

It is evident that the double dual boost converter requires a smaller inductor against the traditional boost but also against the interleaved boost. Both may have more than two phases in the case of the interleaved boost and the double dual boost, but the advantage remains. As can be seen, the reduction of the stored energy requirements on capacitors is due to the increase in voltage gain. Another advantage is the reduction of voltage stress on semiconductors. In all cases, semiconductor voltage stress is calculated as (5).

$$V_{stress} = \frac{V_g}{1-D}. \tag{5}$$

A larger voltage gain results in a smaller duty cycle, which also reduces the voltage stress in semiconductors. The result of this comparison can be verified by theoretical analysis or by computer simulation.

On the other hand, a disadvantage of the double dual boost converter is that one of the drains of the transistors (s_2) is not connected to the input ground. A kind of inverted bootstrap can be implemented. Furthermore, the load and the source do not share a common ground; double dual converters can be used in applications in which common ground is not required. Those applications may include renewable energy generation systems [15], [16], [17], [18], [19], [20].

From the present example, we can corroborate that the energy stored by inductors is smaller in the double dual boost converter, with respect to the traditional interleaved boost configuration. This is due to a significant reduction in the inductance value, which is required to achieve the same specified input current ripple. The double dual boost requires approximately 60% of the inductance that is required by the interleaved boost converter (see Fig. 6). On the other hand, the peak current increases only slightly from 5.33A to 5.72A (about 7%). It is then important to emphasize that this peak energy increase is not caused by the double dual interconnection per se. In fact, the average current is the same for inductors in the interleaved boost and the double dual boost converter. The small increase is fully ascribed to the inductance reduction, which can be considered as a relevant advantage in terms of the inductor size and costs.

Additionally, it can be noticed that the provided example considers computations for both converters with respect to the same input current ripple. Since, the inductors in the double dual boost resulted in a smaller size, it is a straightforward matter to use a smaller inductance specification that can match the same peak current through inductors. In such case, the double dual boost converter would require inductances equal to 227.8 μH, which are still lower than the 267.65 μH of the traditional interleaved boost converter.

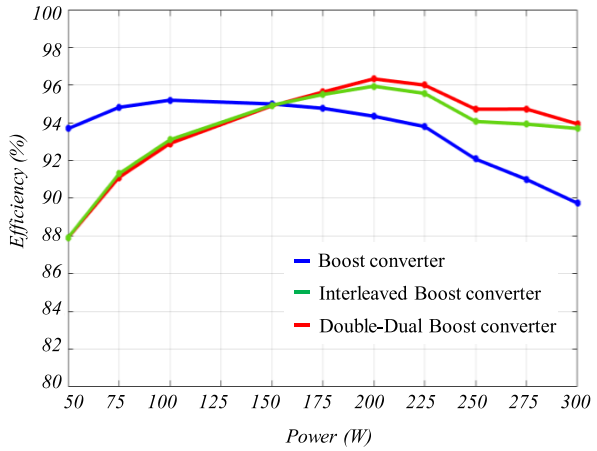

FIGURE 9. Efficiency of converters under comparison.

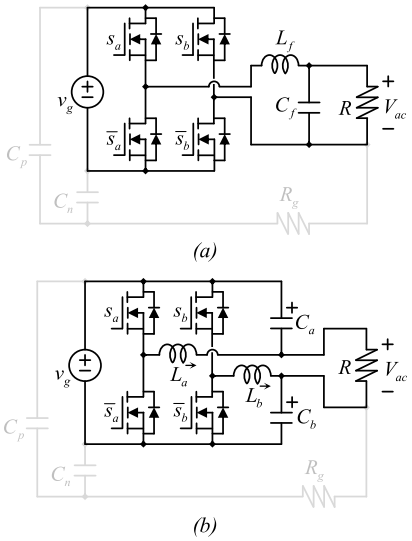

FIGURE 10. Common mode current paths in inverters (a) the classical H-bridge inverter (b) the double dual buck converter [20].

To complement this analysis, an efficiency comparison of the three topologies under discussion is presented, see in Fig. 9. The same design parameters were used to calculate conduction and switching losses, as well as the overall converters' efficiency. The output power and input voltage were adjusted to be consistent with the polarization curve of a fuel cell. From the graphic, it can be seen that for low power, the single stage boost converter is more efficient than the interleaved and DD topologies. This is mainly due to the switching losses, which become more significant in the topologies with more semiconductor devices. Additionally, from 150W to 300W the interleaved and double dual topologies become more efficient than the traditional boost converter. The double dual converter is more efficient than the interleaved boost converter at the rated power this is due to the smaller duty cycle required to obtain the 200V output voltage.

The cost of the converters can be then evaluated in terms of the component expenses and power density. For example, since the output of the double dual boost converter has a modular structure, requiring small capacitors instead of a single high voltage capacitor, the converter scores high in power density and bypasses the need of expensive high-voltage output capacitors. In addition, even when the component count of the double-dual topology is slightly higher, the voltage/current ratings of the components (inductors and semiconductors) are smaller, which results in lower cost component-wise.

Additionally, there is an important advantage of double-dual configurations with respect to traditional topologies, in terms of minimization of common mode currents. Fig. 10 shows two feasible inverter topologies, the classical H-bridge inverter and the double dual buck converter [20], Fig. 10 also shows the ground path, in which parasitic capacitances may drain a small amount of current from the source chassis, and through the system ground, this is called common-mode current.

This was first observed in large power motor drivers [47], [48], [49]. Currently, a similar phenomenon is observed in renewable energy applications, for example, in grid-tie transformer-less inverters [50], [51]. Parasitic capacitances shown in Fig. 10 can be small and present a relatively large impedance at the grid frequency. Still, they may present a low impedance at the switching frequency and their harmonics. There are already limitations to this current in international standards, i.e., the DIN VDE 0126–1-1 requires their RMS value to be smaller than 300 mA [51], [52].

It was demonstrated in [20] that the double dual buck converter helps to reduce the amount of common-mode current considerably. It also can be observed from Fig. 10(b) the ground resistance path has a continuous voltage, while in Fig. 10(a), it has a discontinuous voltage (pulsating at the switching frequency.

We can conclude that the DD boost is the most studied topology of the family (see Fig. 5). It exhibits higher voltage gains than the traditional interleaved boost configurations, requiring less energy storage to achieve the same input current ripple specification. Furthermore, the DD buck has been recently studied (Fig. 10), and its main advantage is that it can produce positive, negative, or alternating voltage, and then it can be used as an inverter. In addition, as an advantage against the traditional H-bridge, the DD buck has low common mode voltage and current. Finally, the double dual buck-boost is the only converter which has not been fully explored, with no evident advantages. Its dualization results in a step-up converter topology.

IV. THE VOLTAGE GAIN OF DOUBLE DUAL TOPOLOGIES

Fig. 5 shows the first members of the proposed DD converters subfamily as an extension to the basic DC-DC DD converters family.

In all cases, both transistors are driven with the same duty cycle; however, the switching functions are phase-shifted

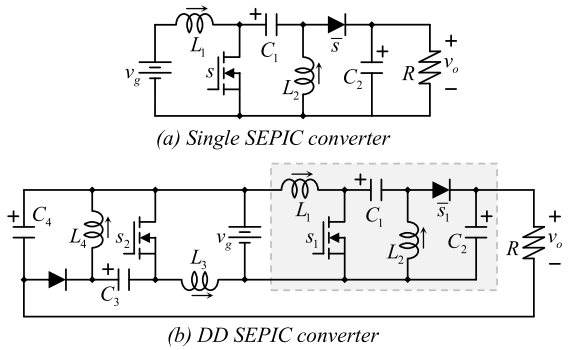

FIGURE 11. Single and DD SEPIC converters.

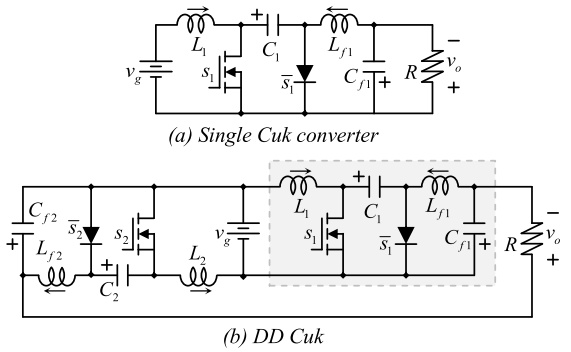

FIGURE 12. Single and DD Ćuk converter [23].

by 180°. In the interleaved version, switching functions are phase-shifted by 360°/n, with n the number of switching stages connected in parallel.

Individual switching stages preserve their voltage gain. However, after the load connection, the voltage gain of the proposed converters differs from the traditional single topologies. For example, the traditional boost converter has a voltage gain of

$$G_{boost} = \frac{1}{1-D}. \tag{6}$$

While the gain of the double dual boost converter is

$$G_{DDboost} = \frac{1}{1-D} + \frac{1}{1-D} - 1 = \frac{1+D}{1-D}, \tag{7}$$

which comes from the fact that the output voltage is equal to both capacitors' voltages following (6) minus the input voltage since they are connected in subtractive series, as observed in Fig. 3(a).

A similar situation happens in the DD buck converter, where capacitors are in additive series among them but in subtractive series with respect to the input voltage source. Therefore, the gains for the single and the DD buck converters are, respectively,

$$G_{buck} = D, \quad G_{DDbuck} = 2D - 1. \tag{8}$$

In the DD buck-boost converter, both capacitors and input voltage are in additive series; hence, the gains for the single and the DD buck-boost converters are, respectively,

$$G_{buck-boost} = \frac{D}{1-D}. \tag{9}$$

$$G_{DDbuck-boost} = \frac{D}{1-D} + \frac{D}{1-D} + 1 = \frac{1+D}{1-D}. \tag{10}$$

It is worth noticing that the DD boost and the DD buck-boost have the same gain but with a different output voltage polarity. Moreover, in the DD buck-boost converter, the voltage through capacitors has a smaller level for the same voltage gain. Besides, the DD buck-boost converter has a discontinuous input current.

Fig. 11 shows the DD single-ended primary-inductor SEPIC converter.

Notice that capacitors are in additive series between them, but the input voltage is in subtractive series. Therefore, the gains for the single and DD SEPIC converters are (11) and (12), respectively.

$$G_{SEPIC} = \frac{D}{1-D}, \tag{11}$$

$$G_{DDSEPIC} = \frac{D}{1-D} + \frac{D}{1-D} - 1 = \frac{3D-1}{1-D}. \tag{12}$$

Fig. 12(a) shows the traditional Ćuk converter, while Fig. 12(b) shows the DD Ćuk converter [23], which is derived from the traditional Ćuk converter with the systematic procedure discussed in Section II.

As expected, all capacitors and input voltage sources are in additive series; however, the polarity of the output voltage in each individual switching stage is in the opposite direction compared to the SEPIC converter. Therefore, the gains for the single and DD Ćuk converters are, respectively,

$$G_{Cuk} = \frac{D}{1-D}. \tag{13}$$

$$G_{DDCuk} = \frac{D}{1-D} + \frac{D}{1-D} + 1 = \frac{1+D}{1-D}. \tag{14}$$

We conclude that fourth order double dual converters have similar advantages as the DD boost. Their voltage gain is higher, and they do not display step-down capabilities. From their voltage gain analysis, we also conclude that their minimum voltage gain is one. In the case of the the double dual Cuk converter, it holds the advantages of its classical counterpart, having a continuous input current and their output capacitors have continuous current, which is beneficial from the EMI point of view.

A. THE DOUBLE DUAL VERSION OF FC TOPOLOGIES

There is a sub-family of converters that may be derived from the family of second-order converters (Fig. 1), but in this case, the output capacitor connection is changed from the negative to the positive terminal of the power supply; see Fig. 13(a). This family of converters can be referred to as flying capacitor (FC) converters [24].

Fig. 13(b) shows the equivalent circuits according to the switching state, from which the following large-signal

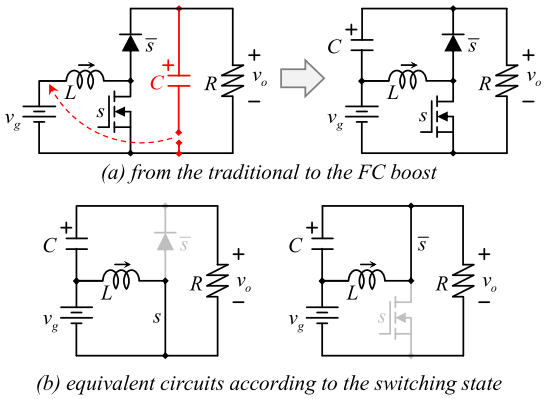

FIGURE 13. (a) Deriving the FC boost from the traditional boost and (b) equivalent circuits according to the switching state.

equations can be written as (15)-(16).

$$L\frac{di_L}{dt} = dv_g - (1-d)\,v_C. \tag{15}$$

$$C\frac{dv_C}{dt} = (1-d)\,i_L - i_o. \tag{16}$$

From (15)-(16) an equilibrium of the converter can be expressed as (17)-(18).

$$V_C = V_g\frac{D}{1-D}. \tag{17}$$

$$I_L = I_o\frac{1}{1-D}. \tag{18}$$

Although the capacitor has a different voltage than the traditional boost, the converter gain is not affected since the input source and the capacitor provide the output in the following manner:

$$V_o = V_g + V_g\frac{D}{1-D} = V_g\frac{1}{1-D}. \tag{19}$$

By applying the same procedure as in Fig. 12(a) to the buck and the buck-boost converter, the set of second-order converters can become an FC family. Fig. 13 show other FC converters of the second order (basic) family, along with their double dual version.

Fig. 14(a) shows the FC boost converter. Their operation can be considered equivalent to the traditional boost. The advantage is a reduced voltage across the capacitor, and the disadvantage is that the input current is not continuous but pulsating. Fig. 14(b) shows the double dual flying capacitor (DD-FC) boost converter.

Fig. 14(c) shows the FC buck and the case of the FC boost; their operation is like the traditional buck. In this case, without any additional advantage to the best of our knowledge.

Fig. 14(d) shows the DD-FC buck converter.

Fig. 14(e) shows the FC buck-boost, and Fig. 14(f) shows the DD-FC buck-boost converter. The derivation of the FC buck-boost may be performed in the same way as others, see Fig. 15(a).

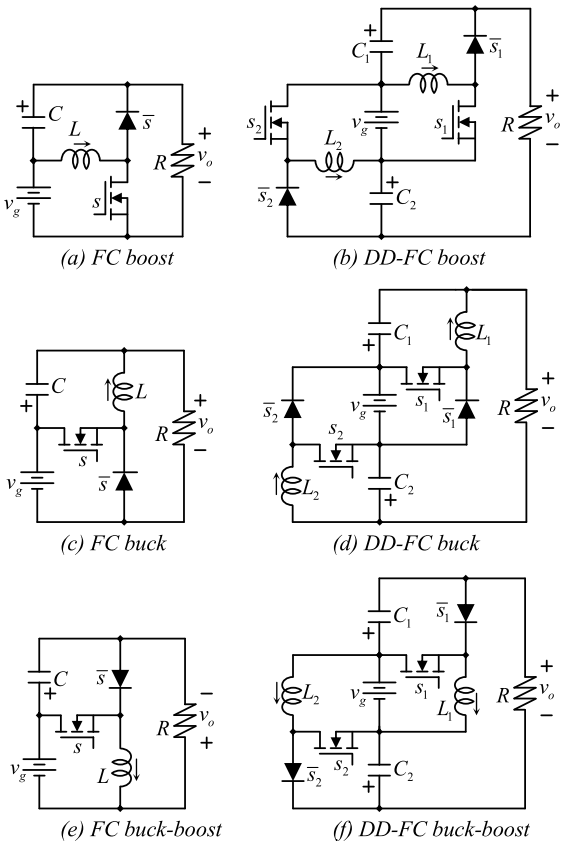

FIGURE 14. The set of FC converters [24], and the DD-FC converters.

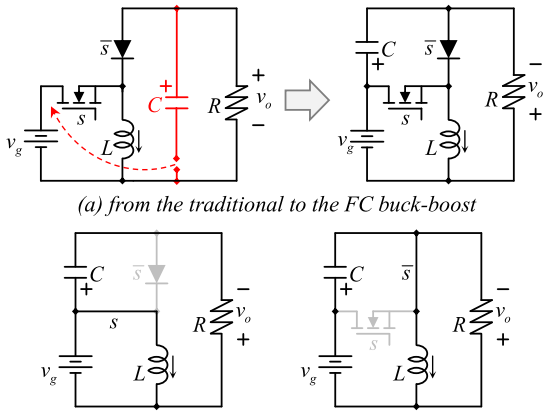

FIGURE 15. (a) Deriving the FC buck-boost from the traditional buck-boost and (b) equivalent circuits according to the switching state.

Fig. 14(b) shows the equivalent circuits according to the switching state, from which the following large-signal equations can be written.

$$L\frac{di_L}{dt} = dv_g - (1-d)\left(v_g - v_C\right). \tag{20}$$

$$C\frac{dv_C}{dt} = (1-d)\,i_L - i_o. \tag{21}$$

From (20)-(21) an equilibrium of the converter can be expressed as:

$$V_C = V_g \frac{1}{1-D}. \tag{22}$$

$$I_L = I_o \frac{1}{1-D}. \tag{23}$$

Although the capacitor has a different voltage than the traditional boost, the converter gain is not affected since the output is given by the capacitor's voltage minus the input voltage source.

$$V_o = V_g \frac{1}{1-D} - V_g = V_g \frac{D}{1-D}. \tag{24}$$

The disadvantage of the FC buck-boost converter is that the capacitor sustains a larger voltage compared to the traditional buck-boost converter, the voltage in the FC topology is like the boost converter (see (22)). But it has an advantage. It provides continuous input and output current, which is a remarkable difference from the traditional topology in which both input and output current is discontinuous.

FC converters preserve the same gain of traditional converters, and thus the voltage gain of DD-FC converters can also be expressed as (7), (8), and (10).

The DD-FC buck-boost converter is of special interest because its input current is continuous, which is in sharp contrast with the DD-FC boost and DD-FC buck converters, as well as with some other converters where the input current is pulsating. Moreover, the DD-FC buck-boost can be configured as an interleaving structure, which can further reduce the input current ripple. In addition, current ripple canceling techniques can also be designed and implemented to obtain zero input current ripple for a specific duty cycle [16].

In Table 1 we summarize the main converter specifications encompassing output voltage gains, voltage stress across semiconductors and input current ripples for the five traditional DC-DC converter topologies (boost, buck, buck-boost, SEPIC and Cúk) and their double-dual versions. It is worthwhile to notice that some parameters depend on the duty cycle value.

We conclude that the family of flying capacitor double-dual converters hold the advantages of their classical counterparts. In the case of the boost topology, since it has two capacitors that exhibit lower voltage than the output voltage we can say their voltage rating is low.

V. OTHER DOUBLE DUAL TOPOLOGIES

The DD version of several other converters has been previously introduced in the power electronics literature. For instance, the combination of voltage multiplier cells with non-isolated DC-DC converters was explored in [25], where the converter shown in Fig. 16(a) was proposed.

The DD version of this combination was later explored in [26], where a six-phase converter was studied. Fig. 16(b) shows the combined converter in a four-phase configuration. This converter can be further extended as proposed in [27].

TABLE 1. Comparison of key specifications of the traditional power converters.

	Voltage Gain	Voltage stress in switch	Input current ripple
Boost	$\frac{1}{1-D}$	$\frac{V_g}{1-D}$	$\frac{DV_g}{2f_sL}$
DD-Boost	$\frac{1+D}{1-D}$	$\frac{V_g}{1-D}$	$\left\lvert\frac{(1-2D)V_g}{2f_sL}\right\rvert$
Buck	D	V_g	*n.a*
DD-Buck	$2D-1$	V_g	*n.a*
Buck-Boost	$\frac{D}{1-D}$	$\frac{V_g}{1-D}$	*n.a*
DD-Buck-Boost	$\frac{1+D}{1-D}$	$\frac{V_g}{1-D}$	*n.a*
Sepic	$\frac{D}{1-D}$	$\frac{V_g}{1+D}$	$\frac{DV_g}{2f_sL}$
DD-Sepic	$\frac{1+D}{1-D}$	$\frac{V_g}{1+D}$	$\left\lvert\frac{(1-2D)V_g}{2f_sL}\right\rvert$
Cuk	$\frac{D}{1-D}$	$\frac{V_g}{1+D}$	$\frac{DV_g}{2f_sL}$
DD-Cuk	$\frac{1+D}{1-D}$	$\frac{V_g}{1+D}$	$\left\lvert\frac{(1-2D)V_g}{2f_sL}\right\rvert$

Fig. 17(a) shows the non-isolated soft-switching DC-DC converter proposed in [28], which is similar to a multilevel boost converter [2], with resonant charge interchange among capacitors. Fig. 17(b) shows its DD version studied in [29]. Converters in Fig. 11(b) and Fig. 12(b) have been drawn in the DD format to look similar to those in Fig. 3(b).

There are other topologies that utilize this concept, whose figures are not included here for space constraints. For instance, in [30], a high step-up DC-DC converter is proposed. This converter utilizes a built-in transformer with a voltage multiplier cell and the DD concept. The converter is based on cells that have not been individually presented. Other similar topologies have also appeared in the power electronics literature [31], [32]. A double dual Fly-back converter was presented in [33]. Then, in [34], a DD version of [35] is presented, where the authors explore the concept of coupling inductors to increase the converter gain.

A. COMBINATIONS

It is also possible to combine converters having a DD structure. For example, [36] combines an upper buck with a lower

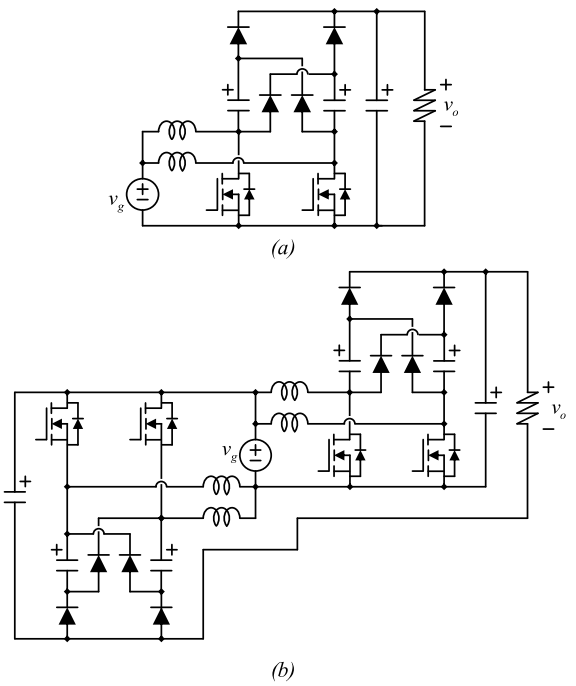

FIGURE 16. (a) Converter studied in [25], and (b) the fourth phases version of the converter studied in [26].

boost module, which provides bidirectional power flow without synchronous rectification. In [37], a combination of an upper series-capacitor boost is presented (see [38]) for the single topology with a lower stage of a simple boost topology.

We conclude that emerging topologies can be connected in a double-dual fashion. This means that there are plenty of possibilities that have not been yet explored, and their dualization opens the door for a whole new area of DC-DC converter research.

VI. INVERTED (SOURCE AND LOAD) TOPOLOGIES

DC-DC converters may be designed for unidirectional power flow or bidirectional power flow [1]. The way of transforming a unidirectional converter into a bidirectional converter is by adding new transistors in an antiparallel connection with the original diodes plus new diodes in an antiparallel connection with the original transistors. For instance, applying this procedure to the buck converter would lead to the converter shown in Fig. 18(a), which can now work as a boost converter if the source and load are exchanged.

This procedure can also be applied to a DD converter. For instance, the bidirectional DD boost converter was used in [39] for a battery management system that requires bidirectional power flow. If transistors and diodes/transistors are simply exchanged, then the buck converter of Fig. 1(a) becomes the boost converter of Fig. 1(b) and vice-versa.

This well-known procedure [1] may be applied to the DD topologies, leading to yet another list of topologies. It should not be surprising that some of those topologies are already available in the literature.

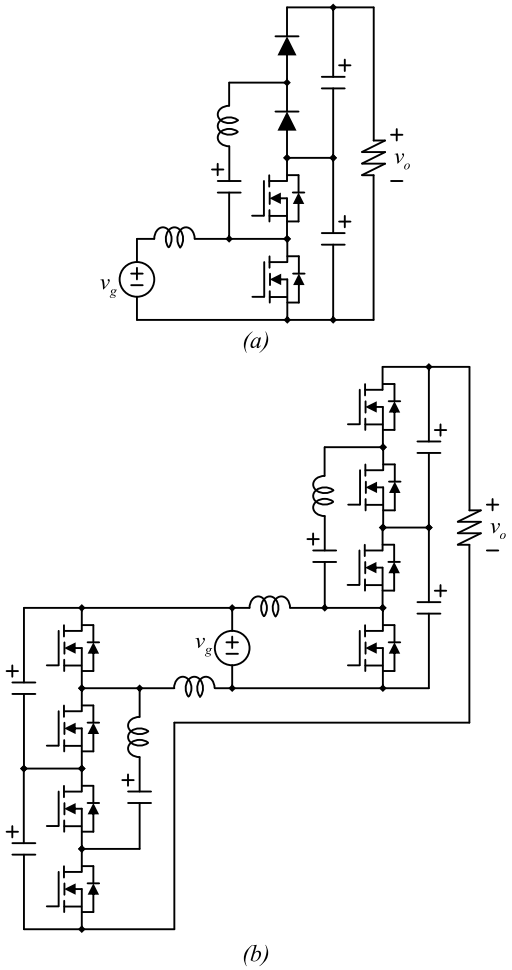

FIGURE 17. (a) Soft-switching converter studied in [28], and (b) its DD converter version studied in [29].

For example, Fig. 19(a) shows the inverted DD boost converter, while Fig. 19(b) shows a recently proposed topology [40], which is, in essence, the same circuit of Fig.8(a) with an output low pass filter. In the same way, [41] presents a DD version of an inverted series-capacitor buck converter.

It is worth noticing that the current through the inductors shown in this subsection is negative since the power flow is opposite, but voltage polarities do not change. Fig. 20 shows the inverted version of the DD buck and DD buck-boost converter.

The same procedure for the exchange between source and load can be applied to the DD SEPIC and DD Cuk converter shown in Fig. 11 and Fig. 12, respectively.

Flying capacitor converters can also admit the exchange between source and load; hence three other converters can be derived, see Fig. 14. Other examples of inverted versions of DD converters can be found in [42] and [43].

We conclude that the source and load inverted topologies hold the advantages of the DD boost converter, as they can be exploited for buck implementations, as shown in [40]. This represents a significant advantage since, as mentioned

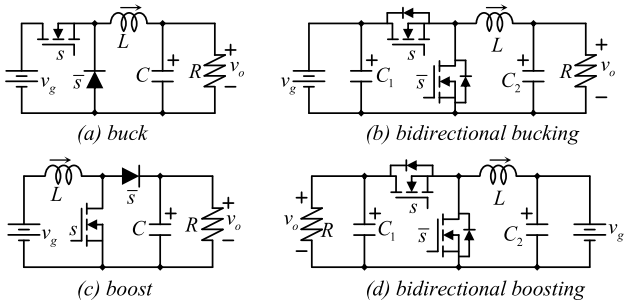

FIGURE 18. Bidirectional converters (buck or boost).

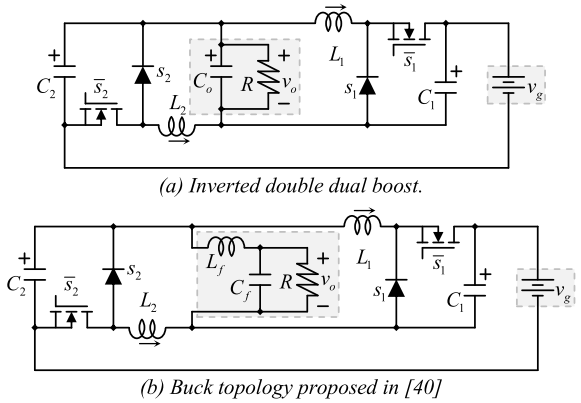

FIGURE 19. Inverted DD boost.

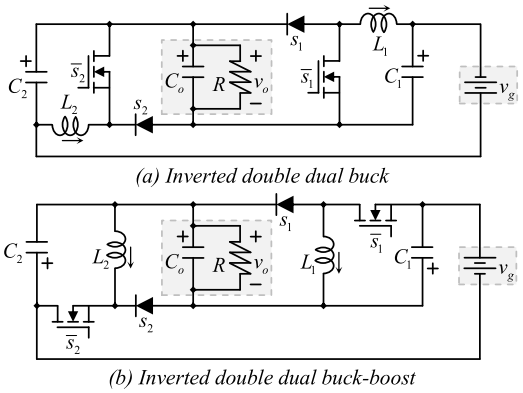

FIGURE 20. Inverted DD buck-boost.

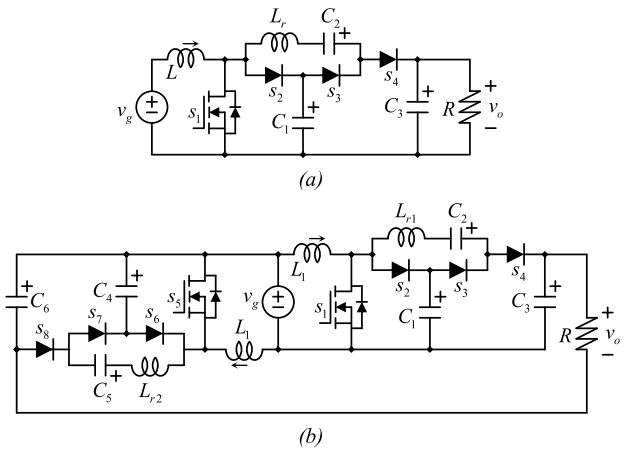

FIGURE 21. (a) Converter studied in [25], and (b) schematic of the experimental prototype.

before, some buck-boost topologies lose their ability to buck the voltage when connected in a double dual form. But the load and source inversion allows to utilization of a wide range of topologies to perform the buck action.

VII. ADVANTAGES IN REAL-TIME IMPLEMENTATIONS

Double-dual topologies display several advantages in terms of applications that require real-time implementations. These benefits have been initially explored for the double-dual boost converter; see e.g., [10] and [15].

The first relevant advantage is the fact that in contrast with traditional interleaved topologies, double-dual configurations do not require closed-loop current balancing. This follows from the fact that the converter output capacitors are not required to exhibit the same voltage. This advantage permits simplifying the control implementation as reported in [10] and [15]. Additionally, as reported in [15], the point of perfect input current ripple cancellation can be arbitrarily selected, as opposed to the traditional point-of-view when perfect cancellation only occurs with a duty cycle, e.g., equal to 0.5.

In both [10] and [15], it is also reported that the small-signal and large-signal models of double-dual configurations can be easily handed in discrete time, which facilitates a digital implementation. This feature highlights the current trends of double-dual converters, which encompass practical real-time digital control implementations, effective current-ripple mitigation, and output-voltage control for renewable energy conversion systems.

VIII. EXPERIMENTAL VERIFICATION

In this section, we present a series of experimental tests to demonstrate the most important characteristics of a double dual topology. For the experiments, we used the single-stage converter previously presented in [25], which is a boost converter combined with a voltage multiplier, as shown in Fig. 21(a). The circuit in [25] presents the following equilibrium or steady state operation:

$$V_{C1} = V_{C2} = V_g \frac{1}{1-D}; V_{C3} = V_g \frac{2}{1-D}. \tag{25}$$

$$I_o = \frac{V_{C3}}{R}; I_L = I_o \frac{1}{1-D}. \tag{26}$$

$$I_{Lr} = 0. \tag{27}$$

The inductor L_r is in series with the capacitor $C_{2;thus}$, their common equilibrium current is zero. In fact, their function is to smoot the current interchange among paralleled capacitors.

In Fig. 21(b), we show the DD version of the converter; as can be seen, it meets the design criteria previously presented

TABLE 2. Experimental prototype.

Component's parameters	
s_1, and s_5	FDD390N15A
L_1, and L_2	100 µH
C_1 to C_6 (all caps)	4 µF
s_2, s_4, s_6, and s_8	V8PM12-M3/86A
s_3 *and* s_7,	V20PWM12CHM3/I
Operating conditions	
Input voltage Range	V_g = 20 V to 36V Nominal=24V
Output voltage	V_o= 200V
Output power	250 W

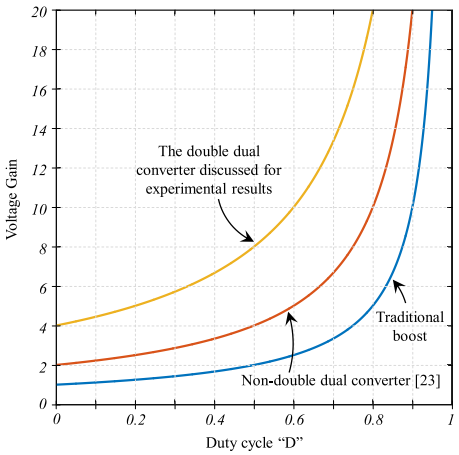

FIGURE 22. The voltage gain of the experimental converter compared to that of the traditional boost and their non-double dual version.

and has the typical topological structure of a double dual converter.

The equilibrium of the DD version of the circuit can be expressed as

$$V_{C1} = V_{C2} = V_{C4} = V_{C5} = V_g \frac{1}{1-D}. \tag{28}$$

$$V_{C3} = V_{C6} = V_g \frac{2}{1-D}. \tag{29}$$

$$V_o = V_{C3} + V_{C6} - V_g = V_g \frac{3+D}{1-D}. \tag{30}$$

$$I_o = \frac{V_o}{R}. \tag{31}$$

$$I_g = I_o \frac{3+D}{1-D}. \tag{32}$$

$$I_{Lr1} = I_{Lr2} = 0. \tag{33}$$

The voltage gain of the experimental converter, shown in Fig. 22, can be obtained from (30). Table 2 shows the components parameters and the operating conditions of the experimental prototype of Fig. 21(b).

Fig. 23 shows some relevant waveforms of the converter, particularly the current through inductors L_1 and L_2, the input current i_g, the voltage across the capacitors C_4 and C_6, the output voltage v_o, and the voltage across the switch s_1,

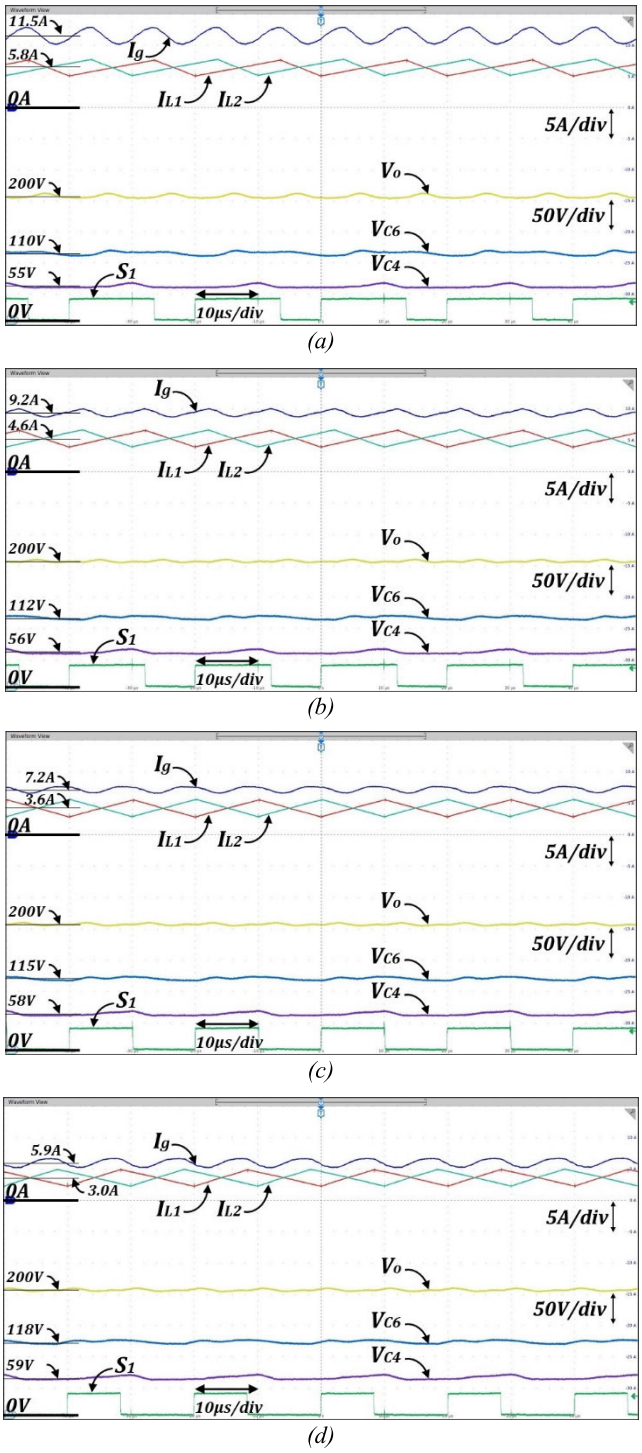

FIGURE 23. Relevant signals for 200W output power under $V_o = 200$ V. The signals include the switching functions for s_1, input current i_g, current through inductors i_{L1} and i_{L2}, voltage across capacitors v_{C4} and v_{C6}, and the output voltage, for (a) $V_g = 20V$, (b) $V_g = 24V$, (c) $V_g = 30V$, and (d) $V_g = 36V$.

which is naturally complementary to the switching function. Waveforms were captured with an output voltage regulated to 200V, while the input voltage was changed with the following values: 20V (Fig. 23(a)), 24V (Fig. 23(b)), 30V (Fig. 23(c)), 36V (Fig. 23(d)).

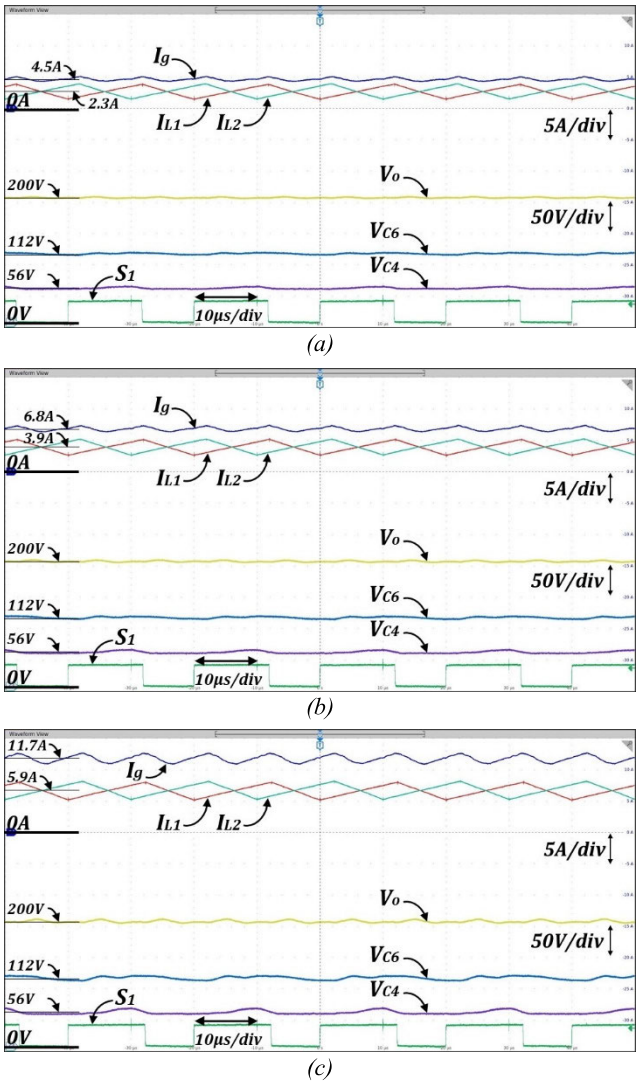

FIGURE 24. Relevant signals for varying output power under $V_g = 24V$ and $V_o = 200$ V. The signals include the switching functions for s_1, input current i_g, current through inductors i_{L1} and i_{L2}, voltage across capacitors v_{C4} and v_{C6}, and the output voltage, for (a) $P_O = 100W$, (b) $P_O = 150W$, (c) $P_O = 200W$.

As can be seen, the input current ripple has a different value in each plot due to the change of duty cycle that is needed for adjusting the output voltage when the input voltage is changed. Please notice that the voltage in capacitor C_6 is always twice the voltage in capacitor C_4. These results are in good agreement with the theoretical expectations.

In Fig. 24, the same converter variables are plotted but now using nominal input voltage $V_g = 24$V and varying the output power with the following levels: 100W (Fig. 24(a)), 150W (Fig. 24(b)), 250W (Fig. 24(c)). As can be seen, in all cases, not only the current through each inductor is smaller than the input current, but also the input current ripple is smaller than the individual inductors' ripple. The voltage ratio between capacitor C_4 and C_6 is the same in all cases and correspond to a portion of the output voltage.

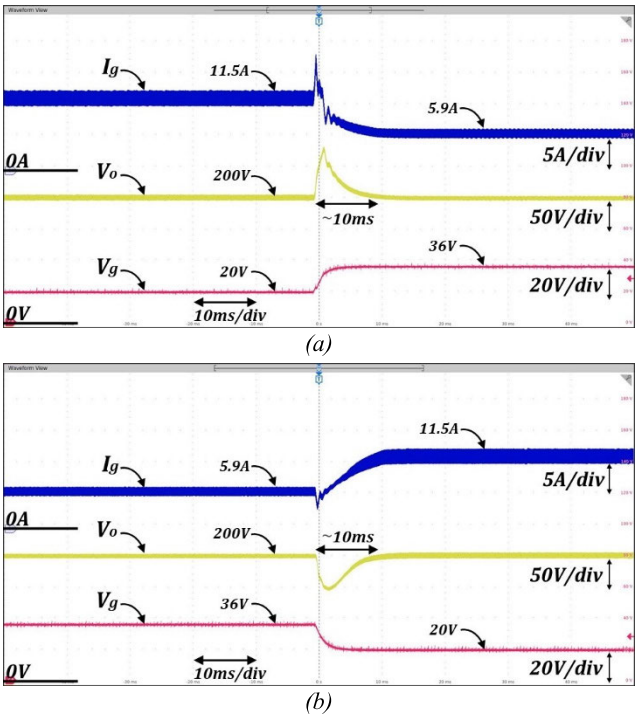

FIGURE 25. Dynamic response of the DD converter under close loop control and input voltage sudden variation. (a) For a change in the input voltage from 20V to 36V. (b) For a change in the input voltage from 36V to 20V.

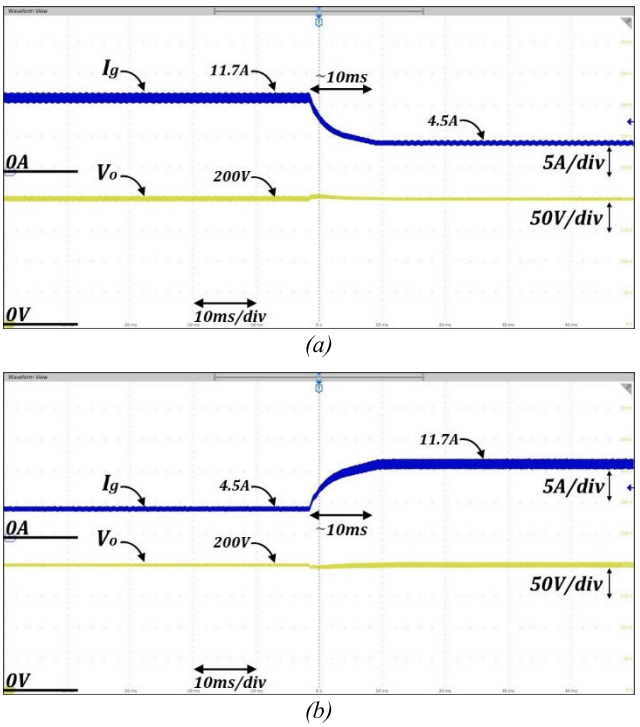

FIGURE 26. Dynamic response of the DD converter under close loop control and output load sudden variation. (a) For a change in load from 150W to 250W. (b) For a change in load from 250W to 150W.

The converter was also tested under closed-loop control for dynamic performance verification. As can be seen in Fig. 25,

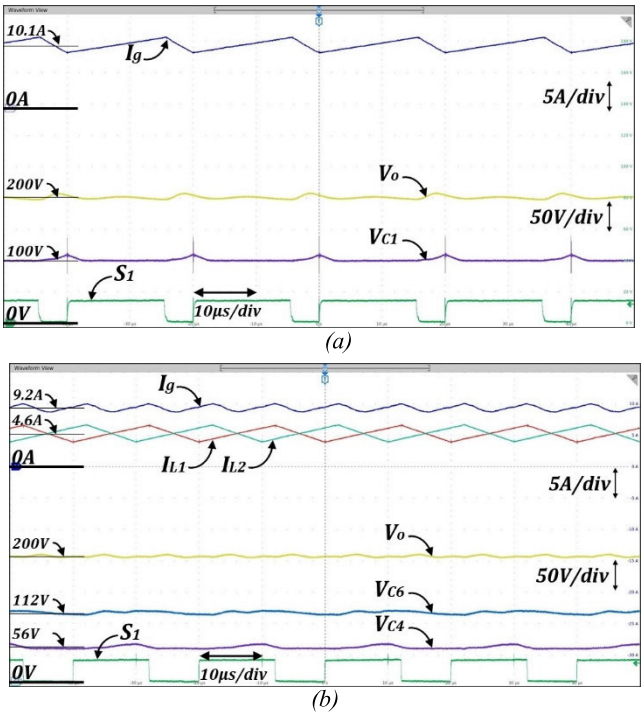

FIGURE 27. Comparison of the single stage converter against its double dual version. (a) Important waveforms of single stage converter. (b) Important waveforms of the DD version.

TABLE 3. Parameters of the single stage converter.

Component's parameters	
S_1	STW56N65M2
L_1	500 µH
C_1 to C_3 (all caps)	4 µF
s_2, s_3 and s_4	APT60S20BG
Operating conditions	
Input voltage Range	V_g = 20 V to 36V Nominal=24V
Output voltage	V_o= 200V
Output power	250 W

the input voltage was suddenly changed from 20V to 36V (Fig. 25(a)) and back from 36V to 20V. In both cases, the input current and output voltage present an overshoot with a bounded response and settling time from the transitions of about 10ms. Furthermore, due to the change of operating point, the input current and output voltage ripples present different magnitudes.

In Fig. 26, a second closed-loop test is shown. In this case, the output power was changed from 100W to 250W (Fig. 26(a)) and back from 250W to 100W (Fig. 26(a)). Again, the behavior of the converter is stable, and the input current and output voltage variables are well-bounded with almost no overshoot.

To get a better idea of the performance of the double dual converter compared to the single stage circuit, an additional prototype was built for the converter shown in Fig. 21(a) using similar specifications of the DD version, as can be seen in Table 3.

The two converters were tested under similar conditions of input voltage (24V) and output power (200W). In Fig. 27 relevant waveforms of the two converters, operating in steady state, are shown.

It can be seen that the input current is larger in the case of the single stage converter due to the lower efficiency. Both converters have similar input current ripple, however, the inductor in the case of the single stage circuit is five times larger than each individual inductor in the DD circuit which result in a lower density converter. The output capacitor of the single stage circuit needs to hold the whole output voltage compared to the DD version in which all capacitors are rated for only a portion of the output voltage.

IX. CONCLUSION

This article is dedicated to the family of Double Dual (DD) converters. It initially explores the double dual boost converter and proposes a systematic procedure to obtain DD topologies from existing topologies. The article also presents other members of the family of DD converters, either derived from the basic second-order converter as well as the four-order converters and flying capacitor converters. Finally, we introduce a short survey of DD converters available in the literature and presented in an individual manner. In contrast to other reviews of DC-DC converters available in the literature, this is the first one dedicated to double dual topologies, which are emerging as a strong field in DC-DC converter research. Some of the presented topologies utilize the change of power flow along with the double dual connection.

Double dual converters show advantages such as a larger voltage gain in the case of a boost converter or a lower voltage gain in the case of a buck converter. Furthermore, most of them have a continuous (non-pulsating) voltage from the input to the output reference, resulting in a low common-mode voltage desirable in renewable energy applications.

A particular converter was obtained with the described procedure, and an experimental prototype was built. Finally, the results with one of the new topologies are presented to corroborate the principle of the described topological derivation.

REFERENCES

[1] R. W. Erickson and D. Maksimovic, *Fundamentals of Power Electronics*, 2nd ed. Boston, MA, USA: Kluwer, 2004.

[2] J. C. Rosas-Caro, J. M. Ramirez, F. Z. Peng, and A. Valderrabano, "A DC–DC multilevel boost converter," *IET Power Electron.*, vol. 3, no. 1, pp. 129–137, Jan. 2010.

[3] D. Bang Viet, Y. Lembeye, J. P. Ferrieux, J. Barbaroux, and Y. Avenas, "New high power–high ratio non isolated DC–DC boost converter for fuel cell applications," in *Proc. 37th IEEE Power Electron. Spec. Conf.*, Jun. 2006, pp. 1–7.

[4] C. Wang, "Investigation on interleaved boost converters and applications," Ph.D. dissertation, Virginia Polytech. Inst. State Univ., Blacksburg, VA, USA, Jul. 2009.

[5] S. Choi, V. G. Agelidis, J. Yang, D. Coutellier, and P. Marabeas, "Analysis, design and experimental results of a floating-output interleaved-input boost-derived DC–DC high-gain transformer-less converter," *IET Power Electron.*, vol. 4, no. 1, p. 168, 2011.

[6] R. Saadi, M. Bahri, M. Y. Ayad, M. Becherif, O. Kraa, and A. Aboubou, "Dual loop control of fuel cell source using non-isolated IBC-IDDB converter for hybrid vehicle applications," *Energy Proc.*, vol. 50, pp. 155–162, Jan. 2014.

[7] F. Forest, J.-J. Huselstein, T. Martire, D. Flumian, T. A. Meynard, Y. Abdelli, and A. M. Lienhardt, "A nonreversible 10-kW high step-up converter using a multicell boost topology," *IEEE Trans. Power Electron.*, vol. 33, no. 1, pp. 151–160, Jan. 2018.

[8] C. A. Villarreal-Hernandez, J. Loranca-Coutiño, J. C. Mayo-Maldonado, J. E. Valdez-Resendiz, P. M. García-Vite, A. Valderrabano-Gonzalez, and J. C. Rosas-Caro, "A double dual boost converter with switching ripple cancellation for PEMFC systems," *Electronics*, vol. 9, no. 10, p. 1592, Sep. 2020.

[9] M. Kabalo, D. Paire, B. Blunier, D. Bouquain, M. G. Simoes, and A. Miraoui, "Experimental validation of high-voltage-ratio low-input-current-ripple converters for hybrid fuel cell supercapacitor systems," *IEEE Trans. Veh. Technol.*, vol. 61, no. 8, pp. 3430–3440, Oct. 2012.

[10] F. S. Garcia, J. A. Pomilio, and G. Spiazzi, "Modeling and control design of the interleaved double dual boost converter," *IEEE Trans. Ind. Electron.*, vol. 60, no. 8, pp. 3283–3290, Aug. 2013.

[11] Y. Huangfu, S. Zhuo, F. Chen, S. Pang, D. Zhao, and F. Gao, "Robust voltage control of floating interleaved boost converter for fuel cell systems," *IEEE Trans. Ind. Appl.*, vol. 54, no. 1, pp. 665–674, Jan. 2018.

[12] S. Zhuo, A. Gaillard, L. Guo, L. Xu, D. Paire, and F. Gao, "Active disturbance rejection voltage control of a floating interleaved DC–DC boost converter with switch fault consideration," *IEEE Trans. Power Electron.*, vol. 34, no. 12, pp. 12396–12406, Dec. 2019.

[13] Q. Xu, W. Jiang, F. Blaabjerg, C. Zhang, X. Zhang, and T. Fernando, "Backstepping control for large signal stability of high boost ratio interleaved converter interfaced DC microgrids with constant power loads," *IEEE Trans. Power Electron.*, vol. 35, no. 5, pp. 5397–5407, May 2020.

[14] P. Lin, W. Jiang, J. Wang, D. Shi, C. Zhang, and P. Wang, "Toward large-signal stabilization of floating dual boost converter-powered DC microgrids feeding constant power loads," *IEEE J. Emerg. Sel. Topics Power Electron.*, vol. 9, no. 1, pp. 580–589, Feb. 2021.

[15] C. A. Villarreal-Hernandez, J. C. Mayo-Maldonado, G. Escobar, J. Loranca-Coutino, J. E. Valdez-Resendiz, and J. C. Rosas-Caro, "Discrete-time modeling and control of double dual boost converters with implicit current ripple cancellation over a wide operating range," *IEEE Trans. Ind. Electron.*, vol. 68, no. 7, pp. 5966–5977, Jul. 2021.

[16] C. A. Villarreal-Hernandez, O. F. Ruiz-Martinez, J. C. Mayo-Maldonado, G. Escobar, J. E. Valdez-Resendiz, and J. C. Rosas-Caro, "Minimum current ripple point tracking control for interleaved dual switched-inductor DC–DC converters," *IEEE Trans. Ind. Electron.*, vol. 68, no. 1, pp. 175–185, Jan. 2021.

[17] J. E. Valdez-Resendiz, J. C. Rosas-Caro, J. C. Mayo-Maldonado, and G. Calderon-Zavala, "Input-current/output-voltage ripple mitigation in the double dual boost converter," *Electr. Power Syst. Res.*, vol. 162, pp. 150–160, Sep. 2018.

[18] A. Rodríguez, A. Alejo-Reyes, E. Cuevas, H. R. Robles-Campos, and J. C. Rosas-Caro, "Numerical optimization of switching ripples in the double dual boost converter through the evolutionary algorithm L-SHADE," *Mathematics*, vol. 8, no. 11, p. 1911, Oct. 2020.

[19] S. Zhuo, A. Gaillard, Q. Li, R. Ma, D. Paire, and F. Gao, "Current ripple optimization of four-phase floating interleaved DC–DC boost converter under switch fault," *IEEE Trans. Ind. Appl.*, vol. 56, no. 4, pp. 4214–4224, Jul. 2020.

[20] J. C. Rosas-Caro, G. Escobar, P. R. Martinez-Rodriguez, S. Iturriaga-Medina, J. C. Mayo-Maldonado, and J. E. Valdez-Resendiz, "Differential and common-mode model-based controller for the double-dual buck transformerless inverter," *Int. J. Electr. Power Energy Syst.*, vol. 131, Oct. 2021, Art. no. 107065.

[21] [Online]. Available: https://2fca7bd6-9a97-4678-bc9f-28d3354f6ea2.filesusr.com/ugd/047f54_2048eb9bd5297ff942eea6c421b95698.pdf

[22] H. Moradisizkoohi, N. Elsayad, and O. A. Mohammed, "An integrated interleaved ultrahigh step-up DC–DC converter using dual cross-coupled inductors with built-in input current balancing for electric vehicles," *IEEE J. Emerg. Sel. Topics Power Electron.*, vol. 8, no. 1, pp. 644–657, Mar. 2020, doi: 10.1109/JESTPE.2019.2943301.

[23] N. T. Kalantari, S. G. Sani, and Y. Sarsabahi, "Implementation and design of an interleaved Cuk converter with selective input current ripple elimination capability," *Int. J. Circuit Theory Appl.*, vol. 49, no. 6, pp. 1743–1756, 2021.

[24] J. E. Valdez-Resendiz, V. M. Sanchez, J. C. Rosas-Caro, J. C. Mayo-Maldonado, J. M. Sierra, and R. Barbosa, "Continuous input-current buck-boost DC–DC converter for PEM fuel cell applications," *Int. J. Hydrogen Energy*, vol. 42, no. 51, pp. 30389–30399, Dec. 2017.

[25] M. Prudente, L. L. Pfitscher, G. Emmendoerfer, E. F. Romaneli, and R. Gules, "Voltage multiplier cells applied to non-isolated DC–DC converters," in *IEEE Trans. Power Electron.*, vol. 23, no. 2, pp. 871–887, Mar. 2008.

[26] M. Maalandish, S. H. Hosseini, S. Ghasemzadeh, E. Babaei, R. S. Alishah, and T. Jalilzadeh, "Six-phase interleaved boost DC/DC converter with high-voltage gain and reduced voltage stress," *IET Power Electron.*, vol. 10, no. 14, pp. 1904–1914, Nov. 2017.

[27] M. Maalandish, S. H. Hosseini, S. Ghasemzadeh, E. Babaei, and T. Jalilzadeh, "A novel multiphase high step-up DC/DC boost converter with lower losses on semiconductors," *IEEE J. Emerg. Sel. Topics Power Electron.*, vol. 7, no. 1, pp. 541–554, Mar. 2019.

[28] Y. Park, B. Jung, and S. Choi, "Nonisolated ZVZCS resonant PWM DC–DC converter for high step-up and high-power applications," in *IEEE Trans. Power Electron.*, vol. 27, no. 8, pp. 3568–3575, Aug. 2012.

[29] H. Jeong, M. Kwon, and S. Choi, "A high gain non-isolated soft-switching bidirectional DC–DC converter with PPS control," in *Proc. IEEE Energy Convers. Congr. Expo. (ECCE)*, Oct. 2017, pp. 1723–1727.

[30] M. F. Guepfrih, G. Waltrich, and T. B. Lazzarin, "High step-up DC–DC converter using built-in transformer voltage multiplier cell and dual boost concepts," *IEEE J. Emerg. Sel. Topics Power Electron.*, vol. 9, no. 6, pp. 6700–6712, Dec. 2021.

[31] W. Li, W. Li, Y. Deng, and X. He, "Single-stage single-phase high-step-up ZVT boost converter for fuel-cell microgrid system," *IEEE Trans. Power Electron.*, vol. 25, no. 12, pp. 3057–3065, Dec. 2010.

[32] Y. Deng, Q. Rong, W. Li, Y. Zhao, J. Shi, and X. He, "Single-switch high step-up converters with built-in transformer voltage multiplier cell," *IEEE Trans. Power Electron.*, vol. 27, no. 8, pp. 3557–3567, Aug. 2012.

[33] V. Cardoso, S. L. Brockveld Jr., T. B. Lazzarin, and G. Waltrich, "Double boost-flyback converter," *IET Power Electron.*, vol. 13, no. 6, pp. 1163–1171, 2020.

[34] Y. Tang, D. Fu, T. Wang, and Z. Xu, "Analysis of active-network converter with coupled inductors," *IEEE Trans. Power Electron.*, vol. 30, no. 9, pp. 4874–4882, Sep. 2015.

[35] L.-S. Yang, T.-J. Liang, and J.-F. Chen, "Transformerless DC–DC converters with high step-up voltage gain," *IEEE Trans. Ind. Electron.*, vol. 56, no. 8, pp. 3144–3152, Aug. 2009.

[36] D. Gao, Z. Jin, J. Liu, and M. Ouyang, "An interleaved step-up/step-down converter for fuel cell vehicle applications," *Int. J. Hydrogen Energy*, vol. 41, no. 47, pp. 22422–22432, Dec. 2016.

[37] K. J. Reddy and N. Sudhakar, "High voltage gain interleaved boost converter with neural network based MPPT controller for fuel cell based electric vehicle applications," *IEEE Access*, vol. 6, pp. 3899–3908, 2018.

[38] J. C. Rosas-Caro, G. Escobar, J. E. Valdez-Resendiz, J. C. Mayo-Maldonado, F. Beltran-Carbajal, and C. Del-Valle-Soto, "Analysis of the input current-ripple in the series-capacitor boost converter," *IEEE Trans. Ind. Electron.*, vol. 68, no. 10, pp. 10303–10308, Oct. 2021.

[39] M. G. Simões, C. L. Lute, A. N. Alsaleem, D. I. Brandao, and J. A. Pomilio, "Bidirectional floating interleaved buck-boost DC–DC converter applied to residential PV power systems," in *Proc. Clemson Univ. Power Syst. Conf. (PSC)*, Mar. 2015, pp. 1–8.

[40] M. Esteki, B. Poorali, E. Adib, and H. Farzanehfard, "Interleaved buck converter with continuous input current, extremely low output current ripple, low switching losses, and improved step-down conversion ratio," *IEEE Trans. Ind. Electron.*, vol. 62, no. 8, pp. 4769–4776, Aug. 2015.

[41] M. Esteki, B. Poorali, E. Adib, and H. Farzanehfard, "High step-down interleaved buck converter with low voltage stress," *IET Power Electronics.*, vol. 8, no. 12, pp. 2352–2360, 2015.

[42] P. C. Heris, Z. Saadatizadeh, and N. Rostami, "Transformerless quadratic-based high step-down DC–DC converter with wide duty cycle range," *IET Power Electron.*, vol. 12, no. 3, pp. 368–382, Mar. 2019.

[43] M. Esteki, N. Einabadi, E. Adib, and H. Farzanehfard, "A high step-down DC–DC converter with low switch voltage stress and extremely low output current ripple," in *Proc. 7th Power Electron. Drive Syst. Technol. Conf. (PEDSTC)*, Feb. 2016, pp. 134–139.

[44] Y. Huangfu, Y. Ma, H. Bai, L. Xu, A. Wang, and R. Ma, "A family of high gain fuel cell front-end converters with low input current ripple for PEMFC power conditioning systems," *Int. J. Hydrogen Energy*, vol. 46, no. 53, pp. 27156–27172, Aug. 2021.
[45] J. E. Valdez-Resendiz, J. C. Mayo-Maldonado, A. Alejo-Reyes, J. C. Rosas-Caro, and F. Beltran-Carbajal, "A family of double dual DC–DC converters," in *Proc. 11th Int. Conf. Power Electron., Mach. Drives (PEMD)*, 2022, pp. 107–113.
[46] M. Zhu and F. L. Luo, "Enhanced self-lift Cûk converter for negative-to-positive voltage conversion," *IEEE Trans. Power Electron.*, vol. 25, no. 9, pp. 2227–2233, Sep. 2010, doi: 10.1109/TPEL.2010.2047269.
[47] S. Chen, T. A. Lipo, and D. Fitzgerald, "Source of induction motor bearing currents caused by PWM inverters," *IEEE Trans. Energy Convers.*, vol. 11, no. 1, pp. 25–32, Mar. 1996.
[48] F. Wang, "Motor shaft voltages and bearing currents and their reduction in multilevel medium-voltage PWM voltage-source-inverter drive applications," *IEEE Trans. Ind. Appl.*, vol. 36, no. 5, pp. 1336–1341, Oct. 2000.
[49] S. Chen and T. A. Lipo, "Circulating type motor bearing current in inverter drives," *IEEE Ind. Appl. Mag.*, vol. 4, no. 1, pp. 32–38, Jan./Feb. 1998.
[50] M. H. Hedayati and V. John, "EMI and ground leakage current reduction in single-phase grid-connected power converter," in *IET Power Electron*, vol. 10, no. 8, pp. 938–944, Jul. 2017.
[51] G. E. Valderrama, G. V. Guzman, E. I. Pool-Mazun, P. R. Martinez-Rodriguez, M. J. Lopez-Sanchez, and J. M. S. Zuniga, "A single-phase asymmetrical T-type five-level transformerless PV inverter," *IEEE J. Emerg. Sel. Topics Power Electron.*, vol. 6, no. 1, pp. 140–150, Mar. 2018.
[52] *Automatic Disconnection Device Between a Generator and the Public Low-Voltage Grid, Paragraph 4.7.1. Photovoltaik*, Standard DIN VDE 0126-1-1, DKE Deutsche Kommission Elektrotechnik Elektronik Informationstechnik IM DIN UND VDE, Feb. 2006.

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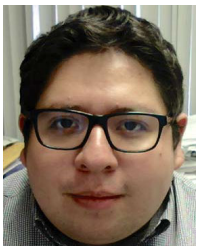

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