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RESEARCH ARTICLE

Ultra-Wide Band On-Chip Circulator With Sequentially Switched Delay Lines (SSDL)

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ABSTRACT The Sequentially-Switched Delay Lines (SSDL) consists of a set of RF switches and transmission lines of equal length which provides magnetless nonreciprocity with no theoretical bandwidth limit. SSDL circulator architectures are presented in this paper on a GaN MMIC. The SSDL circulators presented here demonstrate nonreciprocity from 10 MHz to 1.2 GHz with isolation between the transmitter and receiver which is greater than 20 dB for most of the measured frequency range. The insertion loss of the GaN MMIC SSDL circulator is reduced to below 3 dB from 10 MHz to 800 MHz, by using matching circuits at the gates of the switching transistors. The spurious-free operation of the SSDL circulator is also verified from 10 MHz to 1 GHz. It is also demonstrated that with passive bootstrapping, SSDL insertion loss is further reduced to about 2 dB and P1 dB performance can be significantly enhanced by an additional 10 dB. The time-modulation/switching strategy to achieve broadband magnetless nonreciprocity has the potential to be used in future STAR and full duplex communication systems.

INDEX TERMS Circulator, full duplex communication, GaN MMIC, magnetless, nonreciprocity, passive bootstrapping, STAR, time-modulation.

I. INTRODUCTION

As the boundaries of spectral efficiency for existing wireless systems continue to be pushed, full-duplex wireless networks have become the focus of many research groups in the academic and industrial sectors. Communication systems currently in use such as base stations and cellular phones function both as transmitters and receivers. Dual function is achieved through either time division duplex (TDD) or frequency division duplex (FDD); the transmitted and received signals are separated from each other either in different time slots or in different frequency channels. The fixed bandwidth allocation of FDD and the guard intervals which separate the uplink and downlink in TDD have a negative impact on a spectrum which is becoming more and more scarce [1], [2]. In-band full duplex [1] is the ability to transmit and receive simultaneously over the same frequency band, which has the prospect of doubling spectral efficiency. Circulators can achieve in-band full duplex and have traditionally exploited the properties of magnetic materials to create nonreciprocal signal flow [3]. However, their physical size is dependent upon the wavelength of operation, making them difficult to integrate with modern integrated circuits (ICs). As a potential alternative, the nonreciprocal transfer characteristics of transistors have been used to realize active circulators. These circulators offer small physical size and are more compatible with IC technology [4], [5], [6], but pay the price of limited power and noise performance.

Recently magnetless nonreciprocal approaches based on time-modulations have received much attention [7], [8], [9], [10], [11], [12], [13], [14], [15], [16], [17], [18], [19], [20], [21], [22], [23], [24], [25], [26], [27], [28], [29], [30], [31], [32], [33], [34], [35], [36], [37]. They are based on the fact that the space-time reversal symmetry in a non-magnetic device can be broken by adding a new dimension, i.e., time-varying property into the material system. Time modulations can be introduced through either parametric modulations or switching. Narrow band non-reciprocity in the VHF and wireless communication bands was demonstrated in [7], [8], and [9] through the use of parametrically coupled

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resonators in ring and wye configurations. Nonreciprocal behavior has also been realized through the commutation of MEMS resonators [10] with a total power consumption of approximately 38uW. Nonreciprocity over a broad RF bandwidth has been achieved on a printed circuit board as well as a monolithic microwave integrated circuit (MMIC) based on the Time-Varying Transmission Line (TVTL) concept [11], [12], [13], [14]. Switching based circulator was first demonstrated on a CMOS chip which utilizes a nonreciprocal phase shifter i.e. gyrator formed by a staggering commutating N-path filter [15]. The gyrator was later extended to a switched delay line configuration [16], [23] for its broadband performance. The gyrator was then further enhanced for high power handling and antenna balancing [17]. The ultra-wide band circulator operating from DC to RF based on Sequentially Switched Delay Line (SSDL) was first proposed and demonstrated with off-the-shelf components in [18] and [19]. Several variations and realizations of the similar concept on different technology platforms were reported in [20], [21], [22], [23], [24], [25], [26], [27], [28], [29], [30], [31], [32], [33], [34], [35], and [36]. In particular, [25], [26] presented a nonreciprocal network based on switched acoustic delay lines to create a significant delay time with compact physical size. This allows a reduction in the switching frequency which relaxes the performance requirement of the switch itself. Additionally, the magnetless nonreciprocity concept has seen a significant amount of application in bandpass filters [29], [30], [31], [32]. The key idea behind SSDL is a series of sequential switching actions that are added to the electrical signal path in a speed synchronous to that of the signal propagating on the path. If the signal has a defined rising and falling edge, the switches should be turned on right before the signal arrives and turned off right after the signal departs to avoid distorting the signal. For a continuous signal, it can first be separated in time by a SPDT switch into two alternating segments down to their own paths. The switching synchronization is then applied to both paths alternatively and the two segments of the signal are finally combined at the output to recover the original signal. As the switching actions are only synchronized with the wave propagation in one-direction in the fashion of true time delay, a frequency independent non-reciprocity can be achieved, assuming there is not frequency dispersion in the signal propagation path. The original SSDL circuit architecture presented in [18] and [19], as shown in Fig. 1 is composed of a set of five single-pole double-throw (SPDT) switches and six transmission lines of equal length. It is possible to simplify the structure in Fig. 1 by reducing the length of transmission lines T1, T2, R1, and R2 to zero, and then merging the TX and RX switches with the two SPDT switches (shown in the middle of Fig. 2 to form a double-pole, double-throw (DPDT) switch. The ANT port is left as the same SPDT switch.

This simplification to the original design in [18] and [19] results in a 2-line SSDL configuration shown in Fig. 2, which has been reported in [20], [21], [22], [23], [24], [25], [26], [27], and [28]. It allows the exact same nonreciprocal behavior with lower insertion loss as well as a smaller surface area for on-chip integration. This design can be extended further by replacing the SPDT switch at the ANT port with a DPDT switch as shown in Fig. 3, which forms a four-port circulator.

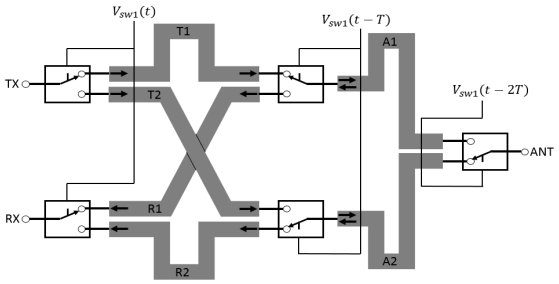

FIGURE 1. Original six-line architecture of the sequentially-switched delay line (SSDL) circulator.

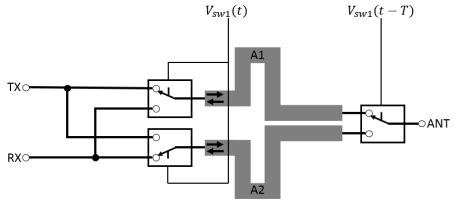

FIGURE 2. Simplified three-port, two-line architecture of the sequentially switched delay line (SSDL) circulator.

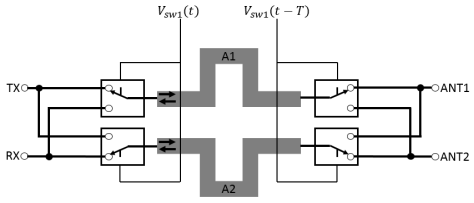

FIGURE 3. Simplified four-port, two-line architecture of the sequentially switched delay line (SSDL) circulator.

In this paper, we will present an on-chip realization of the SSDL circulator concept as illustrated in Fig. 3 on a GaN MMIC platform. Some preliminary experimental results over different generations of MMIC implementations have been briefly reported in [33], [34], [35], [36], and [37]. This paper will serve as a comprehensive summary of the latest results with the addition of design details on the MMIC implementation and theoretical discussions on the performance limit. In particular, this paper demonstrates that the insertion loss of MMIC SSDL circulators can be significantly improved (<3dB from DC to 900MHz) with the presence of impedance matching circuitry at the RF switch gates. It should also be noted, in comparison with other concurrent circulator designs based on switched delay lines, this work selects to over-multiplex the signal at a speed dictated by the Nyquist rate and the circulator can potentially operate free from switching noise if a low pass filter is applied to the output port. The rest of this paper is organized in the following manner: the general concept of SSDL is described

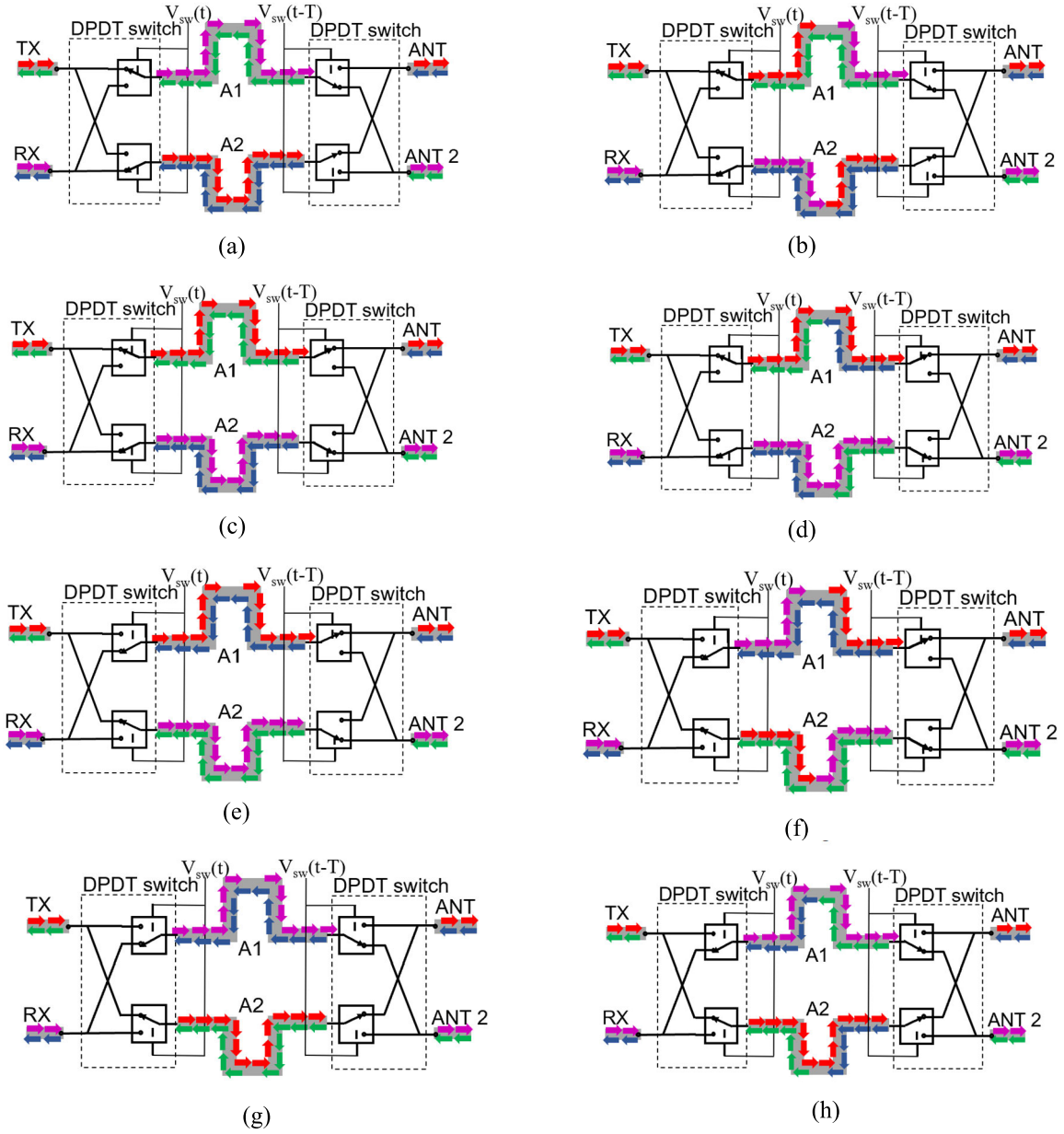

FIGURE 4. Positions of the switches along with the transmitted and received waveforms (a) at time 0+, (b) at time 0.5T, (c) at time T+, (d) at time 1.5T, (e) at time 2T+, (f) at time 2.5T, (g) at time 3T+, (h) at time 3.5T for a four-port device.

using a timing diagram analysis and theoretical representations of the signals that travel through the device. Following this are the design considerations for the SSDL circulator with experimental methods and results. Finally, the spectral performance of SSDL is verified and a short summary of the work is presented.

II. TIMING DIAGRAM ANALYSIS OF SSDL OPERATION

The dynamic process of wave propagation through a two-line SSDL circulator has been well explained in [20] and [24] and it is now illustrated with the assistance of a set of timing snapshots. The timing diagram in Fig. 4 illustrates the process of wave propagation at the four switching moments of each cycle. Note that the transmitted wave from TX to ANT, the transmitted wave from RX to ANT2, the received wave from ANT to RX and the received wave from ANT2 to TX are represented respectively by the colors red, magenta, blue and green. The TX, ANT, ANT 2 and RX ports are connected to the correct transmission line for a time of 2T. Each timing instance will be explained with respect to the switching action of the double-pole double-throw (DPDT) switch. Fig. 4(a) represents the locations of the transmitted and received waves at time 0+. The (+) sign indicates that the devices have just completed their switching action. The DPDT switches synced

to $V_{sw}(t)$ (left side of Fig. 4(a)) has just connected the TX and RX ports to transmission lines A1 and A2, respectively. The ANT and ANT2 port switches have been on for a time T+. This allows for the first set of received pulses (green signal in A1 and blue signal in A2) to begin populating both A1 and A2 simultaneously with the tail end of the set of transmitted pulses (the magenta signal in A1 and red signal in A2), which arrive at their respective ANT2 and ANT ports. The transmitted and received waves that occupy A1 and A2 at the same time do not interfere with each other because they travel toward different directions. By the time of t = 0.5T in Fig. 4(b), it can be seen how the magenta signal going from RX to ANT2 is being unloaded off the A1 to ANT while also being loaded onto A2 from RX and the red signal going from TX to ANT is being unloaded off the A2 to ANT while also being loaded onto A1 from TX. The green and blue receive signals still traverse their respective A1 and A2 line from ANT2 and ANT, unchanged since the time t = 0+. Progressing in time to Fig. 4(c), it is a time snapshot at T+. In this case, the $V_{sw}(t)$ synced DPDT switches stays in its same position while the ANT and ANT2 side DPDT switches synced to $V_{sw}(t-T)$ change their connections. Here, the next set of transmitted pulses (the red signal in A1 and magenta signal in A2) can be seen fully along A1 and A2 which will be sent out through the ANT and ANT2 side DPDT switches. It is important to note that right before the ANT and ANT2 ports switches flipped, the tail end of the first set received pulses (green signal in A1 and blue signal in A2) were captured at the ANT port. By the time of t = 1.5T in Fig 4(d), it can now be seen that the green received signal originally from ANT2 is being unloaded off of A1 as the blue receive originally from ANT is being loaded off while the blue received signal originally from ANT is being unloaded off of A2 as the green received signal originally from ANT2 is being loaded off As time moves forward to Fig. 4(e), the switch positions are now seen at time 2T+. The left side DPDT switches have flipped orientation again after being in its previous state for a time 2T. Now, the TX and RX ports are respectively connected to transmission lines A2 and A1. The first set of received pulses (green signal in A1 and blue signal in A2) now completed its journey. Also, the second set of transmitted pulses (the magenta signal in A1 and red signal in A2) just begins to traverse again. As time advances further, the positions of the transmitted and received waves in the circulator are seen at time 3T+ in Fig. 4(g). Here, the ANT and ANT2 port side DPDT switches switch transmission line connections again after being in its previous state for a time of 2T. Here, the second transmitted pulses (the red signal in A1 and magenta signal in A2) now fully occupy their respective transmission lines in the towards ANT and ANT2 ports directions while the second set of received pulses (blue signal in A1 and green signal in A2) fully occupy their respective transmission lines in the towards RX and TX ports directions. By the time of t = 3.5T Fig. 4(h) it can now be seen that the green received signal originally from ANT2 is being unloaded off of A2 as the blue receive originally from ANT is being loaded off while the blue received signal originally from ANT is being unloaded off of A1 as the green received signal originally from ANT2 is being loaded off. As time progresses further, the switches and positions of the signal pulses match those of Fig. 4(a) again.

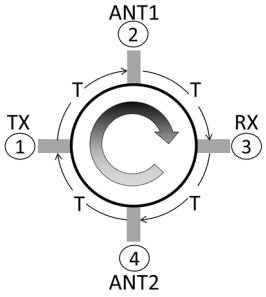

FIGURE 5. Circulator symbol illustrating clockwise signal propagating in a 4-port SSDL circulator.

To summarize, the SSDL Circulator operates by separating transmitted and received signals in time and recombining them at their respective ports connecting to the transmitter (TX), the receiver (RX) and the antenna (ANT) as the original signal. A signal appearing at any of these ports is split into pulses which have a time duration of 2T. These pulses are multiplexed through the circulator and mathematically their voltages are multiplied by the normalized switch control voltage at each switch junction. Carrying out the derivations for the two-line four-port circulator shown in Fig. 3 leads to the following voltage transfer relationships among the different ports:

$$ANT1^{-}(t) = TX^{+}(t-T) \tag{1}$$
$$RX^{-}(t) = ANT1^{+}(t-T) \tag{2}$$
$$ANT2^{-}(t) = RX^{+}(t-T) \tag{3}$$
$$TX^{-}(t) = ANT2^{+}(t-T) \tag{4}$$

The above results show that the time delay from port to port is identical. The overall switching diagrams in Fig. 4(a-h) correspond with this process. Therefore, signals enter the circulator and travel through the circulator in a clockwise fashion, as shown by the symbol illustrated in Fig. 5, with a time delay which corresponds to the delay of a single transmission line.

One can thus write the 4-port scattering parameter of an ideal SSDL circulator as follows,

$$[S] = \begin{bmatrix} 0 & 0 & 0 & e^{-jT} \\ e^{-jT} & 0 & 0 & 0 \\ 0 & e^{-jT} & 0 & 0 \\ 0 & 0 & e^{-jT} & 0 \end{bmatrix} \tag{5}$$

Note that terminating port 4 with an open circuit load yields the following relations,

$$\begin{cases} V_1^{-} = e^{-jT} V_4^{+} \\ V_4^{-} = e^{-jT} V_3^{+} \\ V_4^{-} = V_4^{+} \end{cases} \tag{6}$$

This results,

$$V_1^- = e^{-j2T} V_3^+ \tag{7}$$

The 4-port scattering parameters now reduces to one for 3-port, i.e.,

$$[S] = \begin{bmatrix} 0 & 0 & e^{-j2T} \\ e^{-jT} & 0 & 0 \\ 0 & e^{-jT} & 0 \end{bmatrix} \tag{8}$$

In practice, one can simply terminate port 4 with a matched load for full-duplex 3-port operation that requires separation of the transmitting and receiving paths.

III. SSDL CIRCUIT DESIGN

The SSDL circulator designs presented in this paper are carried out on the 0.2um GaN HEMT process from Northrop Grumman Aerospace Systems (NGAS). They are based on switching frequencies of 1.25GHz and 2.5GHz. The time delay match between the signal propagation and switch timing is what allows for the theoretically infinite bandwidth operation of the SSDL circulator. For this condition to be satisfied, each transmission line must have a delay time equivalent to T, which is an electrical length of 90 degrees at the switching frequency. Using the LineCalc program in Agilent ADS, the required straight-line microstrip lengths for switching frequencies of 1.25GHz and 2.5GHz are 23.8mm and 11.9mm, respectively. For a compact on-chip implementation, one must meander the microstrip lines to reduce the overall chip dimensions.

An RF switch is characterized by its on-resistance and off-capacitance which set the time constant of the switch itself. Since the SSDL circulator is designed to switch at high frequencies, the time constant must be low to avoid significant losses during circulator operation. Fig. 6(a) and (b) shows the schematics of two topologies used to construct the RF single-pole double-throw (SPDT) switch. In the first topology shown in Fig. 6(a), the switch is symmetrical about the RFOUT port, with each throw arm consisting of two series transistors and one shunt transistor. The series transistor devices have seven gate fingers with a total periphery of 805um. The shunt transistor device has 3 gate fingers with a total periphery of 120um. The control signals are such that $\overline{V_{sw}(t)}$ is the differential signal of $V_{sw}(t)$, which respectively control the connection of RF2 and RF1 with RFOUT. Two of these SPDT RF switches are combined in parallel with each other to form a double-pole double-throw (DPDT) RF switch. This configuration has the following features. The first is that the shunt device grounds any leakage current through the RF path when it is in the OFF state. The second is the protection against a short circuit condition for the RF signal when the opposing path is in the OFF state.

Without the additional series transistor device at the terminal of each throw arm, the SPDT switch would have the shunt device as its first element observed when looking from the output of the switch arm. If this was the case, the combination forming the DPDT switch would present a short circuit to ground for the RF signal in the parallel path. The advantage of this topology is the high isolation of the switch brought forth by the series and shunt combination, but this is at the price of complexity and higher insertion loss as the signal power through the drains and sources may leak to the gate control paths through multiple gate connections.

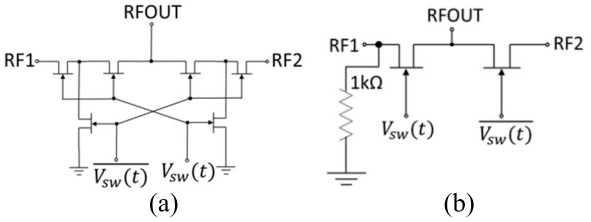

FIGURE 6. RF SPDT switch used in the two-line SSDL Circulator (a) topology one with a series-shunt-series configuration (b) topology two with a single series configuration.

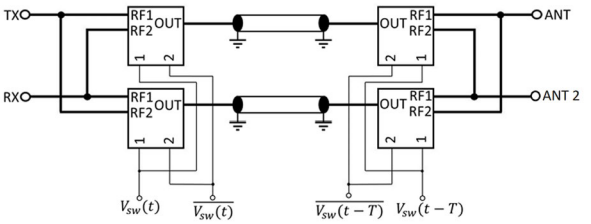

FIGURE 7. General block diagram of the four-port, two-line SSDL circulator.

In an effort to reduce the complexity of the switch design, the second SPDT switch topology was shown in Fig. 6(b), The simplified switch design accomplishes the same goals as the switch shown in Fig. 6(a) with only one series transistor in each throw arm, which reduces the total on-resistance and thus the insertion loss of the switch. Each series transistor has seven gate fingers with a total periphery of 805um. Again, two of the SPDT switches of Fig. 6(b) are placed in parallel to form the DPDT switch for use in the SSDL circulator. Fig. 7 shows the schematic of the full two-line SSDL circulator. Each rectangle represents a SPDT switch displayed in Fig. 6(a) or (b), with two connected in parallel to form the DPDT switch for the TX and RX ports (left side of Fig. 7) and the ANT port (right side of Fig. 7). To produce the eight total switching signals shown in Fig. 7 (two of $V_{sw}(t)$, $\overline{V_{sw}(t)}$, $V_{sw}(t-T)$ and $\overline{V_{sw}(t-T)}$ each), 90 and 180 degree couplers are used as shown in Fig. 9. The port shown at the bottom right of Fig. 10 is terminated into a matched load so that a three-port SSDL circulator is formed. When two of the SPDT switches of Fig. 6(b) are connected in parallel as shown in Fig. 10, notice that the 1kohm resistor provides a reference path to ground for both the RF1 and RF2 ports of the upper and lower SPDT switches, respectively.

The impedance seen looking into the switch gate must also be considered in the design of the SSDL circulator. In order to improve the performance of the circulator, an L-section matching circuit consisting of two inductors is used to trans-

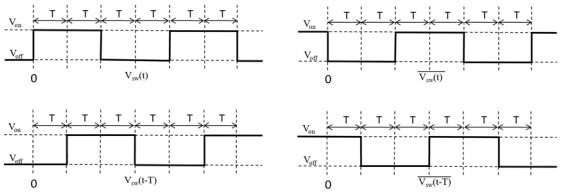

FIGURE 8. Voltage control sequences for the sequentially switched delay line circulator concept.

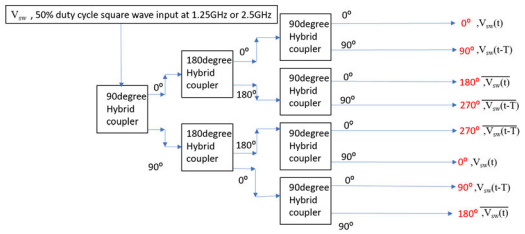

FIGURE 9. Building a switching control network from couplers for the sequentially switched delay line circulator.

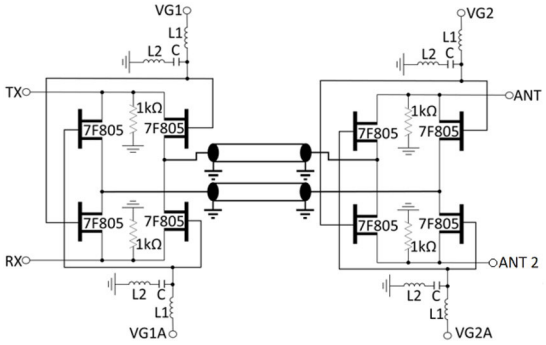

FIGURE 10. Circuit schematic overview of the four-port, two-line SSDL circulator with gate matching designed to switch at 1.25GHz.

form the capacitive switch gate into a 50ohm impedance. The "7F805" label associated with each transistor device means that each has 7 fingers with a total periphery of 805um. L1 has a value of 13.4nH at 1.25GHz and L2 has a value of 11.1nH at 1.25GHz. There is a DC voltage that is applied to the switch gates so that the switching signal properly turns each switch path on and off. The capacitor in series with the shunt inductance keeps the DC gate bias from being pulled directly to ground, which has a value of 27pF. Fig. 12 shows one such design switching at 1.25GHz with the single series transistor topology.

IV. INSERTION LOSS PERFORMANCE ANALYSIS

Comparing to RF circulators made of magnetic materials, the insertion loss of current non-magnetic circulators is generally higher. Therefore, it is important to understand the theoretical limit of SSDL circulator insertion loss for a given technology. The analysis carried out here is assuming no leakage of the signal to the control path and the insertion loss is only contributed by the on-resistance and the off-capacitance of

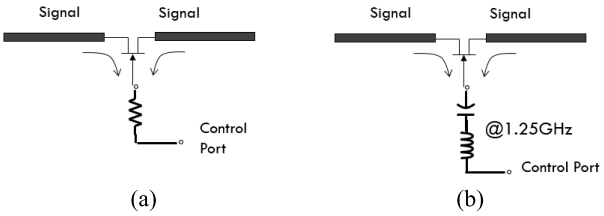

FIGURE 11. Circuit schematic showing low frequency and high frequency equivalent of bootstrapping.

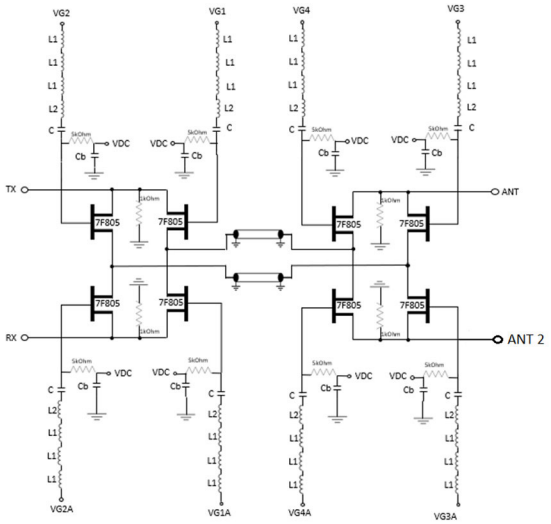

FIGURE 12. Circuit schematic overview of the four-port, two-line SSDL circulator with passive bootstrapping designed to switch at 1.25GHz.

the switch. The transistor that is used to construct a switch has a technology dependent figure of merit defined as,

$$f_{FOM} = \frac{1}{2\pi R_{on} C_{off}} \tag{9}$$

where Ron is the on-resistance and the off-capacitance Coff of the transistor and the input power into the SSDL circulator can be written as,

$$P_{input} = \frac{1}{2} I^2 Z_0 \tag{10}$$

where I is the current flowing on the transmission line and Z0 is the characteristic impedance of the transmission line. For the single series switch topology shown in Fig. 6(b), every time when the switch is turned on from off, the energy stored in the off-capacitance of the transistor is lost. During one switching cycle of 4T, the transitions from off to on states in each DPDT switch happens once for all four transistors, which leads the capacitive power loss given by

$$P^C_{loss} = \frac{1}{2} f_s C_{off} V^2 \cdot 4 = \frac{1}{2} I^2 \cdot 4 f_s C_{off} Z_0^2 \tag{11}$$

where fs is the switching frequency and the Ohmic loss at the switch is yielded as,

$$P^R_{loss} = \frac{1}{2} I^2 R_{on} \tag{12}$$

as the wave encounters the on-resistance of one transistor at any given time. The power lost in each DPDT switch is thus given by summing the capacitive power loss in (11) with the Ohmic power loss in (12), yielding

$$P_{loss} = \frac{1}{2} I^2 \left(4 f_s C_{off} Z_0^2 + R_{on}\right) \tag{13}$$

The fractional power loss is then derived as:

$$\frac{P_{loss}}{P_{input}} = 4 f_s C_{off} Z_0 + \frac{R_{on}}{Z_0} \tag{14}$$

It is noted that the two loss terms in (14) have a fixed product, therefore the minimum insertion loss is achieved when these two terms are equal to each other (15).

$$\frac{R_{on}}{Z_0} = 4 f_s C_{off} Z_0 \tag{15}$$

With some basic algebra dividing both sides by Z0 (16).

$$\frac{R_{on}}{Z_0^2} = 4 f_s C_{off} \tag{16}$$

Then multiplying both sides Ron, it can be found that:

$$\left(\frac{R_{on}}{Z_0}\right)^2 = 4 f_s C_{off} R_{on} = \frac{2 f_s}{\pi f_{FOM}} \tag{17}$$

Therefore, the optimum condition for switch design is to choose the periphery of the transistor to make

$$R_{on} = Z_0 \sqrt{\frac{2 f_s}{\pi f_{FOM}}} \tag{18}$$

With this optimum matching condition and taking account of the fact two DPDT switches are needed in the SSDL, the fundamental limit of SSDL circulator insertion loss is defined as:

$$IL = 1 - 2\frac{P_{loss}}{P_{input}} = 1 - 4\frac{R_{on}}{Z_0} = 1 - 4\sqrt{\frac{2 f_s}{\pi f_{FOM}}} \tag{19}$$

For example, in the current NGAS 0.2um GaN MMIC process, a typical transistor has an on-resistance of 4 Ohm-mm and an off-capacitance of 0.31pF/mm, which gives a switch figure of merit of 128GHz. At the switching frequency of 1.25GHz and a 50Ohm reference impedance system, the optimum on-resistance of the switch should be,

$$R_{on} = Z_0 \sqrt{\frac{2 f_s}{\pi f_{FOM}}} = 4\Omega \cdot mm \tag{20}$$

Under this optimum match, the insertion loss given by (19) is 1.65dB. This loss is in addition to the loss of the meandered microstrip line which is approximately 0.3 to 0.5dB. It is also evident from (20) that the insertion loss can be further reduced when technology with a higher switch figure of merit is used. However, in practice, as it will be shown in the next sections, the leakage of the RF signal to the gate control path may be the primary reason that prevents the theoretical limit shown in (19) from being reached.

It should be noted that the quoted 0.2um GaN process has Ron of 1.8Ohm-mm and Coff of 0.378pF/mm according to the foundry provided PDK, which corresponds to a figure of merit of 234GHz. However, in our own device characterization, it was found the capacitance of the GaN transistor, particularly Cgs and Cgd, are significantly (2.5 times) higher than the PDK model values, possibly because the PDK model was derived under a high drain biasing voltage condition, and aiming mainly for power amplifier applications. The revised transistor model of 128GHz figure of merit also provided much better agreement in ADS simulations with measured results.

V. BOOTSTRAP CIRCUIT

One problem transistor switches may experience in high speed switching applications are the self turning-on effects. This occurs when the gate voltage is set to pinch off yet the RF voltage swing across the drain and source during the turning-off states reach to a threshold so that the V_{gs} or V_{gd} may become greater than the pinch-off voltage. The self turning-on effects limit the power handling of switches to a level much lower than what the break down voltage of or the maximum power dissipation the device allows.

Bootstrapping is a technique used frequently to increase the P1dB in RF switches. By adding a high-value resistor at the gate, the resistance and the drain/source-to-gate capacitance forms a network with long response time which ensures that the gate voltage follows that of the drain and source for RF and avoids unwanted turning ON and OFF scenarios. This traditional architecture utilizing the gate resistor is shown above in Fig. 11 (a). However, the conventional architecture works only for when the switching rate is much lower than the RF frequency. It does not work for SSDL as the required switching rate is faster than the signal frequency. If a resistor was placed in series with the switch transistor, the time constant created by the large resistance and series device capacitance would severely degrade the performance by attenuating the control signal input. A high-Q series LC resonator, resonating at the switching frequency, is thus used instead for bootstrapping in the SSDL circulator. The impedance response versus frequency for a series LC resonator creates a low impedance at resonance, and a high impedance out of band. This means that the switching signal can be passed to the gate, yet the RF signal will see a high impedance looking into the gate and continue across the drain-source as intended. A schematic of the SSDL with passive bootstrapping is presented below in Fig. 15, which shows a cascade of four inductors with one capacitor to realize the needed Q for the LC tank, where L1 has a value of 11nH at 1.25GHz and L2 has a value of 10nH at 1.25GHz. C is 235fF. It will be shown in the later sections the proposed bandpass bootstrap circuit improves both the insertion loss and power handling of the SSDL circulator significantly.

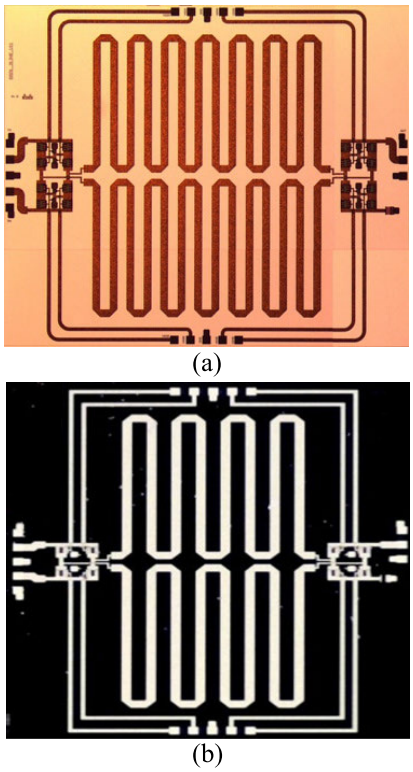

FIGURE 13. SSDL MMIC circulator switching at 1.25GHz with (a) switch topology one in Fig.7 and (b) switch topology two in Fig.7. No gate matching for either case.

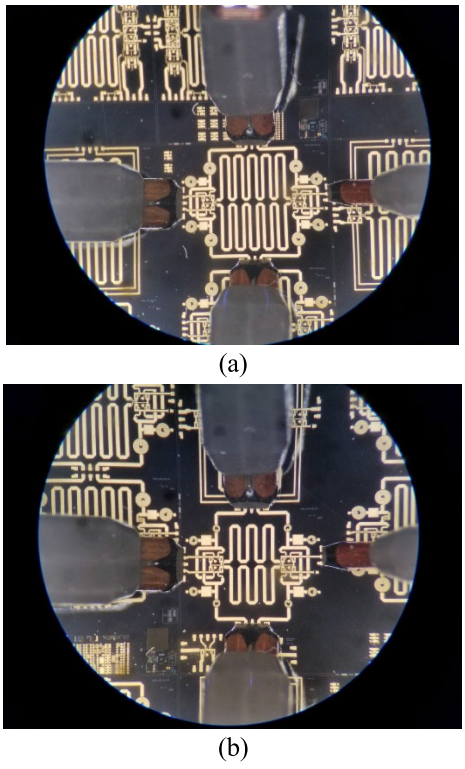

FIGURE 14. Pictures of SSDL MMIC circulator (a) switching at 1.25GHz (b) switching at 2.5GHz, both with switch topology two and gate matching.

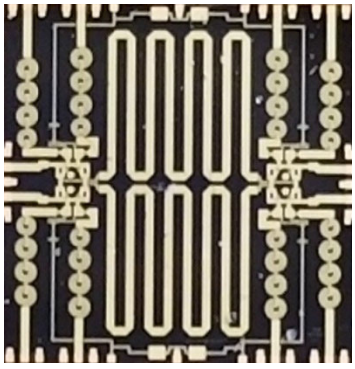

FIGURE 15. Pictures of SSDL MMIC circulator switching at 1.25GHz with passive bootstrapping.

VI. EXPERIMENTAL METHODS

To understand the different design trade-offs as they relate to the SSDL circulator performance, a total of five MMIC prototypes of the two-line three-port SSDL circulator are designed and fabricated using Northrop Grumman's 0.2um GaN HEMT process. The first two designs are based on the same switching frequency of 1.25GHz but with different switch topologies as shown in Fig. 10 and different delay line lengths. Both designs are with gates of transistors unmatched and connected to a 70 Ohm transmission line. The third and the fourth designs are for different switching frequencies of 1.25GHz and 2.5GHz and the gates of all transistors are matched with a L-section circuit as illustrated in Fig. 12. The fifth design is a passive bootstrap with a switching frequency of 1.25GHz

The pictures of all of the MMIC chips are shown in Fig. 13-15. They have probing pads which are either ground (represented by G) or signal (represented by S) ports. The transmitter (TX) and receiver (RX) ports are at the left edge of the chip and are connected to a double-pole double-throw (DPDT) RF switch through a G-S-G-S-G probe pad. The antenna (ANT) port is located at the right side of the chip and is connected to a DPDT RF switch through a G-S-G probe pad. These probes are manufactured by Cascade Microtech through which RF signals are applied from a network analyzer. The second switch pole at the right side of the chip is connected to ground through a 50ohm resistor. In theory, the ANT port is connected to a single-pole double-throw (SPDT) RF switch. In this design, a DPDT RF switch at the ANT port identical to the TX/RX side is used and the other switch pole is terminated in a 50 Ohm matched load for simplicity. The two DPDT switches are connected by two meandered microstrip lines which have a 50 Ohm line width of 90um.

In Fig. 13 (a), the chip has a dimension of 5.1mm by 4.3mm. The electrical length of each delay line was originally designed to be 90 degrees at 1.25GHz to match the condition specified by the switching actions. Since the DPDT switches contribute additional passive delay, the delay lines were shortened to 90 degrees at 1.44GHz to resynchronize the switching action with the propagation delay. The adjustment was made

based on the simulation with a preliminary transistor model. The second chip shown in Fig. 13 (b) has a dimension of 4.2mm by 4.9mm. Each delay line has an electrical length of 90 degrees at 2GHz to account for the increased delay by the transistor capacitance. The adjustment was greater based on a refined capacitance model of the transistor. The top and bottom of these two chips have S-S-G-S-S RF pads from left to right through which the switching signals are applied to the device gates. The microstrip lines associated with each transistor gate have an impedance of 70 ohms, which corresponds to a process line width of 41um.

The third chip shown in Fig. 14 (a) has a dimension of 5mm by 4mm. It is designed to switch at 1.25GHz and includes gate matching. Each delay line is further shortened from that in the second chip to an electrical length of 90 degrees at 2.12GHz. In an effort to reduce the complexity associated with driving the switch gates, 4 identical L-section matching circuits are used to split the switching signals and route them to the appropriate transistor. The impedance of the gate lines is 50 ohms. The fourth chip shown in Fig. 14 (b) is designed for switching at 2.5GHz which uses the same switch topology as the third chip. It also contains a similar L-section gate matching circuit. The chip has a dimension of 4.4mm by 3.7mm due to its higher switching frequency, thus shorter delay. Each delay line has an electrical length of 90 degrees at 4.28GHz.

The fifth/last chip shown in Fig. 15, has a dimension of 4.9mm by 5.1mm. After being optimized for best insertion loss, each delay line has an electrical length of 90 degrees at 2GHz.

To test the SSDL MMICs, an external drive network consisting of a power amplifier driving the switches, hybrid couplers, and bias tees is used. Depending upon the version being tested, a 2.5GHz or 1.25GHz CW signal is input to the power amplifier from a signal generator. The single output from the power amplifier is split into four or eight individual drive signals through a hybrid coupler network. The GaN devices are typically in the ON state when a potential of 0V is applied to the gate and are OFF with a minimum potential of -3V. The proper DC offset is applied to each individual drive signal through a bias tee so that the full voltage swing of the gate control signal is presented to the gate of each switch.

VII. EXPERIMENTAL RESULTS

S-parameters of the SSDL circulator are measured with a network analyzer while the aforementioned external drive network is used to dynamically drive the SSDL circulators. The transmitted insertion loss (S_{21}) is measured from the TX to the ANT port, and the received insertion loss (S_{32}) is measured from the ANT port to the RX port. The isolation between the TX and RX ports is crucial for the successful operation of a circulator. The TX/RX isolation (S_{31}) is measured as the amount of RF signal loss observed at the RX port when the TX port is active. For four port circulator measurements, done for the fifth chip, RX to ANT2 (S_{43}), ANT2 to TX(S_{14}) and ANT1/ANT2 insolation(S_{42}) was also

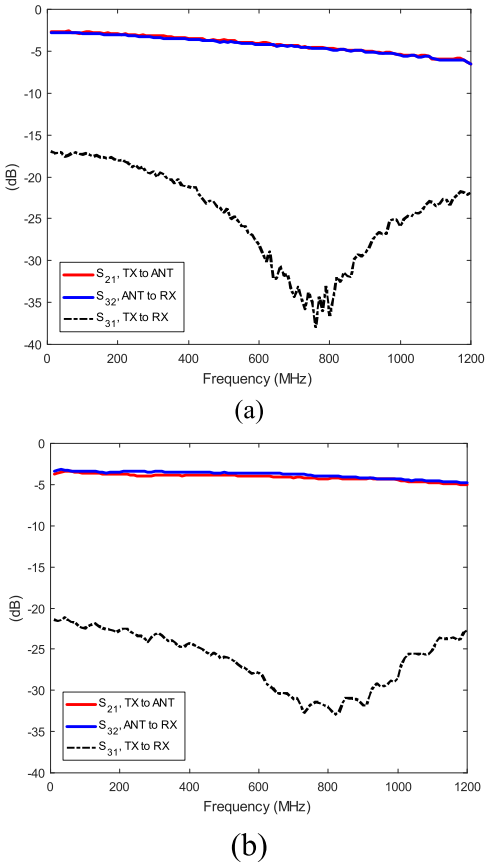

FIGURE 16. Fig.9 **Insertion loss (S21 and S32) and isolation (S31) of the MMIC circulator switching at 1.25GHz (a) with switch topology one (b) with switch topology two, both without gate matching.**

plotted. The 3-port SSDL can be considered as a special case of the 4-port SSDL when the ANT2 port is terminated, e.g., the DPDT is reduced to a SPDT switch. As the 4-port SSDL is more general and symmetrical in its structure, most of the experimental works in the paper were conducted based on the 4-port architecture. This 4-port behavior is simplified to 3 port-like plots where data going from and leaving ANT2 port are omitted for the first four SSDL designs for the sake of simplicity in analyzing insertion loss and isolation.

The experimental results for the insertion loss and isolation of the two gate unmatched chips are plotted in Fig.16 (a) and (b). The first chip has a measured insertion loss from 2.7dB to 5dB from 10MHz to 1GHz, respectively. The isolation ranges from 18dB to 35dB over the measured frequency range, indicating good isolation between the TX and RX ports. The second chip has a measured insertion loss from 3.7dB to 4.3dB from 10MHz to 1GHz, respectively. The isolation between TX and RX is greater than 20dB over the entire measured frequency range. The reduction of the delay line length in the second chip in combination with the use of switch topology two helps to reduce the insertion loss at 1GHz by 0.7dB when compared to the first design with switch topology one. However, the insertion loss at lower end of the frequency degraded by about 1dB, likely due to

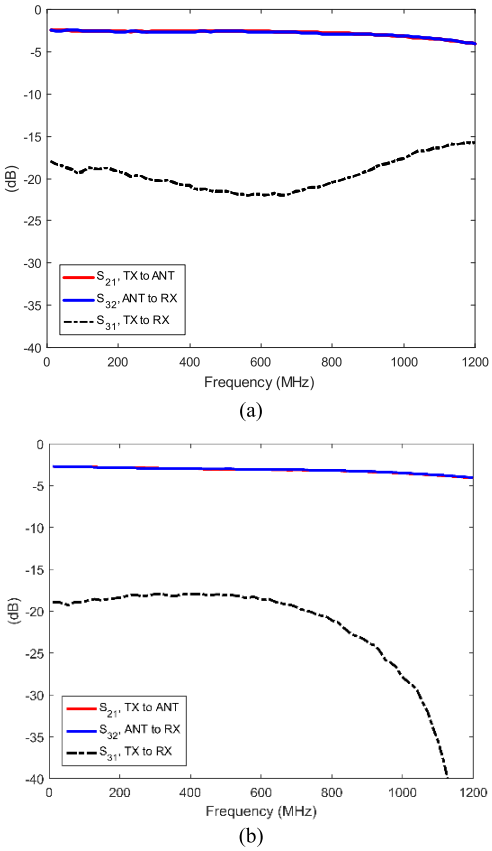

FIGURE 17. Insertion loss (S21 and S32) and isolation (S31) for the third and fourth circulator design switching (a) at 1.25GHz (b) at 2.5GHz with switch topology two and gate matching.

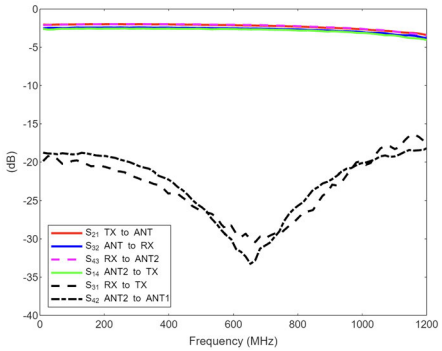

FIGURE 18. Insertion loss (S21, S32, S43 and S14) and isolation (S31 and S42) for the fifth circulator design switching at 1.25GHz with passive bootstrapping.

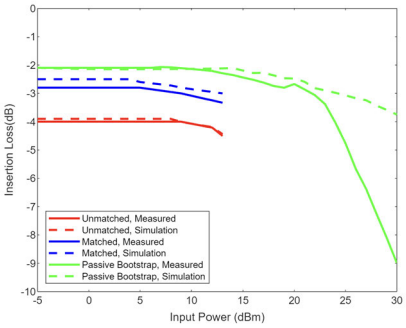

FIGURE 19. Measured P1dB results for the unmatched SSDL (blue trace) with a total power consumption of 320mW, the matched SSDL (red trace) with a total power consumption of 50mW and the passive bootstrap SSDL (green trace) with a total power consumption of 141 mW.

the dispersion of the transmission line loaded with transistor capacitance which is shorter for lower signal frequency and thus misaligned in delay with the switching signal.

The experimental results for the insertion loss and isolation are plotted in Fig. 17 (a) and (b) for the third and the fourth design switching at 1.25GHz and 2.5GHz respectively. Both designs are with switch topology two and L-section gate matching. The insertion loss measures 2.5dB to 3.1 dB from 10MHz to 1GHz for the chip with 1.25GHz switching frequency. The matching circuit placed at the switch gates helps to improve the measured loss to a sub-3dB curve over the entire noise-free operating range from 10MHz to 625MHz as dictated by the Nyquist rate. The isolation is greater than 15dB over the measured frequency range between the TX and RX ports. In the chip switching at 2.5GHz, the Nyquist rate determines the noise-free operating range from DC to 1.25GHz. The insertion loss measures 2.7dB to 3.5dB from 10MHz to 1GHz, respectively. The isolation is again greater than 15dB over the measured frequency range between the TX and RX ports. It is noted that the overall insertion loss has been greatly improved from the gate unmatched cases. This is because the addition of the matching circuit at the gate prevents the leakage of the RF signal through the control path.

The experimental results for the insertion loss and isolation are plotted in Fig. 18 for the fifth design switching at 1.25GHz with passive bootstrapping. The insertion loss measures 2.1dB to 3.0 dB from 10MHz to 1GHz. The isolation is again greater than 20dB over the measured frequency range between the TX and RX ports and between the ANT1 and ANT2 ports. It is noted that the overall insertion loss has been further improved especially below 600 MHz thanks to the high-Q series LC resonator, resonating at 1.25 GHz, further reducing the leakage of the RF signal through the control path.

Power compression is also an important metric for circulator operation. P1dB testing is performed at 500MHz for three cases: first is the second design, i.e., unmatched SSDL circulator switching at 1.25GHz with switch topology two. The P1dB referenced to the output is approximately 10dBm with a total power consumption of 25dBm (320mW) counting the input to all the gates of the transistors, as shown by the blue trace in Fig. 19. The second test case is the third design, i.e. matched SSDL circulator switching at 1.25GHz with switch topology two. The P1dB referenced to the output is approximately 11dBm with a total switch power consumption of 17dBm (50mW) as shown by the red trace in Fig. 19. As expected, the power consumption at the gates are greatly

reduced due to the matching circuit. But it is evident from Fig.18 that the slight increase of P1dB output with the gate matching circuit is due to the reduced insertion loss observed in the SSDL circulator. The third test case is the fifth design, i.e., SSDL circulator switching at 1.25 GHz with passive bootstrapping. The P1dB referenced to the output is approximately 21dBm with a total power consumption of 21.5dBm (141mW) counting the input to all the gates of the transistors, as shown by the green trace in Fig. 19. The IP3 measured in this case is 27dBm. While the power consumption is greater in order to drive the high Q, LC resonator equipped switches, the passive bootstrap SSDL has by far both the best insertion loss and P1dB.

The low power compression in the first four SSDL designs tested is believed to be the result of a lack of high impedance isolation between the gate drive signal and the RF path. As the switching frequency is often much higher than the signal frequency for SSDL circulator, the conventional high resistance gate protection cannot be applied. The improvement in power compression of the passive bootstrap design verifies these assumptions by providing a high impedance gate protection at high frequencies. Future work will be the development of harmonic matching circuits that will simultaneously provide two things: a high impedance looking into the gate from the RF path and a square wave appearing at the switch gate to make the switching more power efficient and avoid duty cycle reduction in a sinusoid driving case.

VIII. SPECTRAL PERFORMANCE

The SSDL circulator works by multiplexing the transmitted and received RF signals to their respective ports. These time-switching operations introduce spurious products which appear at the ports of the circulator. A simplified analysis of the spurious emission from the switching actions was given in [18]. Experimental results are displayed in this section for the fourth SSDL circulator design, switching at 2.5GHz with switch topology two and gate matching in Fig. 20. The SSDL circulator operates in two modes known as over-multiplexing and under-multiplexing. The boundary between the two multiplexing modes is set by the Nyquist rate, which is half of the switching frequency of 2.5GHz. This means that the over-multiplexing operation corresponds to the frequency range of DC – 1.25GHz. At these frequencies, the switching noise appears at frequencies higher than 1.25GHz, so that a lowpass filter can be used to suppress the switching noise. The under-multiplexing mode kicks in when the signal frequency is higher than 1.25GHz. Note that the prior S-parameters testing used RF signals sweeping from 10MHz to 1.2GHz, below the under-multiplexing mode point. In this spectrum testing case, a strictly 1GHz CW tone is applied. This desired signal may appear within the vicinity of the switching noise products as it is close to what the Nyquist rate allows. A bandpass filter may be needed to eliminate this switching noise to protect the front-end. The spectrum observed at the ANT port when a 1GHz CW signal is applied to the TX port is plotted in Fig. 20. The power level

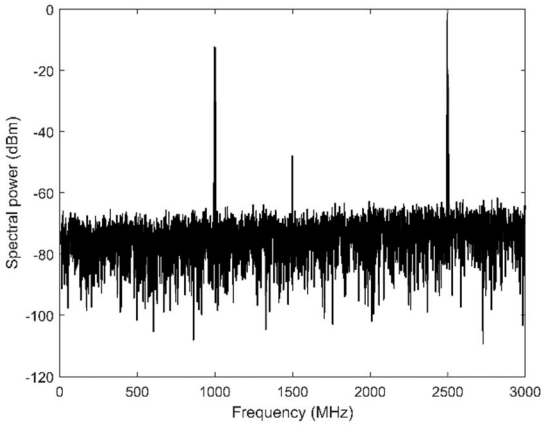

FIGURE 20. Experimental results for the spectrum observed at the ANT port when a 1GHz CW tone is injected into the circulator from the TX port.

TABLE 1. Comparison of magnetless circulators.

Circulator	[9]	[15]	[16]	[17]	[20]	This work (Passive Bootstrap)
Technology	180nm Silicon	65nm Silicon	65nm Silicon	180nm Silicon	45nm Silicon	200nm GaN
Frequency Range	421MHz-446MHz	600MHz-900MHz	610MHz-975MHz	0.86-1.08	22.7GHz-27.3GHz	10MHz-1GHz
Isolation (dB)	20-50	9.6-50	10.1-33	25	9-20.2	19-30
Insertion Loss (dB)	2-4.6	1.7-3.3	1.8-3	2.1(TX)/2.9(RX)	3.2-8.7	2.1 -3
P1dB (dBm)	28	N/A	N/A	30(TX)/21(RX)	21.5	21
IIP3 (dBm)	N/A	27.5	30	5(TX)/37(RX)	N/A	27
Device Area	11mm x 13mm	0.32 mm x 0.32mm	0.32mm x 0.65mm	16.5mm^2	1.2mm x 1.8mm	4.9mm x 5.1mm

is −7dBm. It is successfully recovered at the ANT port as shown and agrees with the Nyquist rate behavior. The spectral component residing at 1.5GHz is the switching noise which is at the difference frequency of the TX signal frequency and the switching clock frequency. The additional loss observed at the ANT port comes from the cabling used to supply the TX signal and capture the ANT spectrum.

IX. CONCLUSION

The Sequentially-Switched Delay Line (SSDL) circulator has the potential to provide full duplex communication over a broad bandwidth in a package size which is more suitable for integration with various integrated circuits. Five SSDL circulator configurations are designed and fabricated on GaN MMIC and their experimental performance is presented in this paper. The fifth one is also compared against other state of the art magnetless circulators in Table 1. The comparison has shown the proposed circulators offer the largest fractional bandwidth that is spurious free. It however, offers a lower power handling comparing to some other works such as [16] and [17] due to its non-resonant, broadband architecture.

Future efforts will focus on further reducing the insertion loss and increasing the power handling through the use of

a faster transistor technology, a more precise switch model and better gate-drain isolation techniques. This non-magnetic circulator concept can lead to the development of transceiver electronics operating over a wide range of frequencies, due to the scalability of the circulator's operating frequency.

ACKNOWLEDGMENT

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