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RESEARCH ARTICLE

Sliding Mode Control of Quadratic Boost Converters Based on Min-Type Control Strategy

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ABSTRACT The paper deals with the control of a quadratic boost converter supplied by low-voltage energy sources, such as photovoltaic panels, fuel cells, or batteries. The control scheme consists of two control loops. A min-type controller governs the inner loop to force the current state of the nominal model to converge in a neighborhood of the equilibrium state. The external loop processes the output tracking error using an integrator, and it allows reconfiguring the converter's working point by changing the equilibrium state given in the input to the internal loop. This configuration assures both zero tracking error of the output voltage and robustness against load and input voltage variations and converter parameter uncertainties. The stability of the whole system is investigated using the hybrid system framework. The proposed control technique has been tested experimentally in a suitably developed (low-cost) setup, and the results show the effectiveness of the proposed approach.

INDEX TERMS Low-cost hardware implementation, min-type control, quadratic boost converter.

I. INTRODUCTION

The deployment of generation systems from renewable energy sources has aroused great interest in DC-DC conversion. Indeed, most of these sources (photovoltaic panels, fuel cells, etc.) and storage systems (batteries, supercapacitors, etc.) are characterized by a low-voltage operating range. To allow the distribution of such energy, a DC-DC conversion stage is needed [1]. Accordingly, a considerable effort has been expended to seek solutions for increasing the static voltage gain and the conversion efficiency. Indeed, a high static gain reduces the number of conversion stages needed when a high conversion ratio is required, and an increase in efficiency allows for minimizing losses.

Due to its high voltage ratio, a good converter topology is the Quadratic Boost Converter (QBC). There exist various configurations, but it is possible to distinguish between two main topologies, the one called Cascade Boost Converter (CBC), which consists of two separate and independent boost stages driven by two switching devices [2], and the one which consists of a single conversion stage with one switching device [3], [4], [5], [6]. Other multi-stage topologies to achieve a higher conversion ratio can be found in literature [7], [8]. Comparisons between converter topologies can be found in the literature. For example, in [9], a comparative study of QBC and CBC converters is proposed. Both can give a high voltage conversion ratio, but the stress for QBC is higher than CBC, therefore, this topology will be more expensive. At the same time, the switching losses are less in QBC since a reduced number of forced switches are used. In [10], a complete efficiency analysis of the QBC, operating with a sliding-mode based control system, has been conducted. It results that the QBC with a single switch is the best candidate for low voltage input applications among the various converter topologies.

Various solutions can be found in the literature, focusing on the control technique used to drive the switching device of the QBC. The sliding mode control

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method has been diffusely applied for controlling DC-DC converters.

References [11] and [12] propose a controller consisting of two control loops. In [11], a PI-type control loop regulates the outer output voltage that also gives the inductor reference current for the inner current loop. The low signal model, corresponding to the averaged state space model, has been used to design the inner control loop. In [12], the output voltage is regulated by a PI compensator that also sets the inner loop's reference current. The design of the inner loop is based on the sliding mode control of the inductor current in the converter input inductor. The outer loop is designed with the frequency domain classical approach. In [13], to obtain a higher conversion ratio and reduce the switching losses, a single quasi-resonant network operates in a zero-current switching way is implemented. In [14], by only measuring the input and output voltages, a hybrid controller, together with an observer for the inductor currents, has been implemented to work with QBC. In [10], a sliding mode method is used for controlling the inner current loop, whereas a PI controller is used for the external voltage control loop, which gives the reference current for the inner loop. The switching surface consists of a linear combination of the input current tracking error and the output voltage tracking error. The implementation of the controller is hardware, with a hysteretic comparator for the inner loop. In [15], a sliding-mode controller for a cascade QBC is proposed, as well as a Lyapunov's stability analysis for load regulation, line regulation, and step response, while in [16] a comparison of static and dynamic performances was carried out for the known QBC topologies operating under sliding-mode control. In [17], a control system for a QBC is proposed based on an inner loop with a sliding mode controller and an outer loop, with integral-type action, for assuring robustness against load and input voltage variations and converter parameter uncertainties. The sliding mode controller is designed with the extended linearization method and ensures local asymptotic stability. Subsequently, the integral controller is designed using classical frequency methods and assures input-output stability.

All of the control strategies above-mentioned operate at a variable switching frequency, and the sliding-mode algorithm directly drives the commutation instant. There are also other control strategies whose implementation uses a Pulse Width Modulator (PWM) module working at a fixed frequency. In [18], for example, a PWM controller is proposed for a QBC. It consists of a current inner loop controlled using a sliding mode method and an outer loop that sets a reference current for the inner loop. Regarding PWM techniques, in [19] and [20], resonant networks have been added to achieve soft-switching and provide highly efficient operating conditions for a wide load and input voltage range. Another approach, slightly different from the previous ones, is based on the Min-Type control strategy. In [21], the analysis and design of a min-type strategy to control a synchronous boost converter in continuous conduction mode are proposed. In [22], to control the converter, a PWM control algorithm is designed, starting from a hybrid model and using an approach based on the averaged state space model, having the duty-cycle as an input variable.

In this paper, a robust control scheme for a QBC is proposed. It consists of a sliding mode internal control loop designed according to the min-type control strategy but, differently than [21], the min-type approach is applied to the QBC. This leads to different conditions, as will be shown in the paper. Moreover, the control strategy proposed in this manuscript follows a different approach from the one described in [18], [19], [20], and [22], where a PWM modulation is proposed, as it foresees that the power switch is controlled at a variable frequency and therefore requires a greater calculation and implementation effort. At the same time, the proposed variable frequency control strategy allows for obtaining better performances in transient behavior. Furthermore, comparing the proposed algorithm with the other sliding-mode algorithms ([10], [11], [12], [13], [15], [16], [17]), here an optimum problem is solved to take into account the entire system state trajectory instead of regulating only the output voltage of the converter. Finally, the results presented in this contribution allow obtaining deterministic guarantees on the convergence that are difficult to obtain with sliding-mode algorithms previously mentioned.

In detail, our proposed controller consists of two loops. The inner loop is designed so that the controller forces the state of the converter model to converge toward the desired equilibrium state. The output voltage tracking error drives the outer control loop. It provides a dynamic feedforward term to reach a null voltage tracking error. In this way, the whole system is robust against input voltage and parameter variations. Finally, an extensive part is dedicated to the experimental implementation using low-cost hardware. In particular, it is explained how the peculiar architecture of the TMS320F28379D, which embeds both a CPU and a dedicated control law accelerator, is exploited to implement variable frequency control algorithms. This part also represents an essential contribution to this work. Experimental results are given to prove the effectiveness of the converter performance when unexpected variations in the input voltage and output load occur.

II. DYNAMIC MODEL OF THE QUADRATIC BOOST CONVERTER

The electrical circuit of the quadratic boost converter considered in this paper is shown in Fig. 1. According to the approach illustrated in [23], choosing the state vector as follows:

$$\boldsymbol{x}^{\top} = \left[i_{L1} \; i_{L2} \; v_{C1} \; v_{C2} \right], \tag{1}$$

assuming as output $y = v_{C2}$, the mathematical model of the QBC of Fig. 1 is given by:

$$\dot{\boldsymbol{x}} = \boldsymbol{A}_{\sigma}\boldsymbol{x} + \boldsymbol{b}V_{in}, \tag{2}$$

$$y = \boldsymbol{c}^{T}\boldsymbol{x}, \tag{3}$$

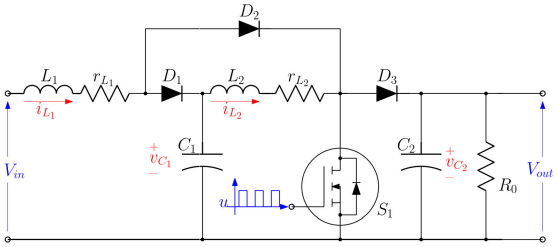

FIGURE 1. Electrical circuit of the quadratic boost converter.

where σ is a piecewise constant function representing the switching state of S_1 and it can assume the values 0 or 1 ($\sigma = 0$ means that the switch S_1 is in the OFF state and $\sigma = 1$ means that the switch S_1 is in the ON state). $\boldsymbol{A}_0$ and $\boldsymbol{A}_1$ are the dynamic matrices corresponding, respectively, to $\sigma = 0$ and $\sigma = 1$, $\boldsymbol{b}$ is the input gain vector and $\boldsymbol{c}^\top$ is the output matrix whose expressions are defined as follows:

$$\boldsymbol{A}_0 = \begin{bmatrix} -\frac{r_{L1}}{L_1} & 0 & -\frac{1}{L_1} & 0 \\ 0 & -\frac{r_{L2}}{L_2} & \frac{1}{L_2} & -\frac{1}{L_2} \\ \frac{1}{C_1} & -\frac{1}{C_1} & 0 & 0 \\ 0 & \frac{1}{C_2} & 0 & -\frac{1}{C_2 R_0} \end{bmatrix},$$

$$\boldsymbol{A}_1 = \begin{bmatrix} -\frac{r_{L1}}{L_1} & 0 & 0 & 0 \\ 0 & -\frac{r_{L2}}{L_2} & \frac{1}{L_2} & 0 \\ 0 & -\frac{1}{C_1} & 0 & 0 \\ 0 & 0 & 0 & -\frac{1}{C_2 R_0} \end{bmatrix}, \quad \boldsymbol{b} = \begin{bmatrix} \frac{1}{L_1} \\ 0 \\ 0 \\ 0 \end{bmatrix}, \quad \boldsymbol{c} = \begin{bmatrix} 0 \\ 0 \\ 0 \\ 1 \end{bmatrix}.$$

Note that the expressions of matrices $\boldsymbol{A}_0$ and $\boldsymbol{A}_1$ are obtained by neglecting the parasitic resistances of the two capacitors, $r_{C1} = r_{C2} = 0$.

In the contest of the switching models, it is important to define the equilibrium states appropriately. This can be made by associating the switching model with an affine averaged model, as illustrated in [23] and [24]. In particular, the affine averaged model, associated with (2)-(3), is given by:

$$\dot{\boldsymbol{z}} = \boldsymbol{A}\boldsymbol{z} + \boldsymbol{b}V_{in}, \tag{4}$$

$$y = \boldsymbol{c}^\top \boldsymbol{z} \tag{5}$$

where:

$$\boldsymbol{A} = \lambda \boldsymbol{A}_{ON} + (1-\lambda)\,\boldsymbol{A}_{OFF},$$

and $\lambda \in [0, 1]$. Note that matrix $\boldsymbol{A}$ is a convex combination of the matrices $\boldsymbol{A}_{ON}$ and $\boldsymbol{A}_{OFF}$, and it is a Hurwitz matrix.

Model (4) allows us to determine the set of its equilibrium states Z_e. This set is defined as:

$$Z_e = \{\boldsymbol{z}_e(\lambda) : \boldsymbol{A}\boldsymbol{z}_e + \boldsymbol{b}V_{in} = 0 \wedge \lambda \in [0, 1]\} \tag{6}$$

whose explicit expression is given by:

$$\boldsymbol{z}_e(\lambda) = \frac{V_{in}}{g}\begin{bmatrix} 1 \\ (1-\lambda) \\ (1-\lambda)r_{L2} + (1-\lambda)^3 R_0 \\ (1-\lambda)^2 R_0, \end{bmatrix} \tag{7}$$

where $g = R_0(1-\lambda)^4 + r_{L2}(1-\lambda)^2 + r_{L1}$.

It is useful to note that the determinant of $\boldsymbol{A}$, given by:

$$\det(\boldsymbol{A}) = \frac{R_0(1-\lambda)^4 + r_{L2}(1-\lambda)^2 + r_{L1}}{C_1 C_2 L_1 L_2 R_0}, \tag{8}$$

is always greater than zero for all $\lambda \in [0, 1]$ and, consequently, there always exists an equilibrium point given by $\boldsymbol{z}_e = -\boldsymbol{A}^{-1}\boldsymbol{b}V_{in}$. The output associated with $\boldsymbol{z}_e$ is $y_e = \boldsymbol{c}^\top \boldsymbol{z}_e$.

III. MIN-TYPE CONTROL STRATEGY

The problem now is that of determining a state feedback control strategy $\sigma(\boldsymbol{x}(t))$ which, starting from a generic initial state $\boldsymbol{x}_0$, leads the state of model (2) to follow a trajectory around an equilibrium state, which allows obtaining a desired output voltage value. In particular, for a given value of desired output voltage, V^*_{out}, it is associated with a value of λ^* obtained by inverting the last relation of (7) as follows:

$$\lambda^* = 1 - \sqrt{\frac{\frac{V_{in}}{V^*_{out}}R_0 - r_{L2} + \sqrt{\left(\frac{V_{in}}{V^*_{out}}R_0 - r_{L2}\right)^2 - 4r_{L1}R_0}}{2R_0}}. \tag{9}$$

Once the value of λ^* has been obtained, it can be substituted to (7) to obtain the desired equilibrium state, ensuring that the output voltage is the desired one, V^*_{out}.

Note that the generic equilibrium point $\boldsymbol{z}_e(\lambda^*)$ is not necessarily an equilibrium point for the dynamics (4)-(5), but it can be an equilibrium for the switching system in a Filippov's generalization. The associated equilibrium points $\boldsymbol{z}_e$ are infinite for the case under study. However, the goal is to regulate the output voltage to a fixed value V^*_{out}, which is related to a specific equilibrium point obtained with $\lambda = \lambda^*$ and λ^* given in (9).

Before giving the control strategy, it is necessary to provide the following assumption and a technical Lemma.

Assumption 1: It is assumed that there exist matrices $\boldsymbol{P} \in \mathbb{R}^{4\times4} \succ 0$ and $\boldsymbol{Q} \in \mathbb{R}^{4\times4} \succ 0$ such that

$$\boldsymbol{A}_{ON}{}^T\boldsymbol{P} + \boldsymbol{P}\boldsymbol{A}_{ON} + 2\boldsymbol{Q} \prec 0$$

$$\boldsymbol{A}_{OFF}{}^T\boldsymbol{P} + \boldsymbol{P}\boldsymbol{A}_{OFF} + 2\boldsymbol{Q} \prec 0$$

Note that Assumption 1 is not a strong Assumption because in Section II it has been shown that both $\boldsymbol{A}_{ON}$ and $\boldsymbol{A}_{OFF}$ are Hurwitz, therefore there always exist matrices $\boldsymbol{P}$ and $\boldsymbol{Q}$ satisfying Assumption 1.

Lemma 1: Given matrices $\boldsymbol{P}$ and $\boldsymbol{Q}$ satisfying Assumption 1, then the same matrices are also a solution of the following linear matrix inequality:

$$\boldsymbol{A}^T\boldsymbol{P} + \boldsymbol{P}\boldsymbol{A} + 2\boldsymbol{Q} \prec 0 \tag{10}$$

where $\boldsymbol{A} = \lambda\boldsymbol{A}_{ON} + (1-\lambda)\,\boldsymbol{A}_{OFF}$, for any value of $\lambda \in [0, 1]$.

Proof: Since $\boldsymbol{A}$ is a convex combination of $\boldsymbol{A}_{ON}$ and $\boldsymbol{A}_{OFF}$, we have

$$\begin{aligned} &\boldsymbol{A}^T\boldsymbol{P} + \boldsymbol{P}\boldsymbol{A} \\ &= \lambda\left(\boldsymbol{A}_{ON}{}^T\boldsymbol{P} + \boldsymbol{P}\boldsymbol{A}_{ON}\right) + (1-\lambda)\left(\boldsymbol{A}_{OFF}{}^T\boldsymbol{P} + \boldsymbol{P}\boldsymbol{A}_{OFF}\right) \prec \\ &\quad - \lambda 2\boldsymbol{Q} - (1-\lambda)2\boldsymbol{Q} = -2\boldsymbol{Q}. \end{aligned} \tag{11}$$

We used Assumption 1 and the fact that both $\lambda \leq 1$ and $1-\lambda \leq 1$. This concludes the proof. □

Using the stability theory of the hybrid systems shown in [25], we will establish stability properties regarding uniform global attractivity of a bounded and closed set. In particular, we will establish the properties of the compact attractor:

$$\mathcal{A} := \{(\boldsymbol{x}, \sigma) : \boldsymbol{x} = \boldsymbol{z}_e(\lambda^*), \sigma \in \{0, 1\}\}, \tag{12}$$

where $\boldsymbol{z}_e(\lambda^*)$ represents an equilibrium point for the averaged dynamics (4)-(5) such that $y = \boldsymbol{c}^\top \boldsymbol{z}_e(\lambda^*) = V_{out}^*$ (V_{out}^* is the desired output voltage). In the following, we induce Global Asymptotic Stability (GAS) of $\mathcal{A}$, corresponding to Lyapunov stability and convergence. Due to the developments in [25, Chapter 7], and compactness of $\mathcal{A}$, GAS is equivalent to Uniform Global Asymptotic Stability (UGAS) defined in [25, Chapter 3] involving Lyapunov stability, uniform boundedness, and uniform attractivity.

Before giving the main result, the following Lemma is considered:

Lemma 2: Consider $\boldsymbol{\xi} = \boldsymbol{x} - \boldsymbol{z}_e(\lambda^*)$ and matrices $\boldsymbol{P}$ and $\boldsymbol{Q}$ satisfying Assumption 1. Then for each $\boldsymbol{x}$:

$$\min_{\sigma\in\{0,1\}} \boldsymbol{\xi}^\top \boldsymbol{P}\left(\boldsymbol{A}_\sigma \boldsymbol{x} + \boldsymbol{B}V_{in}\right) \leq -\boldsymbol{\xi}^\top \boldsymbol{Q}\boldsymbol{\xi}. \tag{13}$$

Proof: Inequality (13) can be proved by using Lemma 1 and the same consideration given in [24, Lemma 1]. Therefore the proof is omitted for the sake of compactness. □

The following theorem can now be introduced.

Theorem 1: Consider $\boldsymbol{\xi} = \boldsymbol{x} - \boldsymbol{z}_e(\lambda^*)$ and matrices $\boldsymbol{P}$ and $\boldsymbol{Q}$ satisfying Assumption 1. Then if

$$\sigma(\boldsymbol{x}(t)) = arg \min_{\sigma\in\{0,1\}} \boldsymbol{\xi}^\top 2\boldsymbol{P}(\boldsymbol{A}_\sigma \boldsymbol{x} + \boldsymbol{B}V_{in}), \tag{14}$$

the attractor (12) is UGAS.

Proof: Let us consider the following Lyapunov function,

$$V(\boldsymbol{\xi}) = \boldsymbol{\xi}^\top \boldsymbol{P}\boldsymbol{\xi}. \tag{15}$$

During flows, we have

$$\langle \nabla V(\boldsymbol{\xi}), \dot{\boldsymbol{\xi}} \rangle = \boldsymbol{\xi}^\top 2\boldsymbol{P}(\boldsymbol{A}_\sigma \boldsymbol{x} + \boldsymbol{B}V_{in}) \leq -2\boldsymbol{\xi}^\top \boldsymbol{Q}\boldsymbol{\xi}. \tag{16}$$

This fact comes directly from Lemma 2 and equation (15). When a transition occurs (from ON to OFF state and vice versa), we trivially get

$$V(\boldsymbol{\xi}^+) - V(\boldsymbol{\xi}) = 0, \tag{17}$$

since there cannot be a discontinuity in the electrical variables that compose the state (1).

UGAS of $\mathcal{A}$ is shown using [26, Theorem 1]. In particular, since the distance of $\boldsymbol{x}$ to the attractor (12) is defined by $|\boldsymbol{x} - \boldsymbol{z}_e(\lambda^*)| = |\boldsymbol{\xi}|$, we have that [26, Equation (6)] is satisfied from the structure of the Lyapunov function (15) and from (16) and (17). Moreover, [26, Theorem 1] requires the construction of the restricted hybrid system $\mathcal{H}_{\delta,\Delta}$ by intersecting the flow set and the jump set with the set,

$$\mathcal{S}_{\delta,\Delta} = \{(\boldsymbol{\xi}, \sigma) : |\boldsymbol{\xi}| \geq \delta \text{ and } |\boldsymbol{\xi}| \leq \Delta\}, \tag{18}$$

and proving semi-global practical persistence flow for $\mathcal{H}_{\delta,\Delta}$, for each value of (δ, Δ). In particular, in order to show the practical and persistent flow, we need to prove that there exists $\gamma \in \mathcal{K}_\infty$ and the scalar $N \geq 0$, such that all solutions to $\mathcal{H}_{\delta,\Delta}$ satisfy,

$$t \geq \gamma(j) - N, \quad \forall t \in \bigcup_{j\in \mathrm{dom}_j \xi} I^j \times \{j\}, \tag{19}$$

see [26] for details. To establish (19), we have that after each transition,

$$\begin{aligned} \boldsymbol{\xi}^\top \boldsymbol{P}\boldsymbol{\xi}^+ &= \boldsymbol{\xi}^\top \boldsymbol{P}\left(\min_{\sigma\in\{0,1\}} \boldsymbol{\xi}^\top 2\boldsymbol{P}(\boldsymbol{A}_\sigma \boldsymbol{x} + \boldsymbol{B}V_{in})\right) \\ &\leq -2\boldsymbol{\xi}^\top \bar{\boldsymbol{Q}}\boldsymbol{\xi}, \end{aligned} \tag{20}$$

from Lemma 2. Therefore, if any solution to $\mathcal{H}_{\delta,\Delta}$ performs a jump from $\mathcal{S}_{\delta,\Delta}$ it remains in $\mathcal{S}_{\delta,\Delta}$ because $\boldsymbol{\xi}^+ = \boldsymbol{\xi}$. Moreover, after the transition, all non-terminating solutions must flow for some time since the electronic device S_1 is not ideal, and they cannot be forced to switch at an infinite frequency. Therefore, each pair of consecutive transitions has a uniform dwell-time $\rho(\delta, \Delta)$. This dwell-time (δ, Δ) implies [26, Equation (4)] with the class-$\mathcal{K}_\infty$ function $\gamma(j) = \rho(\delta, \Delta)j$ and $N = 1$. Then, all assumptions of [26, Theorem 1] are satisfied, and UGAS of $\mathcal{A}$ is concluded. □

Remark 1: The only disadvantage of the proposed method is that it results in a higher computational effort than standard PWM techniques. Indeed, the min-type algorithm proposed in this paper is a variable-frequency algorithm, and it is not possible to trigger the power switch through a PWM modulator. However, it is necessary to drive this signal asynchronously through software instructions. For this reason, the control algorithm must run very fast with a consequent high effort from the computational point of view. Indeed, as it will be better described in Section IV, specific hardware with a dedicated Control Law Accelerator (CLA) was used. The consequence of low running time is a high current ripple.

A. CONTROLLER SCHEME AND DESIGN OF THE OUTER CONTROL LOOP

The inner loop block scheme, consisting of the Min-Type controller and the DC-DC converter, is shown in Fig. 3 (highlighted in red). The reference voltage is the system's input, and the value of λ^*, necessary to obtain $\boldsymbol{z}_e$, is computed by equation (9). The equilibrium state, obtained by (7) with $\lambda = \lambda^*$, represents the input of the control loop, and the feedback signal is the state $\boldsymbol{x}$ of the QBC. The Min-Type controller establishes the input $u \in \{0, 1\}$, according to (14).

In order to cope with load and input voltage variations, and converter parameter uncertainties, an outer loop with an integral-type controller is designed. Indeed, looking at (7), it appears that the equilibrium state for a given value of λ depends on the load, input voltage, and converter parameters. Consequently, if one or more of these quantities vary, the equilibrium state varies with respect to that desired. An efficient way to cope with these variations is that of constructing

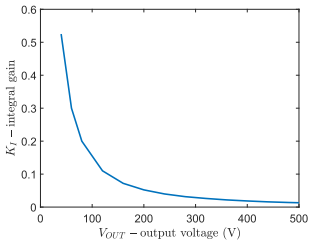

FIGURE 2. Integral gain value vs. output voltage.

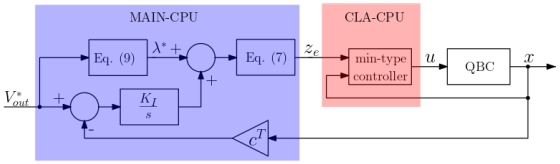

FIGURE 3. Block diagram with an external regulation loop.

an outer control loop, driven by the difference between the reference output voltage and the measured one, able to give a feedforward term Δ_λ, so as the output voltage converges to the reference one.

The outer loop controller is integral-type (K_I/s), and the block scheme of the whole control system is given in Fig. 3. The gain K_I is obtained using frequency domain design techniques to ensure asymptotic stability with a sufficient margin and a sufficient value of the crossover frequency. However, the transfer function of the process used for the controller synthesis varies with the desired equilibrium state. Therefore, adjusting the gain of the integral action is necessary to obtain the desired stability margins and crossover frequency. In practice, it is convenient to construct, off-line, a look-up Table that contains the couples K_I, V_{out}. This can be done by discretizing the output voltage in a finite number of values. For each value of V_{out}, the corresponding value of λ is obtained by using equation (9), and the relative matrix $\boldsymbol{A} = \lambda \boldsymbol{A}_{ON} + (1-\lambda)\,\boldsymbol{A}_{OFF}$ is computed as well. Then, assuming that the internal loop is much faster than the external one, the open loop transfer function can be approximated as follows:

$$W(j\omega) = \frac{K_I}{j\omega}\,\boldsymbol{c}^\top (j\omega \mathcal{I}_4 - \boldsymbol{A})^{-1}\,\boldsymbol{b} \tag{21}$$

Finally the value of K_I is selected in order to impose a crossover frequency, ω_t, such that $\angle W(j\omega_t) = 100$ degrees. This can always be done since a variation of k_I implies a translation of the module and consequently a variation of the crossover frequency without changing the phase. Note that the choice $\angle W(j\omega_t) = 100$ degrees will imply a phase margin equal to $m_\phi = 80$ degrees. Considering the QBC whose parameters are shown in Table 1, Fig. 2 contains the waveform of the integral gain value as a function of the output voltage that allows obtaining a crossover frequency of about 100 rad/s and a phase margin of about $m_\phi = 80$ degree in the range 40 V - 500 V. This waveform can be used to update online the integral gain such that the desired stability margins and crossover frequency are satisfied in a wide range of output voltage variation.

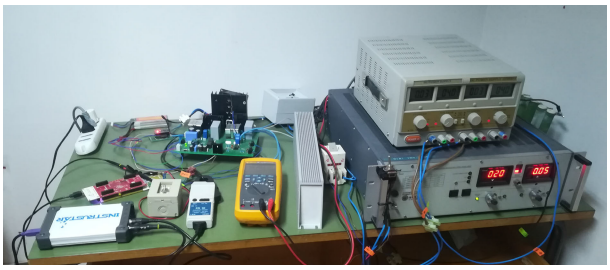

FIGURE 4. Photo of the experimental setup.

TABLE 1. Parameters of the QBC.

COMPONENT	VALUE	MODEL
V_{IN}	24V	
L_1, (L_2)	330, (470) μH	AGP4233-xx4ME
r_{L_1}, r_{L_1}	11.5mΩ	
C_1, C_2	20μF	MKP1848C62090JP4
R_0	380Ω	
$D_{1,2,3}$		C3D06060A
S_1		C3M0065090D

IV. EXPERIMENTAL SETUP

A. DESCRIPTION OF THE EXPERIMENTAL SET-UP

A test setup has been suitably built to validate the proposed control technique. The general architecture of the experimental setup follows the scheme shown in Fig. 3. The converter under test is shown in Fig. 1, and the parameters, as well as the used components, are given in Tab. 1. A photo of the test bench is shown in Fig. 4. The inductor currents I_{L1} and I_{L2} are measured through Hall-effect sensors LEM LTS-15-NP, and the V_{C1} and V_{OUT} voltages are measured through a voltage divider and an operational amplifier LM324 in buffer configuration. The controller has been digitally implemented using the C2000 32-bit TI microcontroller TMS320F28379D with an additional built-in dedicated processor acting as Control Law Accelerator (CLA). In particular, the implementation is developed so that the min-type algorithm runs in the dedicated CLA CPU while the main CPU takes account of other low-frequency tasks as highlighted in Fig. 3. The following subsection will show a detailed workflow of this particular DSP implementation scheme that exploits the peculiar CLA CPU of the TMS320F28379D microcontroller.

The above hardware architecture was chosen because the min-type algorithm proposed in our contribution is a variable-frequency algorithm. For this reason, it is impossible to trigger the power switch through a PWM modulator, but it is necessary to drive this signal asynchronously through software instructions. The use of a dedicated CPU, such as the CLA, allows not only to obtain the maximum calculation frequency for the internal loop (since the CLA has a hardware accelerator for floating point calculations) but also to prevent that the outer loop computation, at a lower frequency, result in slowdowns in the calculation speed of the inner loop. Therefore, the use of two separate CPUs (the main CPU and the CLA) makes it possible to obtain maximum performance for the internal high-frequency loop without creating interference with the low-frequency part of the control system.

B. HARDWARE IMPLEMENTATION

What mainly distinguishes a min-type algorithm from other discrete-time control algorithms is that the time interval between two consecutive commutation instants is not fixed or known. Indeed, this strategy is often classified as a variable frequency technique. Since the main objective of the hardware implementation is to impose a binary level (zero or one) on the digital output connected to the MOSFET driver, this can be accomplished using different techniques. The hardware implementations' first classification can be made based on the number of involved CPUs. Indeed, there may be solutions based on a single CPU core and other solutions based on multi-core devices.

For a single-core CPU device, the easiest way to implement a min-type algorithm is to put the whole code on the main loop of the microcontroller execution workflow. At the beginning of the main loop, the ADC conversion is triggered. After the conversion time, the computation is executed. In the end, the digital output pin connected to the driver is set to be "zero" or "one," depending on the result of the calculations. After the execution of all of these steps, a new loop iteration can start. Even if this kind of implementation is the simplest one, this presents some significant issues. First of all, operating in this way, there is not any execution "guard-time" to accomplish some other secondary tasks like, for example, communication with a host machine to impose a new output voltage set-point or a handshake with a memory to perform logging operations or even, last but not least, a computational time-slot guard to implement an outer-loop that generally runs at a lower frequency. A possible workaround to cope with these issues is to add a "dead-time" on every loop iteration that acts as a computational power reserve to perform these additional tasks. However, even if it is an easy and widely-used solution, this leads to a significant reduction of the main loop execution frequency and, therefore, an overall loss of performance.

Since the single-core implementation scheme presents the above-discussed issues, using a multi-core CPU is a better option to improve performance. For example, with a 2-CPU device, the programmer can delegate the execution of the sliding mode inner loop controller to the first CPU and the execution of the outer loop, and the other low-frequency tasks to the second CPU. In this way, it is possible to obtain the maximum performance in terms of execution time for the sliding mode controller while maintaining a computational reserve power for the other tasks.

For this work, as stated above, we selected the multi-core TMS320F28379D microcontroller by using the DSP-specific CLA CPU to perform the min-type sliding mode control law and the main CPU to accomplish the outer loop as in Fig. 3. The TI microcontroller also offers an internal high-speed bus to exchange data between the two CPUs.

In Figure 5, the workflow of the implementation setup for this work has been reported. In detail, a complete iteration is made up of the following phases:

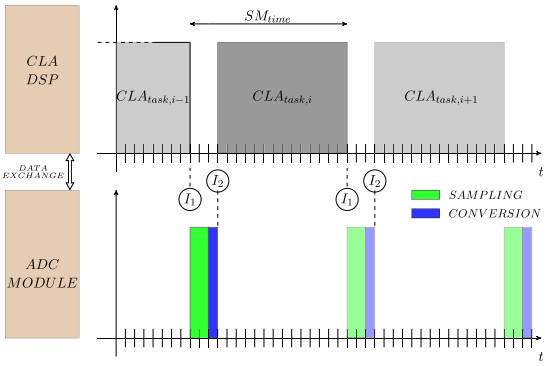

FIGURE 5. CLA/ADC tasks execution on TMS320F28379D.

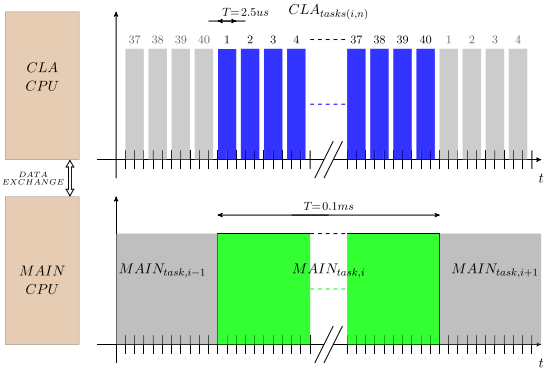

FIGURE 6. CLA/MAIN CPU tasks execution on TMS320F28379D.

- CLA task to perform the control strategy shown in (14).
- ADC parallel sampling.
- ADC parallel conversion.

Concerning Figure 5, the implementation flow is the following (for clarity of the exposure timelines are not in scale). When the $CLA_{task,i-1}$ is completed, the digital output connected to the MOSFET driver is driven according to (14) and an interrupt (corresponding to I_1) is fired to trigger the ADC sampling phase (in green). At the end of the sampling phase, the integrated 4-channel ADC module directly goes to the conversion phase to obtain a digital representation of the state (1) used in (14). Note that while the ADC module is operating, no action occurs on the CLA CPU, and, far more important, the main CPU is not charged with any task related to the min-type sliding mode inner loop. At the end of the ADC conversion phase, another interrupt, corresponding to I_2 in Figure 5, is fired to trigger the start of the $CLA_{task,i}$, thus repeating the overall cycle. So, the minimal time to complete an overall algorithm cycle SM_{time} is the sum of the CLA_{task} time plus the sampling and conversion time. In our implementation, this was almost $2,5us$, corresponding to a maximum update rate of 400kHz. With this value, the maximum achievable commutation frequency on the MOSFET driver pin is 200KHz. Since the main CPU is not involved in implementing the min-type algorithm, it was used to perform

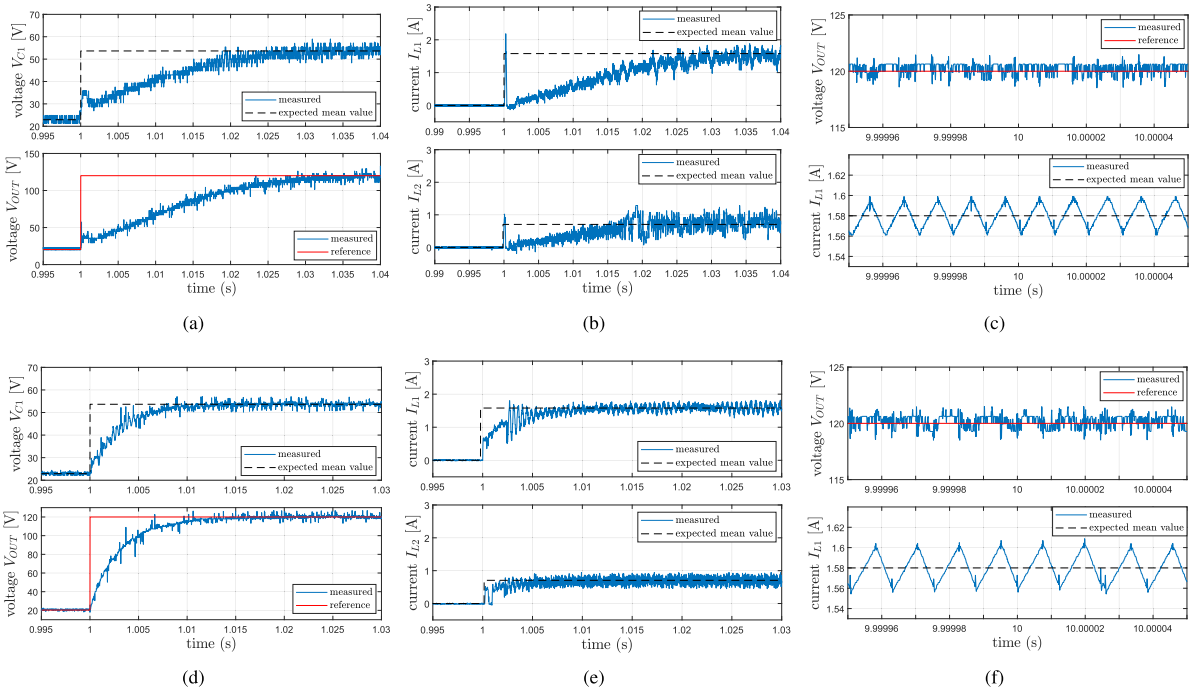

FIGURE 7. (a) V_{C1}, V_{OUT} with PI controller at start-up in *Test 1*, (b) I_{L1}, I_{L2} with PI controller at start-up in *Test 1*, (c) V_{OUT}, I_{L1} with PI controller at steady-state in *Test 1*, (d) V_{C1}, V_{OUT} with Min-type controller at start-up in *Test 2*, (e) I_{L1}, I_{L2} with Min-type controller at start-up in *Test 2*, (f) V_{OUT}, I_{L1} with min-type controller at steady-state in *Test 2*.

other tasks, such as the outer control loop that runs at the lower frequency of 10KHz.

V. EXPERIMENTAL RESULTS

In this Section experimental results are given. In order to provide a comparison with a common and widely used control law for QBC, two sets of experiments have been carried out. The first set of tests, named *Test 1*, shows results obtained by applying a standard PI-PWM controller, while the second test set, named *Test 2*, provides the results obtained by applying the described min-type control strategy. In particular, for both *Test 1* and *Test 2*, a start-up test, a steady-state test, a load variation test, and a supply voltage variation test have been carried out to validate the effectiveness of the proposed controller. For both tests, the reference output voltage has been set to $V_{out}^{ref} = 120$ V.

Figures 7 are relative to the *S*tart-up test for both *Test 1* and *Test 2*. In particular, Figures 7(a) and 7(d) show the behavior of voltages V_{C1} and V_{OUT} at the start-up time that, for clarity of representation has been set to $1s$. The imposed reference for the output voltage $V_{out}^{ref} = 120V$ has been reported in red, while the expected mean value for the voltage on the capacitor C_1, V_{C1}, has been reported in dashed black. Regarding these plots, it results in a settling time on V_{OUT} of about $35ms$ for the PI controller and a settling time of about $15mS$ for the min-type controller; therefore, the min-type controller results to be more than twice faster. Similar considerations apply to the V_{C1} voltage where the settling time is about $30ms$ for the PI controller and about $10ms$ for the min-type one.

Figures 7(b) and 7(e) show the behavior of the inductor currents I_{L1} and I_{L2} at the start-up time. Since only the output voltage V_{OUT} can be imposed on the converter, the expected value for the inductor currents I_{L1} and I_{L2} have been reported with a dashed black line. The settling time for the I_{L1} current with the PI controller results in about $20ms$ while this value is about $5ms$ for the min-type controller, four times faster. Moreover, the waveform of the inductor current I_{L1} from the PI controller presents a significant peak of about $1A$. This behavior is less strong on the inductor current for the min-type controller. Even the ripple seems lower on the min-type controller instead of the one in Test 1.

Figures 7(c) and 7(f) are relative to the behavior of the converter for Test 1 and Test 2 in a steady state condition. In particular, plots in Fig.7(c) are relative to Test 1 while plots in Fig.7(f are relative to the min-type control strategy (Test 2). For both Tests the output voltage V_{OUT} and the L_1 inductor current I_{L1} have been reported. Also this time, the imposed voltage reference $V_{out}^{ref} = 120V$ has been reported with a red line while the expected mean value for the inductor current I_{L1} has been reported with a black dashed line. Regarding the output voltage regulation, from the plots, the two controllers in Test 1 and Test 2 present almost the same behavior with a ripple on the reference voltage of about $\pm 0.5V$. About the currents waveform, it is possible to highlight that, whereas the switching frequency on I_{L1} in Test 1 is fixed at $100Khz$, in Test 2, due to the nature of the min-type control strategy, the frequency can vary and therefore the switching period does not remain the same between two consecutive commutation.

Figure 8 is relative to the behavior of the converter for Test 1 and Test 2 when a variation occurs in the input voltage. In particular, the input voltage has been imposed for these

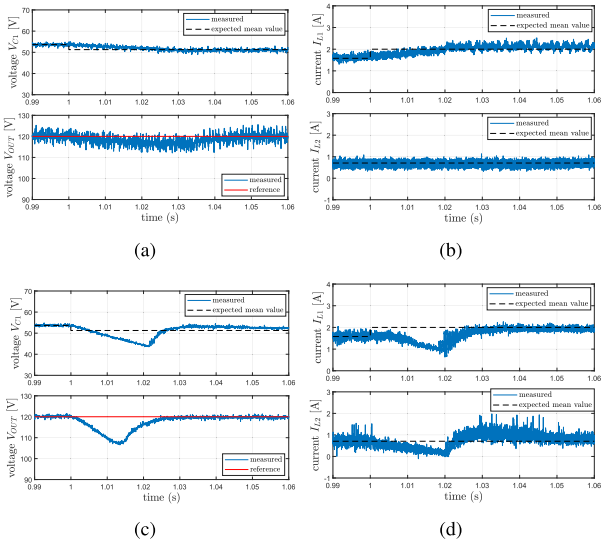

FIGURE 8. (a) V_{C1}, V_{OUT} with PI controller on V_{IN} variation in *Test 1*, (b) I_{L1}, I_{L2} with PI controller on V_{IN} variation in *Test 1*, (c) V_{C1}, V_{OUT} with min-type controller on V_{IN} variation in *Test 2*, (d) I_{L1}, I_{L2} with min-type controller on V_{IN} variation in *Test 2*.

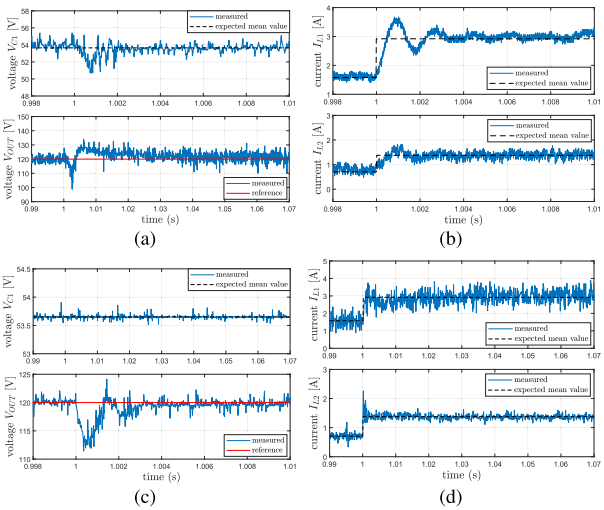

FIGURE 9. (a) V_{C1}, V_{OUT} with PI controller on R_{LOAD} variation in *Test 1*, (b) I_{L1}, I_{L2} with PI controller on R_{LOAD} variation in *Test 1*, (c) V_{C1}, V_{OUT} with min-type controller on R_{LOAD} variation in *Test 2*, (d) I_{L1}, I_{L2} with min-type controller on R_{LOAD} variation in *Test 2*.

tests to change from the nominal value of $24V$ to the reduced value of $20V$. These tests reflect some behaviors that can occur in a practical application, for example, when the converter is connected to a smart grid where the prevalent voltage can fall for overcharge or when the converter is connected to a solar panel and the presence of shading conditions.

Figure 9 is relative to the behavior of the converter for Test 1 and Test 2 when a variation occurs in the load. In particular, for these tests, the load has been imposed to change from the nominal value of 380Ω to the reduced value of 220Ω. These tests reflect some behaviors that can occur in a practical application, for example, when the converter's output is used to charge a battery or power industrial plants and residential houses.

VI. CONCLUSION

In this paper, a min-type control strategy based on a nonlinear switching surface was developed for a quadratic boost converter. The proposed approach allowed control of the whole state of the system, both currents and voltages, ensuring effective control of the converter despite load and input voltage variations. The assumption of fixed switching frequency is no longer used in this work. This had an immediate theoretical effect on the switching frequency during the startup because it introduced hysteresis width, which decreased from its maximum value until zero when the equilibrium point was attained. This led to minimizing the commutations number, especially during the transient time. The infinite switching frequency that would result in a steady state had been precluded by including experimentally a dwell-time constraint, which eventually resulted in an upper bound for the switching frequency. A prototype was constructed to verify the theoretical predictions. The control algorithm was implemented using a microprocessor that processes the samples of inductor currents and capacitor voltages to provide the control signal. The desired equilibrium point was reached after a fast transient, and no inrush current was observed. Adding an outer loop to compensate for input voltage and load variations ensures output voltage regulation.

As a future direction, we would like to investigate the possibility of substituting the external PI loop with a dynamic allocation strategy that allows the imposition of the desired equilibrium point in a robust way and contemporary further improve the transient behavior.

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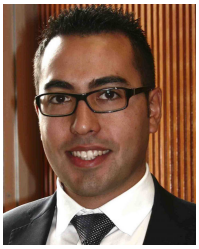

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