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RESEARCH ARTICLE

Design of LDO Regulator With High Reliability ESD Protection Circuit Using Analog Current Switch Structure for 5-V Applications

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ABSTRACT The modern electronic device should be able to provide stable voltage and current under a variety of conditions. The LDO regulator used in the electronic device is a system that requires various voltages and load currents. This paper suggests to the LDO regulator with the high reliability ESD protection circuit that achieves low peak voltage through analog switch structure. The proposed LDO regulator has the function of detecting the output voltage fluctuations depending on the load via an analog switch structure and effectively controlling the peak voltage. In addition, as IC is miniaturized and integrated, circuit failures frequently occur in mobile devices using the low voltage due to electrostatic discharge (ESD). The proposed ESD protection circuit is placed on I/O and power lines to prevent the IC circuit from being destroyed from the inevitable ESD phenomenon. Therefore, in this paper, an ESD protection circuit was built into the LDO regulator to verify high reliability from ESD situations. It was verified that the high reliability of the IC can be improved through effective current discharge due to ESD surge. The proposed LDO regulator, implemented in a 0.13μm BCD process, achieves an undershoot voltage of 25 mV and an overshoot voltage of 28 mV for a load current of 300 mA.

INDEX TERMS LDO regulator, load transient, LDO regulator with built-in ESD protection circuit, ESD protection circuit.

I. INTRODUCTION

As the use of portable devices powered by batteries such as smart phones increases every year, the importance of Power Management IC (PMIC) is being emphasized. PMIC plays a role in converting and controlling the power required by the system to achieve optimal battery performance in portable devices such as smartphones or IoT devices. So, as the demand for battery-powered electronic devices with better performance and higher efficiency continues to grow, engineers seek to deliver best-in-class performance while consuming minimal power. Power management of these devices is becoming increasingly important in the semiconductor industry, making it important to increase the operating time of devices and batteries while reducing overall system cost.

Figure 1 shows the LDO regulators required for smooth operation of small and high-efficiency electronics due to advances in CMOS technology. LDO regulators that can control the output voltage and load current regardless of the rapidly changing load can improve power efficiency by operating at a low potential difference between the input voltage and the output voltage. Since the LDO regulator is a key component in electronic products and mobile systems, dozens are required for each system. This causes a decrease in battery usage time required in a mobile system. Therefore, improving the battery run time of mobile systems has become

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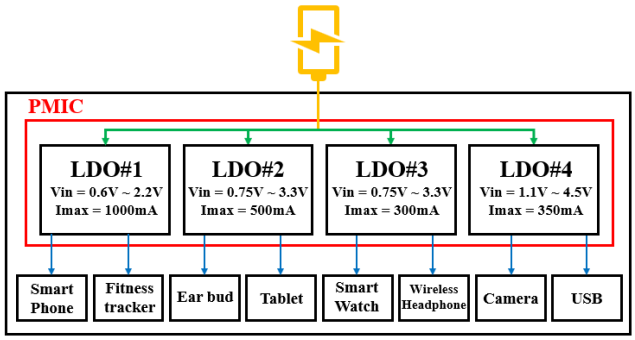

FIGURE 1. PMIC (power management integrated circuit).

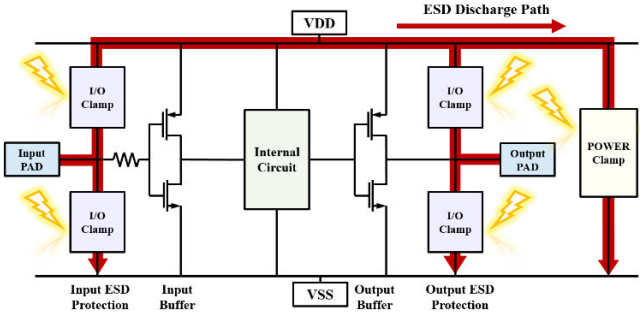

FIGURE 2. General ESD protection network.

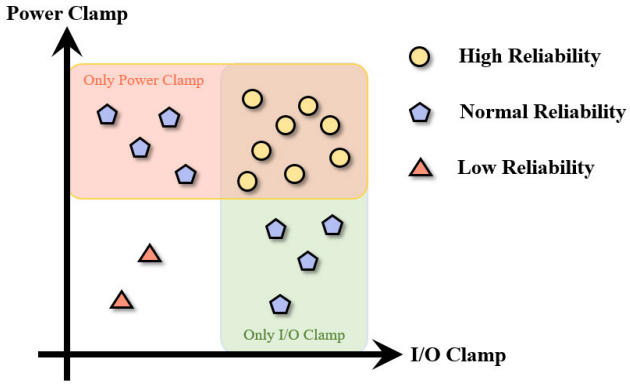

FIGURE 3. Reliability according to ESD clamp.

a more important issue, and it is necessary to develop of LDO regulators for efficient power management of battery-operated electronic products.

Instantaneous changes in load current also affect the LDO regulator's output voltage. The output voltage due to the change in load current is called the peak voltage. If the peak voltage cannot be controlled, it means that it cannot supply a stable voltage to other connected systems. Therefore, the LDO regulator must be able to satisfy various load currents. Therefore, the proposed LDO regulator has constructed a system that can effectively supply and discharge current using an analog current switch structure [1], [2], [3], [4], [5], [6], [7].

The electro-static discharge (ESD) phenomenon is a type of electric overstress (EOS) phenomenon and refers to a phenomenon in which a very high voltage is discharged in an instant due to a phenomenon such as charging or friction that is commonly generated in everyday life between objects accumulating electrostatic charges. Unlike EOS, which usually lasts from several of μs to more than ms, ESD discharges a high voltage of several kV for a very short time of several ns as a single occurrence. In normal cases, the problems caused by the ESD phenomenon in everyday life are not large due to the resistance components between the ESD discharge paths. However, in the semiconductor industry, this is a very important issue that is a major cause of IC destruction. The semiconductor industry is developing day by day and is struggling to put more and more smaller devices into one IC. If a current of several A or more generated by the ESD phenomenon enters such a miniaturized and highly integrated IC within a short time of ns unit, it causes a soft fail or hard fail in the semiconductor IC, interfering with the normal operation of the IC, and as a result not only the IC where the ESD phenomenon has occurred, but also other IC organically connected to it can cause difficulties in securing reliability. Therefore, the ESD phenomenon may occur in the I/O Pad and any node in the semiconductor internal circuit. So as shown in Figure 2, it is essential to ensure the reliability and stability of the IC by safely discharging the ESD phenomenon by embedding the ESD protection circuit inside the semiconductor chip.

Figure 3 shows the reliability of the semiconductor IC according to the presence or absence of the ESD clamp. ESD phenomenon can occur not only in the input pad and output pad of the circuit inside the semiconductor, but also in any node existing in the circuit. In general, since the part exposed to ESD situations is divided into the voltage line and the output line of the IC, when an ESD surge occurs, the ESD current is discharged by forming a discharge path through the I/O clamp or power clamp. For this reason, the I/O clamp and power clamp must be built into the internal circuit to ensure the stability and high reliability of the IC by forming the ESD discharge path smoothly.

Figure 4 (a) shows the ESD design window of the zener diode, and (b) shows the equivalent circuit and ESD design window of the proposed ESD protection device. The ESD Design Window is a very important consideration when designing an ESD protection circuit. If the ESD protection circuit invades the normal operation region of the internal IC, it not only interferes with the normal operation of the internal IC, but also causes an unnecessary increase in power consumption by continuously discharging current. In addition, if the ESD protection circuit invades the breakdown voltage region of the internal IC, it causes the destruction of gate oxide, causing fatal damage to the reliability of IC. Therefore, the key to ESD protection circuitry is to have excellent ESD durability while operating within the design window. As an ESD protection circuit, the diode has a very simple structure and has the advantage of being easy to implement. For this reason, the conventional ESD protection circuit diode is built into the I/O and power clamp of the LDO regulator, but the conventional built-in diode was removed

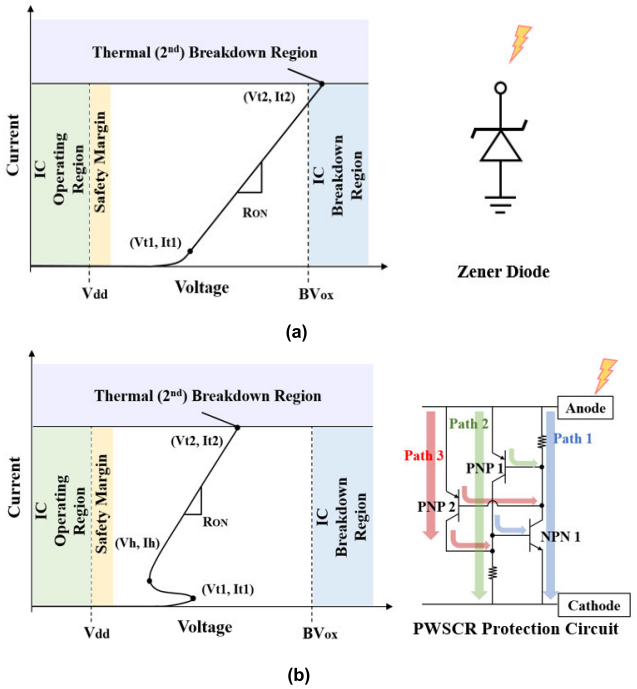

FIGURE 4. The ESD design window (a) Zener Diode (b) Penta-Well ESD protection circuit.

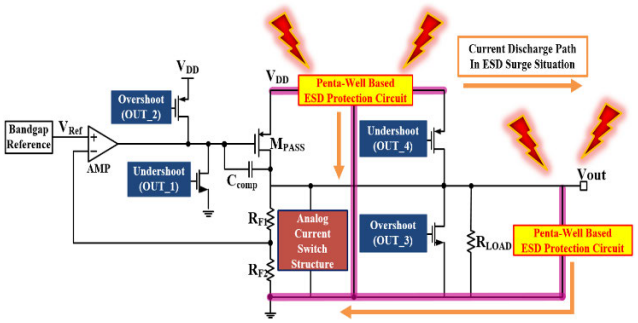

FIGURE 5. LDO regulator with penta-well ESD protection circuit using analog current switch.

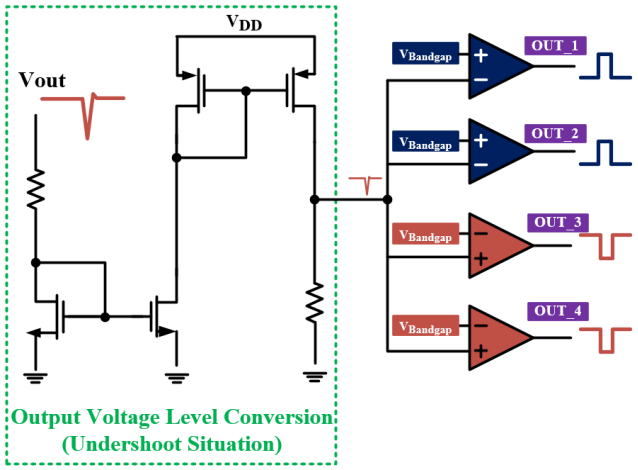

FIGURE 6. Analog current switch according to undershoot situation.

to built-in the proposed penta-well ESD protection circuit. The reason for removing it is that about 7 to 8 diodes, which are conventional ESD protection circuits, are required to embed in a 5 V class application. It is difficult to secure ESD robustness because such a large number of diodes not only occupy a large area of the IC, but also damage the diodes due to insufficient immunity to heat generated to handle the ESD current. Also, referring to the ESD Design Window in Figure 4 (a), the on-resistance of the diode is larger than that of the proposed ESD protection circuit. If the on-resistance is large, it causes damage to the internal circuit even though the limit current has not been reached, thereby degrading the robustness characteristics. Also, since the turn-on voltage of the diode is very sensitive to temperature, the ESD protection circuit using the diode is vulnerable to heat generation. On the other hand, referring to Figure 4 (b), the on-resistance of the proposed ESD protection circuit is lower than that of the zener diode, and thus the robustness characteristics are better. In addition, ESD current discharge with higher current driving capacity is possible by forming a discharge path by positive feedback between NPN BJT and PNP BJT. Therefore it can be confirmed that ESD current is discharged through three paths to have latch-up immune characteristics through high holding voltage [15].

The purpose of this paper is to propose the embedding the ESD protection circuit in the proposed LDO regulator with function of preventing damage and destruction of the IC by stably discharging the overcurrent caused by the ESD surge occurring between the input and output pins. In the event of an ESD event, the ESD protection circuit must be designed so as not to affect the input and output terminals of the LDO regulator due to the formation of a discharge path. Therefore, the I/O CLAMP terminal and the POWER CLAMP terminal of the proposed LDO regulator have built-in ESD protection circuits. The built-in ESD protection circuit is an SCR-based ESD protection circuit, not a diode, and has latch-up immunity due to its excellent current drive capability and high holding voltage. As a result, it is possible to secure excellent reliability by embedding an ESD protection circuit as well as the proposed LDO regulator for 5V class low voltage applications.

II. PROPOSED LDO REGULATOR

A. LDO REGULATOR WITH ANALOG CURRENT SWITCH STRUCTURE

As shown in Figure 5, the proposed LDO regulator can effectively control the output voltage with the analog switch structure according to the change in the load current by inputting it to the analog current switch structure through the output voltage level conversion. It also consists of an analog switch structure and a highly reliable ESD protection circuit.

Figure 6 shows the operation of the analog current switch structure when the proposed LDO regulator experiences an undershoot situation due to load current. An instantaneous drop in output voltage due to undershoot is detected by an analog current switch. After lowering the voltage level of the output voltage, it is applied by the current switch. As a

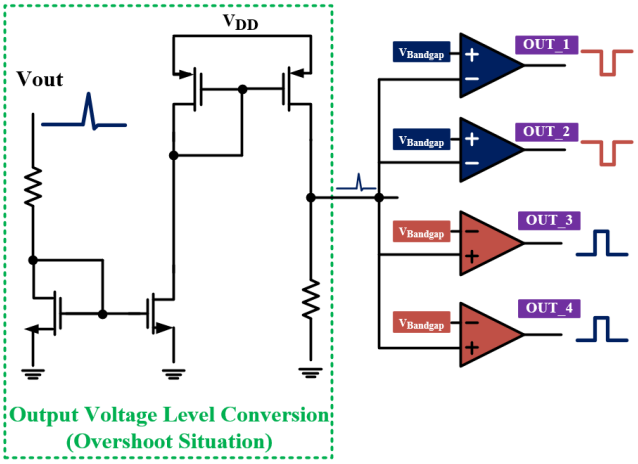

FIGURE 7. Analog current switch according to overshoot situation.

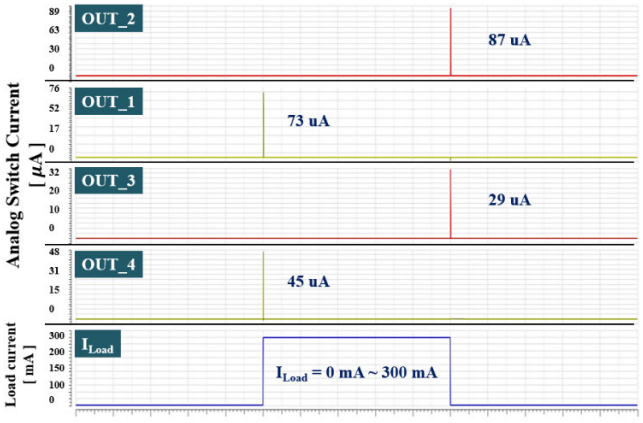

FIGURE 8. Analog current switch simulation result.

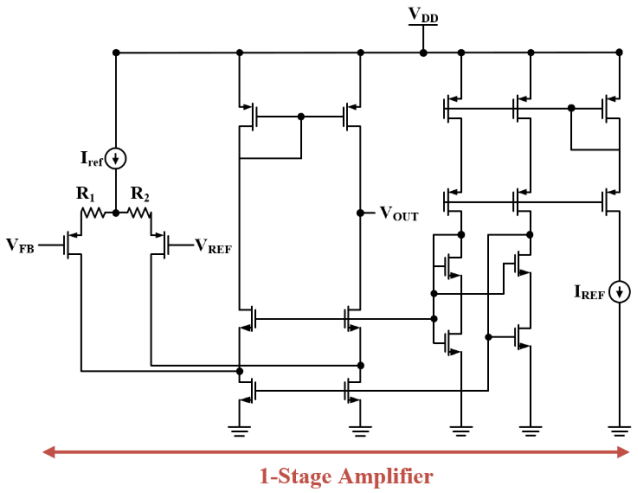

FIGURE 9. Amplifier schematic of the proposed LDO regulator.

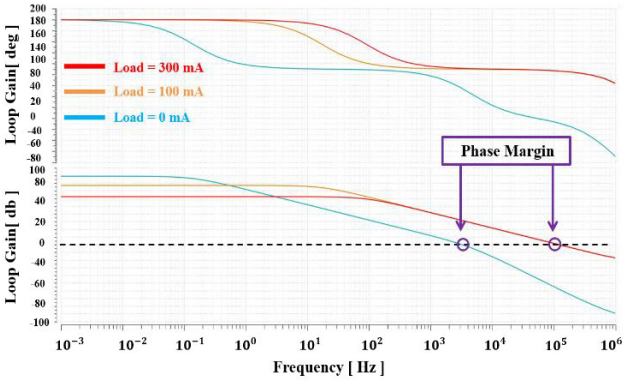

FIGURE 10. Phase margin of the proposed LDO regulator according to the load current.

result, the voltages of OUT_1 and OUT_4 act as switches to provide supply and discharge currents to the pass transistor and the output terminal of the LDO regulator. The switch operation of OUT_2 and OUT_3 is not affected in the case of undershoot. As a result, in the case of an undershoot condition, more current is discharged to the gate terminal of the pass transistor, and at the same time, additional current is supplied from the output terminal to more effectively control the output voltage. Conversely, Figure 7 shows the operation of the analog current switch structure when the proposed LDO regulator experiences an overshoot situation due to load current. An instantaneous increase in output voltage due to overshoot is detected by an analog current switch. After lowering the voltage level of the output voltage, it is applied by the current switch. As a result, the voltages of OUT_2 and OUT_3 operate as a switch to provide supply and discharge current to the output terminal of the pass transistor and LDO regulator. The switch operation of OUT_1 and OUT_4 has no effect in an overshoot situation. As a result, in an overshoot situation, additional current is supplied to the gate terminal of the pass transistor and at the same time additional current is discharged from the output stage, effectively controlling the output voltage.

Figure 8 shows the analog current switch operation simulation of the proposed LDO regulator according to the load current change. In an undershoot condition, supply and discharge currents of 73μA and 45μA are provided due to the switch operation of OUT_1 and OUT_4. Also, in the overshoot situation, supply and discharge currents of 87μA and 29μA are provided due to the switch operation of OUT_2 and OUT_3. It can be seen that the current supplied and discharged to the gate terminal of the pass transistor is greater than the current supplied and discharged to the output terminal of the LDO regulator. The reason is that the pass transistor is the largest element in the LDO regulator, so it has excellent current drive capability. Even a small change is so large that the current drive capability is excellent, so if you can change it by providing additional supply and discharge current, you can effectively control the voltage [8], [9], [10], [11], [12], [13], [14], [15], [16].

Figure 9 shows the amplifier structure of the proposed LDO regulator. The structure of the amplifier is composed of a folded stage. The R1 and R2 resistors of the amplifier are composed of fixed resistors at the output stage, so a resistor that can increase only the gain without changing the bode plot is added.

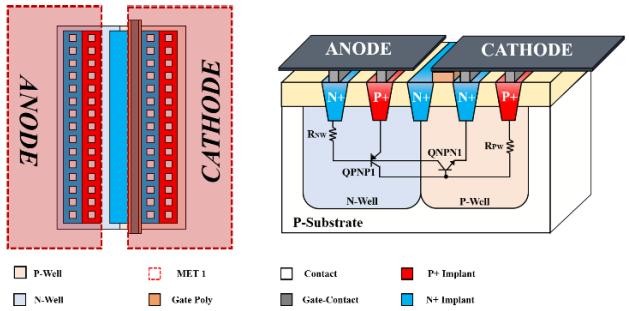

FIGURE 11. LVTSCR (low voltage triggered silicon controlled rectifier).

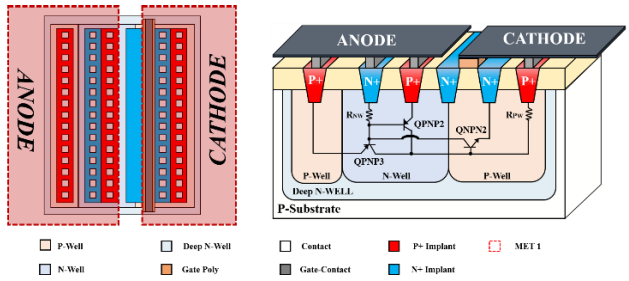

FIGURE 12. LRSCR (low ron silicon controlled rectifier).

Figure 10 shows the phase margin change according to the load current applied to the proposed LDO regulator. The stability of the LDO regulator according to load current changes must be verified. If the LDO regulator cannot guarantee stability, it means that it cannot provide a stable output voltage. AC stability of the proposed LDO regulator was simulated under load current conditions of 0, 100, and 300 mA. The phase margin obtained by the simulation remained 36° at 0 mA, 89° at 100 mA, and 90° at 300 mA.

B. PROPOSED ESD PROTECTION CIRCUIT

Figures 11, 12 and 13 show the cross section and layout of each ESD protection circuit. The resistance of the N/P-Well region of the cross section internal equivalent circuit and the dimensions and characteristics of the parasitic NPN/PNP bipolar transistors are provided for general information. For example, the size of a parasitic NPN/PNP bipolar transistor is determined by the area of the N/P-Well region and the spacing between the N+/P+ implant region. Also, the resistance is the resistance of the N-Well region and P-Well region and is determined by the doping concentration and the Well region. Therefore, since the resistance of each ESD protection circuit and the size of the parasitic bipolar transistor are inherent parts according to process variables, they vary depending on the layout and doping concentration of the N/P-Well region and the N+/P+ implant region.

Figure 11 shows the cross section and equivalent circuit of LVTSCR. LVTSCR is a structure using the advantages of general SCR and GGNMOS. In the SCR structure, the LVTSCR in which the N+ bridge region is additionally formed at the junction region between the N-well and the P-well performs a trigger operation by avalanche breakdown at the junction between the N+ bridge region and the P-well.

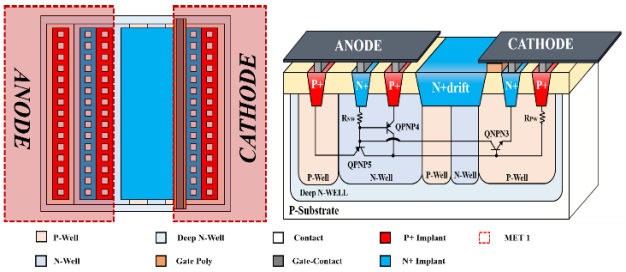

FIGURE 13. PWSCR (penta-well silicon controlled rectifier).

Also, the N+ bridge region and the N+ region are used as a drain and a source, respectively. And additionally forming a GGNMOS structure by forming a gate between the N+ regions, the base width of the parasitic NPN bipolar transistor (QNPN1) is minimized to the channel width of the NMOS transistor, resulting in a low trigger voltage. However, LVTSCR still has a low holding voltage. Due to such a low holding voltage, an unintentional ESD protection circuit operates due to overshooting or noise, and the operation of the internal circuit is fatally operated [16].

Figure 12 and 13 show cross-sections and equivalent circuits of LRSCR and PWSCR. In addition to the parasitic PNP bipolar transistor (QPNP2) and parasitic NPN bipolar transistor (QNPN2) operating in the LVTSCR structure, the LRSCR improves robustness characteristics by adding a P-well and a P+ region to additionally operate a parasitic PNP bipolar transistor (QPNP3) on the discharge path. That is, the parasitic PNP bipolar transistor (QPNP3) forms a parallel connection structure with the parasitic PNP bipolar transistor (QNPN2), and additional hole current is injected into the P-well, thereby increasing the turn-on speed and lowering the on-resistance compared to the conventional LVTSCR. Because of this, it can have high current driving capability. In addition, since the base width of the parasitic NPN bipolar transistor (QNPN2) is minimized to the channel width of the NMOS transistor having the N+ bridge region as a drain and the N+ region as a source, the trigger voltage can be reduced.

In the existing LVTSCR and LRSCR structures, the inflow of ESD surges into the anode resulted in an avalanche breakdown between the N+ region and the P-well. However, the proposed PWSCR ESD protection circuit forms an N+ drift region in contact with the Penta-well and P well to cause avalanche breakdown at the N+ drift region and P well junction when ESD surge is introduced, thereby lowering the trigger voltage and forming a long current path due to the Penta-well to have a high holding voltage. In addition, a parasitic PNP bipolar transistor (QPNP5) is formed by an N+ drift region and a P+ cathode region, an added P+ region, a parasitic PNP bipolar transistor (QPNP4) is formed by a P+ anode region, an N+ drift region and a P+ cathode region, and a parasitic NPN bipolar transistor (QNPN3) is formed by the N+ region, the P-well and the N+ region. Therefore, the proposed ESD protection circuit additionally forms a parasitic PNP bipolar transistor (QPNP5) to operate in parallel with the existing parasitic PNP bipolar transistor

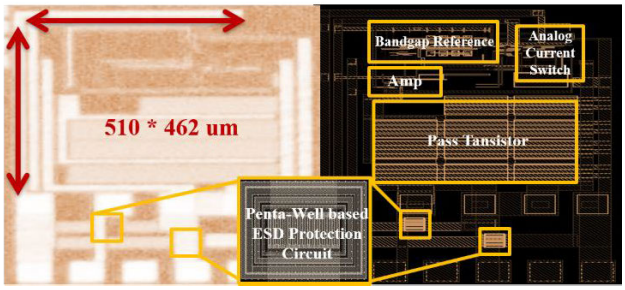

FIGURE 14. Chip layout of analog current switch structure LDO regulator including PWSCR ESD protection circuit.

(QPNP4), which lowers the on-resistance component and has high robustness characteristics.

The proposed PWSCR protection circuit has a characteristic of increasing the holding voltage by forming a long discharge path due to the P-Well and N-Well at the bottom of the N+ drift region. In addition, the length of the base of the parasitic PNP bipolar transistor is long due to the long N+ drift region, and the beta value is lowered, so the current gain is reduced and the holding voltage is increased. Therefore, it has high holding voltage characteristics by adding a penta-well structure and N+ drift region. In addition, the proposed PWSCR protection circuit induces the current flow of the parasitic PNP bipolar transistor into the N+ drift region due to the P-Well at the bottom of the N+ drift region and prevents the current from flowing to the N-Well at the bottom of the N+ drift region, made improving the current driving capability. Therefore, the proposed ESD protection circuit was built into the proposed LDO regulator and designed to operate at a voltage of 3.3V to 4.5V to secure stability and reliability [17], [18], [19], [20].

III. MEASUREMENT

A. LAYOUT OF PROPOSED LDO REGULATOR

Figure 14 shows the chip layout of the proposed LDO regulator. The size of the layout and fabricated chip is shown as 510 × 462μm. The analog current switch structure has a function of effectively controlling the peak voltage by turning on/off the required current according to the size of the load current. In addition, the proposed ESD protection circuit is configured to effectively discharge the ESD surge of mobile devices using low voltage. As a result, the ESD protection circuit of the proposed LDO regulator was built into the I/O CLAMP and POWER CLAMP to secure high reliability against ESD situations.

B. LOAD TRANSIENT RESPONSE

Figure 15 shows the transient response of an LDO regulator without an analog switch structure. It shows that an undershoot voltage of 52 mV and an overshoot voltage of 39 mV are secured when the load current is applied up to 150 mA.

The measurement results of the proposed LDO regulator show the result after the ESD zapping test. The ESD zapping test is conducted to confirm the ESD immunity of a device

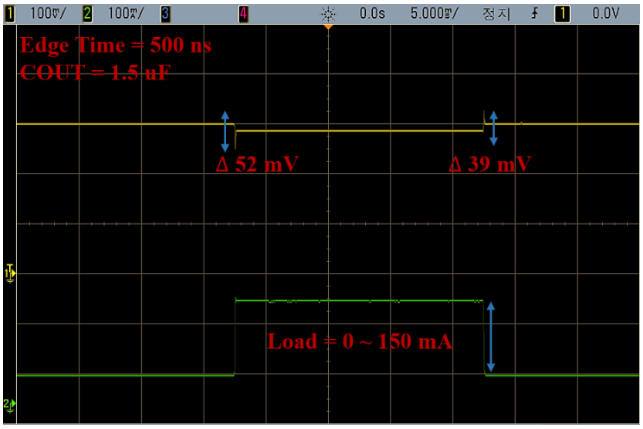

FIGURE 15. Transient response measurement result of conventional LDO regulator.

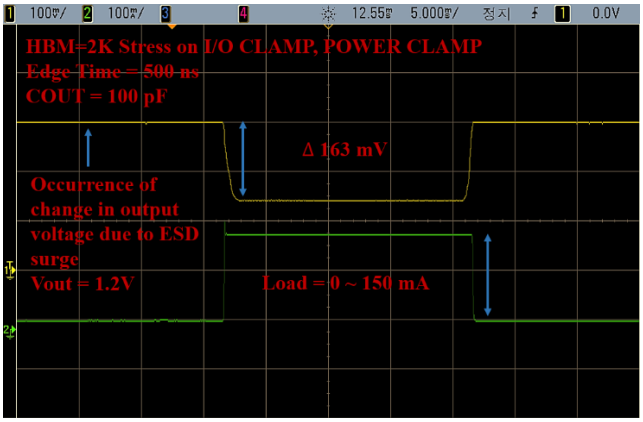

FIGURE 16. Transient response measurement result of analog current switch LDO regulator without ESD protection circuit.

or product. It is also an important test to ensure product performance and reliability because static electricity can cause product malfunction or failure. The ESD zapping test was conducted by discharging three times at interval of 1 second for each mode, and positive ESD stress was applied in the order of HBM (Human Body Model) (4K, 6K, 8K) according to each pin combination of the proposed LDO regulator. As a result, the measurement results of the LDO regulator subjected to the ESD zapping test were the same as those before the ESD zapping test, so the tolerance characteristics of the HBM 8K were secured.

Also, as shown in Figure 16, the transient response characteristics of the LDO regulator without built-in ESD protection circuit can be confirmed. It can be confirmed that an LDO regulator without a built-in ESD protection circuit cannot provide a stable voltage due to the destruction of internal elements caused by ESD surge. The output voltage of the LDO regulator due to the ESD phenomenon appeared to be 1.2 V, which fell by 1.8 V. Also, it can be confirmed that normal regulation operation is not possible due to internal device destruction.

Figure 17, 18, and 19 show the results of measuring the transient response characteristics of the proposed LDO regulator. The proposed LDO regulator has been effectively

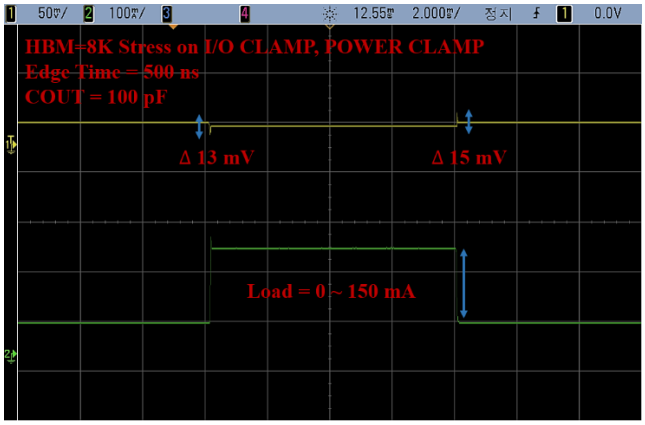

FIGURE 17. Transient response measurement result of analog current switch LDO regulator built-in ESD protection circuit.

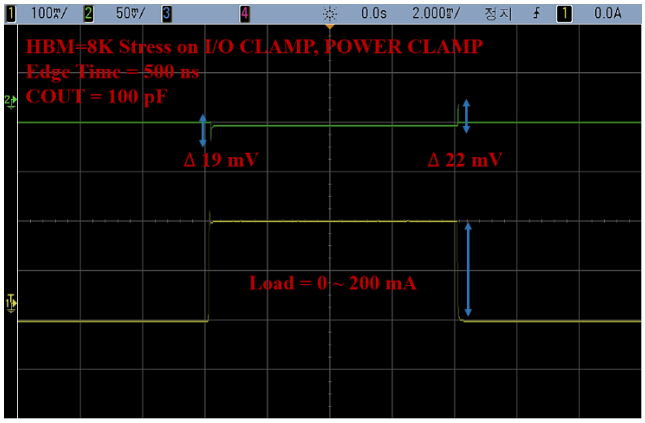

FIGURE 18. Transient response measurement result of analog current switch LDO regulator.

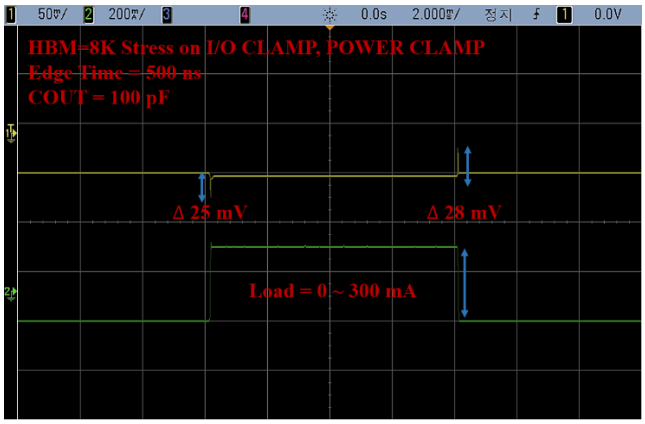

FIGURE 19. Transient response measurement result of analog current switch LDO regulator built-in ESD protection circuit.

improved by adding a function to turn ON/OFF the current using an analog switch to the peak voltage generated by the load current. Figure 17 shows that, when a load current is applied up to 150 mA, an undershoot voltage of 13 mV and an overshoot voltage of 15 mV are ensured. Also, Figure 18 shows the undershoot voltage characteristics of 19mV and overshoot voltage characteristics of 22mV when the load current is applied up to 200 mA. As shown in Figure 19,

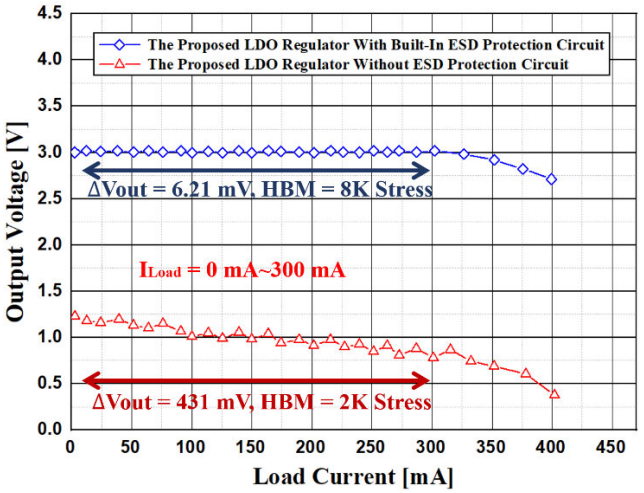

FIGURE 20. Load regulation measurement result of analog current switch LDO regulator.

an undershoot voltage of 25mV and an overshoot voltage of 28mV were ensured when the load current was applied up to 300mA. The LDO regulator including the analog current switch structure shows the peak voltage improvement of 39 mV for undershoot and 24 mV for overshoot by comparing Figure 15 and Figure 17 under the same 150 mA load current condition. In addition, it was verified that the peak voltage can be effectively controlled due to the influence of the analog current switch structure even under the condition of a large load current of 300 mA. As a result, it was confirmed that the analog switch structure of the proposed LDO regulator forms a system that can additionally turn on/off the current in addition to the existing current path and effectively controls the power supply voltage. In addition, it has been verified that the proposed LDO regulator with built-in ESD protection circuit effectively discharges ESD surge even in a large ESD situation of HBM=8K and does not affect the output voltage of the LDO regulator according to the load current.

C. LOAD REGULATION

A stable peak voltage must be secured even in the event of a momentary load current change. However, even at the moment when the load current changes constantly, it must have a stable output voltage value. As shown in Figure 20, the proposed LDO regulator ensured an output voltage change of 6.21 mV even with a constant load current change of 300mA. Therefore, the proposed LDO regulator stably ensured the output voltage value even with the load current that changes instantaneously and the load current that changes constantly. However, it has been verified that the LDO regulator without built-in ESD protection circuit does not perform normal regulation even in a small ESD situation of HBM=2K. As a result, the proposed LDO regulator with built-in ESD protection circuit effectively discharged the ESD surge even under a large ESD condition of HBM=8K, and did not affect the LDO regulator system.

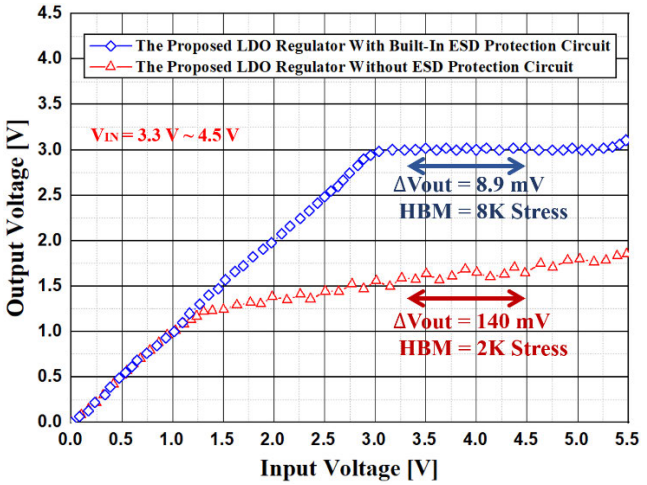

FIGURE 21. Proposed LDO regulator line regulation measurement results.

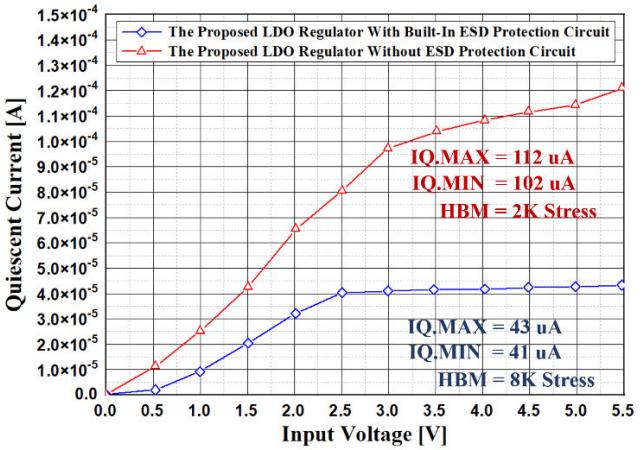

FIGURE 22. Proposed LDO regulator Quiescent Current.

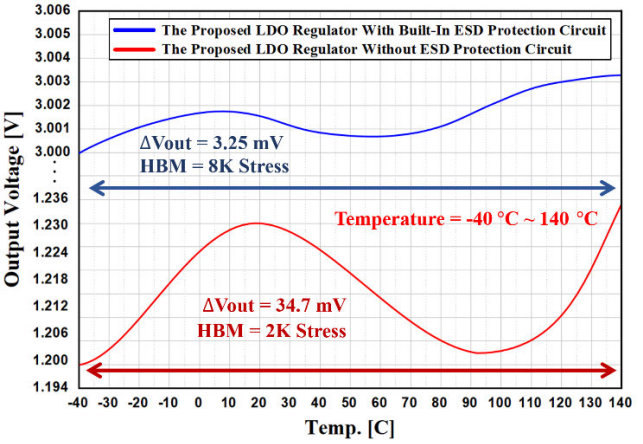

FIGURE 23. Proposed LDO regulator temperature characteristics measurement results.

D. LINE REGULATION

If the LDO regulator is sensitive to input voltage changes, it can affect the output voltage. Therefore, the LDO regulator must control the output voltage stably even with changes in the input voltage. Figure 21 shows the output voltage amount of change of the proposed LDO regulator in the 3.3V to 4.5V range. The proposed LDO regulator ensured an output voltage amount of change of 8.9 mV. However, it has been verified that the LDO regulator without built-in ESD protection circuit does not perform normal regulation even in a small ESD situation of HBM=2K. As a result, it was verified that the proposed LDO regulator with built-in ESD protection circuit stably provides an output voltage even in a large ESD situation of HBM=8K.

E. QUIESCENT CURRENT

If a large amount of current is consumed inside the system due to the limited battery capacity, problems will arise in battery use. This is because there are dozens of circuits designed in the system. Therefore, if the value of quiescent current is too large, it may cause problems in using the battery. Figure 22 presents the quiescent current of the proposed LDO regulator. It was confirmed that the quiescent current was 43μA maximum and 41μA minimum in the input voltage range of the LDO regulator. However, after a small ESD event of HBM=2K, the proposed LDO regulator without a built-in ESD protection circuit not only fails to operate normally due to internal device destruction, but also increases the quiescent current.

F. TEMPERATURE CHARACTERISTICS

Temperature characteristics are directly related to reliability. If the proposed LDO regulator reacts sensitively to the output voltage depending on the temperature change between −40°C and 140°C, a situation arises where the output voltage cannot be controlled stably. Therefore, temperature characteristics are important characteristics to ensure high reliability. Figure 23 shows the temperature characteristics results of the proposed LDO regulator. In the thermal reliability test, the measurement results were obtained using the Hot Chuck Controller to heat the wafer. The temperature characteristics of the proposed LDO regulator and ESD protection circuit were measured with a hot chuck controller. The amount of change in the output voltage of 3.25 mV was confirmed in the temperature range of −40°C to 140°C. As a result, it can be confirmed that the proposed LDO regulator ensured stable output voltage control and reliability according to temperature changes. In addition, it was verified that the LDO regulator without built-in ESD protection circuit does not provide normal temperature characteristics even in a small ESD situation of HBM=2K. As a result, it was verified that the proposed LDO regulator with built-in ESD protection circuit stably provides an output voltage according to temperature characteristics even in a large ESD situation of HBM=8K.

G. PWSCR MEASUREMENT RESULT

The I-V curve shown in Figure 24 shows the results measured using TLP (Transmission Line Pulse) to verify the electrical characteristics compared to the LVTSCR, LRSCR, and the proposed PWSCR ESD protection circuit. To optimize the proposed LDO regulator, the ESD design window must

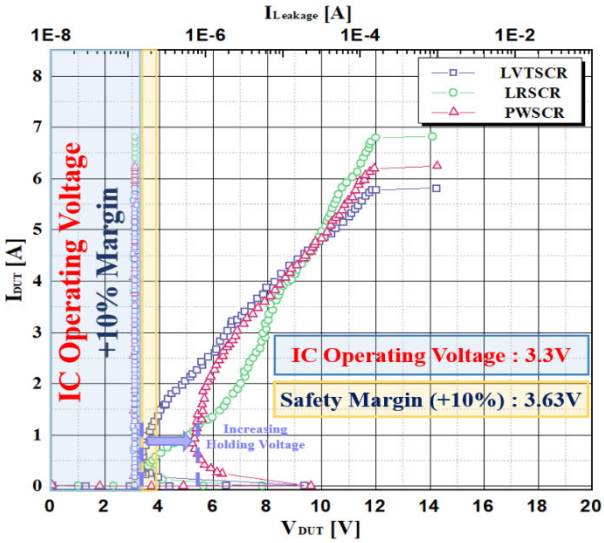

FIGURE 24. TLP I–V characteristics curves of conventional LVTSCR, LRSCR and the proposed PWSCR ESD protection circuit.

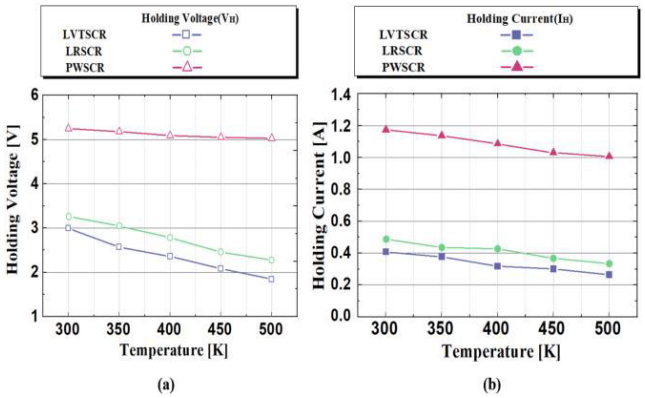

FIGURE 25. High temperature (300∼500K) of proposed LVTSCR, LRSCR and proposed PWSCR ESD protection circuit (a) Holding voltage (b) Holding current.

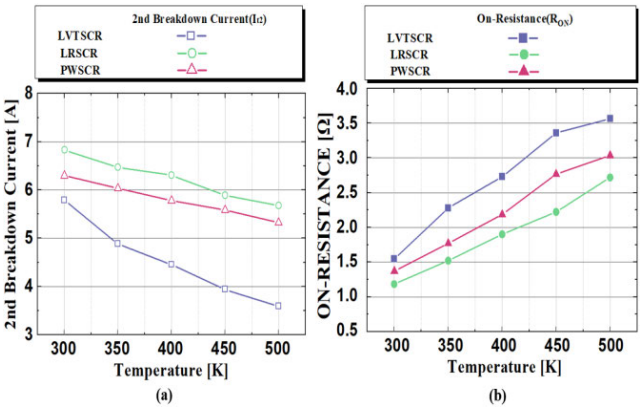

FIGURE 26. High temperature (300∼500K) of proposed LVTSCR, LRSCR and proposed PWSCR ESD protection circuit (a) Second breakdown current (b) On-resistance.

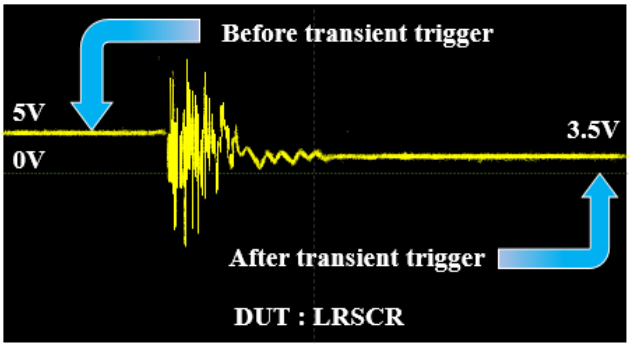

FIGURE 27. TLU measured voltage waveform for the LRSCR.

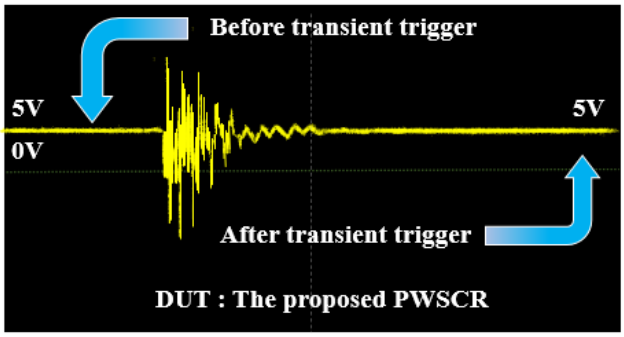

FIGURE 28. TLU measured voltage waveform for the proposed PWSCR.

exceed the maximum operating voltage of the proposed LDO regulator of 3.63V (3.3V + 10% margin). LVTSCR and LRSCR holding voltages of 3.06V and 3.24V, respectively, may invade the operating range of the proposed LDO regulator and cause issues such as latch-up. Since the proposed PWSCR ESD protection circuit has a trigger voltage of 9.76V and a holding voltage of 5.18V, it exhibits a very improved holding voltage, which is suitable for the proposed LDO regulator and can increase reliability by making the proposed regulator operate stably.

Figure 25 and 26 show the results of the thermal reliability test at high temperature (300-500K) of the LVTSCR, LRSCR and the proposed ESD protection circuit. In the thermal reliability test, a hot chuck controller system was used to heat the wafer containing the ESD protection circuit. High-temperature characteristics, which are essential for ensuring thermal reliability, are very important because they greatly affect the ESD protection circuit and It2 (Second Breakdown Current) and the electrical characteristics of the circuit. In addition, as the temperature increases, the base-emitter voltage (VBE) of the parasitic NPN/PNP bipolar transistor decreases, reducing its holding voltage. In addition, as the temperature increases, the heat loss due to the on-resistance of It2 increases and It2 decreases. Looking at the measurement results, at a temperature of 500K, the conventional LVTSCR has a holding voltage of 1.84V and a secondary trigger current of 3.59A, and the LRSCR has a holding voltage of 2.27V and a secondary trigger current of 5.69A. Meanwhile, the proposed PWSCR ESD protection circuit has a holding voltage of 5.027V. The secondary trigger current is still as high as 5.39A, which proves that the proposed ESD protection circuit has excellent thermal reliability and high-temperature characteristics compared to existing LVTSCR and LRSCR.

TABLE 1. Performance comparison of proposed LDO regulators and conventional LDO regulators.

Measurement	This work	[1]	[2]	[3]	[4]	[5]	[6]	[7]	[8]	[9]
Technology (μm)	0.13	0.35	0.35	0.13	0.18	0.18	0.065	0.18	0.18	0.13
Supply Voltage(V)	3.3-4.5	2.3-3.3	3.7	1.2-1.5	1.8	1.2-1.8	0.75-1.2	1.2-1.8	1.4-1.8	1.2-1.5
Output Voltage (V)	3	1.2-2.5	3.25	1	1.2	1	0.55	0.8-1.6	1.2-1.6	1
Load Current: I_{MAX} (mA)	300	1	50	50	10	100	50	100	300	100
Quiescent Current (μA)	43	0.25	26	42	265	0.6-6.9	15.9-487	10.2	0.94-255	6.2
Load Transient (I_{LOAD} Rising) (mV)	25	160	200	140	76	388	113	190	123	234
Load Transient (I_{LOAD} Falling) (mV)	28	93	146	80	44	200	29	200	39	170
Load Regulation (mV)	6.2	1.8	-	0.5	40	1	9	8.1	30	-
Line Regulation (mV)	8.9	0.17	-	0.09	-	3	1.8	-	2.132	-
COUT (pF)	0-100	0-1E3	100	0-400	no limit	0-100	470-1E4	0-100	1E6	0-1E6
Edge time (ns)	500	76	100	100	50	100	100	100	1.92E4	1E3
FOM (V)	2.01E-12	3.04E-12	1.04E-11	1.18E-11	1.01E-10	2.68E-12	1.1E-10	2.04E-12	2.01E-09	1.45E-11
Year	2022	2015	2016	2019	2015	2022	2014	2018	2020	2021

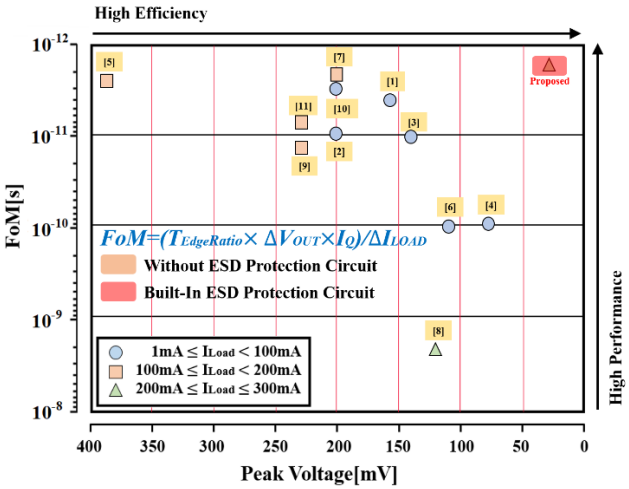

FIGURE 29. Performance and efficiency comparison of proposed LDO regulators and conventional LDO Regulators.

Figure 27 and 28 show TLU (Transient Latch-Up) test results to verify the transient latch-up immunity of the LRSCR and the proposed PWSCR ESD protection circuit. The power supply was connected to a 5V DC voltage corresponding to the operating voltage of the internal circuit. The power supply was connected to a 5V DC voltage corresponding to the operating voltage of the internal circuit of the same node, and the voltage waveform of the subject to be tested was observed through an oscilloscope using a charged capacitor at the anode to reproduce the ESD pulse. According to the TLU experiment results, as shown in Figure 27, due to the low holding voltage of 3.24V of LRSCR, it pulls down to 3.5V. However, as shown in Figure 28, since the holding voltage of the proposed PWSCR is 5.18V, the latch-up immunity was verified as the supply voltage returned to 5V after operation.

Table 1 shows the performance and efficiency comparisons between the proposed LDO regulator and the conventional LDO regulator.

Also, Figure 29 shows the peak voltage and FoM (Figure of Merit) of the LDO regulator having the proposed analog current switch structure. The proposed LDO regulator and the conventional LDO regulator were compared with FoM values. Also, the proposed LDO regulator is the only one with a built-in ESD protection circuit. The proposed LDO regulator secured high reliability for ESD situations at the IC level. As a result, it can be confirmed that the proposed LDO regulator can effectively control the output voltage by configuring an analog current switch structure as shown in Figure 29.

IV. CONCLUSION

It has been verified that the proposed LDO regulator not only secures high reliability with a built-in ESD protection circuit, but also can control stable output voltage even with a large load current. Depending on the load current, additional current supply and discharge paths were formed at the gate node of the pass transistor and the output voltage of the system. Due to the operation of the analog current switch structure, it turns ON/OFF according to the load current, providing an effective supply and discharge path of additional current. As a result, the proposed LDO regulator effectively controlled a large load current change of 300 mA using an analog current switch structure. The ESD protection circuit continue to be used as individual elements. However, the most important topic of ESD protection circuit is to protect IC from ESD situation. Therefore, in this paper, when an ESD situation occurs depending on the presence or absence of an ESD protection circuit, it is confirmed that the output voltage of the LDO regulator does not operate normally, and at the same time, unstable operation due to device damage. As a result, through the LDO regulator with a built-in ESD protection circuit, not only the effective voltage control of the LDO regulator but also the high reliability of the circuit from ESD conditions were verified [21]. The proposed LDO regulator is designed

to ensure reliability at the IC level by embedding an ESD protection circuit with a penta-well structure. The proposed LDO regulator with an analog current switch structure is designed for 5 V applications. In addition, the proposed LDO regulator based on 0.13 μm BCD process was verified for high reliability by embedding an ESD protection circuit of penta-well structure in I/O CLAMP and POWER CLAMP.

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