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RESEARCH ARTICLE

A Single-Source Switched-Capacitor 13-Level High Gain Inverter With Lower Switch Stress

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ABSTRACT A switched-capacitor based 13-level inverter with high gain and reduced switch stress is presented in this article. The 13-level single-phase ac output voltage is achieved with a voltage gain of 6 by utilizing a single dc source, 14 switches, 3 capacitors and 1 diode in the proposed converter. Self-voltage balancing is achieved for different types of loads without the use of complicated control schemes or supplementary circuitry. The proposed topology can generate negative polarity without a back-end H-bridge. Consequently, voltage stresses across the switches are reduced. The voltage stress across the switches is limited to 4 times the input DC voltage. Included also is an analysis of power loss for several components of the proposed converter. A comparison is made with contemporary topologies that require a single dc source at the input in terms of several performance characteristics. Resistive (R) and resistive plus inductive (R-L) loads are simulated in this study. To demonstrate the effectiveness of the suggested converter, a laboratory prototype is constructed. In order to demonstrate the viability of the suggested arrangement, the experimental results for step variation in load demand and variation in modulation index under practical loading situations are obtained.

INDEX TERMS Multilevel inverters, nearest level modulation, switch stress, switched capacitor, single source, microgrid, electric vehicle.

I. INTRODUCTION

For power conversion in renewable energy generation systems (REGS) like solar (PV), fuel cell, and wind turbine installations, multilevel inverters (MLIs) have become increasingly popular. Since their introduction, MLIs have become progressively common among high ac power distribution, microgrids, flexible ac transmission system devices (FACTS), uninterruptible power supply (UPS) systems, and electric vehicles due to their ability to improve power quality, efficiency, operating voltage, dv/dt, switch stress, and harmonic profile. The primary objective of the MLI is to provide an output voltage with characteristics more similar to a sine wave. Using a DC voltage source and a large number of adequately coupled and controlled switching devices, the required voltage waveform can be generated. On the basis of the connection arrangement of switching devices, numerous MLIs have been published [1], [2], [3].

The three MLI topologies that are used the most frequently are the diode-clamped MLI, the cascaded H-bridge (CHB) MLI, and the flying capacitor (FC) MLI. Traditional MLIs have many drawbacks, one of which is the requirement for additional components, such as clamping diodes in diode-clamped MLIs, flying capacitors in FC-MLIs, and additional dc sources in CHB-MLIs. Traditional MLIs also have a number of other drawbacks. Conventional MLIs, such as

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diode clamped and FC-MLI, do not have voltage boosting characteristics, which necessitates the use of complex control techniques for the purpose of balancing the capacitor voltage [4], [5], [6].

A variety of activities are currently under way in order to generate high voltage levels with fewer parts, fewer dc sources, and the capability to self-balance and boost voltage. This is being done in an effort to meet the aforementioned goals. Capacitors, which have been garnering a lot of attention as of late due to their growing prevalence as an approach to the generation of intermediate levels. In the hybrid MLI, flying capacitors, often known as FCs, are an essential component in the process of producing intermediate voltage levels. It is necessary to utilize intricate control circuitry in order to keep the voltages of the capacitors at a constant level. Also, the voltage that is present at the load terminals is only fifty percent of the voltage that is present at the source terminals. In order to raise the output voltage in a manner that does not involve the use of inductors or transformers in proximity to the output terminals, additional research is being conducted. Because these generators normally produce electricity at low voltages, switching capacitor-based voltage boost designs are preferred for the purpose of generating suitable voltage for low or medium-voltage applications. This is because these designs allow the voltage to be increased gradually. In these arrangements, connecting the capacitor to the isolated dc voltage source in parallel charges the capacitor, whilst connecting it to the source in series discharges it. When multiple switched-capacitor modules are connected in series with one another, the magnitude of the output voltage increases [7], [8], [9], [10].

In 1989, Marusarz was the first person to present the concept of a switched capacitor to the public [11]. Since that time, numerous new designs for MLIs based on switched capacitors have been presented, each of which comes with its own unique set of advantages and disadvantages. Switched capacitor MLIs, or SCMLIs for short, are a form of MLI that may provide a higher sinusoidal output voltage using a less number of power supply components than conventional MLIs. In the SCMLI, capacitors are utilized as a different kind of dc source. It is not required to use any additional circuits or complex control algorithms in order to achieve voltage balancing using the capacitors [12], [13], [14], [15], [16], [17], [18].

Taking the thirteen level (13L) topologies with a single dc source into consideration, the authors in [15] proposes a novel K-type 13L SCMLI topology with fourteen switches and four capacitors; however, the voltage gain is only 1.5 and the total standing voltage (TSV) is also high. The authors of [19] can generate the necessary levels with a voltage gain of six. The voltage stress across all 29 switches is limited to the input voltage, despite the high number of switches. The 13L topology presented in [20] has limited the voltage stress across the switches to 4 times the input voltage using 14 switches, but the voltage gain is 3 and the number of capacitors required is also higher at 4. Using 15 switches and 3 capacitors, topology presented in [21] demonstrated a 13L inverter with a maximum switch stress equal to 3 times the input voltage. By using fifteen switches, authors in [22] have presented a six times boosted 13L inverter. The number of switches is further reduced to thirteen in [23], [24], and [25] with a gain of six, and the maximum switch stress is six times the input voltage. The maximum switch stress increases as the number of switches are reduced.

Thus, switch stress, number of switches, number of capacitors and their ratings, and voltage gain, all play an important role for optimal selection of a converter in a particular application. Keeping these points in view a high gain inverter with low switch stress is proposed in this article. The major contribution of the proposed topology and modulation method are as follows.

- The proposed topology utilizes only one dc source, 14 switches, one diode and 3 capacitors for its operation at a voltage gain of 6.
- Three pairs of the switches are complementary, thus reducing the number of driver circuits and complexity.
- Voltage stress across the switches is limited to 4 times the input voltage.
- Since the proposed topology is self-balancing, no additional sensor circuits or capacitor voltage balancing methods are required.
- It also has inductive load ability. These features make it suitable for low-voltage source applications such as PV and fuel cells.

The circuit configuration, its working operation, and capacitors' self-voltage balancing are discussed in Section II. Nearest Level Control (NLC) technique is presented in Section III. Comparison of the proposed topology with the state-of-the-art topologies is presented in section IV. Section V discusses the power loss analysis. Simulation and experimental results for different loading conditions are discussed in section V. Finally, Section VI concludes this article.

II. PROPOSED 13L SCMLI TOPOLOGY

This section discusses the circuit diagram of the proposed 13 level inverter, its working principle, and capacitor self-voltage balancing.

A. CIRCUIT DESCRIPTION

The circuit diagram of the proposed topology is shown in Fig. 1 (c). It is derived from the topologies presented in [5] and [26] as shown in Fig. 1 (a) and Fig. 1 (b). The dc supply used in [25] is replaced with the SPSC Unit-I [27]. It consists of a single dc sources, 12 unidirectional switches (S_1-S_{12}) out which 2 are reverse blocking (S_7, S_8), 1 bidirectional switch (S_{13}), 3 capacitor (C_1, C_2, C_3), and 1 diode. The switch pairs (S_1, S_2), (S_9, S_{10}), and (S_{11}, S_{12}) are complementary to each other, thus reducing the control complexity and reducing the number of drivers. Capacitor C_1 is charged to V_{dc}(input supply), by only switching ON S_4, as C_1 comes in parallel to dc source through the diode. Capacitors C_2 and C_3 are charged to $2V_{dc}$ by adding the voltages of charged capacitor

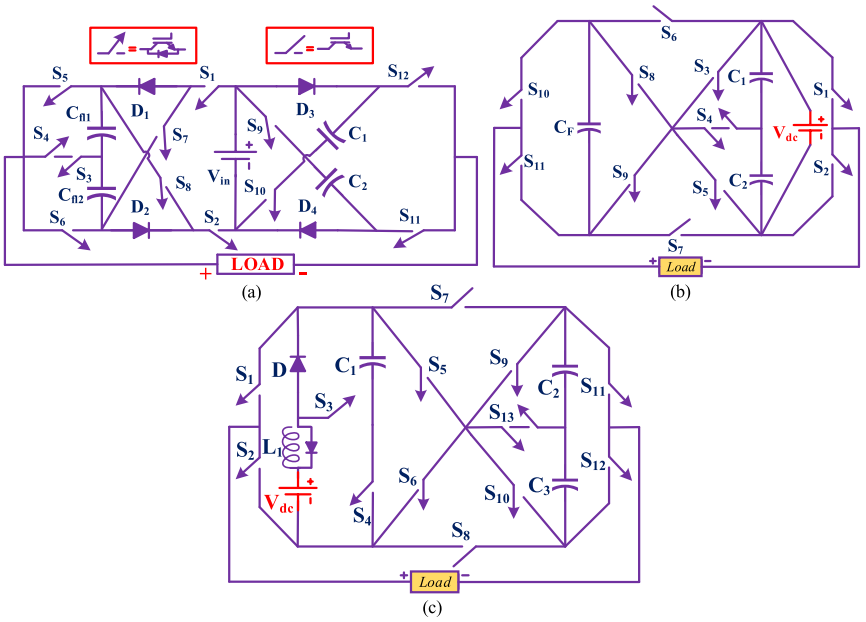

FIGURE 1. Circuit topology (a) presented in [5] (b) presented in [26] (c) proposed 13L SCMLI.

C_1 and dc source. Thus 13 output levels are generated with a peak voltage of $6V_{dc}$. Keeping in mind that the suggested topology has a voltage gain of 6, the maximum blocking voltage that may be applied across the switches is restricted to being no more than four times the input voltage. This is one of the merits of the proposed topology.

B. WORKING PRINCIPLE AND CAPACITOR SELF-VOLTAGE BALANCE

The following section discusses the working of the different operating states of the proposed 13L topology. Fig. 2 and Table 1 demonstrate the conduction paths for positive levels and the switching states for all the 13 levels of the topology. Taking positive levels into consideration,

0^{th} *level* ($0V_{dc}$) : The load terminals are shorted through the switches S_1, S_7, and S_{11} as shown in Fig. 2 (a).

1^{st} *level* ($+V_{dc}$) : Voltage across C_1, V_{dc} is reflected at the output by turning ON the switches S_1, S_4, S_6, S_9 and S_{11} as shown in Fig. 2 (b). In the same state charging of capacitor C_1 also takes place through diode and S_4.

2^{nd} *level* ($+2V_{dc}$) : In the second state, voltage across C_1, V_{dc} and dc source is added and is reflected at the output by turning ON the switches S_1, S_3, S_8, and S_{12}. In this state, capacitor C_3 is also getting charged by turning ON the switch S_5, and S_{13} as shown in Fig. 2 (c). Turning ON S_5, and S_{13} also helps in providing reverse current path in case of inductive loading.

3^{rd} *level* ($+3V_{dc}$) : The voltage across C_1 and C_3 are added in series by turning ON S_1, S_4, S_6, S_{12}, and S_{13}, thus delivering $3V_{dc}$ at the output. C_1 is also being charged as switch S_4 is ON.

4^{th} *level* ($+4V_{dc}$) : In this level, voltage across C_1 and C_2 are added in series with the dc source delivering $4V_{dc}$ at the output via the switches S_1, S_3, S_6, S_{12}, and S_{13}. S_7 is also turned ON in order to provide path for charging of C_2.

5th level: Here, capacitors C_1, C_2 and C_3 are in series through the switches S_1, S_4, S_6, S_9, and S_{12}, thus delivering $5V_{dc}$ at the output. C_1 is also getting charged in this level as S_4 is in ON state.

6^{th} *level:* In this level, C_1, C_2 and C_3 are in series with the dc source through the switches S_1, S_3, S_6, S_9, and S_{12}. Thus, output voltage of $6V_{dc}$ is obtained as shown in Fig. 2 (g).

In a similar manner, it is possible to quickly visualize all 13 switching states by using the switching table that is presented in Table 1. One of this configuration's strengths is that it has a voltage gain of 6, since input dc source is of voltage V_{dc} and the maximum output voltage is $6V_{dc}$. When designing an MLI topology, one of the most significant factors to take into account is the voltage stress across switches which also affects the total standing voltage, abbreviated as TSV. It is defined as the aggregate of the highest voltage stress that develops across the switch at each and every output level. Switches S_3, and S_4 are experiencing maximum voltage stress of V_{dc}, while switches S_1, S_2, S_5, S_6, and S_{13} withstand voltage stress of $2V_{dc}$, and the voltage stress across the switches S_7-S_{12} are $4V_{dc}$ as shown in Fig. 3. Voltage stress across all the switches for all the thirteen levels are demonstrated in Fig. 3 with the help of stacked 3D bar graph. The sum of all switch stresses, regardless of level, never exceed $21V_{dc}$. TSV of the proposed topology is $34V_{dc}$, and TSV_{pu} is 5.67 (34/6).

The voltages of all the three capacitors are self-balanced to the appropriate levels when they are connected in parallel to the source and in series with the load at separate times. This allows the capacitors to maintain their required voltage levels. Because both the time constant and the total parasitic resistance of the charging loops are relatively low, there is

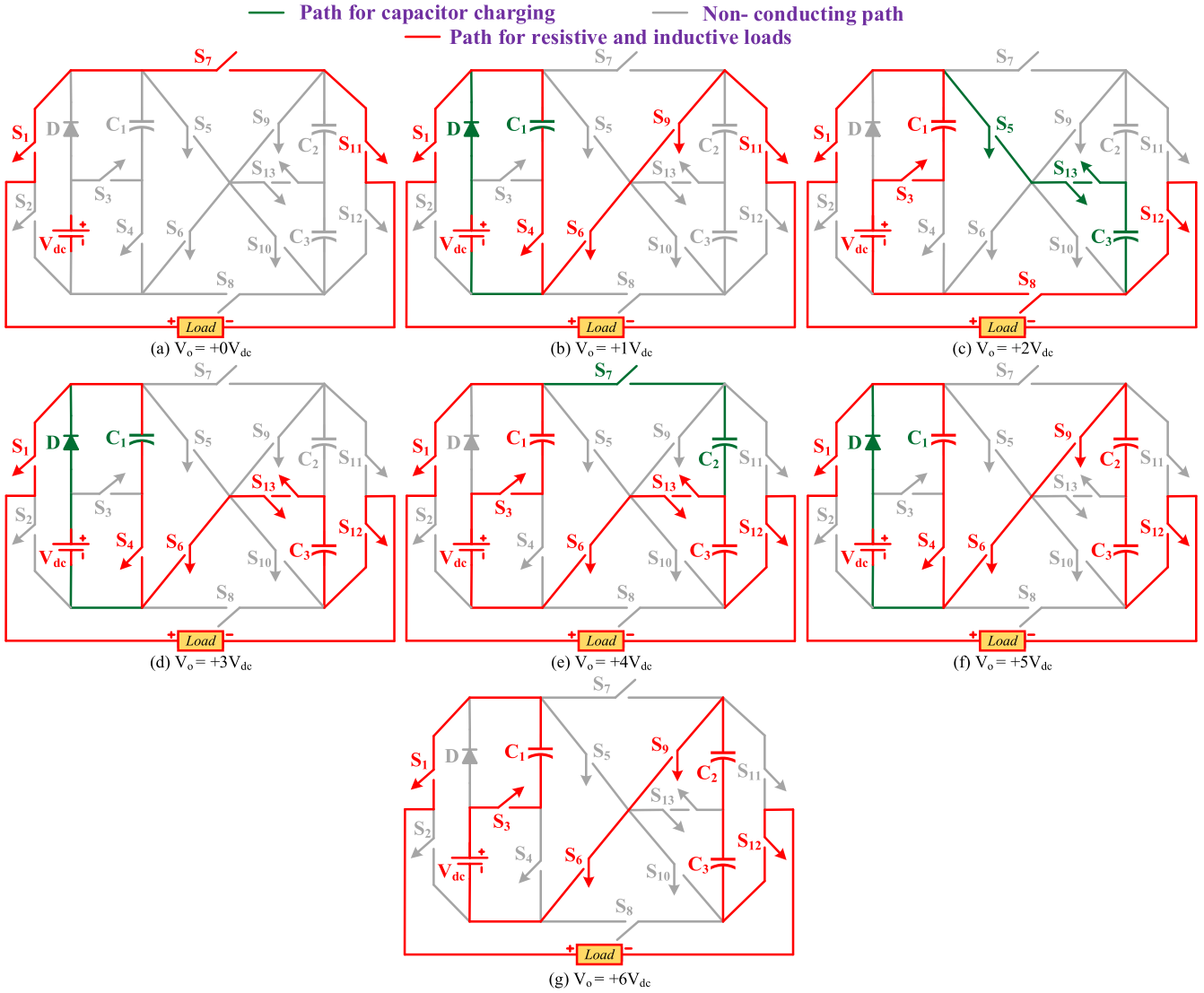

FIGURE 2. Conduction state for all the positive states.

TABLE 1. Switching states for the proposed 13L topology.

S_1	S_2	S_3	S_4	S_5	S_6	S_7	S_8	S_9	S_{10}	S_{11}	S_{12}	S_{13}	C_1	C_2	C_3	V_o ($*V_{dc}$)
1	0	1	0	0	1	0	0	1	0	0	1	0	D	D	D	+6
1	0	0	1	0	1	0	0	1	0	0	1	0	C	D	D	+5
1	0	1	0	0	1	1	0	0	0	0	1	1	D	C	D	+4
1	0	0	1	0	1	0	0	0	0	0	1	1	C	N	D	+3
1	0	1	0	1	0	0	1	0	0	0	1	1	D	N	C	+2
1	0	0	1	0	1	0	0	1	0	1	0	0	C	N	N	+1
1	0	0	0	0	0	1	0	0	0	1	0	0	N	N	N	+0
0	1	0	0	0	0	0	1	0	0	0	1	0	N	N	N	−0
0	1	0	1	1	0	0	0	0	1	0	1	0	C	N	N	−1
0	1	1	0	0	1	1	0	0	0	1	0	1	D	C	N	−2
0	1	0	1	1	0	0	0	0	0	1	0	1	C	D	N	−3
0	1	1	0	1	0	0	1	0	0	1	0	1	D	D	C	−4
0	1	0	1	1	0	0	0	0	1	1	0	0	C	D	D	−5
0	1	1	0	1	0	0	0	0	1	1	0	0	D	D	D	−6

*C-Charging, D-Discharging, N- No change

always enough time for the capacitors to get fully charged regardless of the voltage level. For evaluating the optimum value of capacitors, the longest discharging time (LDT) of the capacitors is to be calculated [2], [28], [29]. The total

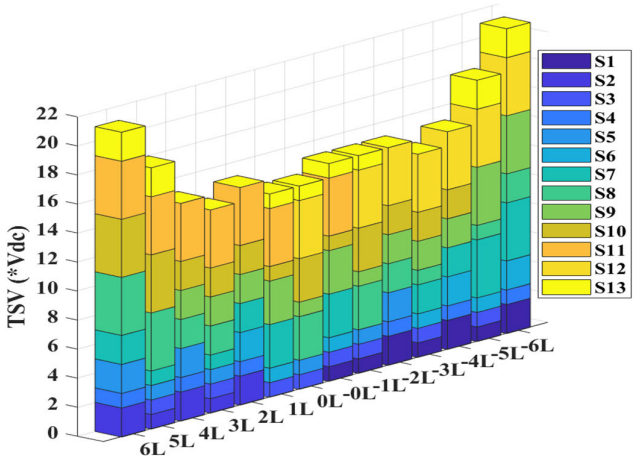

FIGURE 3. Voltage stresses on different components for each levels.

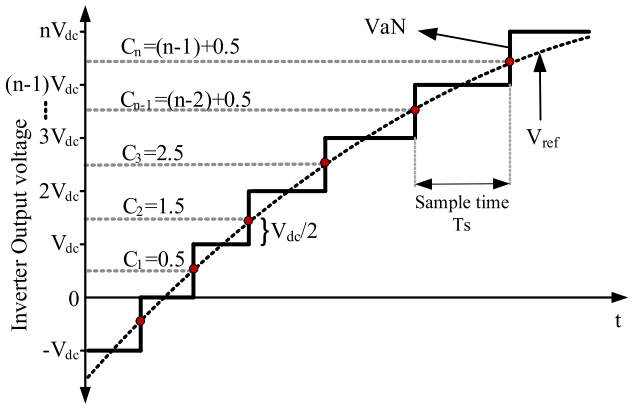

FIGURE 4. Nearest level control waveform synthesis.

discharge of capacitor C during the LDT interval $[t_1, t_2]$ is computed using the following formula,

$$\Delta Q_C = \frac{1}{2\pi f} \int_{t_1}^{t_2} i_L(t)\, dt \tag{1}$$

where f represents the output voltage frequency, and i_L is the load current. From equation (1), the value of capacitance can be calculated as,

$$C = \frac{1}{2\pi f * \Delta V_C} \int_{t_1}^{t_2} i_L(t)\, dt \tag{2}$$

III. NEAREST LEVEL MODULATION

In the case of multilevel inverters, a wide variety of modulation strategies have been researched, evaluated, and implemented. In high-power applications, the most recommended modulation techniques include optimal switching, selective harmonic elimination (SHE), and nearest level control (NLC). In the SHE approach, nonlinear transcendental equations are used analytically to minimize lower-order harmonics. The trigonometric terms of the equation yield many

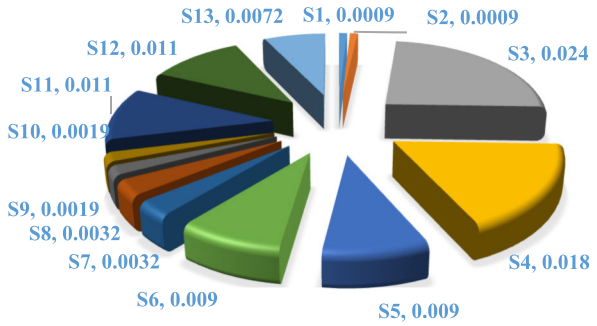

FIGURE 5. Switching loss distribution for different components.

sets of alternating angles. The most challenging component of SHE is the solution of transcendental equations due to their complexity. In order to discover the optimal switching angles in open loop systems, these equations can be solved using various soft computing techniques. However, implementation in closed loop applications is extraordinarily difficult. In applications involving high voltage, the nearest level control methods are utilized. The NLC technique is applied in this case as part of the proposed design in order to control the switches and produce the output waveform that is required. The objective is to implement the NLC method in an inverter with a large number of levels so as to reduce and simplify the processor's calculation. The NLC method's operational mechanism is depicted in Fig. 4. A sampled waveform is generated by making a comparison between a reference sinusoidal waveform and the waveform that is intended for output. The resulting waveform is then rounded off to the nearest level and compared using the switching logic shown in Table 1, in order to generate switching signals for the respective IGBTs.

IV. COMPARATIVE ANALYSIS

In this section, a comparison is made between the proposed 13 level SCMLI topology and various SCMLI configurations reported in the literature having one dc source. The comparison is conducted with respect to parameters such as N_{sw} = number of switches, N_{dd} = number of discrete diodes, N_{dr} = number of gate drivers, G= voltage gain, N_c = number of capacitors, N_T = total number of components, TSV_{pu} = total standing voltage per unit, TCV = total capacitor voltage, MBV= maximum blocking voltage, VRC = voltage rating of capacitors, η = efficiency, THD = total harmonic distortion. The Table 3 shows the comparison of the proposed topology with existing single source 13 level state-of-the-art topologies.

The total number of components (switches, gate drivers, diodes, capacitors) utilized in [6], [24], [30], and [31] is lesser than the proposed topology. However, the maximum blocking voltage of the switch is 6 in [30] compared to 4 in the proposed topology and the voltage gain of [6] is 3, while for the proposed topology it is 6. Also, TCV of the topology presented in [31] is 8 with two of the capacitors

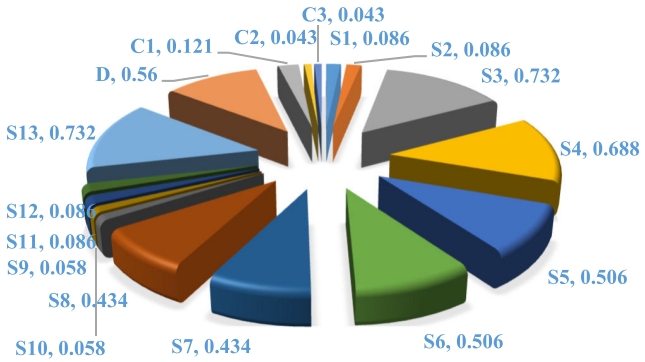

FIGURE 6. Conduction loss distribution for different components.

having a voltage rating of $3V_{dc}$. The voltage gain of the proposed topology and the topologies presented in [19], [21], [22], [23], [24], [25], [30], [31], [32], and [33] is 6, while rest of the topologies have a voltage gain of 3. In [30], two pair of capacitors having a voltage rating of V_{dc} and $3V_{dc}$ are required having total capacitor voltage of 8, while the proposed topology requires one capacitor with voltage rating of V_{dc} and two capacitors with a voltage rating of $2V_{dc}$, thus having total capacitor voltage of 5. The total capacitor voltage of the topology presented in [6] is lowest at 2. The proposed topology has a TSV_{pu} of 6, which is in line with existing topologies. TSV_{pu} is the ratio of the total standing voltage to the maximum output voltage. The output voltage THD of the proposed topology is also lowest at 5.27%, only after [5] which has an output voltage THD of 4.2%. Only one diode is used in the proposed topology. Lesser number of diodes helps in providing paths for reverse current in case of inductive loading. Topologies in [5] and [30] have four diodes, while [32] has 3 diodes. The efficiency of the proposed inverter is also maximum compared to other topologies at 97.4%. Thus the proposed topology performs better in respect to most of the topologies taken for comparison in Table 2. Cost function (CF) defined in [25] is slightly modified to take into consideration of the voltage gain by taking TSV_{pu},

$$CF = \frac{\left(N_{sw} + N_{dr} + N_{dd} + N_c + TSV_{pu} + TCV\right)}{13} \tag{3}$$

The lowest CF is 2.82 for the topology presented in [6], while it is 3.23 for the proposed topology, which is comparable to other topologies listed in Table 2.

V. POWER LOSS ANALYSIS

The switching loss is incurred by the non-ideal behavior of the switching devices and can be computed using a linear approximation of the voltage and current during the turn-on and turn-off periods [5], [8]. The switching losses of the active switches can be obtained as,

Switching loss during turn-off,

$$P_{S,on,k} = f\int_0^{t_{on}} v\,(t)\,i\,(t)\,dt = \frac{1}{6} f V_{s,k} I_{on} t_{on} \tag{4}$$

Switching loss during turn-off,

$$P_{S,off,k} = f\int_0^{t_{off}} v\,(t)\,i\,(t)\,dt = \frac{1}{6} f V_{s,k} I_{off} t_{off} \tag{5}$$

where I_{on} and I_{off} are the currents flowing through the k^{th} switch during turn-on and before turn-off, respectively, f is the switching frequency, and $V_{s,k}$ is the voltage stress across the k^{th} switch. The switching loss of all the fourteen switches may be calculated by multiplying the number of ON (N_{on}) and OFF (N_{off}) switching states in a cycle with (2) and (3) respectively, yielding (4):

$$P_S = \sum_{k=1}^{14}\left(\sum_{m=1}^{N_{on}} P_{S,on,km} + \sum_{m=1}^{N_{off}} P_{S,off,km}\right) \tag{6}$$

The t_{on} and t_{off} are related to the switch used, whereas $V_{s,k}$ is dependent on the inverter circuit design. The proposed topology has lower switch stress restricted to four times the input voltage, thus reducing the switching loss. Also, N_{on} and N_{off} are low for the proposed topology as S_1 and S_2 are either switched OFF or ON in a complete half cycle, and other switches (S_9, S_{10}, S_{11}, S_{12}) also have lesser number of switching, resulting in reduced switching loss.

Conduction loss is mostly caused by the on-state resistances and the forward voltage drop across the devices in the load current route [34], [35]. When the load current reaches its maximum value, the voltage stress across the switches and the conduction loss both peak to their extremes. The number of conducting devices in the highest level should be kept low to reduce this impact. According to the proposed topology, the number of conducting devices in the 6^{th} level is 5, which is lower than the other topologies. So, the proposed topology is more efficient now that these two major losses have been minimized. The power loss in the converter's various parts has been calculated using the Plecs software. Capacitor ESR (equivalent series resistance) losses are also included in conduction loss by taking internal resistance of 0.1 ohm [36], [37]. Resistive loading (R=100Ω) is used to calculate the total power loss of the proposed MLI across all switches. Conduction loss and switching loss together account for the entire power loss. The switching loss distribution of various components at an output power of 200W is shown in Fig. 5. The conduction loss distribution of various components for the same power is shown in Fig. 6. The total switching loss amounts to 0.1012W, while the total conduction loss amounts to 5.259W. The total loss at 200W is 5.34W, which gives an efficiency of 97.4%. Efficiency is thus obtained by using the formula,

$$\eta = \frac{output\ power}{output\ power + losses} \times 100\% \tag{7}$$

VI. SIMULATION AND EXPERIMENTAL VALIDATION

This section discusses the simulation study and experimental validation of the proposed topology.

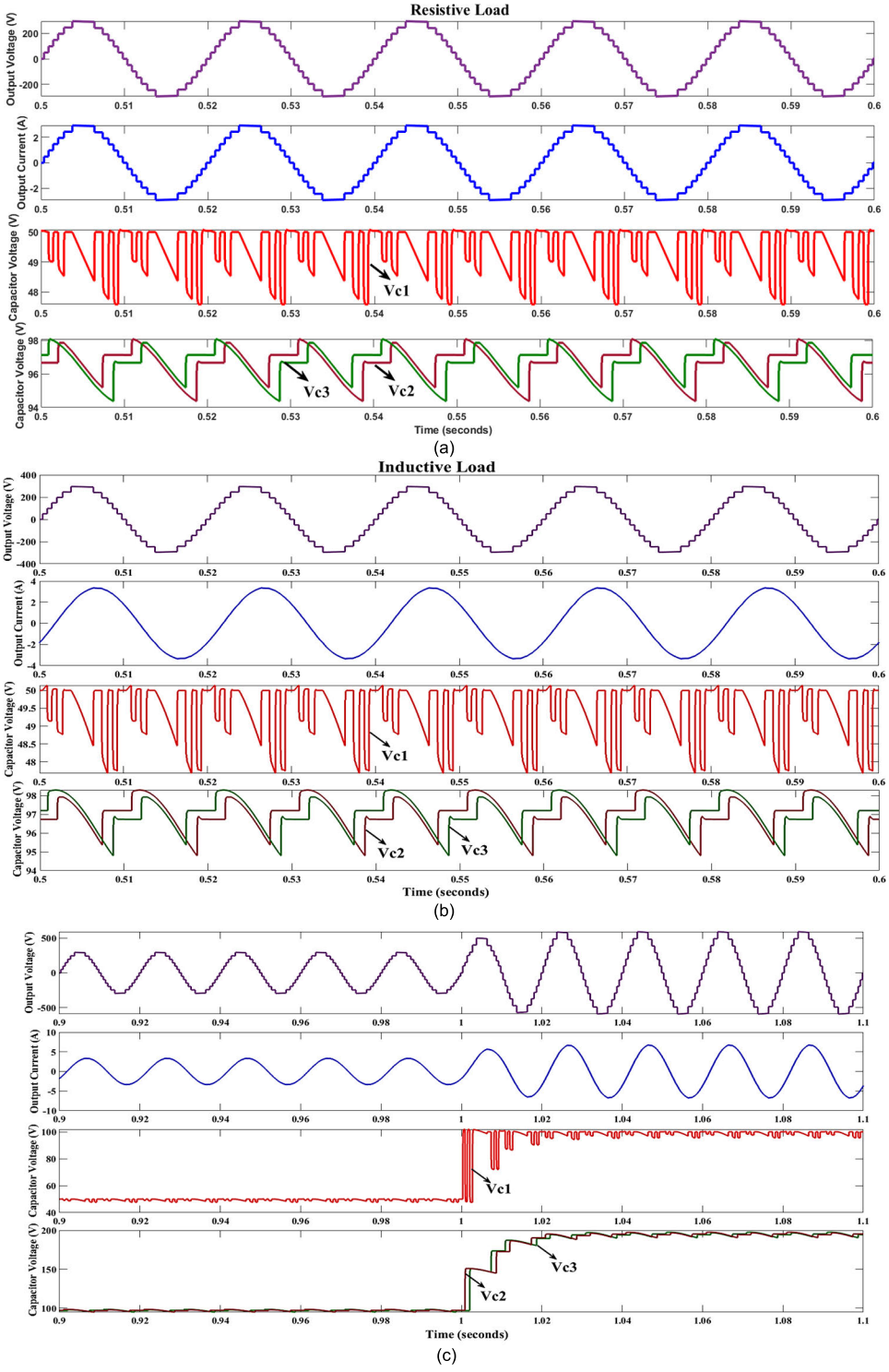

FIGURE 7. Simulation results of the proposed topology. Output voltage, output current and capacitor voltages for (a) resistive load (b) inductive load (c) sudden change in supply voltage, Output voltage, capacitor currents and input source current (d) without inductor (e) with inductor.

A. SIMULATION RESULTS

A model of the thirteen-level inverter is built in MATLAB/Simulink using the values from Table 3 to validate and investigate the effectiveness of the proposed inverter. It is presumed that the switches are real. The simulated output voltage, current, and capacitor voltages for the pure resistive and inductive loads are displayed in Fig. 7 (a) and Fig. 7 (b), respectively. Fig. 7 (c) shows the satisfactory performance

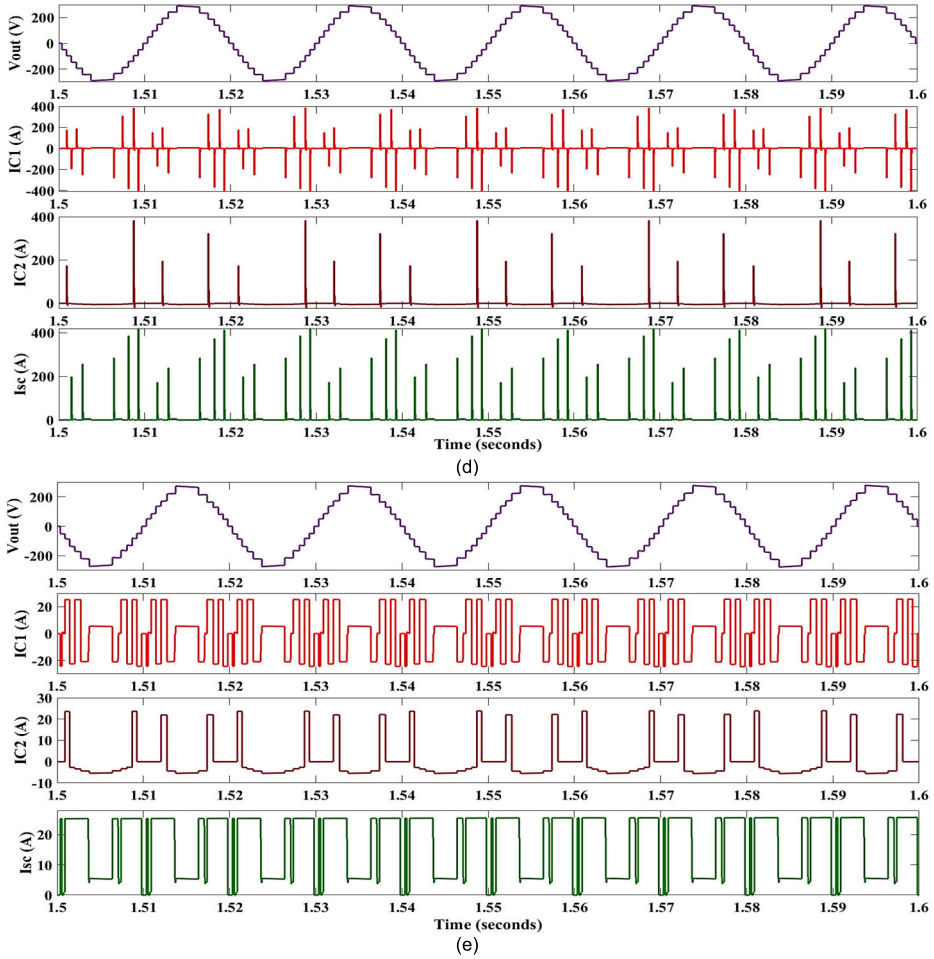

FIGURE 7. ***(Continued.)*** **Simulation results of the proposed topology. Output voltage, output current and capacitor voltages for (a) resistive load (b) inductive load (c) sudden change in supply voltage, Output voltage, capacitor currents and input source current (d) without inductor (e) with inductor.**

of the proposed inverter for the sudden change in supply voltage. The results show that with a single 50V supply, the proposed topology can generate a 13-level output waveform having a step voltage of 50V and a peak voltage of about 300V, which also verifies the voltage gain of 6. Self-balancing of the capacitor voltages and reduced voltage ripple features are also depicted in the waveforms. Fig. 7 (d) and Fig. 7 (e) show the output voltage, all the three capacitor currents, and input source current without and with utilizing the suitable inductor, respectively. The results show a remarkable difference in the source current and the capacitor currents after the utilization of a suitable inductor.

B. EXPERIMENTAL RESULTS

The proposed 13L SCMLI topology was experimentally verified. Experimental prototype used to validate the proposed topology is shown in Fig. 8. The components used and their specifications are given in Table 3. The circuit consists of an insulated-gate bipolar transistor (FGA25N120). While generating gate signals for individual IGBTs, a TLP-250-based gate driver circuit is used. The proposed inverter relies on gating signals sent from a digital signal processor (DSP), specifically a Texas Instruments TMS320F28379D.

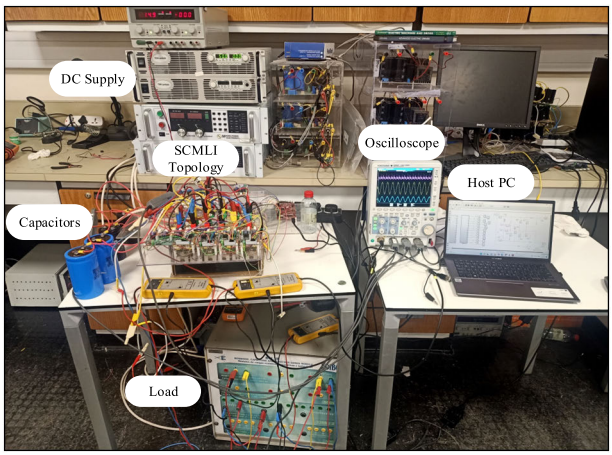

FIGURE 8. **Experimental prototype.**

TABLE 2. Comparison with single sorce 13L SCMLI topologies.

References	N_{sw}	N_{dr}	G	N_{dd}	N_c	N_T	TCV	MBV ($*V_{dc}$)	TSV_{pu} ($*V_{dc}$)	VRC				η (%)	THD (%)	CF
										$0.5V_{dc}$	V_{dc}	$2V_{dc}$	$3V_{dc}$			
[5]	12	11	3	4	4	31	3	2	4.33	2	2	0	0	95.29	4.2	2.95
[6]	13	12	3	1	3	29	2	2	5.67	2	1	0	0	96.5	7.2	2.82
[16]	18	18	3	0	4	40	3	2	5.17	2	2	0	0	96.81	5.5	3.71
[19]	29	29	6	0	5	63	5	1	4.83	0	5	0	0	91.7	15	5.6
[23]	13	13	6	2	3	31	5	3	6	0	2	0	1	94.2	7.2	3.23
[24]	13	9	6	2	3	27	5	3	5.33	0	2	0	1	97.3	--	2.87
[25]	13	13	6	2	3	31	5	3	5.5	0	2	0	1	96.7	--	3.19
[32]	10	10	6	4	4	28	8	6	5.5	0	2	0	2	97.2	11	3.19
[34]	14	14	6	1	3	32	5	3	5.5	0	2	0	1	--	--	3.27
[35]	15	15	6	0	3	33	5	3	5	0	1	2	0	97.3	9.7	3.31
[36]	13	13	6	3	3	32	5	4	5	0	1	2	0	96.5	9.2	3.23
[33]	13	7	6	2	4	26	8	6	5.83	0	2	0	2	96.3	10.74	3.06
[37]	17	14	6	0	3	34	5	3	5	0	2	0	1	95.39	5.58	3.38
[P]	14	13	6	1	3	31	5	4	6	0	1	2	0	97.4	5.27	3.23

* **N_{sw}, N_{dr}, G, N_{dd}, N_c, N_T, TCV, MBV, TSV, VRC, η, THD, [P]** : indicates the number of switches, drivers, voltage gain, discrete diodes, capacitors, total components, total capacitor voltage, maximum blocking voltage (switch stress) across switches, total standing voltage, voltage rating of capacitors, maximum efficiency, output voltage total harmonic distortion, proposed topology

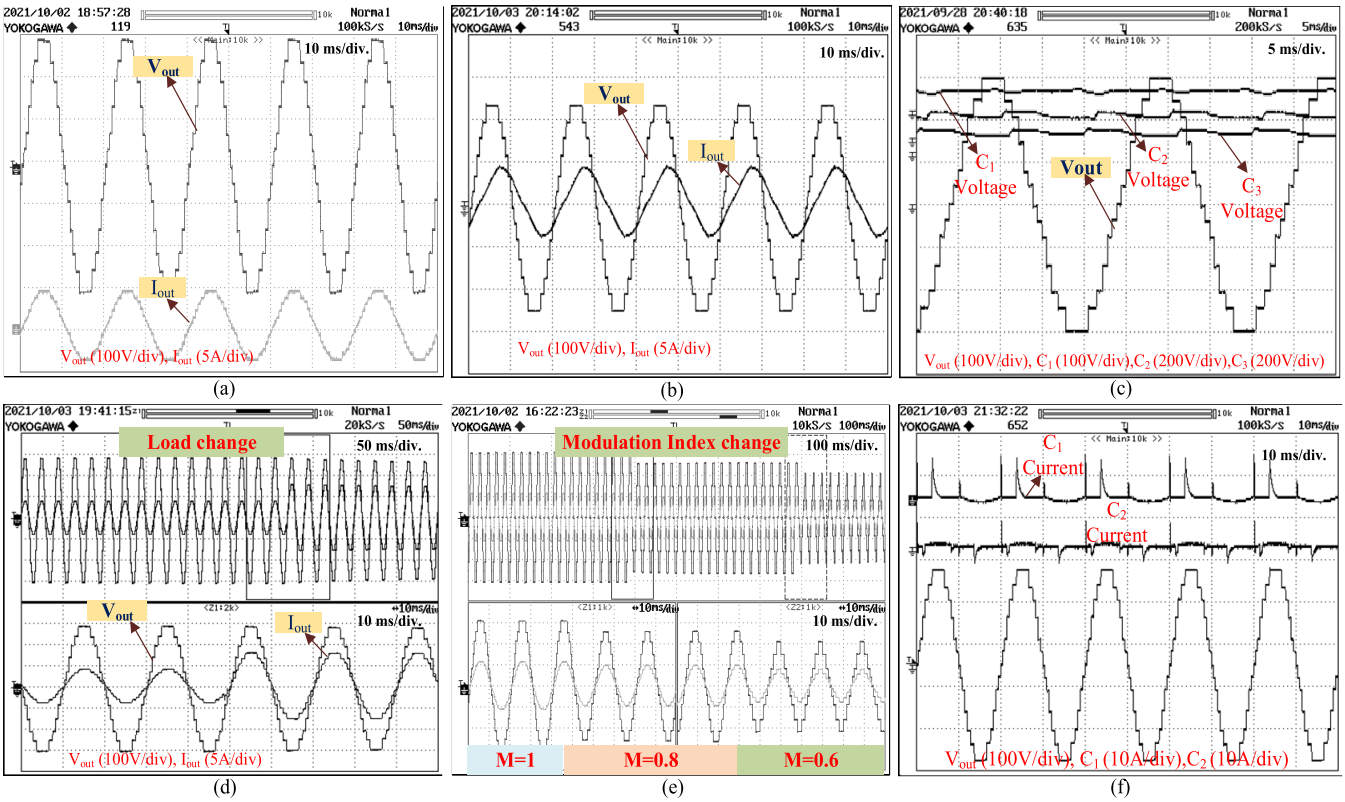

FIGURE 9. Hardware results of the proposed topology (a) output voltage and current for a resistive load of 75Ω (b) output voltage and current for an inductive load of R=75Ω, L=100mH (c) output voltage, and voltage across capacitors C_1, C_2, and C_3 (d) output waveform for dynamic load change (e) output waveform for modulation index change (f) output voltage and current through capacitors C_1,and C_2.

The output voltage and current waveform for a resistive load of 75 ohms is shown in Fig. 9 (a). Based on the applied DC input voltage of 50V, the peak output voltage is almost 300V, confirming the claimed voltage boost of 6. Output volt-

TABLE 3. Simulation and experimental circuit parameters.

Parameters	Simulation	Hardware
Input Voltage	50 V	50 V
IGBT	IGBT	1200 V/25 A (FGA25N120)
Diode	diode	Diode 160D40R
Driver	---	10- 35 V/ ±1.5 A (TLP 250)
Controller	---	TMS320F28379D
Output Frequency	50 Hz	50 Hz
Capacitors: C_1 C_2, C_3	2200 µF	2200 µF/250 V
***R-L* Load**	75 Ω- 150 mH	75 Ω- 100 mH

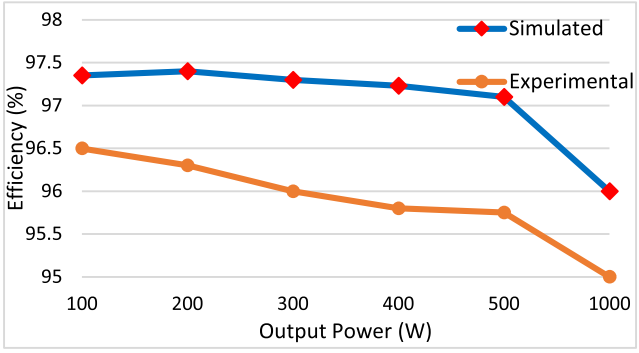

FIGURE 10. Efficiency versus output power of the proposed 13L inverter.

age and current for an inductive load of R=75Ω, L=100mH is shown in Fig. 9 (b). The current waveform is sinusoidal and lagging as expected for the inductive load. Output voltage and the three capacitor voltages are shown in Fig. 9 (c) for the same resistive load. Voltage across C_1 is about 50V (same as input DC voltage source) and the voltage across C_2 and C_3 are around 100V (twice the input DC voltage source). Fig. 9 (d) depicts the inverter's output waveform during a dynamic load change test, in which the load is suddenly halved from 75Ω. It can be observed that the output waveform is stable after the load change. Output waveform when the modulation index (MI) is changed from 1 to 0.8 to 0.6 has been shown in Fig. 9 (e). Capacitor currents of C_1 and C_2 are shown along with the output voltage in Fig. 9 (f). The capacitor currents are reduced by adding a suitable inductor in the charging loop as shown in Fig.1 (c). It is remarkable to note that the inductor place is common for the charging paths of all the three capacitors. Also, a power diode has been connected in parallel with the inductor to make sure that the currents going in the opposite direction have a way to flow freely.

In addition, the efficiency of the proposed inverter has been measured as the pure resistive load is changed from 50Ω to 1000Ω and is shown in Fig. 10. The maximum efficiency achieved is relatively high at 97.4% at an output power of 200W. The efficiency of the experimental prototype is almost similar to the measured one as shown in Fig. 10. The maximum efficiency achieved for the experimental prototype is 96.5%.

VII. CONCLUSION

In this paper, a 13-level sextuple boost inverter with reduced switch stress and self-voltage balancing capability of capacitors is proposed. The proposed SCMLI only needs one DC source, three capacitors, fourteen switches, and one diode to generate the desired single-phase ac output voltage with voltage gain of 6. Further, the maximum voltage stress across the switches is limited to 4 times the input voltage. The proposed scheme is able to reduce the THD of the output voltage up to 5.27% of the fundamental value of output voltage which is in agreement with IEEE standards. By contrasting the proposed SCMLI with state-of-the-art topologies from the literature, the most important aspects of the latter are brought to light. The viability of the proposed converter configuration is verified through experimental results captured using an experimental prototype. At 200 W of output power, the converter reaches its maximum efficiency of 97.4%. The proposed topology is a practical choice for high-current, low-voltage applications like solar PV and fuel cell systems.

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