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RESEARCH ARTICLE

A Resolution Control Loop for TDC-Based Phase Detectors in ADPLLs

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ABSTRACT This paper proposes a resolution control loop that runs in background to control the time resolution of a mid-rise Time to Digital Converter (TDC) used as a phase detector in All-Digital Phase Locked Loops (ADPLLs). The proposed resolution control loop minimizes the TDC resolution until the TDC linear dynamic range equals the range of the input time error. Consequently, PLL in-band phase noise is reduced due to reduction of the Power Spectral Density (PSD) of the TDC quantization noise. Moreover, the linearity of the TDC transfer function across the range of the input time error is guaranteed. On contrary, the counterpart resolution control loop based on Lloyd-Max algorithm does not guarantee the linearity of the TDC transfer function across the range of the input time error. Furthermore, the proposed resolution control loop achieves TDC quantization noise with a lower variance compared to that achieved by the counterpart resolution control loop when applied with a TDC with more than 3 bits. Finally, the hardware implementation of the proposed resolution control loop is more area and power efficient compared to the implementation of the counterpart resolution control loop.

INDEX TERMS All-digital phase locked loops (ADPLLs), time to digital converter (TDC), bang-bang phase detector (BBPD), bang-bang phase locked loop (BBPLL), digital loop filter (DLF), digital controlled oscillator (DCO), time resolution, quantization noise, power spectral density (PSD).

I. INTRODUCTION

Recently, ADPLLs have widely replaced their analog counterparts used for frequency synthesis in RF transceivers and clock-recovery in high-speed serial links [1], [2]. The digital implementation of the loop filter enables ADPLLs to benefit from technology scaling. Moreover, powerful calibration and control loops could be implemented with ADPLLs to correct analog non-idealities and to optimize loop dynamics [3], [4]. The block diagram of a conventional Integer BBPLL is shown in Fig. 1. BBPLL has been an attractive architecture due to the simplicity in design, small area, and low power consumption of the BBPD (1-bit TDC). However, BBPLLs suffer from large quantization noise introduced by the BBPD, besides difficulty in optimizing loop dynamics for minimizing BBPLL output phase noise.

$$K_{1-bit\ TDC} = \sqrt{\frac{2}{\pi}} \cdot \frac{1}{\sigma_{\Delta t}} \tag{1}$$

The BBPLL output phase jitter is composed of a random noise component introduced by the analog circuits and a quantization noise component introduced by the BBPD [4]. If the random noise component is larger than the quantization noise component, the BBPLL operates in a linear regime and the BBPD maintains a linear characteristic calculated by (1), where $\sigma_{\Delta t}$ is the standard deviation of the normal distribution of the time error input to the BBPD. On contrary, if the quantization noise component is larger than the random noise component, the BBPLL operates in a non-linear regime and the BBPD maintains a non-linear characteristic [5], [6]. Consequently, optimizing the BBPLL bandwidth is not straight forward because the BBPD characteristic depends on random noise to quantization noise ratio which is a function of the bandwidth. Therefore, in [4] a loop-gain control

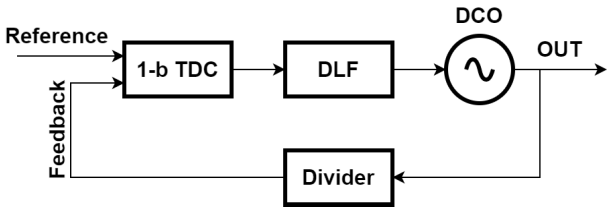

FIGURE 1. Block diagram of a conventional integer BBPLL.

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loop running in background to automatically adapt the DLF proportional gain (β) to obtain the optimum BBPLL bandwidth is proposed. This optimum BBPLL bandwidth occurs at the boundary between the linear and non-linear operation regimes and is characterized by BBPD output with zero autocorrelation as illustrated in Fig. 2.

$$K_{L-bit\ TDC} = \frac{2}{Tres} \tag{2}$$

To overcome the issues associated with BBPDs, replacing the BBPD by a narrow range L-bit TDC is proposed in [7], where L is the number of TDC bits. First, the L-bit TDC extends the linear operation regime of the PLL over the non-linear regime. Second, the gain of the L-bit TDC calculated by (2) is function of TDC time resolution (*Tres*) and is independent of $\sigma_{\Delta t}$. Consequently, L-bit TDC characteristic is independent of PLL noise which facilitates prediction and optimization of the PLL bandwidth. Third, the L-bit TDC has a lower quantization noise compared to BBPD; therefore, L-bit TDC ADPLLs have a lower in-band phase noise compared to BBPLLs. Finally, L-bit TDC ADPLLs have a shorter locking time compared to BBPLLs.

However, operating the L-bit TDC at an improper time resolution causes the behavior of the L-bit TDC to approach that of a BBPD as illustrated in Fig. 3. Consequently, the quantization noise of the L-bit TDC will equal that of a BBPD and in turn the in-band phase noise of the L-bit TDC ADPLL will equal that of a BBPLL. Therefore, a resolution control loop based on Lloyd-Max algorithm is proposed in [8]. This resolution control loop runs in background to adapt the TDC resolution to be equal to the value obtained by Lloyd-Max algorithm [9]. Lloyd-Max algorithm can be generally applied on any quantizer to obtain the resolution at which quantization noise variance is minimized. Moreover, a similar resolution control loop based on Lloyd-Max algorithm has been applied to a digital sub-sampling PLL in [10]. An equivalent approach to Lloyd-Max algorithm is the analysis performed in [11]. In which an expression for calculating the variance of the TDC quantization noise referred at the TDC input is derived. Furthermore, this expression is differentiated to obtain the TDC resolution at which the input referred TDC quantization noise variance is minimized. However, the TDC resolution obtained by the analysis in [11] does not guarantee the linearity of the TDC transfer function across the range of the TDC input time error. Furthermore, another alternative resolution control loop based on jitter monitoring has been proposed in [12]. This resolution control loop monitors the distribution of the TDC input time error and alters the TDC resolution until a local minimum of $\sigma_{\Delta t}$ is achieved rather than targeting a specific time resolution. However, a large number of observation cycles is needed to generate an accurate distribution of the TDC input time error to minimize the probability of wrong decisions [13]. Consequently, the resolution control loop in [12] requires a large settling time. Moreover, it cannot operate simultaneously with a loop-gain control loop because only one ADPLL parameter can be varied at a time. On contrary, the resolution control loop based on Lloyd-Max algorithm can operate simultaneously with a loop-gain control loop to optimize the PLL bandwidth [8], [10]. Therefore, the resolution control loop based on Lloyd-Max algorithm is more attractive than the resolution control loop based on jitter monitoring.

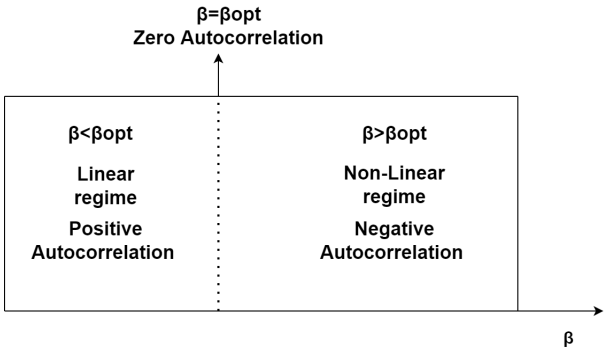

FIGURE 2. Modes of operation of a BBPLL.

In this paper, a resolution control loop running in background to adapt the TDC resolution is proposed. The proposed resolution control loop minimizes the TDC resolution till the TDC linear dynamic range equals the range of the TDC input time error. Therefore, the proposed resolution control loop guarantees the linearity of the TDC transfer function across the range of the TDC input time error. Moreover, the proposed resolution control loop achieves a lower quantization noise variance compared to that achieved by the resolution control loop of [8] when applied to a TDC with more than 3 bits. In addition, the hardware implementation of the proposed resolution control loop is more area and power efficient compared to the implementation of the resolution control loop of [8]. Furthermore, the proposed resolution control loop has a lower settling time compared to that of the resolution control loop of [12] and can operate simultaneously with a loop-gain control loop.

The paper is organized as follows. Section II details the analysis presented in [11] and the hardware implementation of the resolution control loop of [8]. Section III presents the theory and hardware implementation of the proposed resolution control loop. Section IV compares the behavioral simulation results of the proposed resolution control loop and the resolution control loop of [8]. Section V concludes the paper.

II. RESOLUTION CONTROL LOOP BASED ON LLOYD-MAX ALGORITHM

$$Kq = \left(\frac{\sigma_{qin}}{\sigma_{\Delta t}}\right)^2 = \frac{M^2 - 8\cdot\sum_{k=1}^{\frac{M-1}{2}} k\cdot erf\left(\frac{k\cdot\gamma}{\sqrt{2}}\right)}{\frac{2}{\pi}\left(1 + 2\cdot\sum_{k=1}^{\frac{M-1}{2}} \exp\left(-\frac{k^2\cdot\gamma^2}{2}\right)\right)^2} - 1 \tag{3}$$

$$\gamma = \frac{Tres}{\sigma_{\Delta t}} \tag{4}$$

$$M = 2^L - 1 \tag{5}$$

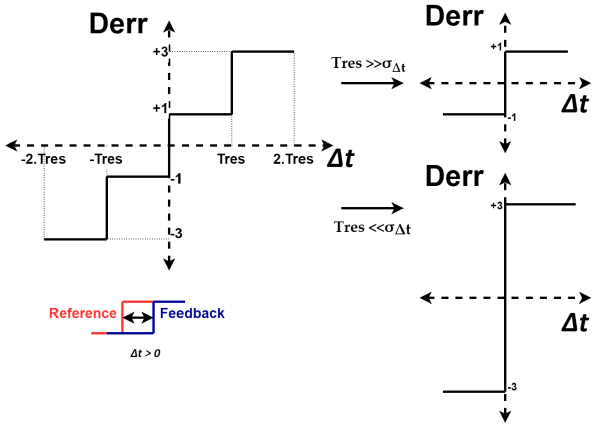

FIGURE 3. Behavior of 2-bit TDC vs TDC resolution.

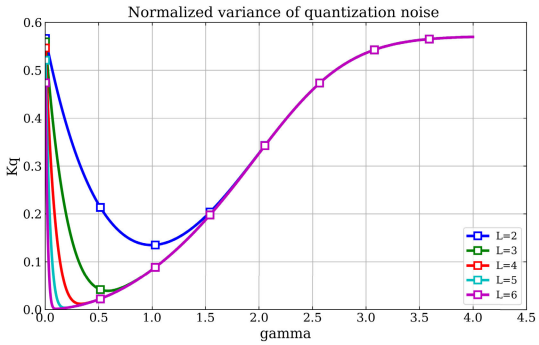

FIGURE 4. Kq for different number of TDC bits.

TABLE 1. TDC metrics achieved by the resolution control loop based on Lloyd-Max algorithm.

L	Resolution	Linear dynamic range	Normalized input referred quantization noise variance
2	$\sigma_{\Delta t}$	$4{\cdot}\sigma_{\Delta t}$	0.135
3	$0.585{\cdot}\sigma_{\Delta t}$	$4.68{\cdot}\sigma_{\Delta t}$	0.039
4	$0.336{\cdot}\sigma_{\Delta t}$	$5.376{\cdot}\sigma_{\Delta t}$	0.012
5	$0.188{\cdot}\sigma_{\Delta t}$	$6.016{\cdot}\sigma_{\Delta t}$	0.0035
6	$0.1{\cdot}\sigma_{\Delta t}$	$6.4{\cdot}\sigma_{\Delta t}$	0.0010

In [11], a time-domain model was used to derive equation (3) for calculating TDC quantization noise variance referred at the TDC input and normalized to the variance of the input time error. The parameter gamma (γ) calculated by (4) represents the normalized TDC resolution to $\sigma_{\Delta t}$. Moreover, M is the number of thresholds of the L-bit TDC calculated by (5). The factor Kq is plotted as a function of γ for different number of TDC bits in Fig. 4. The plot shows that for large and small values of γ the normalized variance of the input referred TDC quantization noise approaches 9/16 which equals the normalized variance achieved by a BBPD [11]. In other words, designing a L-bit TDC with a resolution that is extremely large or small relative to $\sigma_{\Delta t}$ causes the L-bit TDC operation to approach that of a BBPD. Furthermore, the plot shows that there is a normalized resolution at which input referred TDC quantization noise variance is minimized. This normalized resolution can be calculated by equating the differentiation of (3) to zero. Finally, the target TDC resolutions for different number of TDC bits are written in Table 1 along with the achieved TDC linear dynamic range and normalized input referred quantization noise variance. Table 1 shows that the TDC linear dynamic range achieved by the resolution control loop based on Lloyd-Max algorithm is lower than the TDC input time error range ($6{\cdot}\sigma_{\Delta t}$) in case of a TDC with less than 5 bits. Consequently, the linearity of TDC transfer function across the complete range of the TDC input time error is not guaranteed when the resolution control loop based on Lloyd-Max algorithm is applied on a TDC with less than 5 bits.

$$E[D_U] = (+1){\cdot}P(\Delta t > Tres) + (-1){\cdot}P(\Delta t < Tres) \quad (6)$$

$$Tres_{Lloyd-2b} = \sigma_{\Delta t} \quad (7)$$

$$E[D_U] = -0.68 \quad (8)$$

According to Table 1, the target TDC resolution for a 2-bit TDC is $\sigma_{\Delta t}$. Therefore, a resolution control loop that runs in background to adapt the resolution of a 2-bit TDC to equal $\sigma_{\Delta t}$ is proposed in [8]. Fig. 5 shows the block diagram of an ADPLL based on the 2-bit TDC and the resolution control loop proposed in [8]. The signal D_U rises from -1 to $+1$ when the reference signal leads the feedback signal by more than *Tres*. On contrary, the signal D_L falls from $+1$ to -1 when the feedback signal leads the reference signal by more than *Tres*. The working principle of the resolution control loop is as follows. First, the expectation of D_U is calculated as a function of *Tres* using (6). Second, the target resolution in case of a 2-bit TDC is calculated by (7). Finally, substituting (7) in (6) yields (8) that implies that expectation of D_U should equal -0.68 when the target resolution is achieved. Therefore, the sum of 100 samples of D_U should equal -68 on average after convergence of the resolution control loop. Furthermore, the difference between the sum of 100 samples and the reference value of -68 is used to generate an error signal to drive an accumulator that generates the resolution control signal. This resolution control loop can be used with a TDC of any number of bits after adjusting the reference value. The reference values vs the number of TDC bits are written in Table 2.

III. PROPOSED RESOLUTION CONTROL LOOP

$$PSD_{qn} = 10{\cdot}log(\frac{\Delta^2}{12{\cdot}Fsample}) \quad (9)$$

The PSD of the quantization noise of any quantizer can be calculated using (9), where Δ and *Fsample* are the resolution and sampling frequency of the quantizer, respectively. In case of a L-bit TDC used as a phase detector in ADPLL, Δ is the TDC resolution and *Fsample* is the PLL reference frequency (*Fref*). Equation (9) implies that reduction of TDC resolution reduces the PSD of TDC quantization noise. However, (9) is only valid if the TDC linear dynamic range is greater

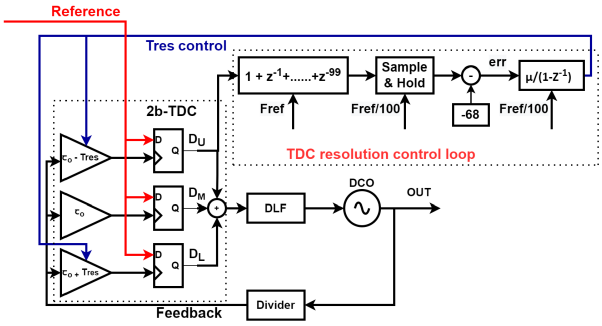

FIGURE 5. ADPLL based on the 2-bit TDC, and the TDC resolution control loop proposed in [8].

TABLE 2. Reference value of resolution control loop of [8] vs number of TDC bits.

L	Reference value
2	-68
3	-44
4	-26
5	-15
6	-8

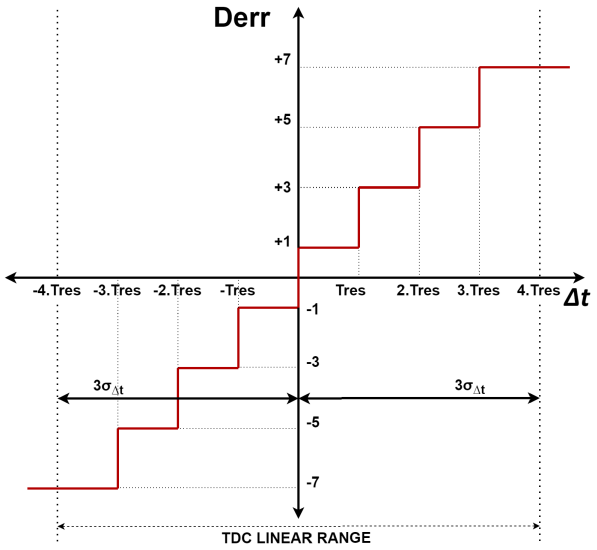

FIGURE 6. Theory of the proposed TDC resolution control loop.

TABLE 3. TDC metrics achieved by the proposed resolution control loop.

L	Resolution	Linear dynamic range	Normalized input referred quantization noise variance
2	$1.5{\cdot}\sigma_{\Delta t}$	$6{\cdot}\sigma_{\Delta t}$	0.1875
3	$0.75{\cdot}\sigma_{\Delta t}$	$6{\cdot}\sigma_{\Delta t}$	0.0469
4	$0.375{\cdot}\sigma_{\Delta t}$	$6{\cdot}\sigma_{\Delta t}$	0.0117
5	$0.1875{\cdot}\sigma_{\Delta t}$	$6{\cdot}\sigma_{\Delta t}$	0.0029
6	$0.09375{\cdot}\sigma_{\Delta t}$	$6{\cdot}\sigma_{\Delta t}$	0.0007

than or equal to the range of the input time error. Therefore, according to (9) the TDC resolution should not be minimized below the value that equates the TDC linear dynamic range to the range of the input time error as illustrated in Fig. 6.

$$Tres_{proposed} = \frac{3{\cdot}\sigma_{\Delta t}}{2^{L-1}} \tag{10}$$

$$Kq_{proposed} = \frac{1}{12}{\cdot}\left(\frac{3}{2^{L-1}}\right)^2 \tag{11}$$

In this paper, a resolution control loop that adapts the TDC resolution for equating the TDC linear dynamic range to the range of the TDC input time error is proposed. Consequently, the TDC quantization noise variance is reduced and the linearity of the TDC transfer function across the range of TDC input time error is ensured. Furthermore, the target TDC resolution achieved by the proposed resolution control loop is calculated using (10). Moreover, the TDC input referred quantization noise variance normalized to the variance of the input time error achieved by the proposed resolution control loop is calculated by (11).

The target TDC resolution, TDC linear dynamic range, and normalized TDC input referred quantization noise variance achieved by the proposed resolution control loop are written in Table 3. According to Table 3, the TDC linear dynamic range achieved by the proposed resolution control loop equals $6{\cdot}\sigma_{\Delta t}$ by construction independent of the number of TDC bits. Consequently, the proposed resolution control loop guarantees the linearity of the TDC transfer function across the range of the TDC input time error independent of the number of TDC bits. On contrary, the resolution control loop of [8] does not guarantee the linearity of the TDC transfer function across the range of the TDC input time error if it is applied on a TDC with less than 5 bits. Furthermore, the normalized TDC input referred quantization noise variance achieved by the proposed resolution control loop is compared to that achieved by the resolution control loop of [8] in Table 4. According to Table 4, the proposed resolution control loop achieves a lower input referred TDC quantization noise variance when applied on a TDC with more than 3 bits.

$$Ref_{count} = 0.15\%{\cdot}2000 = 3 \tag{12}$$

Fig. 7 shows the block diagram of the proposed resolution control loop applied on the 2-bit TDC of [8]. The upper controlled delay cell, generating a delay of τ_o - *Tres*, is split into two controlled delay cells generating a delay of τ_o - 2·*Tres* and *Tres*. The controlled delay cell generating a delay of τ_o - 2·*Tres* is implemented to generate a time

threshold of 2·*Tres*. Therefore, the output of the extra flip flop is a flag signal that rises to high every incident the reference signal leads the feedback signal by more than 2·*Tres*. Moreover, this flag signal is used as a trigger signal to a counter; therefore, the output count represents the number of TDC input samples outside the TDC linear dynamic range. Furthermore, the goal of the proposed resolution control loop is to enclose 99.7% of the TDC input samples within the TDC linear dynamic range. Therefore, the output count should equal 0.15% of the TDC input samples. Consequently, if the counter is reset every 2000 reference cycles the expected output count should be 3 on average as illustrated by (12). This reference count of 3 is deducted from the output count using a subtractor; moreover, this error signal is sampled

TABLE 4. Comparison of Normalized TDC input referred quantization noise variance.

L	Normalized TDC input referred quantization noise variance	
	This work	[8]
2	0.1875	0.135
3	0.0469	0.039
4	0.0117	0.012
5	0.0029	0.0035
6	0.0007	0.0010

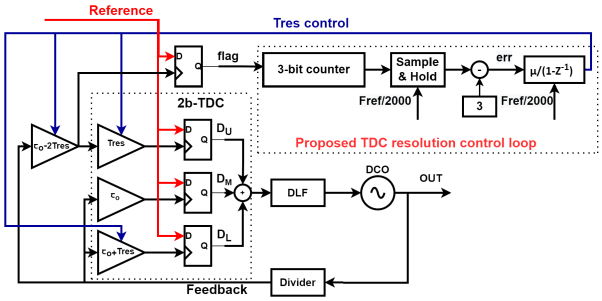

FIGURE 7. ADPLL based on the 2-bit TDC of [8], and the proposed resolution control loop.

by an accumulator at a rate of *Fref*/2000. The accumulator uses the error signal to generate the resolution control signal. The proposed resolution control loop is designed such that the resolution control signal initially sets the TDC with the largest resolution; therefore, the count will be initially 0. Furthermore, when the proposed resolution control loop is enabled, the resolution control signal starts reducing the TDC resolution until the target TDC resolution is achieved at steady state. Consequently, the count starts increasing until it reaches an average of 3 at steady state. Therefore, a 3-bit counter would be enough to allow for counts that are slightly larger than 3.

The hardware implementation of the proposed resolution control loop is more area and power efficient compared to the resolution control loop of [8]. First, the 100-tap finite impulse response (FIR) filter in the resolution control loop of [8] is replaced by a 3-bit counter. Second, the error signal input to the accumulator is a 4-bit signal in the proposed resolution control loop. Therefore, the accumulator has a lower area compared to the accumulator of the resolution control loop of [8] having a 6-bit input signal. Finally, the switching power of the proposed resolution control loop is lower than that of [8] because the error accumulator sampling frequency is reduced from *Fref*/100 to *Fref*/2000. Consequently, reduction of the sampling frequency increases the settling time of the proposed resolution control loop compared to the settling time of the resolution control loop of [8] for the same accumulator step size (μ). However, a fast-tracking control loop is not necessary because PVT variations are generally slow.

IV. SIMULATION RESULTS

A behavioral time domain model for a L-bit TDC based ADPLL along with the proposed TDC resolution control loop has been implemented on python. The block diagram of the

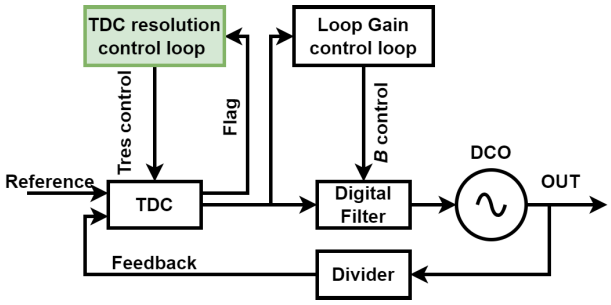

FIGURE 8. Block diagram of the ADPLL python behavioral model.

TABLE 5. Noise parameters.

Block	Noise parameter	Value [dBc/Hz]
Reference	Phase noise floor	-150
Divider	Phase noise floor	-150
DCO	Phase noise @ 1 MHz offset	-100

behavioral model is shown in Fig. 8. Behavioral simulations are performed to verify the functionality and performance of the proposed TDC resolution control loop. Moreover, the TDC resolution control loop of [8] is also modelled and simulated to compare its performance with that of the proposed TDC resolution control loop. A loop-gain control loop is used to adapt the DLF proportional gain (β) to obtain the optimum PLL bandwidth at which output rms phase jitter is minimized [8]. A feedback division ratio (N) of 100 is used to generate a 10 GHz output frequency from a 100 MHz reference frequency. Moreover, the DLF integral to proportional gain ratio is 1/64 and the DCO period gain is 0.4 fs/Lsb. Furthermore, the noise parameters of the PLL building blocks and the input reference clock are summarized in Table 5. Finally, this python model can be used to generate the PSD of the TDC quantization noise by applying Fast Fourier Transform (FFT) on the TDC quantization noise obtained from the behavioral time domain simulations. The model by which the input referred TDC quantization noise is calculated in simulations is illustrated in Fig. 9.

The number of bits of the TDC is set as 6 and the initial TDC resolution set by both resolution control loops is 500 fs. The transient behavior of both resolution control loops when enabled is shown in Fig. 10. The average TDC resolutions achieved by the resolution control loop of [8] and the proposed resolution control loop are 76 fs and 73 fs, respectively. Furthermore, the normal distribution of the input time error when both resolution control loops are applied is plotted in Fig. 11. The standard deviation of the input time error ($\sigma_{\Delta t}$) calculated by the standard deviation function embedded in python is equal to 765 fs. Hence, the simulation results are in close agreement with the theory in Table 1 and Table 3. Furthermore, the higher switching frequency of the resolution control loop of [8] causes its settling time to be lower than that achieved by the proposed resolution control loop for the same accumulator step size of 2^{-10}. However, the steady state variance of the TDC resolution achieved by the proposed

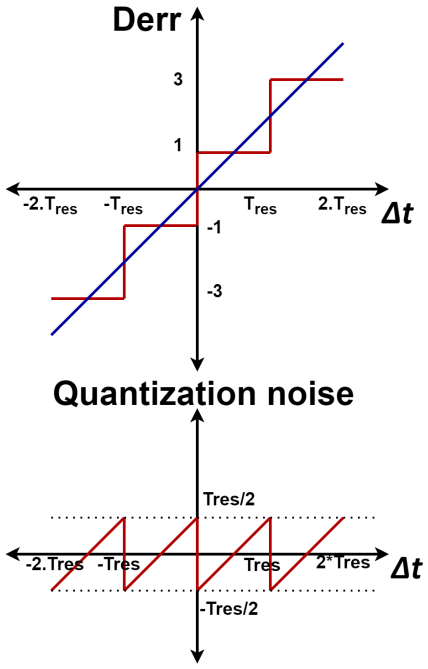

FIGURE 9. Model of TDC quantization noise.

resolution control loop is lower. Finally, the PSD of the input referred TDC quantization noise when both resolution control loops are applied is plotted in Fig. 12. Results in Fig. 12 show that the PSD achieved by the proposed resolution control loop is around 0.5 dB lower than that achieved by the resolution control loop of [8] which is in a close agreement with the theory in Table 1 and Table 3.

Furthermore, the number of TDC bits is then set as 2 and the initial TDC resolution set by both resolution control loops is changed to 1.5 ps. The transient behavior of both resolution control loops when enabled is shown in Fig. 13. The average TDC resolutions achieved by the resolution control loop of [8] and the proposed resolution control loop are 767 fs and 1.15 ps, respectively. Furthermore, the normal distribution of the input time error when both resolution control loops are applied is plotted in Fig. 14. Moreover, $\sigma_{\Delta t}$ of the input time error is calculated by the standard deviation function embedded in python and equals 768 fs. Hence, the achieved TDC resolutions in simulations are in a close agreement with the theory in Table 1 and Table 3. Furthermore, the histograms of the TDC output when both resolution control loops are applied is plotted in Fig. 15. Fig. 15a shows that the normal distribution of the time error input to the TDC is not maintained in the TDC digital output due to the saturation effect encountered when resolution control loop of [8] is applied. On contrary, the proposed resolution control loop ensures the linearity of the TDC transfer function across the complete range of the TDC input time error. Therefore, the TDC digital output maintains a normal distribution when the proposed resolution control loop is applied as shown in Fig. 15b. Finally, the PSD of the input referred TDC quantization noise when both resolution control loops are applied is

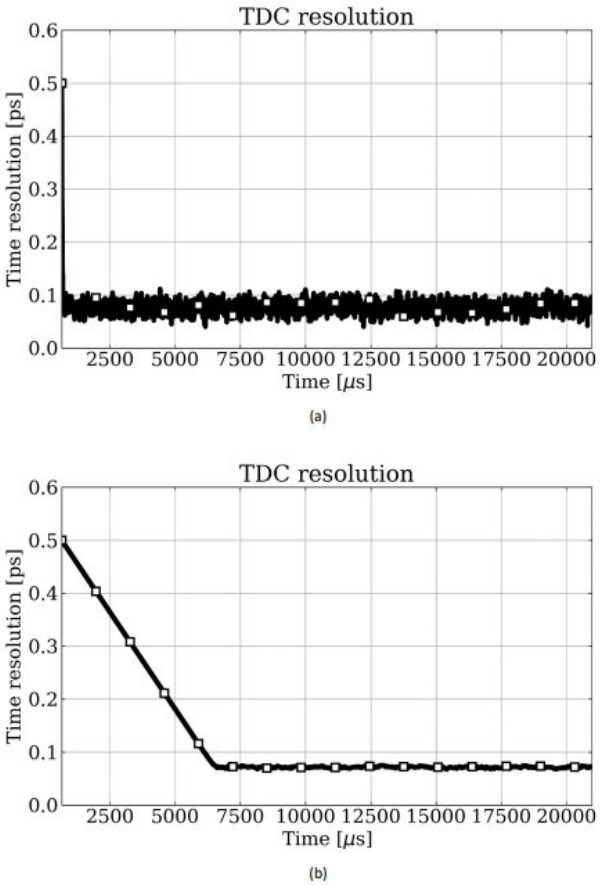

FIGURE 10. Settling of 6b-TDC resolution controlled by (a) resolution control loop of [8] (b) proposed resolution control loop.

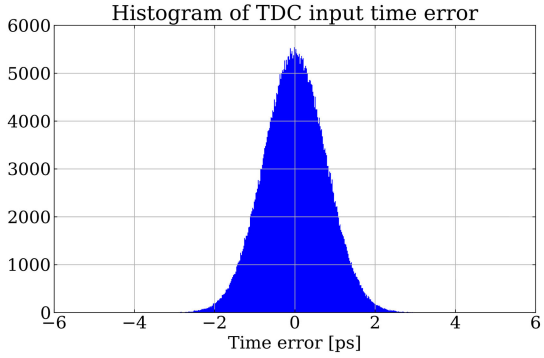

FIGURE 11. Histogram of 6b-TDC input time error.

plotted in Fig. 16. The PSD achieved by the resolution control loop of [8] is generally lower than the PSD achieved by the proposed resolution control loop; however, it does not have a constant value due to the saturation effect. Integrating the PSD of Fig. 16a yields a input referred TDC quantization noise variance of $7 * 10^{-26}$ which is in a close agreement with the theoretical input referred TDC quantization noise variance $7.08 * 10^{-26} = Kq_{Lloyd-2b} * (768 * 10^{-15})^2$, where $Kq_{Lloyd-2b}$ equals 0.12 as shown in Fig. 4. Finally, the PSD of Fig. 16b is in close agreement with the PSD calculated by (9) because the TDC linear dynamic range covers the com-

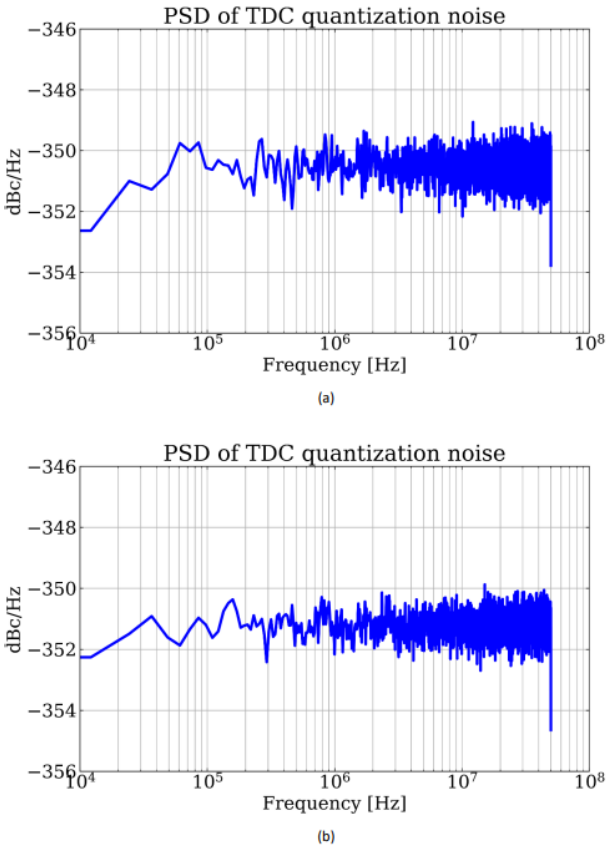

FIGURE 12. PSD of 6b-TDC quantization noise after applying (a) resolution control loop of [8] (b) proposed resolution control loop.

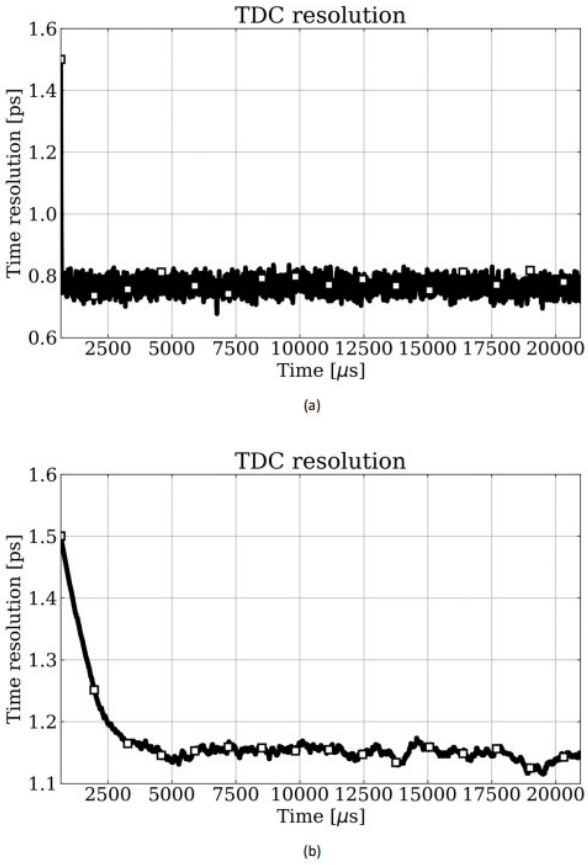

FIGURE 13. Settling of 2b-TDC resolution controlled by (a) resolution control loop of [8] (b) proposed resolution control loop.

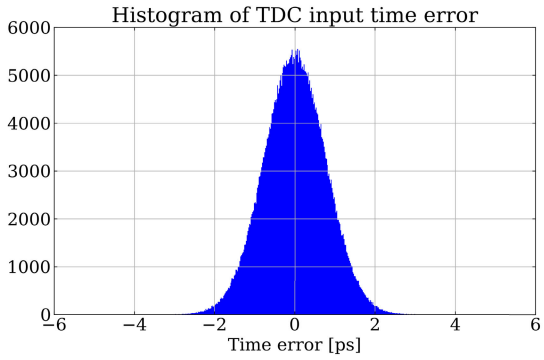

FIGURE 14. Histogram of 2b-TDC input time error.

plete input range without any saturation when the proposed resolution control loop is applied. Moreover, integrating the PSD of Fig. 16b yields a TDC quantization noise variance of $1.1 * 10^{-25}$.

Furthermore, simulation of the ADPLL with a 2-bit TDC was repeated after disabling the proposed resolution control loop and applying a TDC resolution of 3 ps which is larger than that achieved by the proposed resolution control loop, and a TDC resolution of 100 fs which is smaller than that achieved by the proposed resolution control loop. The phase noise of the ADPLL output frequency achieved in these two cases is compared to the phase noise achieved when the proposed resolution control loop is enabled as shown in Fig. 17. The phase noise plots show that the in-band phase noise achieved when a 2-bit TDC with 3 ps time resolution is applied is approximately equal to that achieved when a 2-bit TDC with 100 fs time resolution is applied. Moreover, $\sigma_{\Delta t}$ of the TDC input time error calculated by the standard deviation function embedded in python equals around 790 fs in both cases. This indicates that the behavior of the 2-bit TDC with 3 ps or 100 fs time resolution approaches the behavior of a BBPD.

$$PSD_{qn-bbpd} = 10 \cdot log(\frac{9}{16} \cdot \frac{{\sigma_{\Delta t}}^2}{Fref}) \tag{13}$$

$$S_{\phi_{qn-bbpd}} = 10 \cdot log(\frac{9}{16} \cdot \frac{{\sigma_{\Delta t}}^2}{Fref} \cdot (Fref \cdot 2\pi)^2) \tag{14}$$

$$S_{\phi_{ib}} = 20 \cdot log(\sqrt{(2 \cdot (10^{\frac{-150}{20}})^2 + (10^{\frac{-148.5}{20}})^2) \cdot N}) \tag{15}$$

In order to prove that the 2-bit TDC behavior has approached that of a BBPD, the theoretical ADPLL in-band phase noise is calculated assuming that the 2-bit TDC behaves as a BBPD. Moreover, this theoretical in-band phase noise will be compared to the in-band phase noise obtained

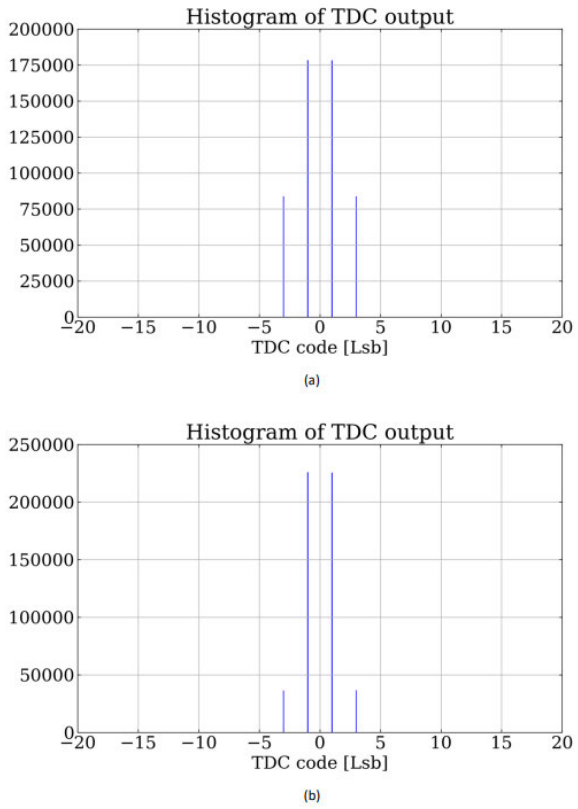

FIGURE 15. Histogram of 2b-TDC output after applying (a) resolution control loop of [8] (b) proposed resolution control loop.

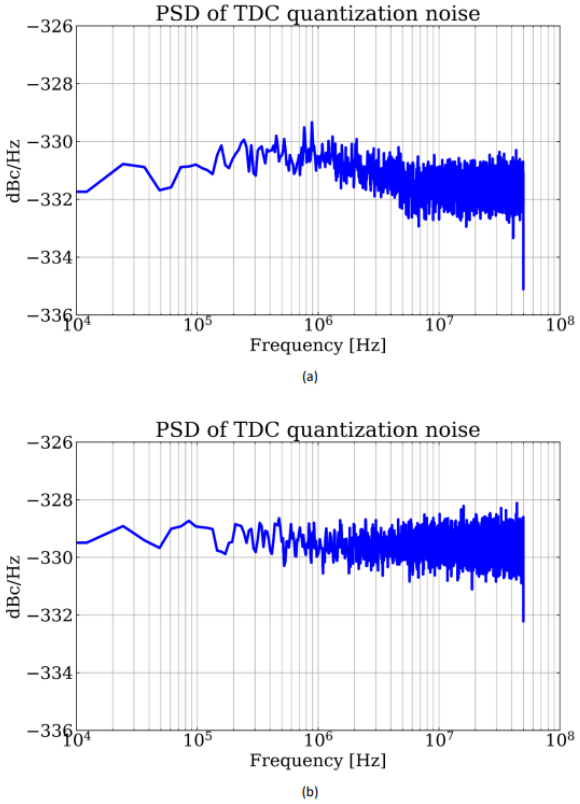

FIGURE 16. PSD of 2b-TDC quantization noise after applying (a) resolution control loop of [8] (b) proposed resolution control loop.

by simulations. The PSD of the BBPD quantization noise ($PSD_{qn-bbpd}$) equals -324.5 dBc/Hz according to (13). Moreover, the phase noise due to the BBPD quantization noise referred at the PLL input ($S_{\phi_{qn-bbpd}}$) equals -148.5 dBc/Hz according to (14). In addition, the theoretical in-band phase noise of the ADPLL output frequency ($S_{\phi_{ib}}$) due to the phase noise of the input reference, feedback divider and BBPD quantization noise equals -104.7 dBc/Hz according to (15). The theoretical in-band phase noise calculated using (15) is in a close agreement with the in-band phase noise in Fig. 17. Hence, the approach of the 2-bit TDC behavior to that of a BBPD when a time resolution of 3 ps and 100 fs is applied has been proved.

$$S_{\phi_{qn-tdc}} = 10 \cdot log(\frac{\Delta^2}{12 \cdot Fref} \cdot (Fref \cdot 2\pi)^2) \qquad (16)$$

However, enabling the proposed resolution control loop causes the 2-bit TDC to operate at a time resolution of 1.15 ps. Consequently, the 2-bit TDC doesn't behave as a BBPD and the PSD of its quantization noise equals -329.5 dBc/Hz according to (9). Moreover, the phase noise due to the 2-bit TDC quantization noise referred at the PLL input ($S_{\phi_{qn-tdc}}$) equals -153.6 dBc/Hz as calculated using (16). In addition, the theoretical in-band phase noise of the ADPLL output frequency due to the phase noise of the input reference, feedback divider and 2-bit TDC quantization noise is calculated using (15) after replacing the phase noise due to the BBPD quantization noise calculated using (14) with the phase noise due to the 2-bit TDC quantization noise calculated using (16). This yields a -106 dBc/Hz theoretical in-band phase noise which is in a close agreement with the simulation results in Fig. 17. Hence, enabling the proposed resolution control loop limits the in-band phase noise of the ADPLL output frequency.

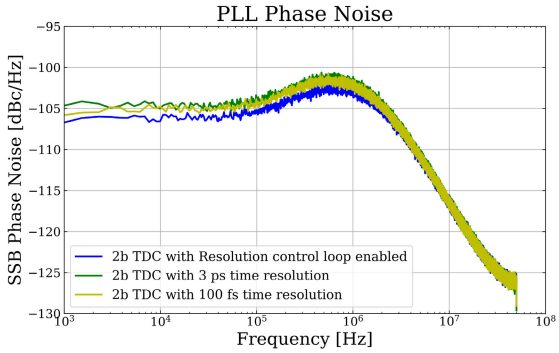

FIGURE 17. Phase noise plot of ADPLL output when applying a 2b-TDC with: the proposed resolution control loop enabled, a 3 ps time resolution, and a 100 fs time resolution.

V. CONCLUSION

A resolution control loop running in background to reduce the TDC resolution until the TDC linear dynamic range becomes equal to the complete range of the input time error

is proposed. Therefore, the proposed resolution control loop ensures linearity of the TDC transfer function across the complete range of the input time error. On contrary, the counterpart resolution control loop proposed in [8] causes TDC saturation when applied with a TDC of less than 5 bits. Moreover, the proposed resolution control loop achieves a lower input referred TDC quantization noise variance compared to the resolution control loop of [8] when applied with a TDC with more than 3 bits. However, the resolution control loop of [8] achieves a lower input referred TDC quantization noise variance compared to the proposed resolution control loop when applied with a TDC with less than 4 bits. Furthermore, the hardware implementation of the proposed resolution control loop is more area and power efficient compared to the implementation of the resolution control loop of [8]. Finally, behavioral simulations for the proposed resolution control loop and the resolution control loop of [8] when applied with a 6-bit and 2-bit TDC have been performed and the simulation results are in a close agreement with the theory presented.

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