IEEE Access
Multidisciplinary ⋮ Rapid Review ⋮ Open Access Journal

Received 20 March 2023, accepted 31 March 2023, date of publication 6 April 2023, date of current version 11 April 2023.

Digital Object Identifier 10.1109/ACCESS.2023.3265081

RESEARCH ARTICLE

A Novel Three-Level Quasi-Switched Boost F-Type Inverter With High Voltage Gain and Self-Balanced Neutral-Point Voltage

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This work was supported by the T2022-33TĐ Project.

ABSTRACT This paper introduces a new topology of three-level quasi-switched boost F-type inverter (3L-qSBFTI) to improve voltage gain compared to traditional impedance-source inverters (ISIs). This topology uses a switched-capacitor (SC) structure to increase the boost factor to twice that of traditional ISIs. Unlike any conventional SC circuits, the currents through capacitors when they are connected in parallel are limited by inductor current. Hence, there is no inrush current through capacitors and semiconductor devices in this operating state. Furthermore, this SC structure helps to obtain self-balanced neutral-point-voltage. The lower-shoot-through (LST) state, which is inserted into P-type small vectors, is used to boost the DC-link voltage. This insertion helps to increase modulation index utilization. As a result, the component voltage rating of the introduced inverter is significantly improved. The comparison study, simulation, and experimental validations have been presented to verify the proposed inverter.

INDEX TERMS F-type inverter, switched-capacitor, quasi-switched boost, self-balanced capacitor voltages, three-level inverter.

I. INTRODUCTION

Recently, multi-level inverters (MLIs) have attracted much attention because of their advantages compared to conventional two-level inverter because of lower component voltage rating, lower switching loss, and higher efficiency [1], [2]. Besides neutral-point clamped inverter (NPCI) and three-level T-type inverter (3L-T^{2}I), three-level F-type inverter (3L-FTI) discussed in [3] is an emerging topology. The literature [3] demonstrated that 3L-FTI can reduce the number of diodes compared to NPCI and increase conversion efficiency than 3L-T^{2}I. However, the conventional MLIs only step-down AC output voltage from a high DC input source. Hence, in some applications where input DC source is very low, the inverter must be stopped because DC-link voltage is not enough for DC-AC operating [4], [5], [6]. For instance, in photovoltaic (PV) system-based grid-connected applications, when PV panels operate in shading conditions, the output voltage of PV is significantly decreased, which is not larger than grid-voltage [4], [6]. As a result, grid-connected operating is interrupted.

To increase the DC-link voltage, a conventional front-end boost DC-DC converter is usually installed before conventional voltage-source inverters (VSIs) [7]. In literature [8], a three-level boost structure is compared with the conventional DC-DC boost converter to highlight its advantage of higher efficiency, better inductor current profile, and better power density. Due to these benefits, the three-level boost converter is also considered to integrate with MLIs and two-level inverter [9], [10], [11]. However, these two-stage inverters do not accept shoot-through (ST) state which is generated by simultaneously gating on all-switches in any inverter phase leg [12].

In recent years, single-stage impedance-source inverters (ISIs) have attracted much attention due to their benefits such as stepping up/down voltage and ST immunity. The first

The associate editor coordinating the review of this manuscript and approving it for publication was Ton Duc Do.

generation of ISIs is Z-source (ZS) inverter (ZSI) explored by Peng in the work [13]. In [14], a ZS network consists of two inductors, two capacitors, and two diodes connected in X-shaped was integrated with conventional 3L-T^{2}I. Derived from ZSI, the works in [15], [16], and [17] presented a quasi-ZS inverter (qZSI) topology which improves component voltage rating and provides continuous input current. Literature [18] demonstrated that ISIs have better performance than conventional two-stage inverters under certain conditions. The works in [19] presented an asymmetrical embedded modified ZS-3LTI (AEMZS-3LTI) to enhance boost factor and voltage gain compared to ZSI/qZSI. Accordingly, the boost factor is improved to twice that of conventional qZSIs. In [19], instead of using the full-ST (FST) state, upper/lower ST (UST/LST) states were employed to achieve buck-boost operating. These UST/LST states are considered to be inserted into small vectors.

The other types of single-stage inverters are topologies that use active switches in impedance-source network to save the number of inductors/capacitors. The literature in [20] introduced an amplitude-enhanced NPCI, which uses only one inductor, two capacitors, one active switch, and two diodes to improve voltage gain and performance compared to conventional Cuk-derived NPC inverter discussed in [20]. The study in [21] discussed a three-level flying capacitors split-source inverter (3L-FC-SSI). This configuration uses only one capacitor and three diodes in boost circuit, the switches in FC inverter circuit are shared for both DC-DC and DC-AC operating.

The quasi-switched boost inverters (qSBIs) can reduce the number of passive component counts compared to traditional ZS/qZS inverters. The works in [22] presented a 3L-qSBT^{2}I with boost factor and voltage gain enhancement compared to traditional ISIs. Furthermore, the inductor current ripple is decreased significantly. The work in [23] presented a new topology of qSBI to reduce the number of switching devices named reduced component count – active impedance-source – three-level inverter (RC^2-AIS-TLI).

In MLIs, neutral-point voltage unbalancing is a significant problem that directly affects the total harmonic distortion (THD) of the output current. A commonly solution for this problem is to use a switched-capacitor (SC) structure which connects two capacitors in parallel in some operating states to balance capacitor voltages [20], [23]. However, this solution generates a high inrush current through semiconductor devices [23]. Moreover, there are a small different between capacitor voltages (approximately 1.31% DC-link voltage) because of parasitic of switching devices [23]. The other solution is to use corresponding modulation techniques [14], [15], [17], [20], [22]. The works in [14], [15], and [17] adjust the time intervals of small vectors to balance neutral-point voltage. The duty ratios of UST/LST states are also used to obtain capacitor voltage balancing in [19]. In literature [22], the duty ratios of boost switches are calculated with the help of proportional-integral (PI) controller to balance capacitor voltages. However, these methods have many drawbacks, including the boost factor effect and computation complexity. Furthermore, the modulation technique-based method requires voltage sensor for any single capacitor.

To summarize, the existing topologies have the drawbacks of low voltage gain and limitations of capacitor voltage balancing technique. This paper will present a new topology named three-level quasi-switched boost F-type inverter (3L-qSBFTI) to overcome these drawbacks. In this topology, a qSB structure with smaller component counts compared to [22] is presented. The space-vector modulation (SVM) method, which replaces all small vectors by LST vectors, is introduced to control this proposed inverter. The main contributions of proposed SVM method and topology can be listed as:

1) high boost factor/voltage gain,
2) improving modulation index/ST duty ratio utilizations
3) self-balanced neutral-point voltage without voltage sensor requirement and inrush current through capacitors and switching devices.

The comparison study, simulation, and experimental results are presented to demonstrate the effectiveness of the proposed inverter. The rest of this paper includes six sections. The introduction of the proposed inverter, its operating principle, and the proposed SVM control method are presented in section II. Section III discusses component selections. Power loss estimation is presented in section IV. Section V introduces comparison between the proposed inverter and existing ISIs. Section VI presents simulation and experimental results. Section VII of this work is conclusion.

II. TOPOLOGY OF THREE-LEVEL QUASI-SWITCHED BOOST F-TYPE INVERTER (3L-QSBFTI)

The proposed 3L-qSBFTI topology is presented in Fig. 1 which is constructed by qSB circuit and 3L-FTI branch. The qSB circuit consists of three diodes $D_1 - D_3$, two active switches S_1 and S_2, two capacitors C_1 and C_2, and one inductor L_B. By directly attaching inductor L_B to input source V_{dc}, the input current is continuous. The FTI circuit includes three phase legs, each leg consists of four switches $S_{1X} - S_{4X}$ ($X = A, B, C$). The operating principle, PWM control scheme, and steady-state analysis are discussed in the rest of this section. Note that the other conventional three-level inverters like NPCI or 3L-T^{2}I can be used instead of 3L-FTI. However, this inverter is introduced to operate in LST mode. Because the ST current in LST mode of FTI just goes through two switching devices S_{2X} and S_{4X} instead of three switches like others, which is detailed as follow. Therefore, the use of FTI can reduce the conduction loss in LST than other configurations.

A. OPERATING MODES

The proposed inverter is introduced to operate under LST mode and non-ST mode, as shown in Fig. 2. The LST mode consists of three sub-modes called LST mode 1 – mode 3. The switching states of semiconductor devices are listed in Table 1.

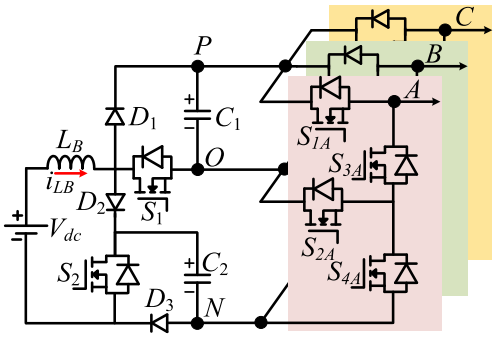

FIGURE 1. Proposed of 3L-qSBFTI topology.

TABLE 1. On/off states of 3L-qSBFTI ($x = a, b, c$).

Mode	ON Switch		ON Diode	V_{XO}
LST1		S_{1X}/or S_{3X}, S_{2X}, S_{4X}	D_1, D_3	$+V_{PN}/2$ /or 0
LST2			D_1, D_2, D_3	
LST3	S_1, S_2	S_{1X}/or S_{3X}, S_{2X}, S_{4X}		
non-ST	S_1	S_{1X}, S_{2X}	D_2, D_3	$+V_{PN}/2$
		S_{2X}, S_{3X}		0
		S_{3X}, S_{4X}		$-V_{PN}/2$

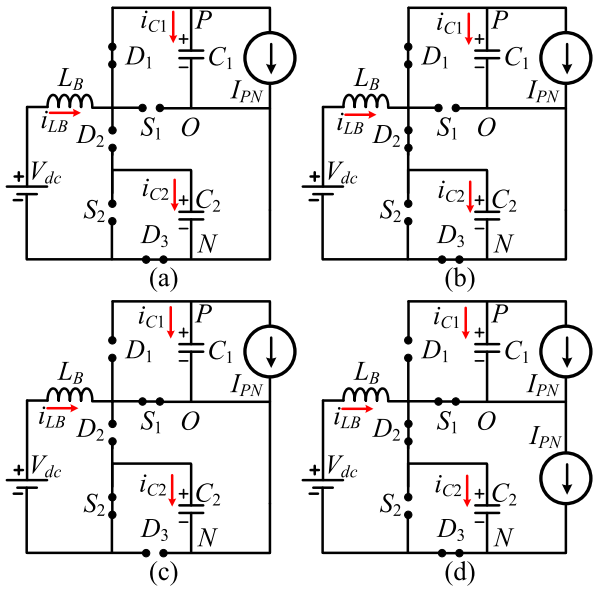

FIGURE 2. Operating modes of 3L-qSBFTI. (a) – (c) LST modes 1 – 3, (d) non-ST mode.

In non-ST mode, switch S_1 is turned on while switch S_2 is turned off, which reverse bias diode D_1 and forward bias diode D_2 and D_3 as shown in Fig. 2(d). The capacitor C_2 is charged from inductor L_B and input DC source V_{dc}, while capacitor C_1 is discharged. The voltage across inductor L_B and currents through capacitors C_1 and C_2 are expressed as:

$$\begin{cases} v_{LB} = L_B \dfrac{di_{LB}}{dt} = V_{dc} - V_{C2} \\ i_{C1} = C_1 \dfrac{dv_{C1}}{dt} = -I_{PN} \text{ and } i_{C2} = C_2 \dfrac{dv_{C2}}{dt} = I_{LB} - I_{PN} \end{cases} \tag{1}$$

where I_{PN} is equivalent current of inverter side.

In this mode, the FTI branch is able to generate three levels of output pole voltage V_{XO}, which are $+V_{C1}$, 0, and $-V_{C2}$, as listed in Table 1. These three voltage levels are denoted by "P," "O," and "N."

In LST modes 1 – 3, the lower switches S_{2X} and S_{4X} of the inverter legs are turned on which directly connects terminal "O" to terminal "N," as shown in Figs. 2(a) – 2(c). In these modes, the DC-link voltage, V_{PN}, is equal to the voltage of capacitor C_1. As a result, the inverter side is just able to generate two output voltage levels which are "P" and "O." Note that this LST state is added into P-type small vector, thus, the output voltage is unaffected by this insertion. For instance, assume that the inverter generates vector [POO] at output voltages. As a result, switches S_{1A}, S_{2A} of phase A, S_{2B}, S_{3B}, S_{2C}, and S_{3C} of phases B and C are turned on, simultaneously. The output pole voltages V_{AO}, V_{BO}, and V_{CO} reach values of $+V_{C1}$, 0-V, and 0-V, respectively. In order to insert LST state, switches S_{4X} of phase operating at state "O" are turned on. In this example, switches S_{4B}, and S_{4C} are triggered on beside above switches. In this case, the V_{AO}, V_{BO}, and V_{CO} still get $+V_{C1}$, 0-V, and 0-V. So, it can be concluded that the LST insertion can be used without affecting output voltage.

In LST modes 1 and 2, switches S_1 and S_2 are gated off, and diode D_3 is always forward biased. When capacitor C_1 voltage is smaller than capacitor C_2 voltage, diode D_1 is forward biased whereas diode D_2 is reverse biased, as shown in Fig. 2(a). Now, the capacitor C_1 is charged by inductor L_B and input source, while capacitor C_2 is disconnected from the power circuit. When capacitor C_1 voltage is charged to equal to capacitor C_2 voltage, LST mode 2, as presented in Fig. 2(b), is activated. Both diodes D_1 and D_2 are forward biased which connects both capacitors in parallel. Two capacitor currents and inverter side current share the inductor current I_{LB}. Assume that the voltages across both capacitors have very small oscillation, these capacitor voltages are self-balanced, approximately. In the proposed LST mode 2, when two capacitors C_1 and C_2 are connected in parallel, the currents through two capacitors are limited by the inductor current. As a result, the inrush current issue is not occurred unlike the traditional SC circuit discussed in [23]. The voltage across inductor L_B and currents of capacitors C_1 and C_2 are expressed as:

$$\begin{cases} v_{LB} = L_B \dfrac{di_{LB}}{dt} = V_{dc} - V_{C1} = V_{dc} - V_{C2} \\ i_{C1} + i_{C2} = C_1 \dfrac{dv_{C1}}{dt} + C_2 \dfrac{dv_{C2}}{dt} = I_{LB} - I_{PN} \end{cases} \tag{2}$$

In LST mode 3, the switches S_1 and S_2 are triggered on, and inductor L_B stores energy from input source and capacitor C_2, as depicted in Fig. 2(c). The following equations are obtained.

$$\begin{cases} v_{LB} = L_B \dfrac{di_{LB}}{dt} = V_{dc} + V_{C2} \\ i_{C1} = C_1 \dfrac{dv_{C1}}{dt} = -I_{PN} \text{ and } i_{C2} = C_2 \dfrac{dv_{C2}}{dt} = -I_{LB} \end{cases} \tag{3}$$

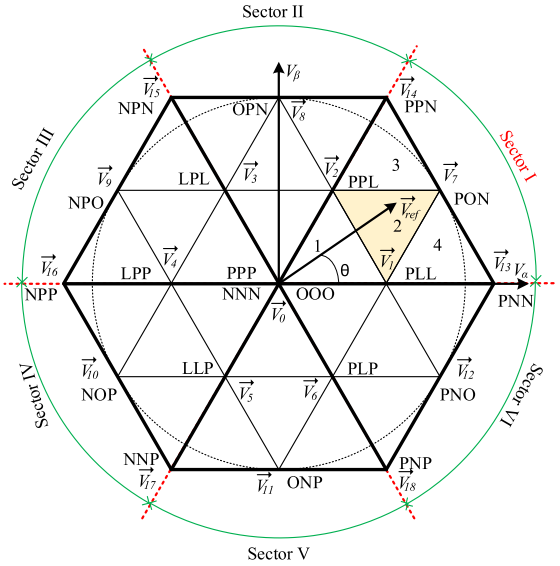

FIGURE 3. Space vector diagram of proposed control method.

B. SVM CONTROL STRATEGY

A space vector diagram (SVD) for the proposed SVM control method is drawn in Fig. 3. In this scheme, all N-type small vectors are removed from SVD, while all P-type small vectors are replaced by LST vectors. The symbol "*L*" in SVD denotes LST state. For example, vector "*PLL*" denotes that phase *A* generates state "*P*" whereas LST state is inserted into phases *B* and *C*. The proposed method divides the SVD into six sectors (I-VI) where each sector is divided into four regions (1 – 4). To analyze the operation of the proposed method, the output voltage vector $\vec{V}_{ref}$ is assumed to be located in region 2 of sector I. In this case, three candidate voltage vectors $\vec{V}_1, \vec{V}_2, \vec{V}_7$ are utilized to generate output voltage. The following equation are presented to show the relationship between these vectors.

$$\begin{cases} \vec{V}_{ref}.T_S = \dfrac{1}{\sqrt{3}} M V_{PN} e^{j\theta} T_S = \vec{V}_1.t_1 + \vec{V}_2.t_2 + \vec{V}_7.t_7 \\ T_S = t_1 + t_2 + t_7 \end{cases} \tag{4}$$

where T_S – switching period; M – modulation index, $M \leq 1$; t_1, t_2, and t_7 are respectively dwell-times of vectors $\vec{V}_1, \vec{V}_2, \vec{V}_7$.These dwell-times can be calculated like any traditional SVM control method as follow [24].

$$\begin{cases} t_1 = T_S - 2MT_S \sin(\theta) \\ t_2 = T_S - 2MT_S \sin(\pi/3 - \theta) \\ t_7 = 2MT_S \sin(\theta + \pi/3) - T_S. \end{cases} \tag{5}$$

The switching sequence of this region is selected as: [*PPL*]-[*PLL*]-[*PON*] and return, as shown in Fig. 4. The switch S_2 is turned on within LST states. Based on (5), the minimum of total dwell-times of LST vectors is expressed as $2(1-M)T_S$. Thus, the duty ratio D of switch S_2 must be defined as:

$$D \leq 2(1-M) \tag{6}$$

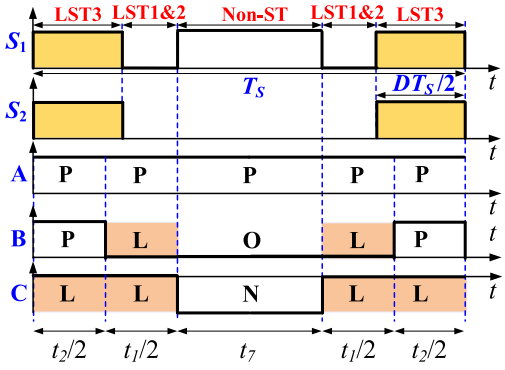

FIGURE 4. Switching sequence for region 2 of sector I, and control signals of switches S_1 and S_2.

C. STEADY-STATE ANALYSIS

As shown in Fig. 4, the time interval of LST mode 3 is expressed as DT_S, in any switching period. The rest time interval of sampling period T_S is the total time interval of LST modes 1 and 2, and non-ST mode. As discussed above, two capacitor voltages V_{C1} and V_{C2} are self-balanced. Therefore, the inductor L_B voltages in LST modes 1 and 2, and non-ST mode are equal. In steady-state, the average value of inductor voltage is zero, thus, capacitor C_1 and C_2 voltages are calculated as:

$$V_{C1} = V_{C2} = \frac{V_{dc}}{1-2D} \tag{7}$$

The boost factor, B, of the inverter is defined as:

$$B = \frac{V_{PN}}{V_{dc}} = \frac{V_{C1} + V_{C2}}{V_{dc}} = \frac{2}{1-2D} \tag{8}$$

The fundamental harmonic of output phase voltage ($V_{X,peak}$) is calculated as:

$$V_{X,peak} = \frac{1}{\sqrt{3}} M V_{PN} = \frac{2}{\sqrt{3}} \times \frac{M V_{dc}}{1-2D} \tag{9}$$

The voltage gain, G, of the inverter is expressed as:

$$G = \frac{V_{X,peak}}{V_{dc}/2} = \frac{4}{\sqrt{3}} \times \frac{M}{1-2D} \tag{10}$$

D. IMPLEMENTATION STEP

The flowchart of the proposed SVM method in any switching period T_S is shown as Fig. 5. In order to implement the proposed control method, the parameters of input voltage V_{dc}, DC-link voltage V_{PN}, and output voltage ($V_{X,peak}$, and ~~θ~~) must be given, firstly. Next, the duty ratio D and modulation index M are calculated by applying (8) and (9), respectively. Based on modulation index M and ~~θ~~, the location of reference vector (sector and region) is determined. The dwell-time calculation, switching sequence, and LST phases are obtained by the same way as section II-B. Finally, the PWM signals of all inverter switches are generated.

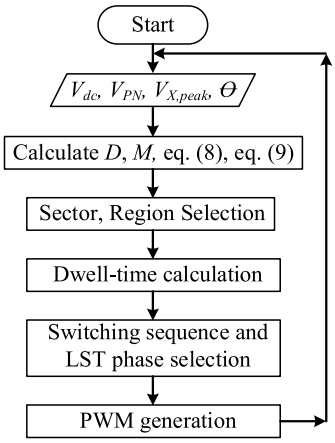

FIGURE 5. The flow-chart of the proposed SVM method in any switching period.

III. DESIGN GUIDELINES

A. INDUCTOR AND CAPACITOR DESIGNS

As the inductor L_B is attached to input DC source, the input current is equal to inductor current. Assuming that the inverter efficiency is defined as $\eta\%$, the average value of inductor current is expressed as $P_O/(\eta\% V_{dc})$, where P_O is output power. Based on (3) and (7), the inductor current ripple ΔI_{LB} is calculated as:

$$\Delta I_{LB} = \frac{2V_{dc}(1-D)DT_S}{L_B(1-2D)} \tag{11}$$

The inductor L_B current ripple must be smaller than $x\%$ of inductor current I_{LB}. Therefore, the inductor L_B is selected as:

$$L_B \geq \frac{2\eta\% V_{dc}^2(1-D)DT_S}{x\% P_O(1-2D)} \tag{12}$$

where $x\%$ is maximum acceptable inductor current ripple.

Based on (3), the capacitor voltage ripples ΔV_{C1} and ΔV_{C2} are calculated as:

$$\begin{cases} \Delta V_{C1} = \dfrac{I_{PN}DT_S}{C_1} \\ \Delta V_{C2} = \dfrac{I_{LB}DT_S}{C_2} = \dfrac{P_O DT_S}{\eta\% V_{dc} C_2} \end{cases} \tag{13}$$

Similarly, the capacitors C_1 and C_2 must be selected in term of $\Delta V_{Cj} \leq y\% V_{Cj}$ $(j = 1, 2)$. Therefore, capacitances of these capacitors are expressed as:

$$\begin{cases} V_{C1} \geq \dfrac{I_{PN}D(1-2D)T_S}{y\% V_{dc}} \\ V_{C2} \geq \dfrac{P_O D(1-2D)T_S}{y\%\eta\% V_{dc}^2} \end{cases} \tag{14}$$

where $y\%$ is maximum acceptable capacitor voltage ripple.

B. SEMICONDUCTOR DEVICE SELECTION

All semiconductor devices of qSB circuit and switches S_{2X}, S_{3X}, and S_{4X} are designed to block a half of DC-link voltage, $V_{PN}/2$. While switches S_{1X} of inverter side blocks full DC-link voltage when output pole voltage V_{XO} operates at state "N."

Diodes D_1 and D_3 are designed to transfer inductor L_B current in LST modes 1, 2 and non-ST mode, as shown in Fig. 2. Moreover, switches S_1, S_2, S_{2X}, and S_{4X} are also designed to carry I_{LB}, in LST mode 3. Therefore, the maximum values of diode D_1, D_3, and switch S_1, S_2, S_{2X}, S_{4X} currents are equal to maximum value of inductor current, $I_{LB,max}$, which is calculated as follows.

$$I_{LB,\max} = I_{LB} + \frac{\Delta I_{LB}}{2} = \frac{P_O}{\eta\% V_{dc}} + \frac{V_{dc}(1-D)DT_S}{L_B(1-2D)} \tag{15}$$

The maximum current through diode D_2 is obtained in non-ST mode, as shown in Fig. 2(d), which is expressed as:

$$I_{D2,\max} = I_{LB,\max} - I_{PN} = \frac{P_O}{\eta\% V_{dc}} + \frac{V_{dc}(1-D)DT_S}{L_B(1-2D)} - I_{PN} \tag{16}$$

Switches S_{1X} and S_{3X} of inverter side are designed to transfer inverter side current I_{PN}.

IV. POWER LOSS ESTIMATION

The conduction losses of inductor L_B (P_{LB}) and capacitors C_1 and C_2 ($P_{Cj}, j = 1, 2$) are calculated as:

$$\begin{cases} P_{LB} = r_{LB} I_{LB,RMS}^2 \\ P_{Cj} = r_{ESR} I_{Cj,RMS}^2; \quad j = 1, 2 \end{cases} \tag{17}$$

where r_{LB} and r_{ESR} are series resistors of inductor and capacitors, respectively.

The conduction losses of MOSFETs ($P_{S,cond}$) and diodes ($P_{D,cond}$) are calculated as follow.

$$\begin{cases} P_{S,cond} = r_{DS,on} I_{S,RMS}^2 \\ P_{D,cond} = V_F I_{D,AVG} \end{cases} \tag{18}$$

where $r_{DS,on}$ and V_F are on-resistor and forward-voltage of switch S and diode D.

In any switching period, diode D_1 has two switching actions while diodes D_2 and D_3 have one switching action. These diodes block $+V_{PN}/2$, thus, reverse recovery losses of these diodes are calculated as:

$$\begin{cases} P_{rr,D1} = 2 \times \dfrac{V_{PN}}{2} \dfrac{Q_{rr}}{T_s} \\ P_{rr,D2} = P_{rr,D3} = \dfrac{V_{PN}}{2} \dfrac{Q_{rr}}{T_s} \end{cases} \tag{19}$$

where Q_{rr} is reverse recovery charge of diode.

All switches of the proposed inverter are switching at $+V_{PN}/2$. In any switching period T_S, the switches S_1 and S_2 have two and one switching actions, respectively. The switch S_1 turned on/off at inductor L_B current in LST mode 3, and $(I_{LB} - I_{PN})$ in non-ST mode. While the switch S_2 is just switched at inductor L_B current. Therefore, the switching

TABLE 2. Simulation and experimental parameters.

Parameter/ Components		Values
DC input source	V_{dc}	90 V – 130 V
Output frequency	f_O	50 Hz
Switching frequency	f_s	10 kHz
Boost inductor	L_B, r_{LB}	3 mH/20 A, 0.3-Ω
Capacitors	C_1, C_2, r_{ESR}	2 mF/400 V, 50-mΩ
LC filter	L_f and C_f	3 mH and 10 μF
Resistor load	R	40-Ω
Active switches	S_1, S_2, $S_{1X} - S_{4X}$	MOSFETs 60R060P7 (650-V, 60-mΩ)
Diodes	$D_1 - D_3$	UJ3D1250K2 (1200-V, 1.5-V)

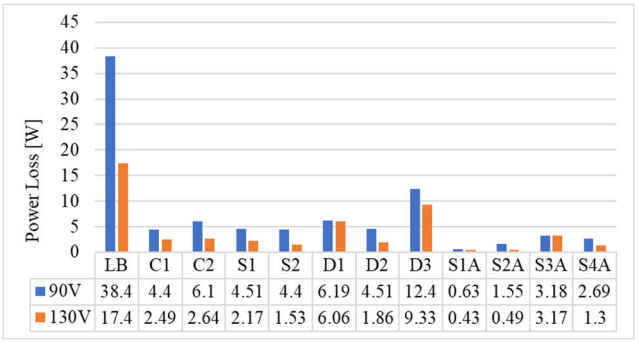

FIGURE 6. Power loss contribution of the proposed inverter at 1-kW under 90-V and 130-V input voltages.

losses of these switches are calculated as:

$$\begin{cases} P_{S1,sw} = \dfrac{1}{2}\dfrac{V_{PN}}{2}(2I_{LB} - I_{PN})\dfrac{t_{ru} + t_{fu} + t_{ri} + t_{fi}}{T_S} \\ P_{S2,sw} = \dfrac{1}{2}\dfrac{V_{PN}}{2} I_{LB}\dfrac{t_{ru} + t_{fu} + t_{ri} + t_{fi}}{T_S} \end{cases} \tag{20}$$

where t_{ru}, t_{fu}, t_{ri}, t_{fi} are voltage rise-time, voltage fall-time, current rise-time, and current fall-time of MOSFET which are determined by MOSFET's datasheet.

The switch S_{4A} has one switching action per switching period T_S, when LST state is added to phase A. In any output period T_O, phase A is used to insert LST in 1/3 time-interval of T_O. Note that the LST insertion just generates switching loss at S_{4X} when phase X has larger time-interval of LST state. For example, when switching pattern shown in Fig. 4 is adopted, the LST state only generates switching loss at S_{4C}. The switching loss at S_{4B} is zero, in this case. Thus, switch S_{4A} has one switching action in any switching period when reference vector locates in sectors III and IV. In LST mode, switch S_{4A} is switched on at $(I_{LB} - I_{PN})$ and switched off at $(I_{LB} - I_{PN})/2$. In non-ST state, the switch S_{4A} has one switching event per T_S in negative half cycle of phase A current I_A ($\theta \in [\pi/23\pi/2]\theta \in [\pi/23\pi/2]$). In this time interval, the switch S_{4A} is switched at $-I_A$. The switching loss of switch S_{4A} is calculated as:

$$\begin{aligned} P_{S4A,sw} = \frac{1}{2\pi}\frac{1}{2}\frac{V_{PN}}{2}\Big[& \int_{2\pi/3}^{4\pi/3} (I_{LB} - I_{PN})\frac{t_{fu} + t_{ri}}{T_S} d\theta \\ & + \int_{2\pi/3}^{4\pi/3} \frac{(I_{LB} - I_{PN})}{2}\frac{t_{fi} + t_{ru}}{T_S} d\theta \\ & - \int_{\pi/2}^{3\pi/2} I_A \frac{t_{ru} + t_{fu} + t_{ri} + t_{fi}}{T_S} d\theta \Big] \end{aligned} \tag{21}$$

In positive half cycle of output current I_A, the switch S_{1A} has one switching event in any switching period, and the switching current is I_A. Thus, the switching loss of switch S_{1A} is calculated as:

$$P_{S1A,sw} = \frac{1}{2\pi}\int_{-\pi/2}^{\pi/2} \frac{1}{2}\frac{V_{PN}}{2} I_A \frac{t_{ru} + t_{fu} + t_{ri} + t_{fi}}{T_S} d\theta \tag{22}$$

Body diodes of switches S_{1A} and S_{4A} have no reverse recovery loss, and switches S_{2A} and S_{3A} have no switching loss. In positive half cycle of I_A, body diode D_{3A} of switch S_{3A} has one switching action per switching period. Therefore, reverse recovery loss of anti-parallel diode D_{3A} is calculated as follow.

$$P_{rr,D3A} = \frac{1}{2\pi}\int_{-\pi/2}^{\pi/2} \frac{V_{PN}}{2}\frac{Q_{rr}}{T_s} d\theta \tag{23}$$

Dead-time loss is very small and can be ignored. The conduction loss and switching loss of other inverter legs are calculated by the same way as phase A loss.

The power loss contribution of the inverter is shown in Fig. 6. The parameters of inverter are listed in Table 2. It can be seen that the power loss of inductor L_B accounts for the largest proportion. For semiconductor loss of boost circuit, the diode D_3 has the largest loss. For loss of inverter branch, the switches S_{3X} and S_{4X} have higher power loss than S_{1X} and S_{2X}. This is because the switch S_{4X} transfers more current value (inductor current) than other switches. Furthermore, switch S_{3X} has high power loss because it has reverse recovery loss of anti-parallel diode.

The efficiency of the proposed inverter in both calculation and simulation are shown in Fig. 7. Furthermore, the simulation results of efficiency of conventional 3L-qSBT^{2}I in [22] is also attached in Fig. 7. Note that the simulation results are obtained with the help of PLCES software. It can be seen that when the input voltage is increased, the system efficiency is also increased. This is because the input current is decreased which leads to decrease conduction losses of inductor and semiconductors. The different between the calculation and simulation for the proposed inverter is very small. Compared to conventional 3L-qSBT^{2}I, the proposed 3L-qSBFTI exhibits higher efficiency in both cases of input voltages, as shown in Fig. 7. Specifically, at 2-kW output

TABLE 3. Overall comparison.

	3L-FC-SSI [21]	ZS-NPC-1LC [14]	AEMZS-3LTI [19]	RC^2-AIS-TLI [23]	3L-qSBT^{2}I [22]	AqZS-TLI [25]	1S-BD-T^{2}I [26]	Proposed Inverter
No. Switches *	0	0	0	1	2	1	1	2
No. Diodes *	3	2	3	2	4	3	1	3
No. Inductors *	1	2	2	1	1	2	1	1
No. Capacitors*	1	2	4	2	2	2	2	2
Self-balanced neutral-voltage	NA	No	No	Yes / having inrush current	No	No	Yes / having inrush current	Yes / no inrush current
Input current	Continuous	Discontinuous	Continuous	Continuous	Continuous	Continuous	Continuous	Continuous
ST duty ratio, D	$2M-1$	$1-M$	$1-M$	$1-M$	$1-M$	$1-M$	$2(1-M)$	$2(1-M)$
Boost factor, B**	$2/(1-D)$	$1/(1-2D)$	$2/(1-2D)$	$2/(1-2D)$	$2/(1-2D)$	$2/(1-2D)$	$2/(1-D)$	$2/(1-2D)$
Voltage gain, G**	$1.15MB$	$1.15MB$	$1.15MB$	$1.15MB$	$1.15MB$	$1.15MB$	$1.15MB$	$1.15MB$
V_C/V_{dc}*,**	B	$(1-D)B$	$(1-D)B/2$	$B/2$	$B/2$	$B/2$	$B/2$	$B/2$
V_S/V_{dc}*	NA	NA	NA	$B/2$	$B/2$	B	$B/2$	$B/2$
V_D/V_{dc}*,**	B	$B/2$	$B/2$	$B/2$	$B/2$	B	$B/2$	$B/2$
$\Delta I_{LB}{\cdot}L_B{\cdot}f_S/V_{dc}$	$D/2$	$D(1-D)B$	$D(1-D)B/2$	$D(1-D)B$	$D/2$	$D(1-D)B$	D	$D(1-D)B$

*: only apply for boost circuit; ** only consider maximum value, NA: not applicable

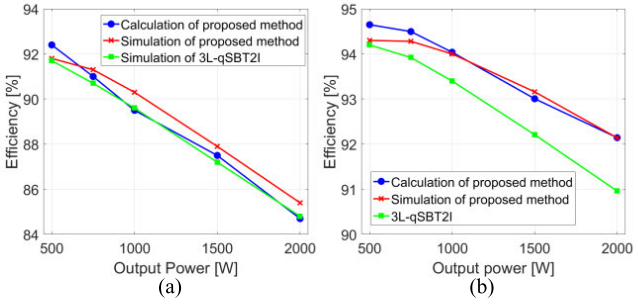

FIGURE 7. Efficiency comparison between the proposed inverter and conventional 3L-qSBT^{2}I. (a) 90-V of Vdc, and (b) 130-V of V_{dc}.

power, the proposed inverter can improve efficiency by 0.4% and 0.8% for 90-V and 130-V input voltages, respectively, compared to the 3L-qSBT^{2}I, as shown in Fig. 7.

V. COMPARATIVE ANALYSIS

To highlight the contribution of the proposed inverter, a comparison between the introduced inverter and some existing inverters, which are the 3L-FC-SSI topology in [21], ZS-NPC-1LC inverter in [14], AEMZS-3LTI topology in [19], RC^2-AIS-TLI topology in [23], 3L-qSBT^{2}I topology in [22], active-qZS-TLI (AqZS-TLI) in [25] and single-stage boost-derived T^{2}I (1S-BD-T^{2}I) in [26], has been presented. These topologies use conventional three-level inverters (TLIs) behind the boost circuit. Because the comparison between FTI and conventional TLIs has been done in [3], so this section just focuses on boost circuit comparison.

A. OVERALL COMPARISON

The overall comparison has been listed in Table 3. Among these topologies, the 1S-BD-T^{2}I uses the smallest number of components. On the other hand, the ZS-NPC-1LC and AEMZS-3LTI do not use active switches in impedance-source network. Instead, they use more inductors and capacitors. As shown in Table 3, ZS-NPC-1LC, AqZS-TLI and AEMZS-3LTI use one more inductor compared to the proposed inverter. Moreover, the AEMZS-3LTI utilizes two more capacitors than the proposed inverter. Compared to RC^2-AIS-TLI, the proposed 3L-qSBFTI has one more diode and one more active switch in the impedance-source network. The introduced topology can save one diode compared to 3L-qSBT^{2}I.

The proposed inverter, RC^2-AIS-TLI, and 1S-BD-T^{2}I can balance capacitor voltages by themselves. While the others must use corresponding control techniques to achieve neutral-point voltage balancing, which makes the control process complicate. However, the methods for RC^2-AIS-TLI and 1S-BD-T^{2}I directly connect two capacitors in parallel, which generates high inrush current through semiconductor devices. For the proposed topology, the capacitor currents occurring when they are connected in parallel are limited by inductor current. As a result, it eliminates the inrush current issue found in [23] and [26].

To boost the DC-link voltage, the inverters in [22] and [23] require zero-vector to insert ST state. Therefore, the maximum slew rate *dv/dt* of output line-to-line voltage is DC-link voltage. While the proposed inverter and inverters in [14], [19], [21], and [26] do not need zero vector to boost DC-link voltage. As a result, the slew rate *dv/dt* of output line-to-line voltage is just a half of DC-link, which improves the THD of output voltage compared to the inverters in [22] and [23].

B. VOLTAGE GAIN AND COMPONENT VOLTAGE RATING COMPARISONS

The results of boost factor, voltage gain, capacitor/boost switch voltage stresses, and inductor current profile investigations are presented in Fig. 8. As shown in Fig. 8(a), the boost factors of the proposed inverter and the works in [19], [22], [23], and [25] are equal which are larger than other inverters. However, as listed in Table 3, for the same value of modulation index M, the utilization of ST duty

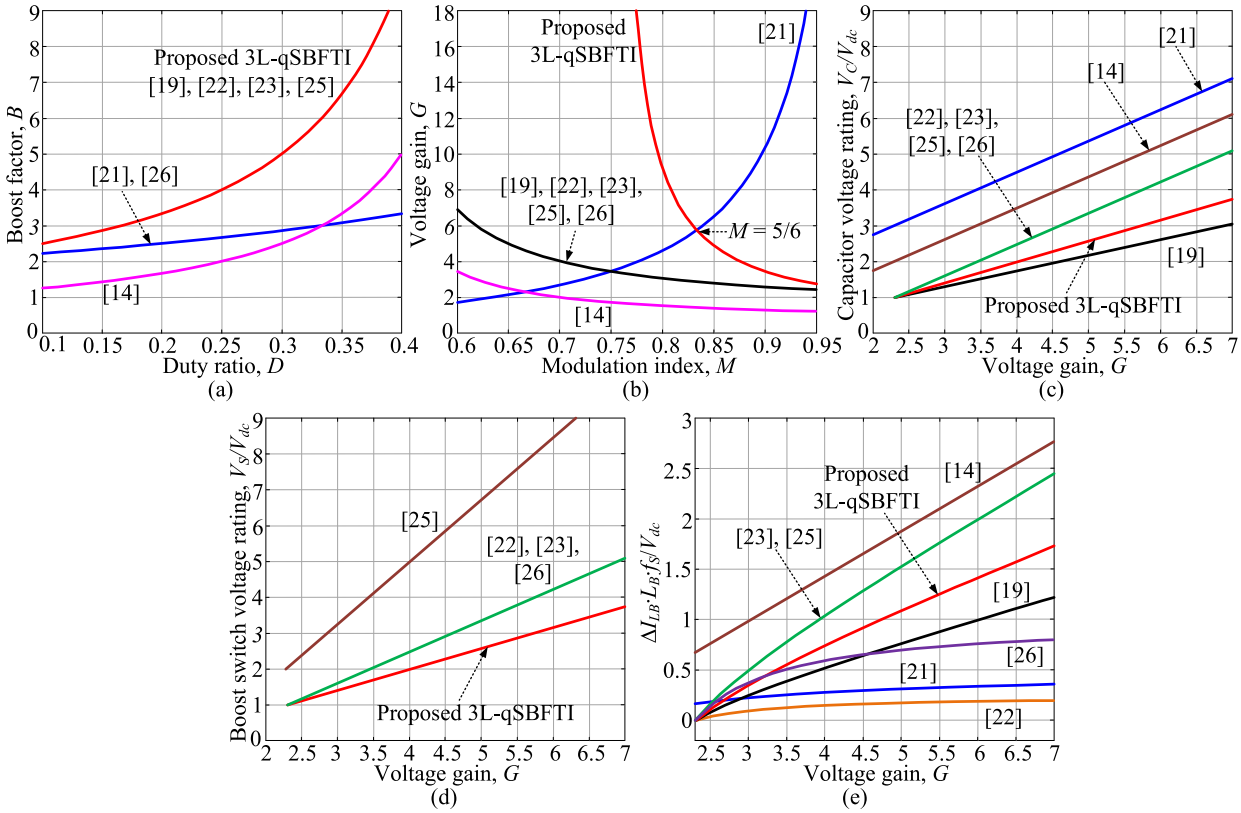

FIGURE 8. Comparison between proposed inverter and others. (a) duty ratio D vs. boost factor, (b) modulation index vs. voltage gain, (c) voltage gain vs. capacitor voltage stress, (d) voltage gain vs boost switch voltage rating, and (e) voltage gain vs. $\Delta I_{LB} \cdot L_B \cdot f_S / V_{dc}$.

ratio D of the proposed method is higher than that of others, so the proposed inverter has higher voltage gain than the inverters in [14], [19], [22], [23], and [25]. In the range of low modulation index ($M \leq 5/6$), the voltage gain of the proposed inverter is higher than 3L-FC-SSI, as shown in Fig. 8(b). In applications using a voltage source inverter following a front-end DC-DC boost converter like PV or fuel cell applications, the DC-link voltage is usually controlled to be 350-V or 400-V for 110-V_{RMS} output voltage [14], [15]. Similarly, the DC-link voltage is fixed at 700-V or 800-V for 220-V_{RMS} output voltage [4]. In these cases, the modulation index is not larger than $5/6 = 0.83$. It demonstrates that the proposed inverter can be used for many practical applications.

With higher voltage gain, the proposed topology can use a larger modulation index M than others for the same value of G. Because the DC-link voltage V_{PN} equals to $2V_{X,peak}/(1.15M)$, so using a higher modulation index M makes the proposed inverter have lower DC-link voltage. As a result, the proposed inverter has lower capacitor voltage rating, as shown in Fig. 8(c). Furthermore, having smaller V_{PN} also leads to have a smaller semiconductor device voltage stress, as presented in Fig. 8(d). Note that the AEMZS-3LTI has lower capacitor voltage stress than the proposed topology because it uses four capacitors instead of two capacitors for the proposed inverter.

The inductor current profile ΔI_{LB} is investigated in terms of the same input voltage, switching frequency f_S, and inductance L_B. It can be seen in Fig. 8(e) that the proposed inverter has a smaller inductor current ripple than ZS-NPC-1LC and RC^2-AIS-TLI. Compared to AEMZS-3LTLI, 3L-FC-SSI, and 3L-qSBT^{2}I, the proposed inverter has a worse inductor current profile.

In summary, the main contributions of the proposed topology can be listed as: 1) improving boost factor and voltage gain, 2) reducing component voltage rating, and 3) self-balanced capacitor voltages without inrush current.

VI. SIMULATION AND EXPERIMENTAL RESULTS

A. SIMULATION RESULTS

The simulation results have been presented with the help of PSIM software to verify the operation of the proposed inverter. Parameters used in simulation are shown in Table 2. The simulation is conducted under 90-V input voltage. The modulation index M and ST duty ratio D are set to 0.68 and 0.275, respectively. Two capacitor voltages, V_{C1} and V_{C2} are boosted to 199-V and 200-V, as shown in Fig. 9(a). Different between these capacitor voltages is very small and can be ignored. The zoom-in waveforms of capacitor voltages and their currents are illustrated in Fig. 9(b).

The DC-link voltage V_{PN} equals to capacitor C_1 voltage during LST modes, and twice of capacitor voltages in

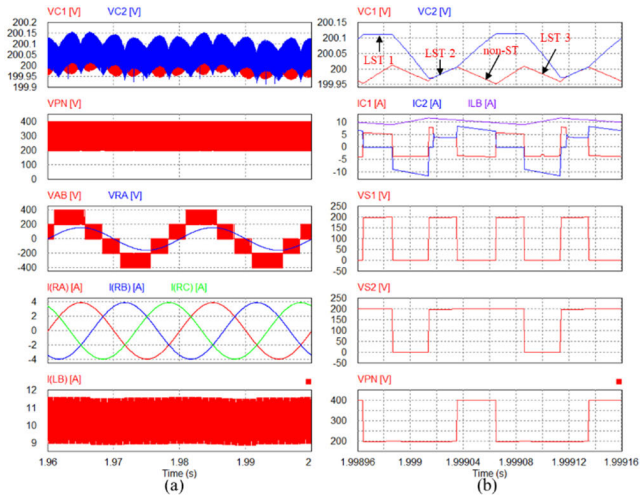

FIGURE 9. Simulation results under 90-V input voltage.

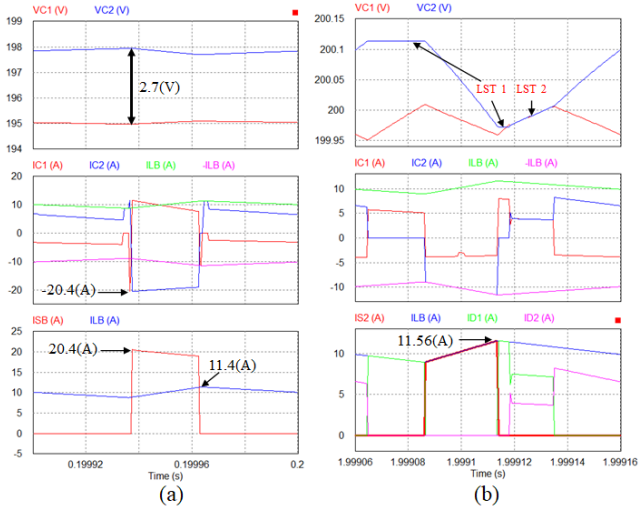

FIGURE 10. Simulation results in one switching period: (a) conventional SC-based inverter in [23], (b) proposed inverter.

non-ST mode, as shown in Fig. 9(b). The peak-value of V_{PN} was measured at 400-V. The output line-to-line voltage V_{AB} has five-voltage levels which are 0-V, $\pm V_{C1}$/or $\pm$ V_{C2}, and $\pm V_{PN}$, as illustrated in Fig. 9(a). Output load voltage V_{RA} is sinusoidal waveform with the help of three-phase low-pass filter (3mH and 10μF) as listed in Table 2. The RMS values of output load voltage and current are measured as 110-V_{RMS} and 2.77-A_{RMS}, respectively. The inductor current ripple is 2.7-A, approximately. It is linearly increased in LST mode 3 and linearly decreased in other operating modes, as shown in Fig. 9(b). Its average current is measured as 10.2-A.

A comparison between the proposed inverter and the conventional SC-based inverter in [23] is conducted to highlight the novelty of the proposed SC structure. The simulation results for the conventional SC-based inverter in [23] are presented in Fig. 10(a). It should be noted that the parasitic resistances of capacitors and switches of [23] are set

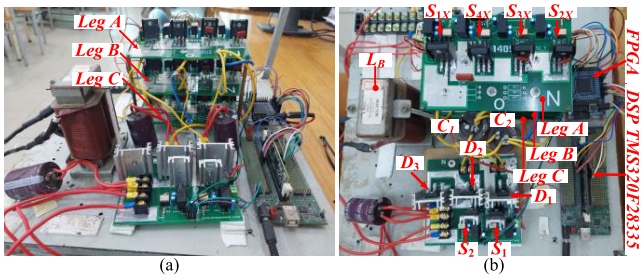

FIGURE 11. Experimental prototype. (a) side-view, (b) top-view.

to 50-mΩ for this simulation. As seen in the Fig. 10(a), the current through capacitors and semiconductor devices are much larger than inductor current. This high inrush current is generated because two capacitors of [23] are directly connected in parallel. Furthermore, the parasitic of devices create a voltage difference between two capacitors, as shown in Fig. 10(a), which does not go to zero.

As shown in Fig. 10(b), for the proposed inverter, when the voltage of capacitor C_1 is smaller than V_{C2}, LST mode 1 is activated which forward biased diode D_1 and reverse biased diode D_2. This mode charges for capacitor C_1 by the current $(I_{LB} - I_{PN})$ while it maintains the voltage of capacitor C_2 as constant. When the voltage of capacitor C_1 is charged to be equal to the voltage of capacitor C_2, LST mode 1 is stopped, and LST mode 2 is activated. Both diodes D_1 and D_2 are forward biased and two capacitors share the current $(I_{LB} - I_{PN})$, with $I_{C1} + I_{C2} = I_{LB} - I_{PN}$. As a result, the capacitor/semiconductor devices currents are limited by inductor current I_{LB} when these capacitors are connected in parallel. Therefore, compared to the conventional SC-based inverter in [23], there is no huge currents through devices. Furthermore, the capacitor voltage different is very small and approximately zero.

B. EXPERIMENTAL RESULTS

The proposed inverter is further verified by experiment with the help of the experimental prototype shown in Fig. 11. DSP TMS320F28335 and FPGA Cyclone II EP2C5T144C8 are utilized to control the inverter. The DSP TMS320F28335 is used to generate PWM for proposed SVM method. Based on these PWM signals, the FPGA performs logical operations (AND, OR, ...) to generate control signals of inverter switches. All MOSFETs 60R060P7 are applied for active switches of the inverter, which are controlled by isolated IC TLP250. Diodes UJ3D1250K2 are applied for diodes D_1–D_3. The proposed inverter is tested under 90-V and 130-V input voltages. The experimental results for these cases are presented in Figs. 12 and 13, respectively. The summary of experimental results is listed in Table 4. The modulation index M is set to 0.68 for two cases, while ST duty ratio D is set as 0.275 for 90-V of V_{dc} and 0.18 for 130-V of V_{dc}.

When the inverter generates values $+V_{PN}/2$ and 0-V at output voltage V_{XO}, switch S_{2X} is always turned on. Therefore,

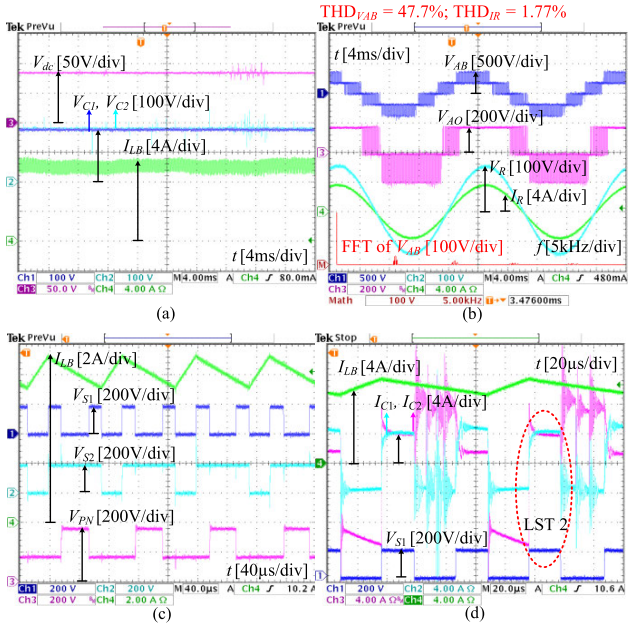

FIGURE 12. Experimental results under 90-V input voltage.

TABLE 4. Summary of simulation and experimental results.

	V_{dc} = 90-V		V_{dc} = 130-V	
	Sim.	Exp.	Sim.	Exp.
V_{C1}	199-V	177-V	203-V	183-V
V_{C2}	200-V	179-V	203-V	186-V
V_{RA}	110-V_{RMS}	104-V_{RMS}	110-V_{RMS}	109-V
I_{RA}	2.77-A_{RMS}	2.55-A	2.77-A	2.66-A
THD$_{VAB}$	42.49%	47.7%	42.7%	46.6%
THD$_{IRA}$	0.259%	1.77%	0.262%	1.7%

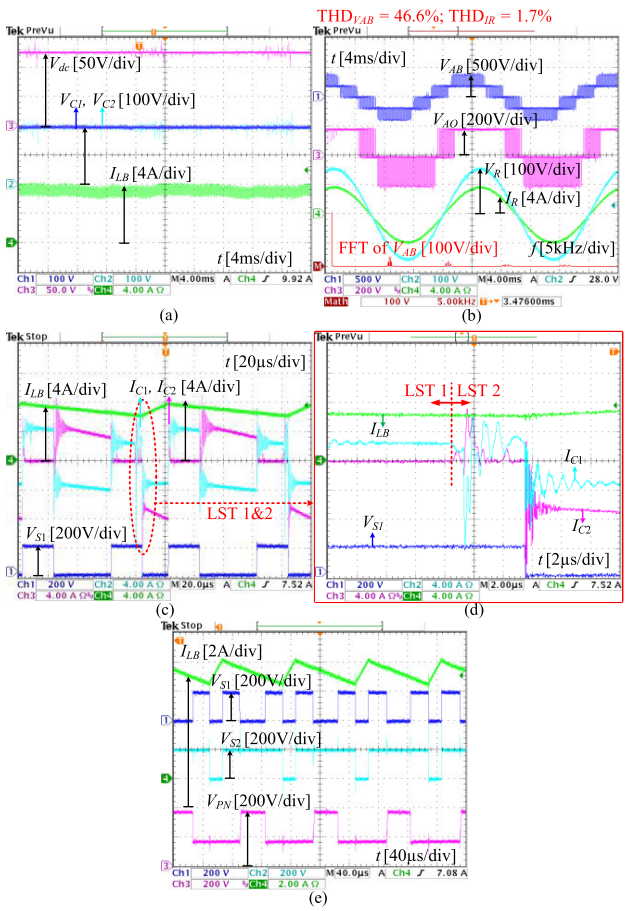

FIGURE 13. Experimental results under 130-V input voltage.

if switches S_{1X} and S_{3X} are simultaneously turned on, the capacitor C_1 is shorted which generates a short-circuit current through S_{1X}, S_{2X} and S_{3X}. It is very harmful to the whole inverter. So, dead-time controller is used for switches S_{1X} and S_{3X}. In this experiment, the dead-time is selected as 1% of switching period, which is 1 μs. Unlike S_{1X} and S_{3X}, the LST state generated by turning on S_{2X} and S_{4X} is allowed in this inverter. Moreover, the switches S_1 and S_2 of boost circuit are also triggered on in this LST state. Therefore, dead-time controller is not needed for these switches.

From 90-V input voltage, the capacitor C_1 and C_2 voltages are boosted to 177-V and 179-V, as illustrated in Fig. 12(a). The different between these capacitors is just 2-V, which is very small and can be ignored. Therefore, it can be concluded that these capacitor voltages are self-balanced. The peak-value of DC-link voltage is the sum of these capacitor voltages which is measured as 356-V, as shown in Fig. 12(c). The top of output line-to-line voltage is varied from zero to V_{PN}, as shown in Fig. 12(b). Based on FFT wave-form of V_{AB}, THD value of output voltage V_{AB} is calculated as 47.7%. THD of output load current is measured as 1.77%. The RMS value of output load voltage and current are measured as 104-V_{RMS} and 2.55-A_{RMS}, respectively. With the proposed SVM technique, the output pole voltage V_{AO} is clamped to terminal "P" in one-third of the output period, as illustrated in Fig. 12(b). In LST mode 3 which is denoted by zero-values of V_{S1} and V_{S2}, the current of inductor L_B increases linearly. In the rest time interval of one switching period, I_{LB} is decreased linearly, as illustrated in Fig. 12(c). The average value of I_{LB} is 10.1-A. The currents of capacitors C_1 and C_2 are presented in Fig. 12(d). It can be seen that these capacitor currents are equal in LST mode 2, which ensures neutral-voltage balancing. Because the experimental prototype is not optimally designed, an unexpected ringing occurs at capacitor currents due to stray inductors and capacitors of power circuit.

Under 130-V of V_{dc} as shown in Fig. 13(a), the V_{C1} and V_{C2} are measured as 183-V and 186-V, which are still balanced with small different as 3-V. With these capacitor voltages, the output load voltage and current achieve 109-V_{RMS} and 2.66-A_{RMS}. The average inductor current I_{LB} is measured as 7.06-A. The FFT of output line-line voltage is presented as Fig. 13(b). Based on this FFT wave-form, the THD of V_{AB} is calculated as 46.6%. The THD of the output load current is 1.7%. The current wave-forms of I_{C1} and I_{C2} are illustrated in Figs. 13(c) and 13(d). It can be seen that the I_{C1} is positive whereas the I_{C2} zero during LST mode 1. In LST mode 2, these capacitors share their currents. As a result, capacitor C_1 and C_2 voltages are still self-balanced.

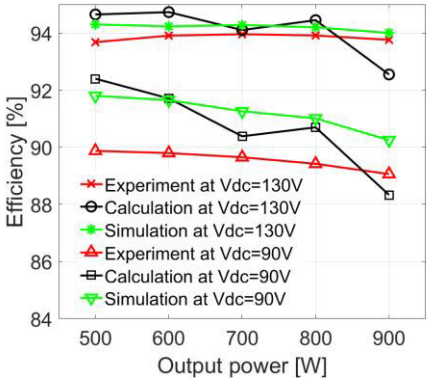

FIGURE 14. Experimental, simulation and calculation efficiency of the proposed inverter under 130-V and 90-V of input voltages.

The experimental, simulation and calculation results for efficiency of the proposed inverter under 130-V and 90-V of input voltages are shown in Fig. 14. The WT3000E power analyzer is used to measure system efficiency. The PLECS software is used to simulation inverter efficiency. The proposed inverter obtains 89% efficiency at 90-V of V_{dc} and 93.7% efficiency at 90-V of V_{dc} with 900-W output power. It still has a small different between simulation, calculation and experiment. However, this different is very small.

VII. CONCLUSION

A new topology of 3L-qSBFTI based on SC structure has been presented. The proposed inverter can limit the inrush current when two capacitors are connected in parallel. As a result, the boost factor and voltage gain of the inverter are significantly improved without increasing current stress on semiconductor devices like any traditional SC-based inverters. The SVM scheme has been presented to control the introduced inverter. Under this strategy, all small vectors are replaced by LST vectors. The ST state of the boost circuit, now, is inserted within LST states to improve ST duty ratio utilization. Accordingly, it can enhance the ST duty ratio to twice of that in conventional ISIs with the same modulation index. The comparison studies about boost factor, voltage gain, component voltage rating are presented to highlight the advantages of the proposed inverter. Because of high voltage gain and boost factor, the proposed inverter can operate with higher modulation index and lower duty ratio of boost switches. It makes the proposed inverter have better performance in low voltage range, low power compared to other single-stage inverters. However, like any SC based inverter, in high voltage range, the performance of proposed inverter is lower than that in low voltage range. Thus, the proposed in inverter is suitable for low voltage applications like PV, fuel cell applications. The simulation and experimental results are also presented to further verify the discussed theory. In the future, an optimal inverter design for PV grid-connected application will be conducted. Moreover, the small-signal analysis will be considered which helps to design controller for the introduced inverter.

NOMENCLATURE

V_{dc}	Input voltage.
V_{LB}	Inductor L_B voltage.
V_{C1}, V_{C2}	Capacitor C_1 and C_2 voltages.
V_{PN}	DC-link voltage.
$V_{X,\text{peak}}$	Peak-value of output load voltage.
V_{AB}	Output line-to-line voltage.
V_{AO}	Output pole voltage.
V_F	Forward-voltage of diode D.
I_{LB}	Inductor L_B current.
I_{C1}, I_{C2}	Capacitor C_1 and C_2 currents.
I_{PN}	Equivalent inverter side current.
I_{RA}	Output load current.
I_S, I_D	Currents of switch S and diode D.
T_S	Switching period.
T_O	Output load voltage/current period.
t_1, t_2, t_7	On-times of $\vec{V}_1$, $\vec{V}_2$, $\vec{V}_7$.
M	Modulation index.
D	Duty ratio of S_2.
Θ	Phase angle of reference vector.
B	Boost factor.
G	Voltage gain.
$\eta\%$	Inverter efficiency.
$x\%$	Maximum acceptable inductor current ripple.
$y\%$	Maximum acceptable capacitor voltage ripple.
P_O	Output power.
P_{LB}, P_{Cj}	Inductor L_B and capacitor C_j power loss.
$P_{S,\text{cond}}$	Conduction loss of switch S.
$P_{S,\text{sw}}$	Switching loss of switch S.
$P_{D,\text{cond}}$	Conduction loss of diode D.
P_{rr}	Reverse recovery loss.
$R_{DS,\text{on}}$	On-resistor of switch S.
Q_{rr}	Reverse recovery loss.
t_{ru}, t_{fu}, t_{ri}, t_{fi}	Voltage rise-time, voltage fall-time, current rise-time, and current fall-time of MOSFET.

ABBREVIATIONS

3L	Three-level.
qSBFTI	Quasi-switched boost F-type inverter.
ISI	Impedance-source inverters.
SC	Switched-capacitor.
LST	Lower-shoot-through.
MLI	Multi-level inverter.
NPCI	Neutral-point clamped inverter.
T^2I	T-type inverter.
FTI	F-type inverter.
PV	Photovoltaic.
VSI	Voltage-source inverter.
ST	Shoot-through.
ZS	Z-source.

ZSI	Z-source inverter.
qZSI	Quasi-Z-source inverter.
AEMZS	Asymmetrical embedded modified Z-source.
FST	Full shoot-through.
UST	Upper shoot-through.
FC-SSI	Flying capacitors split-source inverter.
qSBI	Quasi-switched boost inverter.
RC^2-AIS	Reduced component count active impedance-source.
TLI	Three-level inverter.
THD	Total harmonic distortion.
PI	Proportional-integral.
SVM	Space-vector modulation.
SVD	Space vector diagram.
1S-BD	Single-stage boost-derived.

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