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RESEARCH ARTICLE

Modeling Insights Into the Assembly Challenges of Focal Plane Arrays

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ABSTRACT Ongoing technological advances in photodetector material growth and processing, readout integrated circuits, and robust hybridization (packaging) methods for assembling high-resolution and small-pitch size pixel arrays are the main enabling factors for pushing the frontiers of high-performance Focal Plane Array (FPA) technologies for imaging systems. This paper details the development of analytical and numerical models and demonstrates their use to generate insights into the feasibility of two flip-chip assembly processes for packaging infrared (IR) detector chips. The modeling studies focus on the challenges of forming the indium interconnection arrays in the case of the FPA technologies using Group III-V compound semiconductor materials and ultra-fine pitch pixel array layouts. The accurate alignment of the IR detector chip onto the readout chip in the case of high-density pixel architectures is a critical requirement for the packaging process. To gain a better understanding of this requirement, which has a clear implication for the quality and subsequent reliability performance of the FPA, compression, and reflow bonding process models are developed using suitable modeling approaches and methods and then demonstrated for two distinctive focal plane array design configurations. The novelty of this work is in the developed modeling capabilities utilizing different computational methods, from large deformation and contact analysis finite element to energy-based and harmonic motion mechanics, to characterize and optimize the mechanical and dynamic non-linear behavior of the indium solder joints and their formation during FPA packaging. The feasibility of bonding techniques for different resolution FPAs and under flip-chip misalignment conditions is assessed. The modeling results pointed to a very strict, sub-micrometer flip-chip placement accuracy requirement for the assembly of FPAs with ultra-fine indium bump array resolution.

INDEX TERMS IR detectors, focal plane array, compression bonding simulation, reflow self-alignment modeling, indium joints, ultra-fine pitch flip chip assembly, compound semiconductors.

I. INTRODUCTION

Infrared imaging systems utilizing focal plane arrays have been traditionally developed to meet the demands of military applications such as target acquisition, night vision, weapon and missile seekers, and gas chemical composition measurements. However, there is a growing trend in the past two decades of the technology also expanding into the commercial market. FPAs are increasingly designed, fabricated, and used in a wider range of applications, from medical diagnostics and industrial process control to security and surveillance to astronomy and civil space applications [1], [2], [3], [4]. There has been substantial research and development in IR detectors over the past 20 years, particularly in the context of their miniaturization, detector material developments (namely the use of compound semiconductors), and the design and fabrication of fine-pitch pixel arrays [5], [6], [7]. Current developments in IR detector and FPA technologies are driven by trends and demands for improved sensitivity and resolution of imaging systems, continuing advances

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in sensing material compositions and their processing, and needs for high-yield low-cost fabrication capabilities [8], [9], [10], [11]. For example, investigations by Teng et al. focused on a novel metalorganic chemical vapor deposition method for growing infrared InAs/GaSb superlattice focal plane arrays [10], and Liu et al. reported the successful implementation of an improved CMOS process with a four-layer stack capacitor for the readout integrated circuit (ROIC) chip and demonstrated an FPA ROIC with improved dynamic range [11].

A Focal Plane Array is a sensing device of infrared radiation (IR) that has an array of light-sensing pixels at the focal plane of a lens. The pixels detect incoming infrared radiation and convert the photons into respective electrical signals to form an image. An FPA comprises two parts: (1) *the IR detector array chip*, which is the infrared-sensing element of the sensor, and (2) *the readout integrated circuit* (ROIC), which is the signal-processing component.

FPA packaging - known also as hybridization, remains a key challenge for the industry. This is the process of physical assembly through flip-chip bonding and electrical integration of the IR detector chip and the ROIC. Indium solder is the industry standard for FPA interconnection material [12]. Indium is ductile and malleable which is advantageous in the context of both FPA assembly with compression bonding and in-service operation at cryogenic temperature. This material has also a very low melting point (430K) which in the case of reflow assembly provides a much more favorable reflow profile compared to other solder alternatives. Although the assembly techniques and equipment for indium bumping of IR detectors and ROIC chips are continuously developed and improved in line with FPA miniaturization and enhanced resolution trends [13], [14], the existing know-how and assembly capabilities are by large proprietary and concentrated within a limited number of technology providers. There is very limited published work on the assembly process requirements for focal plane arrays and FPA assembly process optimization.

Computational modeling of assembly processes has been used previously to assess and predict the formation of solder joints and other interconnects of electronic components. For example, Wu et al. studied the plastic deformation mechanisms of a pin interconnect configuration, consisting of a copper pillar, a solder ball, and a copper trace, to assess the thermal compression process parameters that affect the bonding results [15]. A finite element model of the bonding forming for 3-D flip-chip stacked gold stud bumps was developed to simulate the effect of the controlled bonding conditions [18]. Pan et al. deployed energy-based 3-D models to simulate the solder joint formation for a chip capacitor during reflow and the mechanism of chip capacitor self-alignment [19].

The common FPA assembly approach requires the deposition of indium bumps on both the IR detector chip and the ROIC. Most commonly indium is deposited as the last step in the photolithography/ metallization processing of a device wafer [23]. The height and shape of the bumps are determined by the photoresist used and the mask design [24]. For example, for a 5 to 6 μm high indium bump, an 8-9 μm thick photoresist would be typically required. Fig. 1 shows an example of an array of pre-deposited indium bumps, reported by Rogalski [3], with a rectangular prism shape.

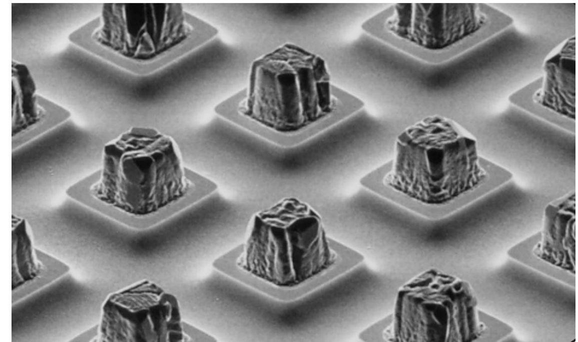

FIGURE 1. An example of an array of pre-bumped indium deposits [3].

Compression bonding as a method of forming interconnects has been also previously researched but predominantly for Cu [21] and Au [22]. The key challenge with the bonding of metals that are not very soft (e.g. Cu) is that the required pressure to enable metallurgical bonding of the mated interfaces causes pressure-induced deformation which is not completely confined within the bump, and hence the interest in different surface finishes that can address this problem. Reported modeling of compression bonding is limited [21] and has a commonly twofold limitation: (1) assumptions for time-independent plasticity of the formed metal, ignoring important time-load effects, and (2) no capture of the non-linear contact nature of the problem.

Thermo-compression bonding is the common approach for FPA assembly. Under the applied compression force, the indium atoms at the contact surface area of two opposing indium bump depositions start to adhere and cohere, ultimately transforming the two bumps into a single entity. Solid-solid diffusion of the indium bumps can be completed even at room temperature, thus avoiding any CTE mismatch issues. Under the compressive force, any voids and air film which may be entrapped at the joint surface interface are also reduced [25]. Prior to bonding, hydrochloric acid (HCl) dip or plasma cleaning can be performed on the indium bumps to remove surface/native oxides that may have formed.

In the case of reflow bonding, the two chips are flipped and aligned in the same way but then the indium solder is melted using hot air reflow to form the FPA interconnects. Indium bump bonding using the reflow process is reported in several experimental studies but remains very limited. Examples include the investigations on reflowing small-size low-resolution arrays [18] and on thin indium films in hermetic sealing of wafer-level MEMS packaging [19], [20], and the reflow process optimization study by Hung et al. where the team managed to achieve 10 μm tall indium solder balls and reported a substantial reduction of bad pixels compared

to thermo-compression assembled IR FPA [26]. FPA flip-chip packaging using reflow gives the advantages of forming indium interconnects with high mechanical strength and the potential for self-alignment of the two chips. The main disadvantage is the assembly processing temperature (above 430K) which induces residual stresses and warpage which can be problematic when the FPA is operated at cryogenic temperature.

In this paper, the assembly processes of high-resolution imaging IR detectors, fabricated using compound semiconductor materials (Group III-V), are investigated using three-dimensional finite element contact analysis, and analytical and energy-based modeling techniques. The modeling approaches are used to assess mainly the impact of chip misalignment on the formation of indium joints with both compression and reflow bonding methods as well as the assembly process feasibility for high-density, ultra-fine pitch pixel arrays. The modeling study generates insights into the assembly process characteristics and the potential processing limitations based on comparative analyses of two distinctive focal plane arrays: (1) 320 × 256 FPA at 30μm pitch and (2) 1280 × 1024 FPA at an ultra-fine pitch of 12 μm. An intermediate package (resolution-wise, 640 × 512) is also studied and is only partly discussed. As this research progresses to the next stages of releasing actual physical assemblies using the discussed flip-chip bonding processes, guided by the results from the presented up-front modeling work, authors envisage the generation of characterization and actual process data that will enable to tune the model's settings and complete the validation of the demonstrated modeling approaches.

II. FPA: PIXEL LAYOUT ARCHITECTURES

Three different IR detector chips are investigated, featuring pixel arrays with the following graded resolutions: (1) 320 × 256, (2) 640 × 512, and (3) 1280 × 1024. A schematic of the IR detector chip/ pixel array and a close view of a mesa pixel structure are presented in Fig. 2. Table 1 details the specifications of the three FPAs. For example, the FPA with the pixel matrix of 320 × 256 has a pitch size of 30 μm and a square mesa pixel size of 25 μm, giving a 5 μm gap between two adjacent pixels. With all FPA designs, contact pads and mesa pixels have sub-micron thickness. The thickness of the mesa isolation layer for the three FPA design configurations is 0.6 μm.

The increasing resolution and decreasing feature sizes trend with the specifications of the 320 × 256, 640 × 512, and 1280 × 1024 FPAs is directly linked to increased assembly alignment (accuracy-wise) requirements and the associated challenges for the packaging posed by higher resolution and smaller pitch pixel array attributes of these structures.

Fig. 3 details a schematic illustration of the cross-section of a pre-bumped IR detector chip aligned to an ROIC chip. Commercial off-the-shelf ROIC chips available from the infrared company FLIR, as detailed in Table 1, are considered for the three resolution formats of the arrays, given the match they offer for the presented resolution and pitch size configurations [27], [28], [29]. As an example, the readout integrated circuit for the assembly of the 320 × 256 IR detector chip is the FLIR ISC9809 ROIC [27]. This ROIC has a 320 × 256 matching format with a 30 μm pitch size. The die size in this instance is 11.35 mm by 10.65 mm as measured to the edge of the scribe lane. The ROIC chips are processed on 5-inch (125 mm) wafers that have a thickness of 625 μm +/− 25 μm.

The gallium antimonide (GaSb) substrate of the detector chip is a pre-assembly feature only and is commonly designed to have a thickness comparable to the thickness of the ROIC. Once the FPA hybrid stack is formed and the IR chip is bonded onto the ROIC, the GaSb substrate is removed. Thus, the photo-sensing chip in a final FPA is only a few microns thick, comprising the absorber layer, barrier layer, and mesa pixels only, as detailed in

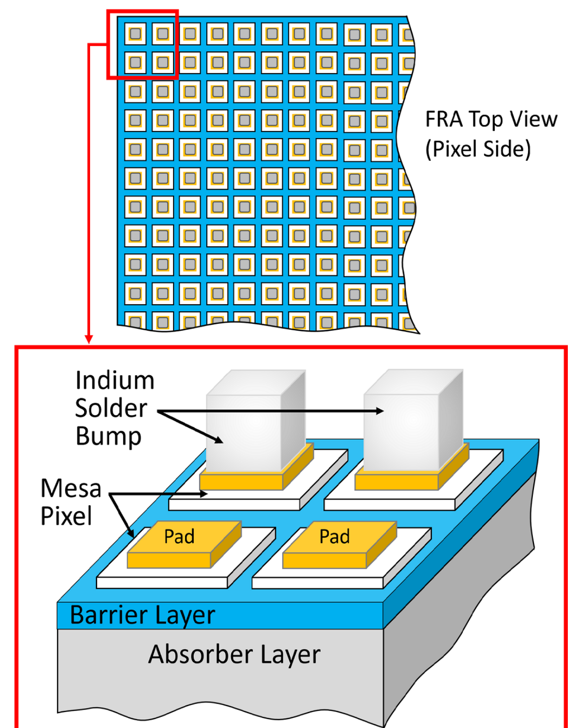

FIGURE 2. Schematic outline of the IR detector chip pixel array domain (top) and close view of the pixel structure and pre-bumped indium deposits (bottom).

TABLE 1. High resolution FPA specifications.

FPA Assembly Cases	FPA #1	FPA #2	FPA #3
Pixel Array Format	320×256	640×512	1280×1024
Number of pixels, N_p	81,920	327,680	1,310,720
Pixel Pitch (μm)	30	20	12
Pixel size (μm)	25×25	17×17	9×9
Contact pads (μm)	10×10	10×10	8×8
ROIC Chip Reference	FLIR ISC9809	FLIR ISC0402	FLIR ISC1308
Adopted reference to FPA Assembly Case	320×256	640×512	1280×1024

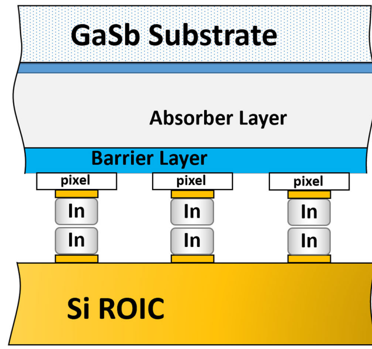

FIGURE 3. Schematic of the cross section of an aligned IR detector chip to Si ROIC for FPA assembly. Pre-bumped indium solder is on the pads at both the sensor and the ROIC chips.

Figs. 2 and 3. A solder joint is obtained by two pre-bumped indium depositions – on the IR detector chip and the ROIC pads respectively. The combined two indium depositions for the 320 × 256 and 640 × 512 FPA assemblies have volume 1.0E-6 mm^3. In the case of the 1280 × 1024-pixel format, the total indium volume for a joint is 0.52E-6 mm^3.

III. FPA: BILL OF MATERIALS AND PROPERTIES

FPA assembly materials, excluding the indium solder, are assumed to have elastic behavior. Temperature-dependent data, where available, are included in the respective models. The required material properties for the ROIC chip (Si), IR detector chip substrate (GaSb), and contact pads (Au) are summarized in Table 2. The utilized linear coefficient of thermal expansion (CTE) data for silicon and indium is taken from [30]. The absorber layer, pixel, and barrier layer materials, as illustrated in Figs. 2 and 3, are Group III-IV compound semiconductor materials with values for Young's modulus, Poisson's ratio, and CTE approximately 60 MPa, 0.3 and 5.5-6.0 ppm/K, respectively.

The indium solder visco-plastic behavior is modeled using the Anand inelastic strain rate model. The material model constants for indium are taken from [31] and the model has been previously demonstrated in the modeling of the thermal fatigue performance of FPA interconnects under cycling thermal load at cryogenic conditions [32], [33]. The models for the dynamic behavior of liquid indium, related to self-alignment of flip-chip in the case of FPA assembly using the reflow bonding process, require also the following additional properties of indium, sourced from [34] and [35]:

1) Density, $\rho = 7026$ kg/m^3
2) Viscosity, $\mu = 0.001867$ Pa.s
3) Surface tension, $\gamma = 0.56$ J/m^2

IV. MODELING OF THE FPA ASSEMBLY WITH COMPRESSION BONDING PROCESS

A. MODELING APPROACH FOR COMPRESSION BONDING

The modeling approach is developed to enable the assessment of the impact which applied compression loads on the IR detector chip have on the indium joint formation. The finite element method and ANSYS simulation software are used to develop detailed three-dimensional (3D) finite element models of the FPA assembly at a local level, representing the FPA spatial domain associated with one pixel and the formation of a single joint within the full assembly array.

TABLE 2. Material properties data used in the models.

Material	Young's Modulus (GPa)	Poisson's Ratio	CTE ($ppm \cdot K^{-1}$)
Indium (In)	12.8 @ 270K 10.7 @ 335K 8.55 @ 400K	0.45	30.5 @ 270K 32.7 @ 335K 34.8 @ 400K
Silicon (Si)	168.0	0.28	2.5 @ 270K 2.6 @ 300K 2.8 @ 430K
Gold (Au)	77.2	0.42	14.4
Gallium antimonide (GaSb)	76.0	0.30	6.1 @ 270K 6.5 @ 335K 6.8 @ 430K

Fig. 4 details the finite element model of the FPA for simulation of the compression bonding condition and the application of the respective model boundary conditions (BCs), i.e. the applied pressure (bonding force) and the structural constraints (displacement degrees-of-freedom, DOF). The contact boundary (3D surface) specified in the analysis of the indium-to-indium (In-In) dynamic contact/deformation is also detailed in the figure. This contact boundary is defined over the regions where the expected (i.e. IR detector chip indium bump to ROIC indium bump contact boundary) or potential (i.e. indium to the pad's vicinity areas) contact may take place during bonding. In ANSYS, the contact modeling capability with 3D surface-to-surface element types TARGE170 and CONTA174 is exploited under the assumption of no separation (with sliding permitted) contact behavior and friction coefficient 1.46 [36].

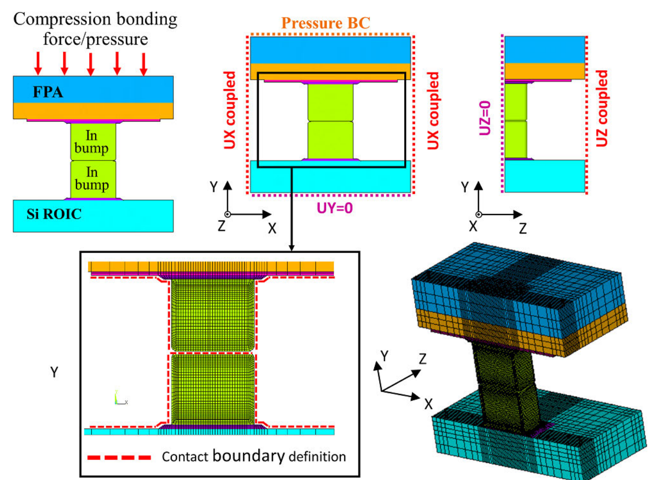

FIGURE 4. Local (pixel-level) three-dimensional FE model for compression bonding simulation of indium joint formation in focal plane arrays, with details for the model boundary conditions and the contact surface definitions.

The simulations for non-linear transient analysis are undertaken under the condition of large deformations. The formation of the single indium joint is a result of a diffusion process (not simulated here) at the established contact interface of the two indium deposits. The developed model assumes that there is no lateral movement of the flipped chip during bonding. The modeling results are obtained under the assumption of compression bonding undertaken at room temperature.

The compression bonding force profile is simulated using an equivalent pressure boundary condition in the model. The pressure is first ramped linearly from 0 to the load profile peak value (P_{max}) and then is maintained constant at that level for the remaining duration of the load application. The reported results are obtained with a ratio of the pressure ramp-up time to the dwell time of 1:3 but this profile can be optimized to achieve different indium joint characteristics. The compression force depends on the FPA specification and is set to provide a bonding force of 3N per mm^2 of indium-indium contact area which is sufficient to ensure that indium will undergo inelastic deformation [37]. This condition is equivalent to applying compression forces of 0.20 mN and 0.13 mN per joint for the 320 × 256 and 1280 × 1024 FPAs, respectively. The dwell duration was guided by the criterion to achieve solder joint collapse from the initial pre-bonded total height of the two indium depositions in the range of 40-50% [38].

B. MODELING COMPRESSION BONDING MODELING RESULTS

The accuracy of placement of the IR detector chip is given with the value of Δp (see Fig. 5) which measures the offset between two corresponding pads (on the ROIC and IR detector). Three different levels of misalignment are modeled, as detailed in Fig. 5, and referenced as Cases A, B, and C:

- Case A: Exact positioning ($\Delta p = 0\ \mu m$)
- Case B: Moderate misalignment ($\Delta p = 1\ \mu m$).
- Case C: Large misalignment ($\Delta p = 2\ \mu m$).

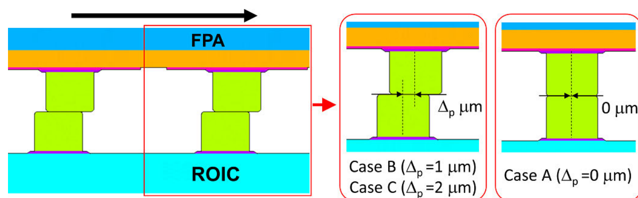

FIGURE 5. Compression bonding case studies with perfect FPA chip-to-chip alignment (Case A) and with two different levels of misalignment for the IR detector chip on the ROIC (Cases B and C).

Due to the inelastic (visco-plastic) behavior of indium, the deformation of the formed joint takes place during the entire bonding profile, including the dwell phase where the applied force remains constant. Figure 6 details the shape deformation of the indium bump assuming the investigated placement accuracy cases. These results point to a clear and substantial impact that the inaccurate placement has on the assembly of the IR detector chip. Shape irregularity of indium bumps, uncertain bonding contact, and reduced joint height are issues that magnify as the level of misalignment increases. The risk of joint formation outside the contact pad is also present and it is a possibility, as in the case of the focal plane arrays assembled under the scenario of 2 μm initial chip misalignment (Case C). However, bonding load profile optimization can mitigate the risk of such defects. The final joint formed under 2 μm initial chip misalignment has approximately 6% and 10%, for the 320 × 25 and 1280 × 1024 FPA assemblies respectively, lower stand-off height compared with the joint obtained with perfect alignment of the chips (Case A). As detailed in Fig. 6, under the simulated compression bonding condition the indium joint collapse is predicted in the range of 47-53% from the initial height.

In addition to the deformed shapes, the models also provided a quantitative evaluation of the expected collapse of the IR detector chip as the indium joints deform under the applied time-pressure load profile. The simulation results confirmed that the FPA deformation is confined in the indium solder only. Hence, the IR detector chip collapse is defined by the achieved stand-off height of the indium solder joints in the final FPA assemblies. The stand-off height of the indium joints is a key assembly parameter as it has a major impact on the resulting thermo-mechanical behavior of the assembly and the thermal fatigue reliability of the indium interconnects. Although under the investigated misalignment levels indium joints are always formed, it should be noted that for larger initial misalignments there is a possibility of the IR detector die slipping, leading to non-bonding. While not part of this study, the misalignment limits for different indium configurations leading to IR detector slipping can be investigated similarly, using variants of the developed models for the case of a larger (>2μm) initial misalignment.

Figures 7 and 8 show the transient results for the vertical collapse of the IR detector chip, respectively the joint height change, for the 320 × 256 and 1280 × 1024 FPAs. Starting with a total pre-bonding height of the indium depositions of 14 μm in the case of the 320 × 256 FPA (see Fig. 7), the stand-off-height of the indium joints under the applied bonding profile is predicted to be 7.3 μm and 6.9 μm for the perfect chip alignment (Case A) and for the 2 μm misalignment (Case C), respectively. Larger misalignment causes faster and more aggressive collapse of the IR detector chip. The modeling results provide also insights into the indium behavior during load application, pointing to three distinctive regions: (1) an initial elastic-dominated indium response in the first 10-15s of the compression profile, depending on the level of initial misalignment, (2) followed by inelastic (visco-plastic) deformation and major joint collapse in the time up to 20s (note bonding force peak is achieved at time $t = 20$s), and (3) continuing creep-dominated deformation and stress-relaxation under the constant pressure maintained over the dwell time of the load profile (20-80s).

Similar deformation behavior is found with the indium joints in the 1280 × 1024 FPA (see Fig. 8). However, due to

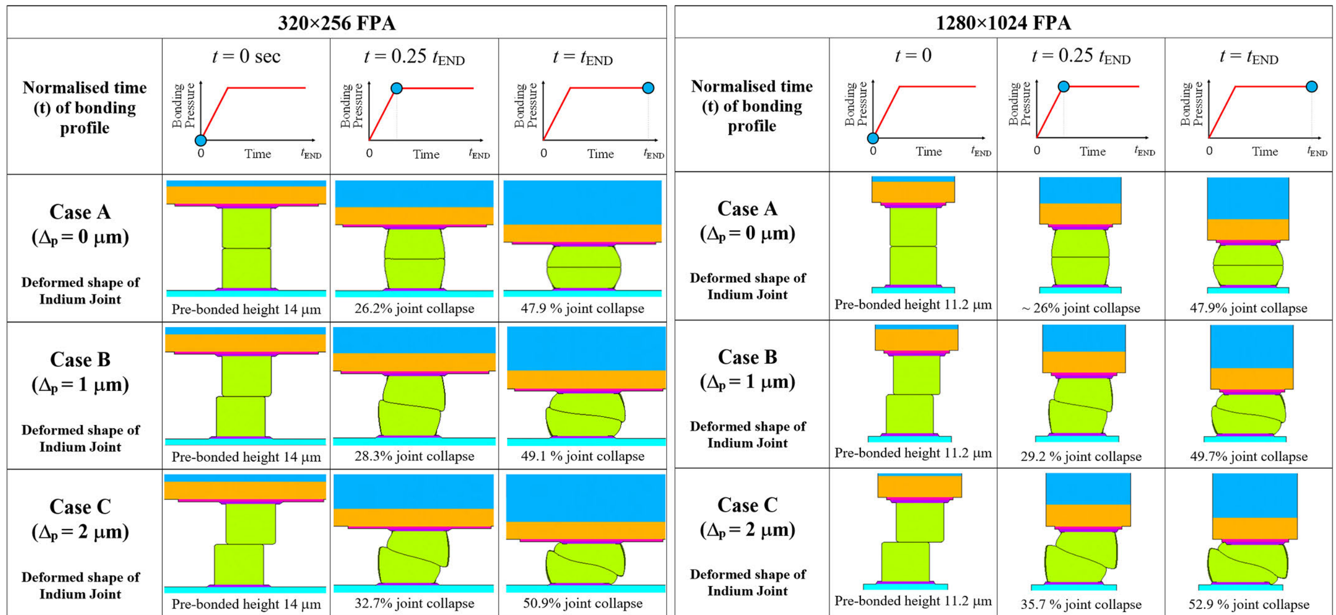

FIGURE 6. Modeling predictions for the effect of placement accuracy on indium joint formation and joint deformed shape (true scale factor, 1.0). The fraction of joint collapse from the initial pre-bonded stand-off height of the two indium deposits, $H_0 = 14.0$ μm for 320 × 256 FPA and $H_0 = 11.2$ μm for 1280 × 1024 FPA, is detailed under each plot.

the smaller joint size in this assembly, misalignments of 1 μm and 2 μm have a greater impact on the joint collapse, relative to the result obtained under the perfect alignment case. Initial pre-bonded total indium height is 11.2 μm - predicted to drop down to 5.85 μm and 5.25 μm for the final, fully formed indium joints with Case A and Case C, respectively. This result shows that the effect of misalignment increases with decreasing pixel pitch size and indium bump volumes, affecting notably the stand-off height of the interconnects in the assembled FPA.

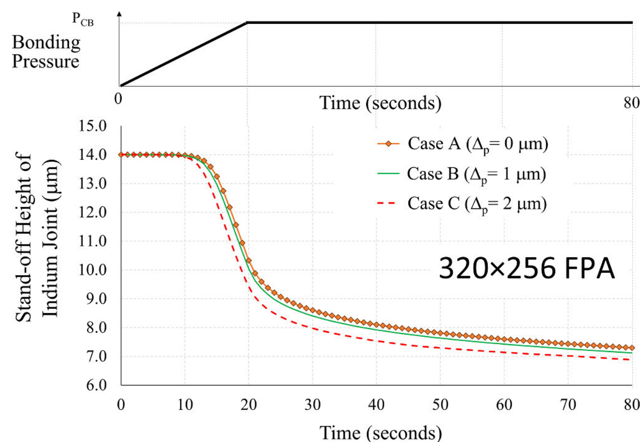

FIGURE 7. Modeling results for the collapse of the IR detector chip of 320 × 256 FPA during the application of the compression bonding load. Case study based on $t_{END} = 80$ sec. Pre-bonded indium deposits height (at $t = 0$ sec) is 14 μm. The final indium joint stand-off height achieved at the end of the process, at t_{END}.

Transient simulation results for the In-In contact area dynamics, the magnitude of sliding at the mated indium surfaces, and contact pressure provide further insights into

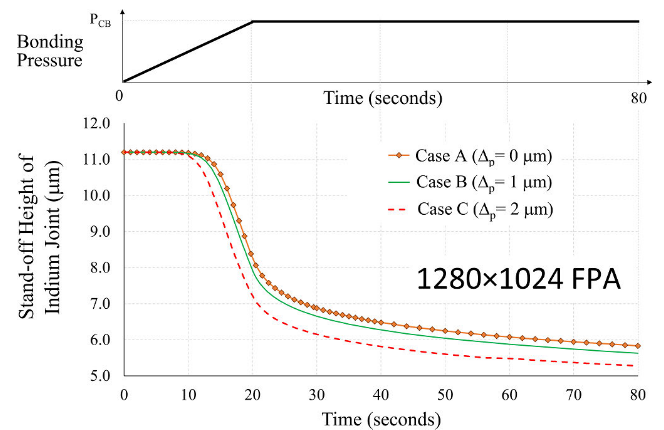

FIGURE 8. Modeling results for the collapse of the IR detector chip of 1280 × 1024 FPA during the application of the compression bonding load. Case study based on $t_{END} = 80$ sec. Pre-bonded indium deposits height (at $t = 0$ sec) is 11.2 μm. The final indium joint stand-off height achieved at the end of the process, at t_{END}.

the solder joint formation. Figure 9 shows a comparison of the contact pressure distribution at the end of the ramp phase of the applied pressure profile ($t = 20$s) and the respective area-weighted averaged contact pressure value. As higher initial chip misalignment is associated with a smaller contact area for the mated indium deposits, under a fixed bonding force magnitude the resulting pressure would be higher. For the 1280 × 1024 FPA results in Fig. 9, the contact area-weighted averaged pressure Case C initial chip misalignment is about 25% higher compared with the perfectly aligned assembly Case A. Unfortunately, this does not result in a joint with higher quality as such higher pressure is not required and can

be detrimental. First, the contact pressure with the aligned chips (Case A) is above the yield strength of indium, as evident from the visco-plastic deformations in Figs 7 and 8, and therefore sufficient to trigger the diffusion bonding process. Secondly, the uniformity of the pressure distribution at the contact surface is an important characteristic too, and one which is compromised when the chips are misaligned (see Fig. 9).

The model can be used also to characterize the evolution of the contact surface in terms of area size. While with all misalignment scenarios, the contact area increases continuously over time under the applied bonding force profile, for an FPA with a larger initial misalignment the final joint contact area is always smaller. For example, the final 1280 × 1024 FPA joint formed under initial misalignment 1 μm (Case B) and 2 μm (Case C) feature indium-to-indium contact areas that are 2.5% and 8.0% smaller than the contact area for the FPA with $\Delta p = 0$ μm, respectively.

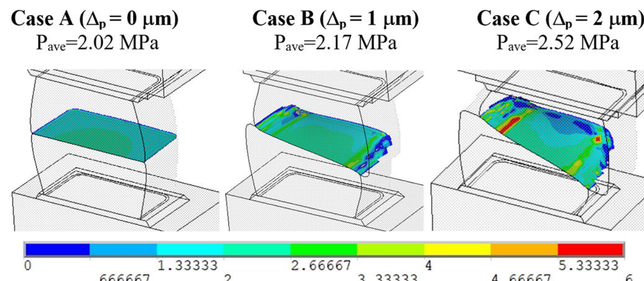

FIGURE 9. 1280 × 1024 FPA: Contour plots of the In-In contact pressure (MPa) at the end of the bonding force ramp up phase (at $t = 20$ sec) and model predictions for the In-In contact-area-weighted averaged contact pressure P_{ave} at $t = 20$ sec.

A phenomenon of concern is also the potential sliding which may occur at the contact surface; when it is present, such In-In sliding compromises the quality of the diffusion bond. The model predictions for the value of the contact area-weighted average of the cumulative sliding distance show that larger chip misalignment causes significantly higher sliding at the In-In contact boundary. Figure 10 details the results obtained for the 1280 × 1024 FPA. The parameter value is found to increase by 2 orders if the alignment is compromised by 2 μm. Figure 11 provides further information by showing the contour plots of the accumulated sliding distance at the end of the compression bonding process.

The main conclusion is that misalignment of a few microns may be possible to tolerate as a joint can be formed but the resulting undesired indium joint shape and the uncertain (variable) lower stand-off height mean that the FPA performance and expected reliability will be compromised. Misalignment can be problematic in the context of implementing a robust control of the bonding force which avoids excessive indium bump collapse and mitigates the risk of joint formation outside the area of the contact pad, and joint bridging for ultra-fine pitch sizes.

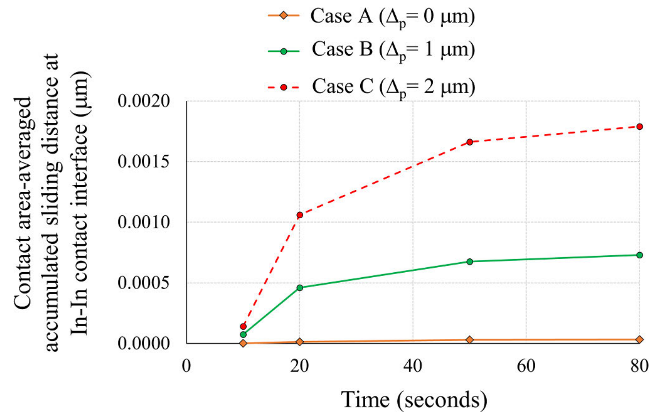

FIGURE 10. 1280 × 1024 FPA: Modeling predictions for the In-In contact-area-weighted averaged accumulated sliding distance (μm) during the compression bonding.

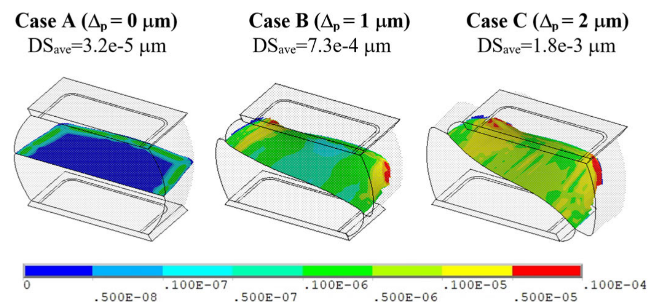

FIGURE 11. 1280 × 1024 FPA: Contour plots of the accumulated sliding distance (mm) for the In-In contact interface at the end of the compression bonding load (at $t = 80$ sec) and model predictions for In-In contact-area-weighted averaged accumulated sliding distance DS_{ave} at $t = 80$ sec.

V. ANALYTICAL MODELING OF THE FPA ASSEMBLY SELF-ALIGNMENT DURING REFLOW BONDING

A. MODELING APPROACH FOR REFLOW BONDING

The modeling of the reflow process for FPAs is based on models that assess the following two phenomena:

1) *Reflow-Induced Misalignment*: Misalignment between the IR detector chip and the ROIC caused by the different thermal expansion (CTE mismatch) of the two chips under the reflow thermal load (approximately $\Delta T = 130$K), and
2) *IR Detector Chip Motion during Reflow*: IR detector chip motion and the associated centering/restoring force (promoting flip-chip self-alignment) during reflow, at temperature above the melting temperature of indium, for misaligned chips in the initial flip-chip placement.

1) MODELING THE REFLOW-DRIVEN MISALIGNMENT

The alignment of the objects at an elevated temperature is affected by the level of their differential thermal expansion, and this would apply to the IR detector array and the Si ROIC chips if their assembly is performed using the reflow

process. A schematic of the reflow-induced differential CTE mismatch is illustrated in Fig. 12.

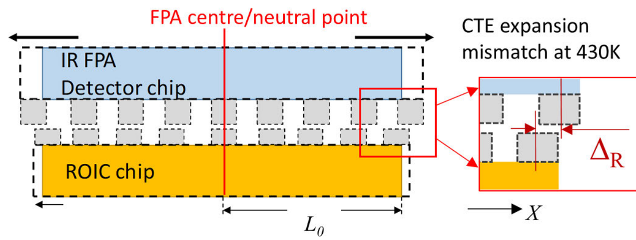

FIGURE 12. Misalignment caused by the coefficient of thermal expansion (CTE) mismatch between the IR detector chip (GaSb substrate) and the Si ROIC chip during reflow. Maximum misalignment (Δ_R) at peripheral In-In depositions.

To assess quantitively the expansion of the two chips, the one-dimensional (1D) linear thermal expansion equation is used:

$$dl = L_0 \alpha \Delta T \tag{1}$$

where dl is the change in length (m) of the object, L_0 is the initial length (m), α is the linear thermal expansion coefficient (m/m.K) of the material, and ΔT is the applied thermal load (K). In the IR detector chip, the GaSb substrate is the main layer in the multi-material chip construction and has a thickness that is two orders of magnitude larger compared with the combined thickness of the other materials (absorber and pixels, and barrier layers). In addition, the properties of these other materials are very similar to the properties of the GaSb substrate, and therefore the thermal linear expansion of the IR detector chip is dictated by the expansion behavior of the GaSb. This allows for a simplified calculation of the reflow-induced misalignment under the assumption of representing the entire IR detector chip and the ROIC as single material domains of GaSb and Si, respectively.

The relative in-plane difference ΔU between two opposing pads of the two chips located at a distance L_0 from the neutral (center) point of the chips can be expressed as:

$$\Delta U = dl_{GaSb} - dl_{ROIC} \tag{2}$$

where dl_{GaSb} is the linear expansion of the GaSb substrate (m), respectively of the IR detector chip, and dl_{ROIC} is the linear expansion of the Si ROIC (m), both calculated using (1). Given the melting temperature of indium is 430K, the following input data is used with the equations (1) and (2):

- GaSb coefficient of thermal expansion at 430K, $\alpha_{GaSb} =$ 6.8 ppm/K.
- Silicon (Si) coefficient of thermal expansion at 430K, $\alpha_{Si} = 2.8$ ppm/K.
- Thermal load $\Delta T = 130$K, the minimum load needed in the reflow profile before achieving melting of the indium solder.

The predicted values for reflow-induced misalignment ΔU using the approximate 1-D model given with (1)-(2) have been validated with a detailed three-dimensional (3D) finite element model of the true IR detector multi-material composition (actual topology). The absolute difference between the two predicted values for the relative in-plane misalignment of two matching indium bumps, on both sides of the two chips and at the corner of the array (location of extreme misalignment), was found to be $<1\%$. This model validation exercise confirmed that in the evaluation of misalignment between the IR detector chip and the ROIC, the simple approximate 1D model (1)-(2) can be used with confidence.

It should be noted that a solution for the reflow-induced misalignment issue is to calculate the expected misalignment at reflow temperature and account for that in the design of the IC detector chip or ROIC. However, such a solution will force the bonding process choice towards reflow only because the two chips will not be aligned as a result at lower temperatures associated with the (thermo-)compression bonding process alternative.

2) MODELING THE IR DETECTOR CHIP MOTION DURING REFLOW

The modeling approach makes use of an analytical modeling methodology that enables to capture of the physics of the chip harmonic motion during the phase of reflow when the solder is in a liquid state [39]. In this study. the modeling approach is tailored towards a model which predicts the time scale characteristics of the flipped IR detector chip oscillatory motion and the acting centering force impact on the indium solder behavior. The model's primary use is to assess if the IR detector and the ROIC chips will self-align during reflow and the time required to achieve that.

When the temperature is above the melting temperature of indium solder during reflow, the indium bums change phase and become liquid. While in this molten state, an initially misaligned flip-chip (IR detector onto ROIC) is subjected to a centering force due to the indium surface tension forces. This centering force would lead to an oscillatory motion of the flipped IR detector chip. A one-dimensional model formulation for this problem is considered, as detailed in Fig. 13. As annotated in the figure, under the model assumption for linear solder velocity distribution, the indium solder velocity $v(y,t)$ can be expressed as

$$v(y,t) = \frac{y}{H}\dot{U}(t) \tag{3}$$

where $U(t)$ is the IR detector chip displacement at time t, y is the distance from the top of the ROIC to the point of velocity evaluation, H is the height of the molten indium bump and

$$\dot{U}(t) = \frac{\partial U(t)}{\partial t}$$

is the IR detector chip velocity.

The chip harmonic motion is given with the equation:

$$m\ddot{U}(t) = F_c - F_d \tag{4}$$

where m is the mass of the IR detector chip, F_c is the centering force and F_d is the damping force. The damping force is

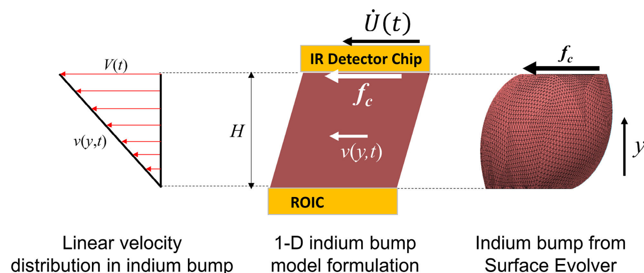

FIGURE 13. One-dimensional model formulation for FPA liquid indium motion under surface tension induced restoring force.

assumed to be only induced by the friction between the chip and the indium and hence can be expressed as

$$F_d = \mu S \left[\frac{\partial v(y,t)}{\partial y} \right]_{y=H} = \gamma \dot{U} \tag{5}$$

where

$$\gamma = \mu \frac{S}{H}$$

is the viscous damping coefficient, μ is the indium solder viscosity and S is the interface area of the IR detector chip with the indium joints. The centering force can be expressed using Hooke's law as

$$F_c = -KU \tag{6}$$

where K is the spring constant. The spring constant (K) and the height of the molten solder joints (H) are unknown but can be evaluated using surface tension energy minimization methods. This is detailed later in this section. In this work, the surface tension energy minimization methods available with the software tool Surface Evolver are used [40]. Surface Evolver enables the modeling of surfaces shaped by surface tension, gravitational, and other energies so that a user-defined initial surface is iteratively evolved toward minimal energy by a gradient descent method.

Combining (4)-(6) gives the following damped mass-spring system model for flip-chip motion during reflow in the case of misaligned chips:

$$\frac{\partial^2 U}{\partial t^2} + \frac{2}{\tau_0}\frac{\partial U}{\partial t} + \omega_0^2 U = 0 \tag{7}$$

where

$$\omega_0 = \sqrt{\frac{K}{m}} \tag{8}$$

is the undamped angular frequency, and

$$\tau_0 = 2\frac{mH}{\mu S} \tag{9}$$

is the time scale of the oscillation amplitude decay.

The above model can be solved analytically and has the following solution:

$$U = U_m \cos(\omega t + \phi) \tag{10}$$

where

$$U_m = U_0 \sqrt{1 + (\omega \tau_0)^{-2}} e^{\left(-\frac{t}{\tau_0}\right)} \tag{11}$$

$$\omega = \frac{2\pi}{\tau_c} = \omega_0 \sqrt{1 - \frac{1}{(\omega_0^2 \tau_0^2)}} \tag{12}$$

$$\tan(\phi) = -(\omega \tau_0)^{-1} \tag{13}$$

and U_m is the decaying amplitude, ω is the angular frequency, U_0 is the initial chip misalignment, τ_c is the time scale of the oscillatory motion and ϕ is the phase angle.

The surface tension and IR chip mass effect on the liquid indium joints are evaluated using Surface Evolver. A series of calculations are undertaken using a single indium bump model and assuming different initial misalignment values U_0 (in this work, U_0 from 0 to 8 μm) and computing the respective centering force values per indium bump f_c in each instance. These modeling results can then be used to identify the unknown spring constant (K) in the definition of the centering force in (6). In addition, the Surface Evolver surface tension model prediction for the height of the liquid joint, H, is also obtained and used as an input in the analytical model (7).

B. MODELING RESULTS FOR FPA SELF-ALIGNMENT DURING REFLOW BONDING

The misalignment of the corresponding contact indium-to-indium bumps, on the IR detector and the ROIC sides respectively, due to the thermal expansion caused by the applied reflow thermal load is most critical at the peripheral joints of the pixel array. This is because these bumps are furthest away from the center (neutral point) of the chip. We consider X as the direction along the longer dimension of the pixel array, and indium bumps in the external row of the array at a distance L_{max} from the chip center line. The relative difference ΔU between displacements of two corresponding indium bumps, on the IR detector chip and the ROIC side respectively at the peripheral row along X, is obtained using (2). This is the misalignment along X due to thermal expansion during reflow, denoted as Δ^R, and calculated as follows:

- 320 × 256 FPA and $L_{max} = 4.8$ mm: $\Delta_R = 2.5\ \mu$m
- 640 × 512 FPA and $L_{max} = 6.4$ mm: $\Delta_R = 3.3\ \mu$m
- 1280 × 1024 FPA and $L_{max} = 7.7$ mm: $\Delta_R = 4.0\ \mu$m

If the misalignment due to the physical placement inaccuracy of the IR detector chip onto the ROIC chip is denoted as Δ_P, to have the reflow assembly process as a feasible bonding option, the following feasibility condition has to be satisfied:

$$\Delta_P + \Delta_R < \Delta_{MAX} \tag{14}$$

where Δ_{MAX} is the maximum misalignment that a given pitch size for the FPA assembly can tolerate. Based on geometric observations and predictions for the solder joint shape from Surface Evolver, in the case of the 320 × 256 and 640 × 512 FPAs, $\Delta_{MAX} = 8\mu$m is the limiting value for the formation of a single joint under the surface tension force during reflow. This limiting value is determined by several requirements:

TABLE 3. Summary of results for reflow induced flip-chip misalignment.

FPA Assembly: Risk Level / pad size and gap between pads	320×256: 10 μm pads with 20 μm gap	640×512: 10 μm pads with 10 μm gap	1280×1024: 8 μm pads with 4 μm gap
Distance from FPA neutral point L_0(mm)	4.8	6.4	7.7
Δ_{MAX} / μm	8	8	2
Misalignment from reflow CTE mismatch: Δ_R (μm)	2.5	3.3	4.0
Reflow Feasibility: $\Delta_P + \Delta_R < \Delta_{MAX}$	Yes, if $\Delta_P < 5.5$ μm	Yes, if $\Delta_P < 4.7$ μm	No, even if $\Delta_P = 0$ μm

(1) minimum overlap between the 10 × 10 μm opposing contact pads with pre-deposited indium bumps, (2) no solder wetting outside the contact pad, and (3) no bridging of adjacent joints. In the case of the 1280 × 1024 FPA assembly, the gap between adjacent pads is 4 μm, and hence $\Delta_{MAX} = 2\mu$m is identified as the misalignment beyond which bridging of adjacent indium joints can start occurring due to their collapse while in the molten state and talking the barrel-like shape under tension forces.

The model results from (1)-(2) and (14) are summarized in Table 3. The main conclusion is that the reflow process for FPA assembly may be a feasible bonding method with lower resolution FPAs but for ultra-fine pitch designs, such as the case of the 1280 × 1024 FPA, this process cannot be used. The reason for this is that the differential CTE mismatch-driven misalignment, which for the 1280 × 1024 FPA is $\Delta_R = 4$ μm at the peripheral indium-to-indium bumps on the matching IR detector and ROIC sides, will cause the bridging of adjacent joints in the peripheral regions of the flip-chip assembly. This will be the case even if the two chips are perfectly aligned during the initial, pre-reflow, placement ($\Delta_P = 0$ μm). For FPAs with larger pitch sizes, as in the case of 320 × 256 and 640 × 512 designs, reflow bonding can be a viable packaging technique but will require in practice achieving an alignment in the pre-reflow placement of the IR detector onto the ROIC typically better than 4 μm.

Given the assessment that the 1280 × 1024 FPA cannot be packaged using the reflow bonding method, the analytical modeling of the chip motion in the context of self-alignment is performed only for the 320 × 256 and 640 × 512 FPA architectures. The results from the Surface Evolver showed that the height of the liquid indium joints for both FPAs is identical, with an approximate value of 10.3 μm. This means that the effect of the IR detector chip mass (which is different for the two FPA cases) on the resulting shape of the indium joints is negligible and that the surface tension forces in the liquid indium are the dominant factor. Consequently, the respective Surface Evolver predictions for the centering force and the computed spring constant are very similar for both assemblies.

Figure 14 details the Surface Evolver predictions for the values of the centering force per indium bump as a function of the 320 × 256 IR detector chip displacement relative to the ROIC. The same graph shows that for small misalignments the centering force can be approximated with a straight line. The slope (gradient) of this line defines the spring constant k. The spring constant k per bump for the 320 × 256 FPAs is calculated as 0.7011 N/m. It is also confirmed that the spring constant k per bump for the 640 × 512 FPA is practically the same, for the reasons discussed above, with a difference between the two spring constant values found to be by less than 0.03%. To obtain the values for the centering force and the spring constant for the respective IR detector chip, the values of the two parameters are summed over the number of bumps in the full pixel array matrix. As an example of calculating the centering force, if the IR detector chip is displaced (i.e. misaligned) by 3μm to the ROIC at a given bump location, the centering force associated with that single indium bump is $f_c = 0.2103\text{e-}5$ N.

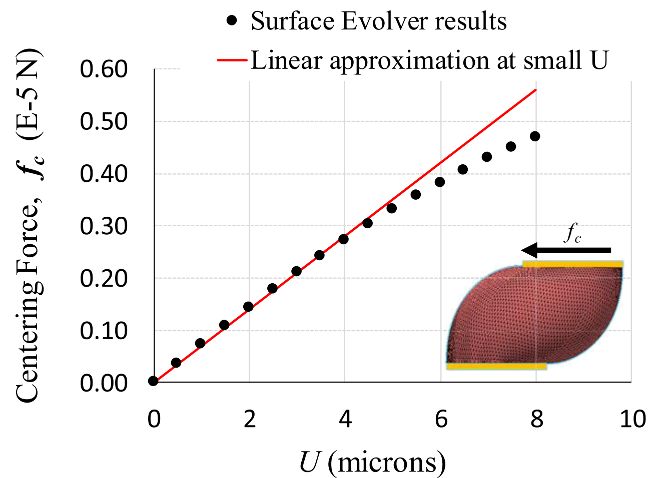

FIGURE 14. Surface Evolver results for the centering force per single indium joint (f_c) versus chip displacement U (misalignment) in the case of the 320 × 256 FPA. The slope of the corresponding linear approximation at small U provides the spring constant value per single indium joint, $k = 0.70114$ N/m.

Once the spring constant is obtained, the analytical model (7) for the harmonic motion of a misaligned chip during reflow is used to evaluate the self-alignment response of the reflowed chips. The value of the damping ratio,

$$\zeta = \frac{1}{\omega_0 \tau_0} \tag{15}$$

for both the 320 × 256 and 640 × 512 FPAs is less than 1. This is a criterion for having oscillatory motion with an amplitude that is gradually decreasing to 0, meaning self-alignment is taking place. This can be explained by the low indium solder viscosity and the chip-to-indium joint small interfacial area. With self-alignment predicted, the model can also inform on the time required for the oscillatory motion

to decay to zero (the condition for perfect alignment), and if this can occur within the reflow window and while indium is above its melting temperature. This assessment is based on the predictions for the time scale of the oscillation amplitude decay τ_0 using (9) and the time scale of oscillatory motion τ_c using (12). The respective modeling predictions are:

1) 320 × 256 FPA: $\tau_0 = 0.561$s and τ_c =0.0004743s
2) 640 × 512 FPA: $\tau_0 = 0.237$s and τ_c =0.0003080s

Given that common reflow profiles implement time intervals above the solder melting temperature in the order of tens of seconds, the above-identified time constants for the FPA reflow bonding are evidence that the flip-chip assembly will self-align under a typical reflow profile. This will be the case with any feasible initial IR detector chip misalignment (displacement). The rate of change of the decaying amplitude U_m, obtained using (11), can be also predicted. Figure 15 shows the chip motion decay magnitude for two scenarios assuming initial chip displacement of 3.0 and 4.5 μm. The self-alignment of the 640 × 512 FPA is found to be faster compared to the case of the 320 × 256 assembly. For the case of the slowest flip-chip self-alignment shown in Fig. 15 – the 320 × 256 FPA with initial chip displacement of 4.5 μm, the IR detector chip is aligned to the ROIC to 0.76 μm and 0.13 μm after 1 sec and 2 sec, respectively.

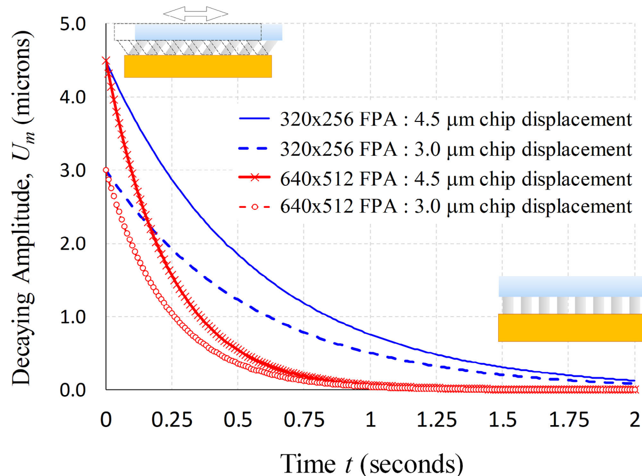

FIGURE 15. Predicted decay of the IR detector chip oscillatory motion for 320 × 256 and 640 × 512 focal plane arrays in the case of initial displacements of 3.0 μm and 4.5 μm of the detector chip to the ROIC.

VI. CONCLUSION

Focal plane array assembly models for compression bonding and reflow were developed and demonstrated for high-resolution pixel arrays, including an ultra-fine pitch 1280 × 1024 package design. The effect of misalignment of the IR detector chip onto ROIC on the quality of the formed indium joints was investigated. The modeling results for FPA assembly using compression bonding led to the following main conclusions:

- Inaccurate placement of the detector chip onto the ROIC will compromise the resulting indium joint quality and will result in interconnects with variable/uncertain heights. Larger misalignment increases the risks of excessive chip collapse, sliding at the indium-indium mated surfaces, and hence compromised diffusion bonding, smaller contact area/ reduced mechanical strength, and formation of the joint outside the contact area.
- Uncertainty in placement accuracy makes the optimal compression bonding parameter setup problematic as different levels of misalignment result in the formation of indium joints with different characteristics under the same compression bonding conditions.
- Assembly machinery capable of providing accuracy of chip placement <2 μm for compression boding, in general, is a key requirement. Ultra-fine pitch assemblies need to be aligned more accurately, with a micrometer or better accuracy, and may be feasible to assemble only with compression bonding.
- Force-induced deformation in the FPA under compression bonding is always completely confined within the formed indium joint.
- Increasing the number of pixels in the FPA array requires higher bonding force/pressure, and hence the bonding process conditions for different pixel arrays with different sizes/resolutions should be optimized separately. The developed process model can be used to inform and guide the optimal bonding profile for placement equipment with different placement accuracy.

The choice of reflow bonding as an assembly process requires careful assessment as with some ultra-fine pitch, high-density pixel arrays it may not be a feasible option at all. An important evaluation of the misalignment from both chip positioning and CTE expansion mismatch at the elevated reflow temperature is required. The main findings from the study are:

- Ultra-fine pitch FPAs such as the investigated 1280 × 1024 FPA cannot be reflowed. Even if an exact initial placement of the two chips is achieved, the thermal load associated with reflow causes relative displacement at the periphery of the two chips which is similar to the gap between two adjacent pixels and hence will result in the bridging of adjacent joints.
- For the discussed 320 × 256 and 640 × 512 FPAs, reflow will require chip placement accuracies of <4 μm. With such accuracy, the additional misalignment between the ROIC and the IR detector chip due to reflow-induced thermal mismatch (in the range of 2.5-3.5μm) can be accommodated while still ensuring no indium joints bridging and minimum required overlap between corresponding indium bums on both sides of the flip-chip.
- Where reflow is feasible, self-alignment is taking place with a time constant for the motion decay < 0.6 sec. The time constants are small enough to get the two chips aligned with each other.

Future work will focus on assembly trials for packaging IR detectors onto ROIC that will enable the optimization of model parameters through the availability of measured

process data and experimental validation of the developed process models.

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