IEEE Access
Multidisciplinary | Rapid Review | Open Access Journal

Received 6 March 2023, accepted 26 March 2023, date of publication 5 April 2023, date of current version 12 April 2023.

Digital Object Identifier 10.1109/ACCESS.2023.3264531

RESEARCH ARTICLE

Analysis and Design of Power-Efficient H-Band CMOS Frequency Doubler Employing Gain Boosting and Harmonic Enhancing Techniques

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This work was supported by the Institute of Information & Communications Technology Planning & Evaluation (IITP) funded by the Korean Government (MSIT) under Grant 2019-0-00060.

ABSTRACT This article presents a power-efficient frequency doubler employing gain boosting and harmonic-enhancing techniques. With a single transistor only, the gain boosting technique can reach the maximum achievable gain (G_{max}) by adding embedded passive components, thereby obtaining high voltage swings. Then, the transistor's nonlinearity is essential, which is maximized by the harmonic transition scheme of the transistor operation along with high voltage swings. In addition, a harmonic reflector and a harmonic leakage canceller are employed for the second harmonic enhancement. The harmonic reflector prevents unwanted harmonic mixing by minimizing the incoming second harmonic current fed back to the input. The harmonic leakage canceller suppresses the leakage loss of the second harmonic current present at the output. Furthermore, thanks to a proposed dual-band output matching network, the output impedance is conjugately matched to achieve the G_{max} at the fundamental frequency while it is matched to extract the second harmonic output power simultaneously. To verify the proposed techniques, the prototype was designed as a single-stage circuit that does not require additional amplifying stages, which led to higher power efficiency and lower chip area. Implemented in a 65-nm CMOS process, the measurement results show a saturated output power of 0.9 dBm and 3-dB bandwidth of 26 GHz (237–263 GHz), respectively, while requiring a chip area of 0.071 mm^2. Total power efficiency, including the effect of injected signal power, is 2.87 % while consuming only 37 mW dc power.

INDEX TERMS CMOS, dual-band matching network, frequency multiplier, harmonic reflector, maximum achievable gain, nonlinearity, terahertz.

I. INTRODUCTION

Sub-terahertz (THz) is an attractive frequency band for radar, imaging, and next-generation communication systems, which are promising solutions in beyond 5G (B5G) and 6G with its inherently wide bandwidth and short wavelength [1], [2], [3]. The generation of a high spectral purity signal in this frequency band is challenging but needs to be ensured to realize the practical sub-THz systems. Limited maximum oscillation frequency (f_{max}) of the transistor and lossy passive components prevent the sub-THz systems from achieving high spectral purity currently [4].

Then, the frequency multiplication is a promising alternative to implement the spectrally pure sub-THz signal source. However, a conventional frequency multiplier (FM) provides μW level output power [5], [6]. Most of the reported sub-THz FMs focused on solutions to resolve the low output power issue. Several works to improve the output power have been

The associate editor coordinating the review of this manuscript and approving it for publication was Yiming Huo.

reported by employing additional amplification at either input or output but entail the high dc power (low power efficiency) and large chip size [6], [7], [8].

The sub-THz FMs can be categorized into mixer-based or frequency multiplication-based FM [9], [10], [11], [12], [13], [14]. In the mixer-based FM, two inputs are injected, while one of the mixed tones is extracted to generate the frequency multiplication. Passive mixer reduces the dc power consumption but exhibits low output power. On the other hand, the Gilbert-cell-based active mixers [9], [10] suffer from low power efficiency and limited headroom.

Frequency multiplication-based FM adopts either N-push [11], [12], [13] or the waveform shaping architecture [14], which creates harmonics of the input signal by using nonlinearities of the transistor. Then, the matching network extracts and delivers the desired harmonic to the load.

In this work, we propose a frequency doubler with a gain boosting technique to improve the harmonic output power while ensuring good power efficiency without requiring additional amplifying stages [15]. Then, by adopting the dual-band matching method, the second harmonic signal is effectively extracted and delivered to the load while maintaining the high fundamental gain. Furthermore, a detailed analysis on effective generation and extraction of the second harmonic signal is provided.

This article is organized as follows. Section II describes the architecture discussion of the frequency doubler for the high output power. The fundamental and second harmonic characteristics of the proposed architecture are analyzed in Section III. The second harmonic extracting and delivering methods are explained in Section IV. The implementation and measured results of the proposed frequency doubler in comparisons with prior sub-THz FMs are presented in Section V, followed by the conclusion in Section VI.

II. ARCHITECTURAL DISCUSSIONS ON POWER-EFFICIENT FREQUENCY DOUBLER

A. FREQUENCY DOUBLER: PRIOR WORKS

Fig. 1 shows the conventional architectures of the frequency doubler: balanced in Fig. 1(a) and single-ended in Fig. 1(b). The active core in Fig. 1 refers to several combinations of implementations with transistors and passive components, which can function as a nonlinear generating apparatus to create generating harmonics (e.g., twice the input frequency). The balanced architecture in Fig. 1(a) naturally extracts even harmonics from the common node of the balanced output. However, the balanced architecture at the sub-THz band suffers from low output power because the common node of the active core, which is typically the drain node of the transistor, is a virtual ground at the fundamental frequency. Then, the output node of the active core is not an optimal point to generate a high voltage swing due to low impedance, and thus the strength of the generated harmonic signal is degraded. The harmonic generation of the active core is related to the amount of nonlinearity. Due to the low voltage swing, it is difficult for

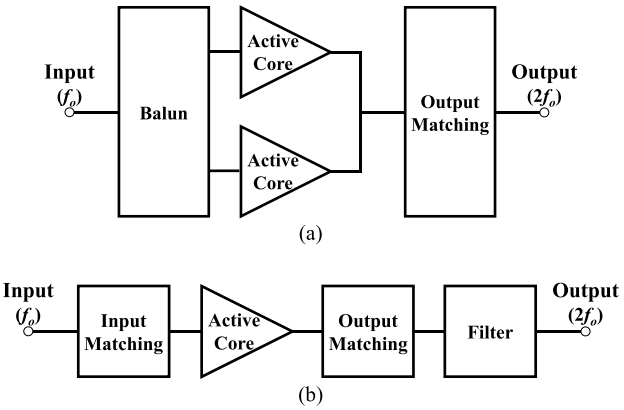


FIGURE 1. Frequency doubler architectures: (a) balanced and (b) single-ended.

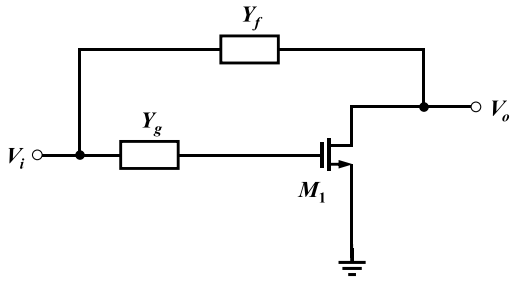


FIGURE 2. Proposed gain boosting technique with embedded passive components (G_{max}-core) applied to frequency doubler.

the transistor to enter the triode and/or cutoff region, and as the transistor operates linearly, the intensity of the generated harmonic signals decreases. In addition, since the balanced architecture requires a differential input pair, a bulky passive balun is necessary, which incurs a large chip area.

On the other hand, the single-ended architecture in Fig. 1(b) can achieve a high voltage swing because the output is not a virtual ground at the fundamental frequency and does not require a balun for the differential input pair. However, since there are various harmonic signals at the output of the active core, there is an accompanying complexity and issue in extracting the desired second harmonic signal while maintaining the nonlinearity of the active core high.

Therefore, for the power-efficient frequency doubler, the single-ended architecture is adopted in this work. In addition, the chip size is further reduced by adopting and configuring the frequency doubler with a single stage. Since the single-ended architecture uses only one active core, the nonlinearity of the active core should be maximized to improve the second harmonic generation. In [16], two essential elements to maximize the second harmonic power are presented: optimum gate-to-source voltage (V_{gs}) and drain-to-source voltage (V_{ds}) waveforms for high voltage swings and a harmonic transition according to the operation region of the transistor.

The active core using the conventional single transistor cannot achieve high voltage swings in the sub-THz band due to the limited f_{max}. However, by employing the gain boosting

technique in our work, the single active core in the single-ended architecture can reach the maximum second harmonic power by satisfying the above conditions due to the highest fundamental gain and voltage waveforms.

B. G_{max}-CORE ADOPTING GAIN BOOSTING TECHNIQUE

Fig. 2 shows the proposed active core employing the gain boosting technique for the frequency doubler. The power gain of the active core reaches the maximum achievable gain ($G_{\max}$) by embedding the passive components [17], [18], [19], [20]. The proposed active core, denoted as $G_{\max}$-core, is applied to the frequency doubler to obtain the required voltage waveforms from the maximum second harmonic power conditions. First of all, the $G_{\max}$-core provides the high voltage swing at the fundamental frequency, which is quite challenging in the conventional single transistor architecture at the sub-THz band. High V_{ds} swing enabled by the proposed architecture further enlarges the V_{gs} swing through additional passive voltage gain. Secondly, it satisfies a harmonic transition condition according to the operating region of the transistor. The harmonic generation of the transistor occurs due to the changes in its operating range, which includes saturation, triode, and cutoff regions [21]. If the transistor operates only in the saturation region, the amount of harmonic generation is limited. To maximize the second harmonic power, only one transition between the saturation and triode regions or saturation and cutoff regions is desired since the transition creates the second harmonic output currents with different phases each other [16].

This paper focuses on the harmonic transition between the saturation and triode regions while preventing the active core (transistor) from entering the cutoff region. Various $G_{\max}$-core-based amplifiers reported earlier [17], [18] operate in class-A. The class-A operation provides 360 degrees of conduction angle, and thus, the transistor does not enter the cutoff region. Furthermore, the same dc bias condition at input and output as in [17] and [18] does not require an ac coupling capacitor nor the gate biasing circuit, which is a significant source of insertion loss at the sub-THz band. Hence, we propose the adoption of the $G_{\max}$-core for the maximum second harmonic power.

III. FREQUENCY DOUBLER WITH G_{max}-CORE

In this section, we discuss the operation principle of the $G_{\max}$-core at the fundamental and second harmonic frequencies in order to generate high output power for the frequency doubler.

A. OPERATION PRINCIPLE AT FUNDAMENTAL FREQUENCY

The $G_{\max}$ condition is achieved by adding linear-lossless-reciprocal embedded components to the single transistor [18]. These embedded components come from using two or three passive circuits at the gate, drain, and source nodes [18], [22].

As shown in Fig. 2, for implementing the active core in the frequency doubler, two embedded passive components are added for the active core: series and parallel embedded components at the gate and gate-to-drain, respectively. Fig. 3 shows the comparison in simulated power gains from the common-source transistor with and without embedded components, and both are biased at $V_{gs,\mathrm{dc}} = V_{ds,\mathrm{dc}} = 1$ V. As mentioned above, this equal dc bias condition at the gate and drain nodes is employed to prevent the transistor from entering the cutoff region. As shown in Fig. 3, the cutoff frequency (f_t) and $f_{\max}$ are 167 GHz and 353 GHz, respectively, when the transistor width of 86.4 μm is used. The transistor parameters, such as C_{gs}, C_{gd}, C_{ds}, R_g, R_{ds}, and g_m of the transistor, are simulated to be 82 fF, 29 fF, 44 fF, 0.94 Ohm, 43 Ohm, and 118 mS, respectively. By embedding the linear-lossless-reciprocal components, the maximum available gain (G_{ma}) of the transistor can reach the $G_{\max}$ [17]. As shown in Fig. 3, the G_{ma} of the single transistor without embedded components is always lower than the $G_{\max}$, but the G_{ma} of the common-source transistor with the embedded components

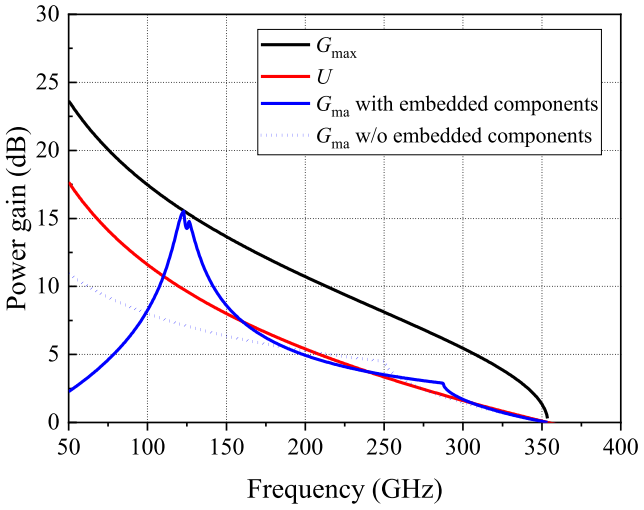


FIGURE 3. Simulated power gains of a 86.4 μm common-source transistor with and without embedded components.

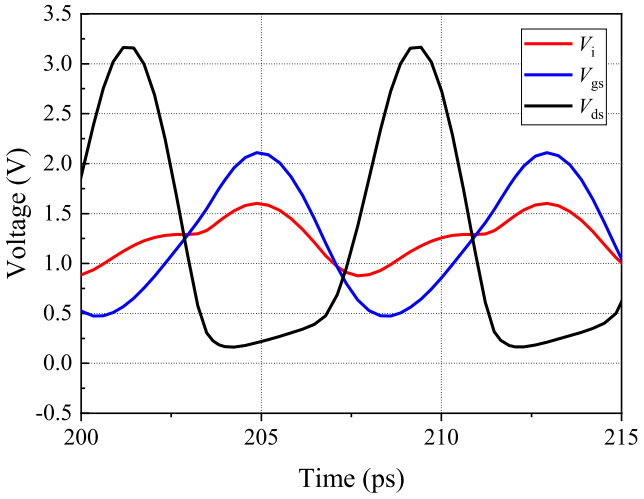


FIGURE 4. Simulated input (V_i), gate-to-source (V_{gs}), and drain-to-source (V_{ds}) voltage waveforms with the $G_{\max}$-core.

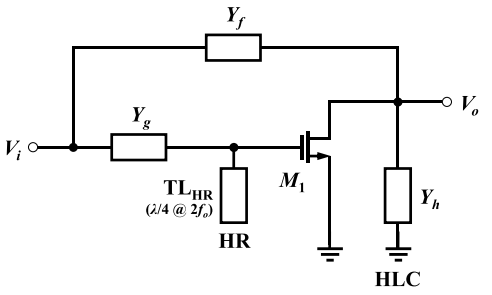


FIGURE 5. Schematic of the G_{max}-core with the second harmonic enhancing techniques.

reaches the theoretical $G_{\max}$ at the fundamental frequency of 125 GHz, where Y_g and Y_f are implemented with 6.15 and 31.4 pH inductors. As introduced in [18] and [19], the design of embedded components can be fulfilled by calculating a value satisfying the following condition.

$$G_{\max} = (2U - 1) + 2\sqrt{U\,(U - 1)}, \tag{1}$$

where U is the unilateral gain [18]. For the proposed frequency doubler, only one solution value is adopted since two embedded components are used for the compact implementation.

The increase in the second harmonic signal by the gain boosting technique can be ascertained from the nonlinear simulation (PSS in SpectreRF). The voltage amplitude of the second harmonic signal at the drain node of the transistor is 67 mV and 469 mV without and with the gain boosting technique, respectively. As mentioned above, the improvement results from the nonlinearity enhancement of the transistor by increasing the fundamental gain.

Fig. 4 shows the voltage waveform of each node in the $G_{\max}$-core from the nonlinear simulation and verifies that the two elements (conditions) required for the power-efficient frequency doubler are satisfied. For the simulation, both input and output are conjugately matched, and the input power of 6 dBm is applied. As depicted in Fig. 4, the input voltage (V_i) at the $G_{\max}$-core is amplified by the embedded passive component of Y_g, and then a high V_{gs} swing is obtained accordingly. A high V_{ds} swing is also followed by inverted amplification. The desired condition for V_{gs} and V_{ds} waveforms [16] are satisfied. Also, V_{gs} is always higher than the threshold voltage (V_{th}), and thus, the transistor does not enter the undesirable cutoff region. V_{ds} waveform satisfies the pseudo-half-sine waveform, which creates the desirable harmonic profiles (the combination of the fundamental and second harmonic signals) and is out-of-phase with V_{gs}.

B. OPERATION PRINCIPLE AT SECOND HARMONIC FREQUENCY

At the sub-THz band, the generated second harmonic current at the output port is easily lost due to the leakage current through the parasitic output capacitor. Then, in the proposed frequency doubler, an admittance of Y_h, denoted as harmonic leakage canceller (HLC), is in shunt with the parasitic output

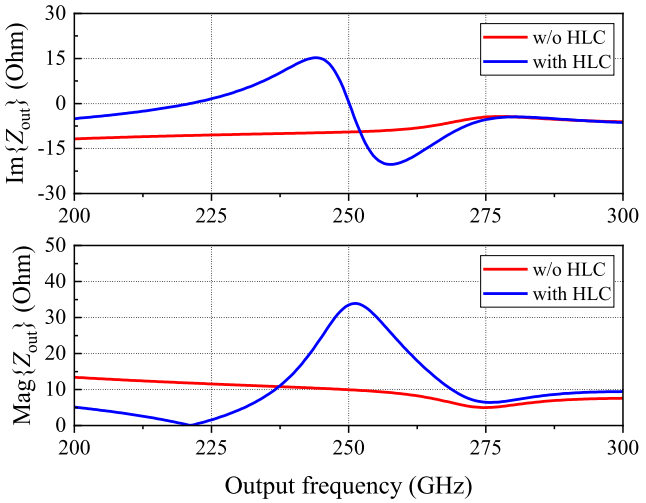


FIGURE 6. Comparison of simulated output impedance with and without the HLC near the second harmonic frequency.

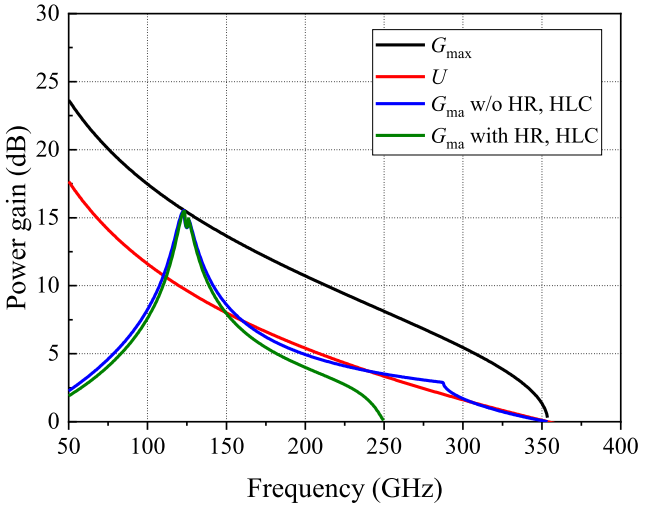


FIGURE 7. Simulated power gains of the G_{max}-core using a 86.4 μm common-source transistor with and without the harmonic enhancing techniques.

capacitance to eliminate the current-stealing components. The admittance of Y_h is satisfied at the second harmonic frequency as below, where Y_{out} is output admittance seen at the output of the $G_{\max}$-core.

$$Y_h = -\text{Im}\,\{Y_{\text{out}}\} \tag{2}$$

Fig. 6 shows the effectiveness of the proposed HLC by comparing the output impedance at the $G_{\max}$-core near the second harmonic frequency of 250 GHz. The imaginary part of the output impedance (Z_{out}) is near zero by the adoption of Y_h, and the magnitude of the Z_{out} is maximized.

Furthermore, the harmonic reflector (HR) [23] is applied between Y_g of the embedded passive components and the gate node of the transistor M_1. The HR suppresses the harmonic current fed back into the gate terminal from the drain terminal. This harmonic current as the feedback signal at

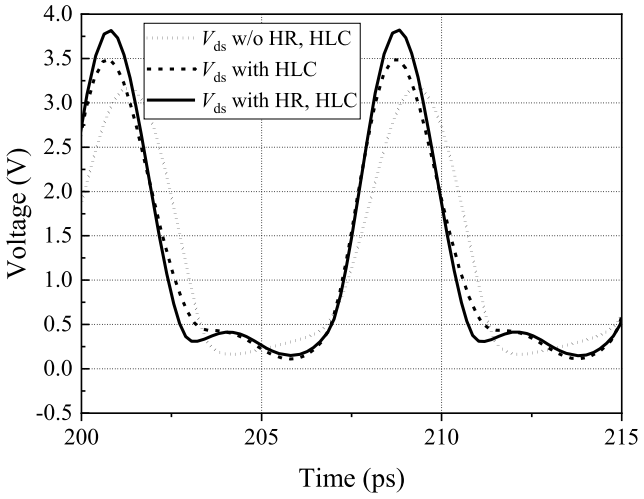


FIGURE 8. Comparison of drain-to-source voltage waveforms with and without harmonic enhancing techniques.

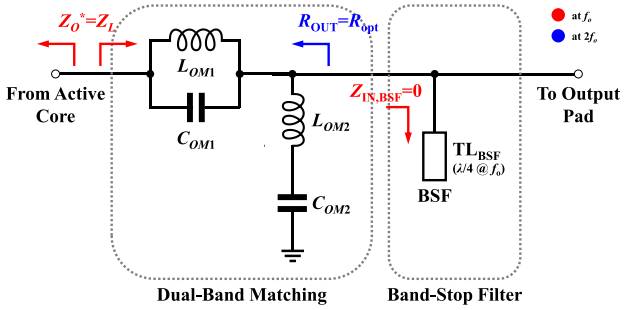


FIGURE 9. Schematic of output matching and fundamental rejection for the efficient second harmonic extraction.

the gate node introduces undesired harmonic mixing, which acts as a source of conversion gain reduction for the frequency doubler. In this work, the HR is implemented using the quarter-wavelength shunt open-stub (TL_{HR}), as shown in Fig. 5. For implementing the HR, the length of this transmission line as the shunt open-stub should satisfy the condition below in order to obtain the low impedance at the second harmonic frequency.

$$l_{TL} = \frac{\lambda}{4} \tag{3}$$

The aforementioned harmonic enhancing techniques, the HLC and HR, are applied to the same common-source transistor to verify the effectiveness, and simulation results are shown in Fig. 7. The G_{max}-core with the harmonic enhancing techniques is also achieving the G_{max}

Fig. 8 shows the simulated V_{ds} waveforms with the G_{max}-core in Fig. 5. The second harmonic is strengthened by adding the HR and HLC to the input and output of the G_{max}-core, respectively, and provides a higher and narrower pulse shape. It also manifests the noticeable change of V_{ds} waveform resulting in the increase of the second harmonic signal. The positive peak of V_{ds} further increases, and a valley shape is created in the clipping region at the negative peak [24].

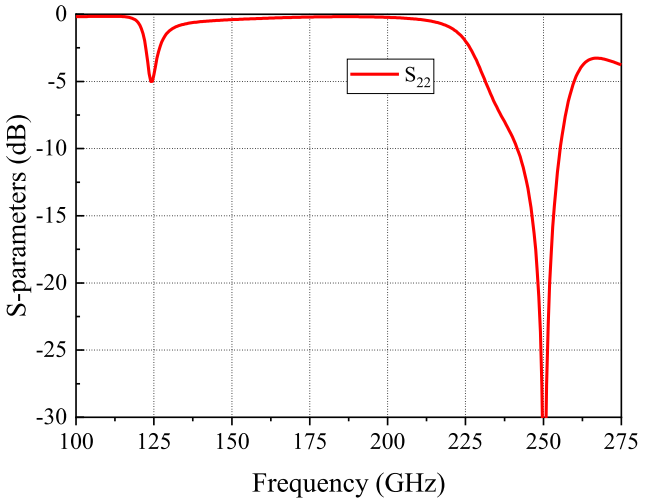


FIGURE 10. Simulated output return loss seen by the load without band-stop filter for dual-band output matching.

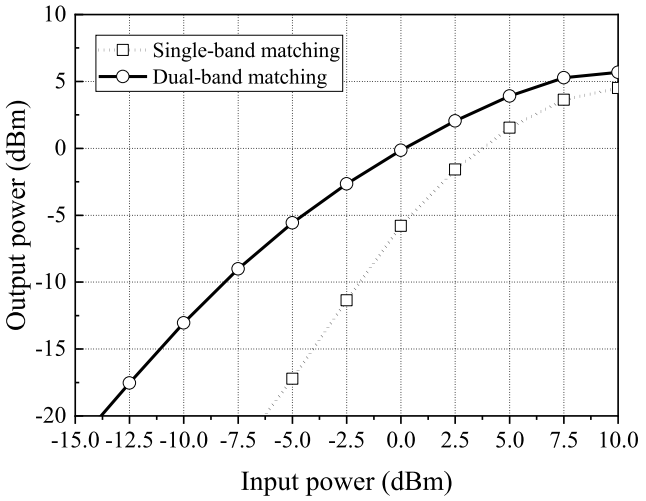
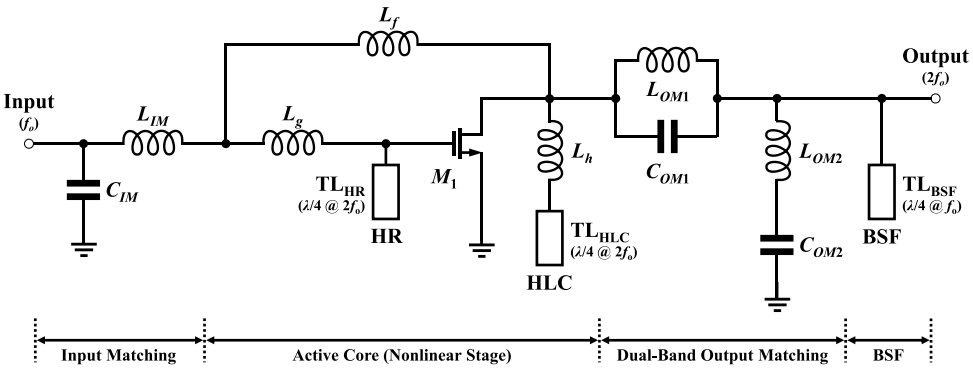


FIGURE 11. Simulated output power versus input power with proposed output matching network (dual-band matching) in comparison to conventional matching network (single-band matching).

The presented waveform in Fig. 8 resembles the class-F_2 operation [24], [25].

IV. PROPOSED G_{max}-CORE OUTPUT MATCHING NETWORK FOR FREQUENCY DOUBLER DUAL-BAND OUTPUT MATCHING NETWORK

The conventional balanced frequency doubler extracts the second harmonic signal from the common node of two active cores. On the other hand, with the proposed single-ended frequency doubler, we require an efficient second harmonic extraction out of all (even and odd) harmonics present at the output. Simultaneous fundamental frequency matching at the input and output ports is desired to take advantage of the maximized fundamental gain. Furthermore, the second harmonic should also be matched at the output port to maximize the second harmonic signal delivery to the output load.



Component	Value	Component	Value
L_g	5.1 pH	M_1	86.4 μm
L_f	26.1 pH	TL_{HR}	$\lambda/4$ @ $2f_o$
L_h	6.5 pH	TR_{HLC}	$\lambda/4$ @ $2f_o$
L_{IM}	31 pH	TL_{BSF}	$\lambda/4$ @ f_o
L_{OM1}	12.4 pH	C_{IM}	48 fF
L_{OM2}	35.6 pH	C_{OM1}	55.8 fF
		C_{OM2}	75 fF

FIGURE 12. Complete schematic of the proposed frequency doubler and its design parameters.

Then, the output of the $G_{\max}$-core is matched at the fundamental and second harmonic frequency by the dual-band matching network shown in Fig. 9, which is realized by the combination of four reactive components. This dual-band impedance transforming technique and analytical solutions were originally presented in [26], which applied to the frequency doubler at the sub-THz band. The real and imaginary parts of the output impedance can be transformed into the desired load impedances at two different frequencies. As shown in Fig. 10, the simulated output return loss without a band-stop filter matches well at the fundamental (125 GHz) and the second harmonic frequencies (250 GHz). Here, the fundamental frequency shows a higher (worse) return loss than the second harmonic frequency because it is matched with low impedance in consideration of the band-stop filter. Without the dual-matching technique, V_{gs} and V_{ds} waveforms cannot satisfy the maximum second harmonic power condition presented earlier. Fig. 11 shows the effectiveness of the proposed dual-band matching network.

A. FUNDAMENTAL REJECTION

The fundamental tone rejection is also necessary for the frequency doubler. Then, the band-stop filter (BSF) is employed here with its simplicity and strong fundamental rejection strength over other schemes, such as a high-pass filter and the band-pass filter [27]. The BSF can be implemented using the quarter-wavelength shunt open-stub at the fundamental frequency cascaded after the dual-band output matching network, as shown in Fig. 9. The input impedance of this shunt stub satisfies the null condition at the fundamental frequency, and then the fundamental signal is completely suppressed.

V. IMPLEMENTATION AND MEASUREMENT RESULTS

A. LAYOUT IMPLEMENTATION

The proposed frequency doubler is designed to operate within H-band (220-325 GHz) as the promising candidate band for B5G/6G applications among sub-THz bands. Fig. 12 shows the complete schematic of the proposed H-band CMOS frequency doubler, along with the design parameters of each component. The inductive reactances are realized utilizing the series inductance of a transmission line, and the parasitic parallel capacitance of transmission lines and various junctions for the connection of each transmission line is carefully considered and optimized. As shown in Fig. 12, to implement Y_h, ac short-circuit is utilized for ground by adopting the quarter-wavelength open-stub of TL_{HLC} at the second harmonic frequency. Since Y_h is connected to the drain node of the transistor, the dc bias problem occurs when the dc short-circuit is utilized. Hence, the HLC consists of a combination of inductive reactance and quarter-wavelength open stub. The quarter-wavelength shunt open-stub for the HR dictates the length of the transmission line to be quarter-wavelength at the second harmonic frequency. The HR short-circuits the gate node at the second harmonic frequency.

For the input and output matching of the $G_{\max}$-core, inductors and capacitors are realized by using the series inductance of the microstrip transmission line and the customized metal-oxide-metal capacitors, respectively. The input matching network is conjugately matched to the source impedance at the fundamental frequency. The output matching network is implemented to be conjugately matched at the fundamental frequency and power matched at the second harmonic frequency.

The output matching consists of the dual-band output matching network implemented by combining the series connection of parallel resonance and the shunt connection of series resonance. Among the topologies of the dual-band matching network, a topology with the dc bias path as a series line is applied, and the chosen topology provides the dc voltage of the transistor biased through the output pad. The BSF uses the quarter-wavelength shunt open-stub, as mentioned earlier. This shunt stub has a quarter-wavelength length at the fundamental frequency. All passive components, including junctions, are designed with a full-wave 3D electromagnetic simulator (Ansys High Frequency Structure Simulator, HFSS) and ensure sufficient accuracy in the sub-THz band while minimizing simulation tolerance.

B. MEASUREMENT RESULTS

The proposed frequency doubler was designed in a 65-nm CMOS process. Fig. 13 shows the chip micrograph of the fabricated frequency doubler. Two prototype circuits

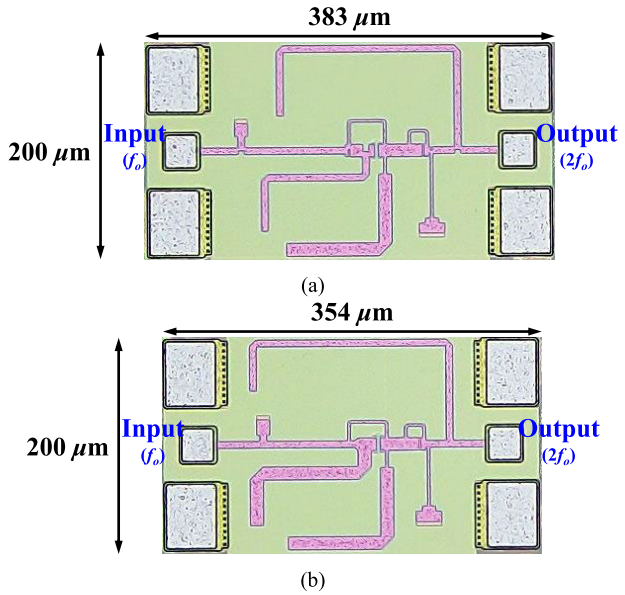


FIGURE 13. Chip micrograph of the proposed frequency doubler prototypes: (a) Version A with $W_{M1} = 76.8\ \mu$m, and (b) Version B with $W_{M1} = 86.4\ \mu$m.

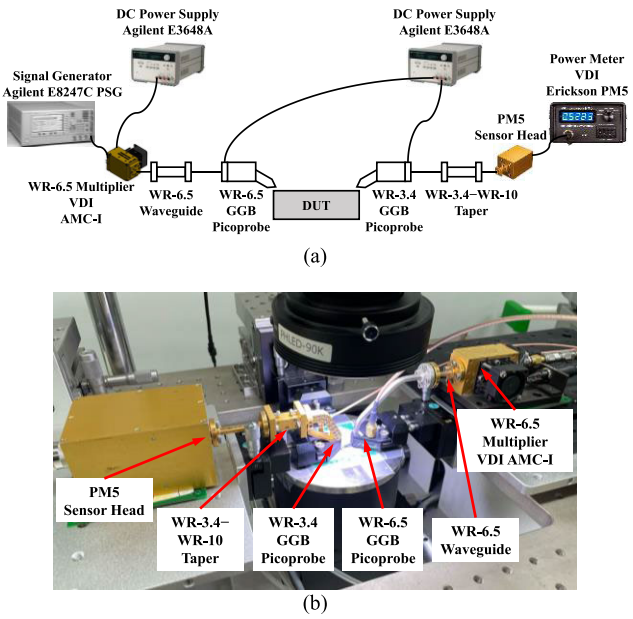


FIGURE 14. Measurement setup and environments.

are fabricated with different widths of the core transistor (M_1). The chip area is only 0.383 mm × 0.2 mm and 0.354 mm × 0.2 mm for versions A and B, respectively. Fig. 14 depicts the measurement setup. An Agilent E8247C PSG signal generator and a VDI WR-6.5 multiplier were used to generate the D-band input signal (f_o), and the H-band output signal ($2f_o$) power was measured using a VDI Erickson PM5. The DC voltages are separated from the RF signals and biased through the input and output probe with bias tees. Measurements were performed by on-wafer probing using GGB Picoprobes, and all the losses of measurement devices, such as waveguide components, were de-embedded.

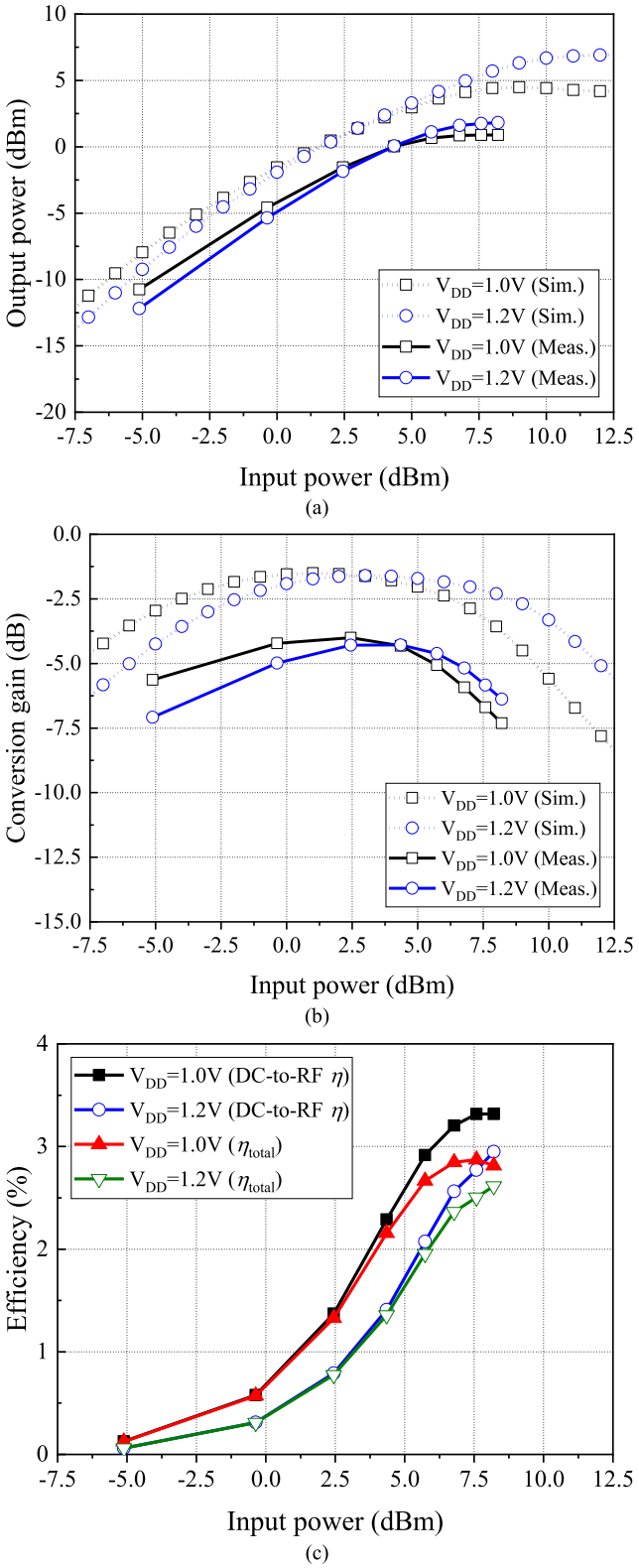


FIGURE 15. Measurement results: (a) output power, (b) conversion gain, and (c) efficiency versus input power at 248 GHz output frequency.

Fig. 15 shows the measurement results of version B compared to the simulation results. The measured saturated output power (P_{sat}) shown in Fig. 15(a) is 0.9 dBm and 1.8 dBm

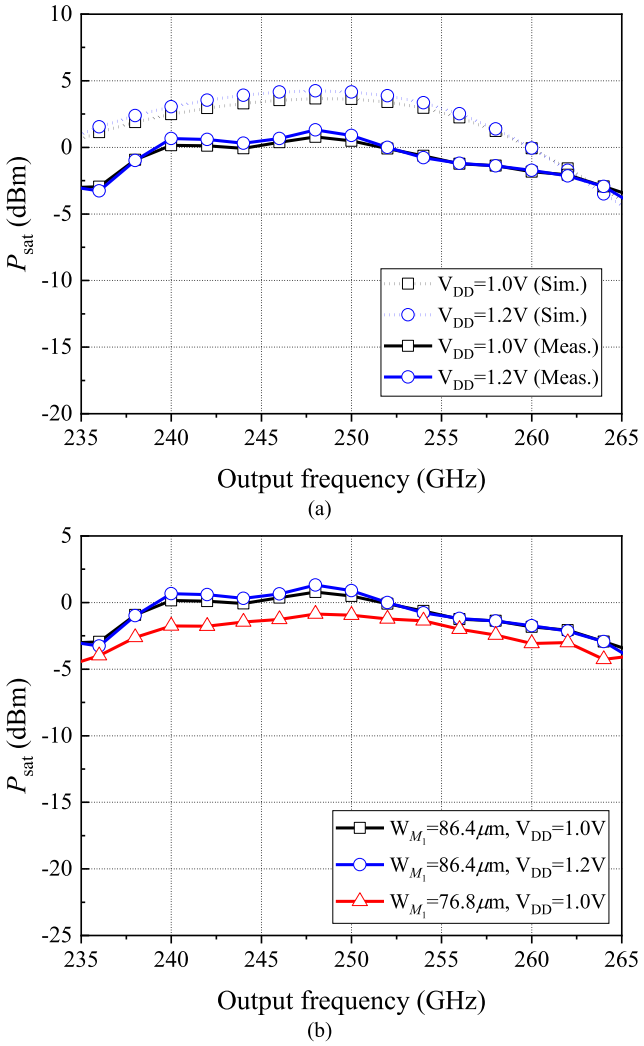


FIGURE 16. (a) Measured and simulated P_{sat} of second harmonic signal as a function of output frequency. (b) Comparison of P_{sat} measured at second harmonic frequency according to transistor size and supply.

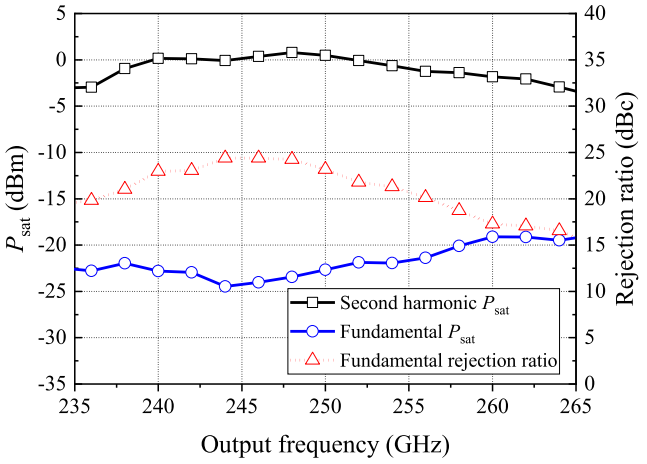


FIGURE 17. Measured P_{sat} of fundamental and second harmonic signals and the FRR as a function of output frequency.

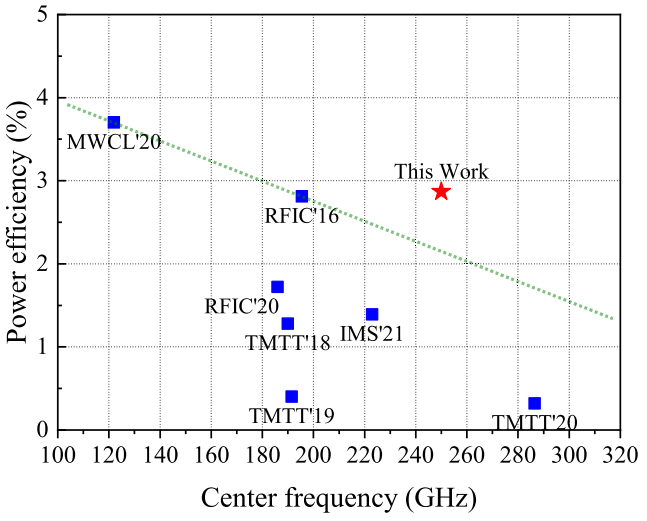


FIGURE 18. Power efficiency comparison between published FMs versus operating center frequency.

at 248 GHz output frequency for the supply voltages at 1 V and 1.2 V, respectively. The measured peak conversion gain (CG) is −4 dB, as shown in Fig. 15(b). The overall trend matches well between measured and simulated results with a difference of 3–4 dB, and this discrepancy is due to the inaccuracy from the transistor's parasitics and passive component artifacts at the sub-THz band. As shown in Fig. 15(c), the maximum DC-to-RF conversion efficiency is 3.32 %, and the maximum total power efficiency (η_{total}), including the input signal power [7], is 2.87 %.

$$\eta_{\text{total}} = \frac{P_{\text{sat}}}{P_{\text{in}} + P_{\text{DC}}} \tag{4}$$

Fig. 16 shows the measured and simulated P_{sat} of version B with the input power of 6 dBm. As shown in Fig. 16(a), the measured output power has wide 3-dB bandwidth (BW) of 26 GHz (237–263 GHz) that corresponds to 10.4 % fractional 3-dB BW (FBW). Fig. 16(b) confirms that the frequency doubler using a larger transistor size shows a higher P_{sat}. Fig. 17 shows, in version B, P_{sat} of the fundamental and second harmonic signals at the output as a function of the second harmonic frequency for the input power of 6 dBm. As shown in Fig. 16, within the 3-dB BW, a high fundamental rejection ratio (FRR) of 17–25 dBc is measured thanks to the presented BSF.

Table 1 shows the performance summary in comparison with prior silicon-based sub-THz FMs. The proposed frequency doubler features a milliwatt-level output power while dissipating low DC power and occupying a compact size of 0.071 mm^2. FM reported in [8] shows high output power but consumes much higher DC power (5×) and a larger chip area than this work.

Fig. 18 depicts the power efficiency of the reported sub-THz FMs as a function of the operating frequency. As the operating frequency increases, it is clearly shown that the power efficiency of FM decreases. The proposed solution outperforms the trends resulting in higher power efficiency than previous works [6], [7], [8], [28], [29], [30], [31].

TABLE 1. Performance summary in comparison with prior silicon-based Sub-THz FMs.

	TMTT'16 H. Lin [28]	TMTT'18 K. Wu [29]	RFIC'20 P. Starke [6]	TMTT'20 A. Ali [30]	RFIC'16 N. Sharma [31]	MWCL'20 D. M. Kang [7]	IMS'21 R. Dong [8]	This Work (Version B)
Technology	90-nm SiGe	130-nm SiGe	130-nm SiGe	130-nm SiGe	65-nm CMOS	40-nm CMOS	40-nm CMOS	65-nm CMOS
f_c (GHz)	235	190	186	286.5	195.5	122	223	250
BW (GHz)	30	60	68	127	51	14	20	26
Multiple	2	2	4	8	2	3	9	2
P_{in} (dBm)	17	6	0.5	-12.7	0	0	−6	7.6
P_{sat} (dBm)	1.8	−2.6	−1	2.3	3	3	4.1	0.9
Peak CG (dB)	−15	−8.6	0	15	3	3	10.1	−4
P_{DC} (mW)	90	39	45	537	70	53.2	185	37
η_{total} (%)	1.08	1.28	1.72	0.32	2.81	3.7	1.39	2.87
FRR (dBc)	> 30	N/A	> 52	N/A	> 40	> 38	N/A	17–25
Amplifying Stage	No	No	Yes	Yes	Yes	Yes	Yes	No
Area (mm^2)	0.54	0.09	1.3	1	0.71	0.36	1.7	0.071

VI. CONCLUSION

This article presents the effective solution of the second harmonic generation with the single active core based on the G_{max}-core and harmonic enhancing techniques. An H-band frequency doubler is implemented by adopting the singled-ended G_{max}-core, leading to a high V_{gs} and V_{ds} swing. While maintaining the G_{max} condition due to gain boosting, the dual-band output matching network maximizes the extraction of desired second harmonic. The proposed H-band CMOS frequency doubler shows >1 mW output power and high power efficiency of 2.87 % without requiring additional amplifying stages. To the best of the authors' knowledge, this work reports the smallest chip area and the highest total power efficiency in sub-THz FMs.

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