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APPLIED RESEARCH

Resonant Network-Based MVDC Circuit Breaker Topologies With Fast Current Breaking Capability

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ABSTRACT This paper presents two improved circuit breaker (CB) topologies based on resonant networks for medium voltage DC (MVDC) applications, such as shipboard power distribution and subsea oil and gas production. The topologies feature simple LC resonant networks that efficiently suppress fault current in just a few tens of microseconds, making them suitable for integration with existing solid-state or hybrid DC CB. Moreover, they also help to minimize the CB energy and reduce (if not eliminate) the requirement for protection devices like surge arresters during fault events. The proposed topologies are first tested using Typhoon Hardware-in-the-Loop (HiL) simulations at 1.2 MW (6 kV, 200 A) power levels and thyristor-based solid-state circuit breakers (SSCB). Then, scaled-down laboratory prototypes, also based on thyristor-based SSCB, are experimentally validated. The results show that both topologies quickly bring the current of the CB's main switch to 0 A. The main circuit pathway requires only a small inductor and switch, resulting in a steady-state efficiency of >99.9%. The resonant network-based design allows for a fast response time of less than 50 μs using a simple and low-cost auxiliary circuit, eliminating the need for complex charging circuitry and protection devices typically used to suppress voltage surges during faults.

INDEX TERMS DC circuit breaker, fault isolation, MVDC, system protection, LC resonant network.

I. INTRODUCTION

MVDC power systems are becoming increasingly popular due to their advantages in various applications, including subsea oil and gas production, shipboard power distribution, data centers, hydrogen electrolyzers, and electric aircraft [1], [2], [3]. Some of the DC systems are in the range of 1.5 kV, 3 kV, etc. (passenger rails) to 1 kV, 6 kV, etc. (electric ships), to 6 kV and above (subsea fossil energy production), with power scales ranging from a few megawatts to tens of megawatts [4], [5]. However, fault handling is a major challenge in these systems [6]. The absence of a natural zero-crossing point in DC systems makes fault current interruption mechanisms a critical concern. DC circuit breakers play a crucial role in protecting and operating these distribution power systems [7]. Additionally, the low impedance of DC power systems leads to a high rate of rising fault currents, which is more severe in medium and high-voltage applications [8]. To effectively handle these fault events, Circuit Breakers (CBs) require a fast-breaking response and the capability to handle overloads.

Traditional mechanical circuit breakers separate the contacts during the turn-off process, causing an arc between the contacts that must be quickly extinguished to break the current efficiently. However, these mechanical CBs are unsuitable for reliable DC power systems due to the absence of zero crossing points and the fast-rising time for fault currents. With the advancement of power semiconductor devices, Solid State Circuit Breakers (SSCBs) are considered as an effective alternative to mechanical CBs in DC power systems. In contrast, SSCBs are prone to significant conduction losses, limited voltage and current ratings, and limited surge current handling capability [9], [10], [11]. At the same time, several solutions have been proposed in the past decade to address these limitations through the use of series/parallel connected devices. However, many challenges remain regarding semiconductor device protection, characteristics, and technology

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limitations [12]. Hybrid Circuit Breaker (HCB) concept, which combines a high-speed mechanical switch or ultra-fast disconnect with semiconductor devices [13], was introduced to overcome some of these obstacles.

In SSCBs, several switching power devices are used based on the application requirements and the availability of the devices' technology. The main metrics to compare among the devices are off-state blocking voltage capability, on-state power losses, and material/device cost. Devices, including thyristors, IGBTs, IGCTs, GTOs, and SiC MOSFETs, were evaluated based on their voltage and current ratings and on-state voltage drop over a range of operating temperatures [14]. The Si thyristor exhibited the highest voltage and current ratings (up to 12 kV, 1.5 kA) among all devices, with a superior surge current handling capability and the lowest on-state voltage drop at temperatures above 50 °C. However, the lack of turn-off current capability resulted in the need for extra auxiliary circuits, leading to increased cost, complexity, and reliability issues in the system. Passive auxiliary circuits to address this requirement were presented in [15], [16], [17], and [18]. On the other hand, modified thyristor structures (GTO/GCT, IGCT, and ETO) integrated with an active turn-off feature have been developed and thoroughly investigated [19], [20], [21], [22], [23], [24], [25]. These active-turn-off thyristors have been extensively studied [10], [26], [27], [28], [29], [30], [31]. The regenerative braking capability of SSCBs was presented in [32]; however, the system complexity and cost can be higher, and the current breaking time is approximately 40 ms.

HCBs consist of power semiconductor switching devices and a fast mechanical switch in the main circuit current path. A protective arrester bank with a higher voltage than the DC system was placed in parallel with the CB to protect the devices during the fault events [13], and voltage balancing circuitry, passive or active, was used across the power semiconductor devices [7], [33], [34]. The interruption speed of the mechanical switch, which can take several milliseconds to break the current, is a concern in HCB design. A 2 MW medium voltage HCB was designed using Silicon Carbide (SiC) emitter turn-off thyristors [35], [36]. The HCB employed two power switching devices connected in series with a mechanical switch that had a current interruption time of 2 ms. Another technology proposed an active fault current-sharing technique to improve medium voltage DC (MVDC) CB performance in shipboard applications [6]. This approach decreased the peak interrupting current of the circuit breaker by controlling power converters connected in parallel with the CB, allowing them to share the fault current.

As a popular solution for high voltage DC (HVDC) system protection, HCB technology was introduced in [13]. It utilized auxiliary power electronic switches, such as IGBTs, connected in series with a mechanical switch to achieve a fast response time. This design had a steady-state loss of nearly 0.01% of the HVDC circuit breaker's rated capacity. However, this design required a considerable sizing of surge absorbers. LC resonant network-based HCBs are being explored further for medium voltage DC (MVDC) applications [37]. This method can also reduce the number of power electronics switches required in the circuit and the need for surge arresters or varistors.

Using an LC network-based auxiliary resonant circuitry in CBs, it will be possible to create a current zero-crossing in the main CB path and also control the response speed based on the application. In SSCBs, especially which use thyristors as the main switch (MS), the devices will be turned off during the current zero crossing with minimal to no surge voltages. In HCBs and SSCBs that use controllable devices like IGBTs, FETs, etc., the current zero-crossing can be timed to dissipate the surge energy and reduce the requirements of the protection devices. In some applications involving mechanical disconnect, it may also lead to a decrease in the amount of chemicals such as sulfur hexafluoride (SF_6), a compound over 20,000 times more potent than carbon dioxide (CO_2) in impacting global warming, used for quenching the surge energy [38].

This paper introduces two resonant network-based CB topologies (topology-I and topology-II) designed to feature fast response time, high efficiency, and ease of implementation. Topology-I uses a single thyristor and a coupled inductor connected in line with the main switch (MS) along with a capacitor for the LC resonance, while Topology-II employs two thyristors, a small diode, and a single inductor along with a capacitor to enable the current zero-crossing. These topologies were evaluated using hardware-in-the-loop (HiL) tests and laboratory experiments on a scaled-down prototype.

The main advantages of the proposed topologies are:

(i) Simple design and implementation - use reliable thyristor switches and don't need complex capacitor charging circuits.
(ii) High steady-state efficiency – achieve over 99.9% based on experimental tests of thyristor-based SSCB.
(iii) Fast response - takes less than 50 μs to reach near-zero fault current levels; it can be further improved by using IGBTs or FETs (SiC, GaN, etc.).
(iv) High reliability - significantly reduces surge voltage across the MS during faults.
(v) Flexibility - can be applied to most existing SSCB and HCB configurations for medium-voltage DC systems.

II. PROPOSED DC CIRCUIT BREAKER TOPOLOGIES AND OPERATING PRINCIPLES

A. PROPOSED TOPOLOGY-I: USING COUPLED INDUCTOR

The proposed CB topology-I, depicted in Figure 1, employs a coupled inductor (with unequal turns ratio) and a charging resistor to regulate the capacitor voltage to the input DC bus voltage (V_g) during steady-state operation. The essential advantage of this design is that by using a 2:1 turns ratio in the coupled inductor instead of 1:1, the auxiliary circuit capacitor can be charged to the same voltage as the MVDC input via a simple LC network arrangement instead of needing to be charged to twice the input voltage for achieving the current

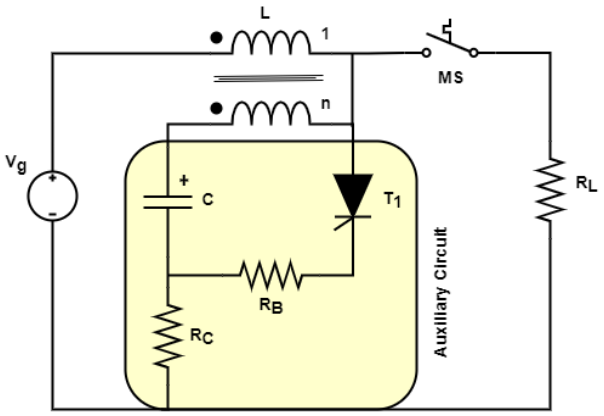

FIGURE 1. Proposed CB topology-I with a coupled inductor having an unequal turns ratio.

zero-crossing. The topology features a single thyristor in the auxiliary circuit, and the MS is connected in series with the primary winding (L_1) of the coupled inductor in the main current path. The secondary winding (L_2) and capacitor (C) are connected in series to facilitate capacitor charging and discharging. A thyristor is used as the main switch (MS) in this study, with the proposed LC topology interrupting fault current to almost zero level within a few tens of microseconds without an additional turn-off commutation circuit. However, other solid state devices (like IGBTs, FETs, etc.) or a hybrid combination of electro-mechanical switches may also be used as the MS. Figure 2 illustrates the operating principle of the circuit, showing its four modes and the corresponding waveforms are displayed in Figure 3.

1) Mode I ($t_0 < t < t_1$): This period is primarily designated for charging the capacitor (C). During this time, the MS is off, and the DC input provides adequate energy for charging the capacitor through resistor R_c. The inductor L has a minimal impact on this subinterval due to the high value of R_c. The voltage and current of the capacitor during this period (as depicted in Figure 3) can be estimated using equations (1) and (2).

$$v_c(t) = V_g(1 - e^{\frac{-t}{C \cdot Rc}}) \tag{1}$$

$$i_c(t) = -\frac{V_g}{Rc} \cdot e^{\frac{-t}{C \cdot Rc}} \tag{2}$$

where V_g is the input DC voltage. Once the capacitor is charged, the current flowing through resistor Rc is negligibly small. The ideal value for R_c can be determined based on the thyristor turn-off state, i.e., when T_1 is turned off after the fault has been isolated by the MS. R_c should be large enough to limit the peak charging current to below the holding current of T_1 but small enough to charge the capacitor reasonably fast (in a few seconds). In other words, R_c should be greater than V_g/I_h, where I_h is the minimum holding current for T_1. For example, if V_g is 6 kV and I_h is 0.18 A, R_c should be more than 33.33 kΩ

2) Mode II ($t_1 < t < t_2$): The MS is closed at $t = t_1$ to allow the flow of power from the DC source to the load, thereby entering the normal operation. In this state, the transmission line is energized, and the auxiliary circuit remains idle.

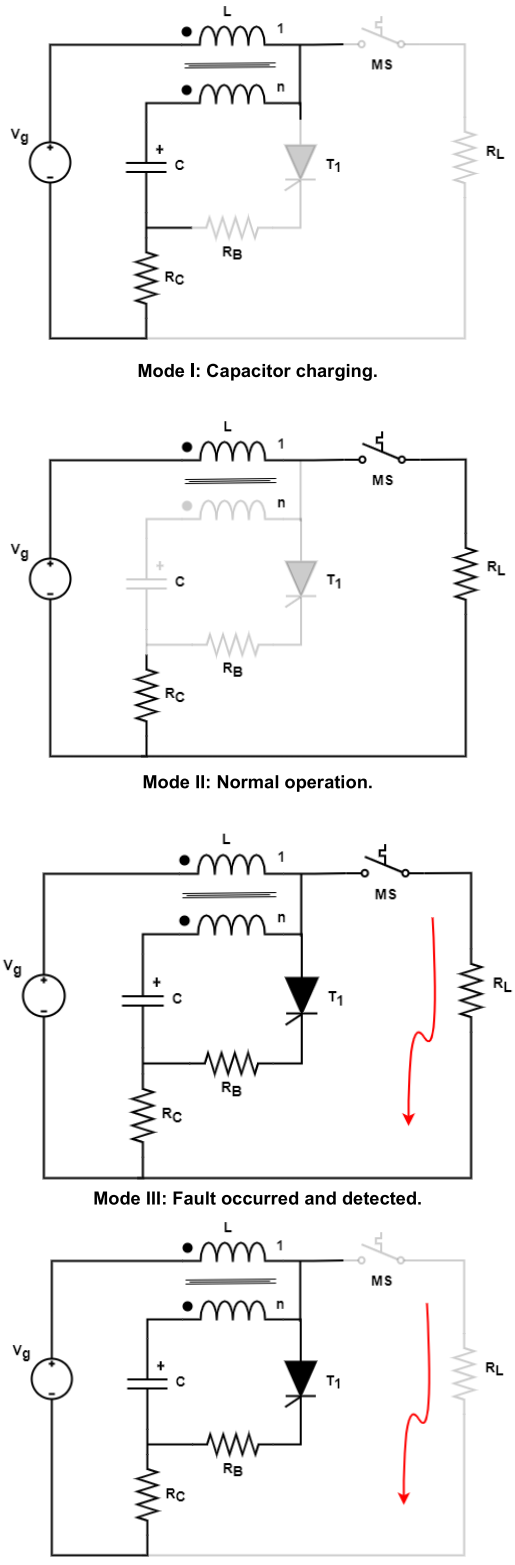

FIGURE 2. Operating modes of topology-I with a coupled inductor.

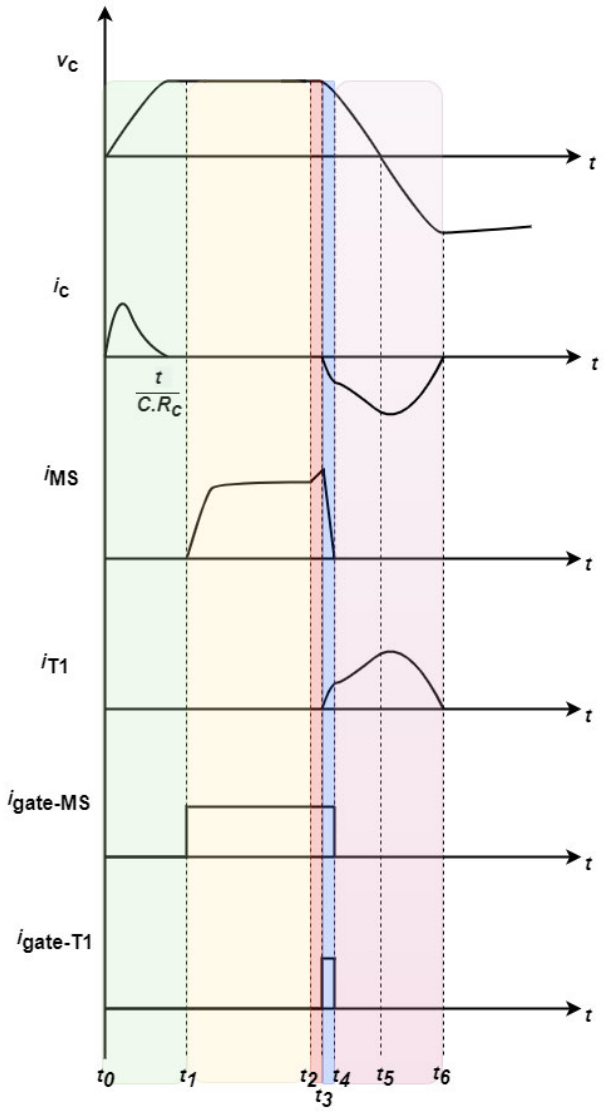

FIGURE 3. Operating waveforms of topology-I.

3) Mode III ($t_2 < t < t_4$): In the event of a fault, the current in the MS increases rapidly, limited only by the primary winding and the inductance of the transmission line. At t_3, when the current reaches the specified fault current limit value (or detection level defined in the controller), a trigger pulse is sent to thyristor T_1. The capacitor then discharges through the secondary winding with opposite polarity, with its current opposing the current of the MS, then quickly reducing it to zero. The resistor R_B, with a small value of a few hundred milliohms, limits the peak current in the auxiliary circuit and adjusts the circuit's quality factor. Once the main switch's current reaches zero, the MS turns off at t_4 to isolate the fault from the power supply.

4) Mode IV ($t_4 < t < t_6$): Once the MS is turned off with zero DC current, the capacitor continues to discharge for a short time through RB and T_1 as shown in Figure 3. When the thyristor current drops below its holding current, the thyristor automatically turns off, and the circuit breaker returns to its

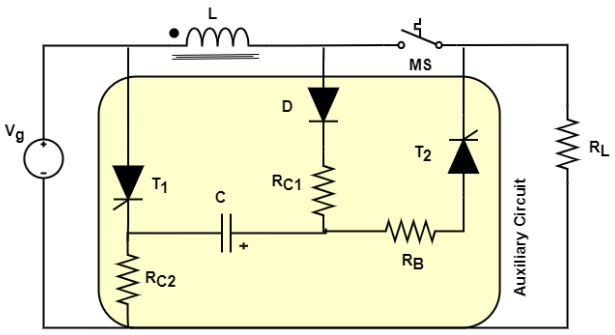

FIGURE 4. Proposed CB topology-II with a single in-line inductor.

state in Mode I. This occurs at t_5 during the quasi-resonant half-cycle period. During this time, the voltage and current of the capacitor can be estimated using equations (3) and (4).

$$v_c(t) = V_g \cos \omega_o t \tag{3}$$

$$i_c(t) = \frac{V_g}{Z_o} \sin \omega_o t \tag{4}$$

where $Z_o = \sqrt{\frac{L_{eq}}{C}}$ is the characteristic impedance, $\omega_o = \frac{1}{\sqrt{L_{eq}C}}$ is the resonant frequency of the LC network after a fault event is isolated, and L_{eq} is the equivalent inductance of the LC network. After the time t_6, the system returns to Mode I.

B. PROPOSED TOPOLOGY-II: USING SIMPLE INDUCTOR

The second proposed topology, referred to as topology-II, uses a simple inductor instead of a coupled inductor and is depicted in Figure 4. This configuration has the potential to reduce the size of the magnetics but requires an additional thyristor compared to topology-I. The components include an inductor L, the main switch MS, and the auxiliary circuit's capacitor C. The inductor, diode D, and resistors R_{c1} and R_{c2} (both equal to R_c) provide the path for charging the capacitor. The fault-handling circuit, consisting of thyristors T_1 and T_2 and the resistor R_B, creates a resonant connection between the capacitor C and the inductor L in case of a fault. The resistor R_B, of a small value, is used to adjust the quality factor of the LC network and fine-tune the current discharge rate. During regular operation, the resistors in the auxiliary circuit are inactive, resulting in minimal power loss and low power rating requirements. The modes of operation for topology-II are shown in Figure 5, with corresponding waveforms in Figure 6.

1) Mode I ($t_0 < t < t_1$): During the capacitor charging period, Mode I is in effect, as illustrated in Figure 5. In this mode, the main switch (MS) remains open, and the capacitor charges continuously through the diode and the resistors R_{c1} and R_{c2}. The high values of R_{c1} and R_{c2} result in the minimal effect of the inductor L during this subinterval. The capacitor voltage and current can be estimated using the equations in

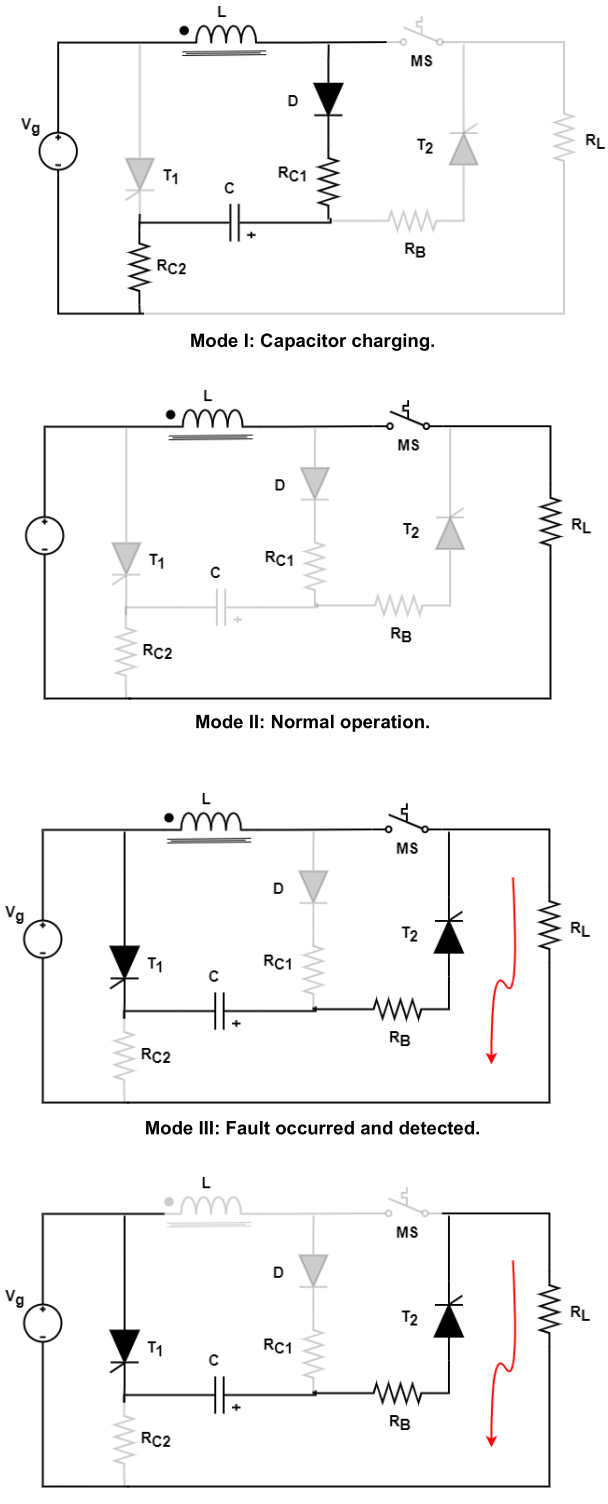

FIGURE 5. Operating modes of topology-II using a simple in-line inductor.

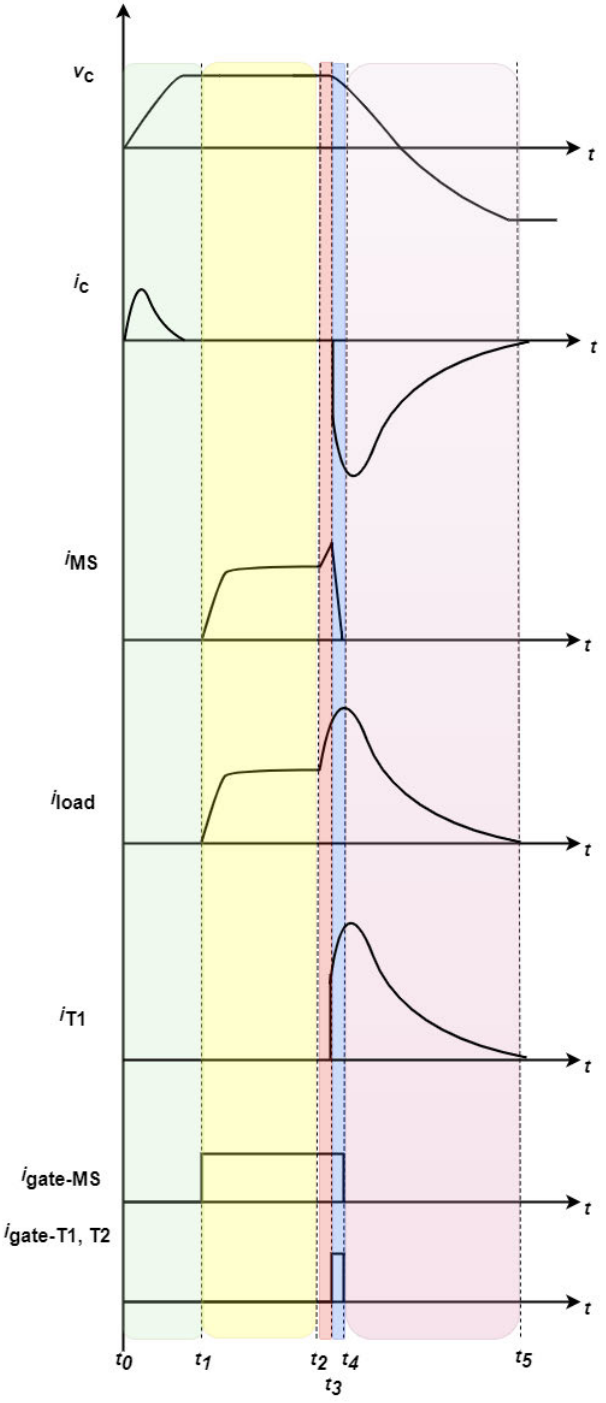

FIGURE 6. Operating waveforms of topology-II.

(5) and (6).

$$v_c(t) = V_g(1 - e^{\frac{-t}{C\cdot(Rc1+Rc2)}}) \tag{5}$$

$$i_c(t) = -\frac{V_g}{(Rc1 + Rc2)} \cdot e^{\frac{-t}{C\cdot(Rc1+Rc2)}} \tag{6}$$

where V_g is the input DC voltage. When the capacitor reaches full charge, only a small current flows through R_{c1} and R_{c2} to sustain the charge.

2) Mode II ($t_1 < t < t_2$): In this operating mode, the main switch (MS) is closed, allowing power to be delivered from the DC source to the load side. The primary path becomes energized while the auxiliary circuit remains inactive.

3) Mode III ($t_2 < t < t_4$): At the occurrence of a fault event, the current flowing through the MS suddenly spikes, and is only restricted by the primary and power line inductances. When this current reaches the set fault current limit value at time t_3, thyristors T_1 and T_2 are triggered simultaneously. This results in the discharge of the capacitor through L_1 and RB, with a current discharge rate that is faster than the rising rate of the fault current. The capacitor discharge continues until the entire fault current is supplied through it, causing the current through MS and L to drop to zero. Finally, MS is opened at time t_4, ending this subinterval.

4) Mode IV ($t_4 < t < t_6$): During this subinterval, the fault current persists in both the load and the auxiliary circuit capacitor. This results in the reverse charging of the capacitor to V_g, causing the current in the auxiliary network to drop to zero. This allows for the natural turn-off of thyristors T_1 and T_2 without needing external circuits. For faster response time, T_1 can be substituted with SiC FETs, IGBTs, or IGCTs, an external control circuit will then be necessary to detect the current and switch the devices off.

III. RESULTS AND DISCUSSIONS

The proposed circuit breaker topologies are designed and tested using a real-time Typhoon HiL unit with a capacity of 1.2 MW (6 kV, 200 A) and a laboratory prototype with a capacity of 500 W (100 V, 5 A), as outlined in this section. The HiL verification is done mainly to test the controllers of the proposed concepts in a simulated practical application, whereas the lab scale protype is able to validate the combined power hardware and control mechanisms. In both the HiL and experimental evaluations, a thyristor is considered as the main switch (MS), assuming a SSCB.

A. HARDWARE IN-THE-LOOP RESULTS: MEGAWATT SYSTEM LEVEL

The datasheet of the thyristor can be found in [39]. The thyristor has a voltage rating of 2.6 kV and an average on-state current rating of 517 A, a maximum on-state voltage of 3.2 V, a holding current of 250 mA, and a turn-off time of 25 μs. For the HiL circuit, four thyristors were connected in series to achieve an off-state blocking capability of approximately 10 kV required for a 6 kV, 1.2 MW application, such as subsea motor drives or shipboard DC distribution.

1) TOPOLOGY-I: BASED ON COUPLED INDUCTOR

The voltage and current waveforms for the CB topology-I (with a coupled inductor) are presented in Figure 7 and Figure 8, tested using a Typhoon real-time HiL system. The testing was conducted using the system parameters listed in Table 1.

The resonant network (L and C) design results in a fast response time of several tens of microseconds, as demonstrated in Figure 7. In normal operation mode (prior to a fault event), the thyristor T_1 is OFF, and no current flows through it, as previously discussed. Upon the MS current exceeding the set fault detection level, T_1 is triggered ON

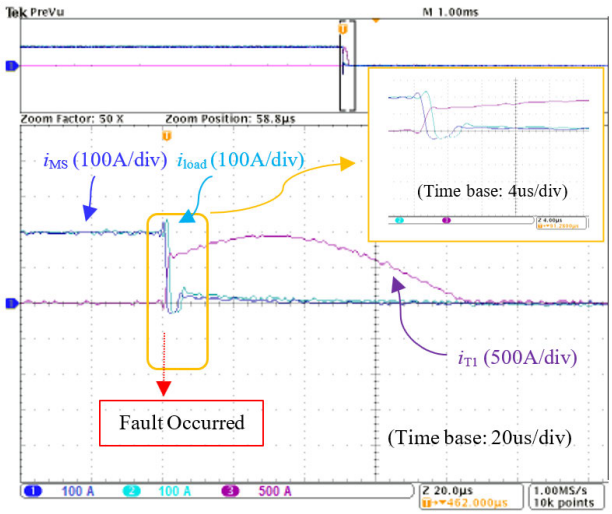

FIGURE 7. Current waveforms for the CB topology-I -based on HiL result, with a fast response time. Ch1 (blue) is the MS current. Ch2 (green) load current. Ch3 (purple) is thyristor T_1 current waveform.

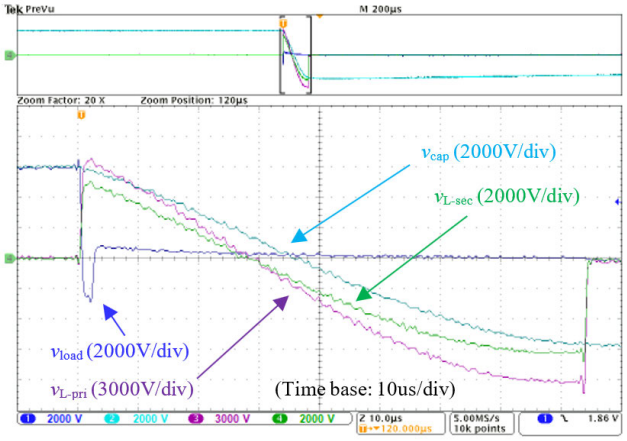

FIGURE 8. Voltage waveforms for the CB topology-I – based on HiL results. Ch1 (blue) is load voltage. Ch2 (green) is capacitor voltage. Ch3 (purple) is coupled primary inductor voltage. Ch4 (green) is coupled inductor secondary voltage.

TABLE 1. HiL system parameters for topology-I.

Parameter	Value	Parameter	Value
DC input voltage	6 kV	Fault detection current	220 A
Rated load current	200 A	Capacitance	4.7 µF
Resistance R_C	100 kΩ	Resistance R_B	1 Ω
Coil inductance	100 µH		

(entering Operation Mode III), causing the capacitor to discharge through R_B and T_1 rapidly. Well within 20 μs, the rapid discharge of the capacitor reduces the main switch current to zero, causing the main switch to turn OFF without the need for surge arresters or other protection devices. The capacitor continues to discharge until its current falls below the thyristor T_1 holding threshold, leading to T_1 turning OFF without any auxiliary circuits. Compared to the CB in [40], the proposed approach has a higher peak secondary

TABLE 2. HiL system parameters for topology-II.

Parameter	Value	Parameter	Value
DC input voltage	6 kV	Fault detection current	220 A
Rated load current	200 A	Capacitance	4.7 µF
Resistance R_{C1}	100 kΩ	Resistance R_{C2}	100 kΩ
Coil inductance	1 mH	Resistance R_B	4 Ω

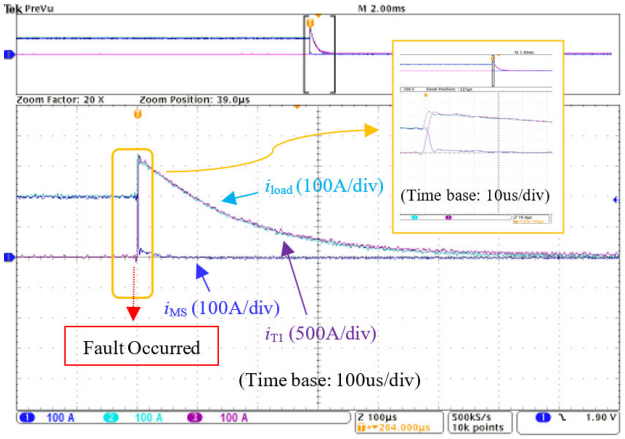

FIGURE 9. Current waveforms for the CB topology-II -based on HiL results with a fast response time. Ch1 (blue) is the MS current. Ch2 (green) load current. Ch3 (purple) is thyristors (T_1, T_2) current waveform.

current in the coupled inductor, but the *mmf* requirement ($n*I_L$(secondary)) remains unchanged. It is fairly straightforward to select thyristors capable of handling this transient current requirement. The thyristor current reaches zero within a few hundred microseconds after the MS OPEN command is given. However, it may take a few milliseconds for the MS to completely turn off in case of HCB.

From Figure 8, it can be observed that the capacitor is charged only to Vg, instead of $2V_g$, as the coupled inductor turn ratio has been designed to be 2:1. Upon the occurrence of a fault event, the voltage across the primary winding increases to about double the input DC voltage, owing to resonant operation. However, this condition is temporary and lasts only for a brief period. Choosing the coupled inductor carefully is essential to ensure that its core does not saturate under these conditions.

2) TOPOLOGY-II: BASED ON SIMPLE INDUCTOR

The parameters for the second proposed topology (topology-II) are detailed in Table 2. This topology utilizes a small in-line inductance. The voltage and current waveforms using the Typhoon HiL system are presented in Figure 9 and Figure 10, respectively. As seen in the waveforms, upon the occurrence of a fault, the capacitor begins discharging at a much faster rate compared to the increase in fault current. This causes the current carried by the main switch to drop to zero in just a few microseconds. Subsequently, the main switch (MS) is opened by a trigger signal. Afterward, the fault current passes

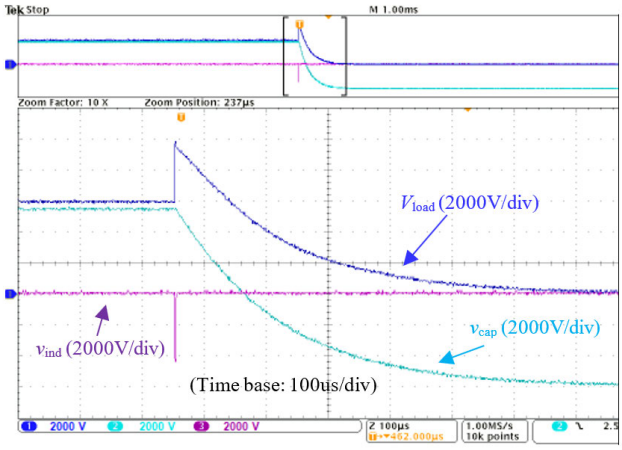

FIGURE 10. Voltage waveforms for the CB topology-II - based on HiL result. Ch1 (blue) is load voltage. Ch2 (green) is capacitor voltage. Ch3 (purple) is the inductor voltage.

through the capacitor and rapidly decreases to a low value within 400 μs. The thyristor and load currents reduce to zero within 600 μs once the fault is handled.

The voltage waveforms of the second proposed topology-II are displayed in Figure 10. One advantage of this topology is that the maximum voltage across the capacitor is limited to the input DC voltage (V_g) in all the operating modes. Additionally, the resonance period is very short, and ends as soon as the inductor current reaches zero and the MS is opened. After the resonance period, the capacitor starts to discharge through the resistance R_B. When the load current becomes zero, the capacitor voltage starts to charge back to the input DC voltage level, but in the opposite direction compared to the initial state (Mode I). The Typhoon HiL test bench is shown in Figure 11.

B. EXPERIMENTAL RESULTS FROM LABORATORY SCALE PROTOTYPE

Experimental prototypes of the two proposed resonant circuit breaker concepts are built and tested on a laboratory scale. The component values of the resistors and resonant L-C network are consistent with those used in the larger HiL design. The prototypes operate with a DC bus voltage of 100 V and a load current of 5 A. The inductors in the experimental setups used powdered iron as the core material. The results of the laboratory tests are in reasonable agreement with the performance of the megawatt-scale system discussed earlier via the Typhoon HiL unit.

1) TOPOLOGY-I WITH COUPLED INDUCTOR

In Figure 12, the experimental current waveforms for the CB topology-I utilizing a coupled inductor are presented. Upon detection of a fault event, the thyristor T_1 is triggered ON, causing the capacitor to rapidly discharge and quench the MS current in under 20 μs. The MS is then opened with minimal to no voltage surge, as its current drops to zero. Over the

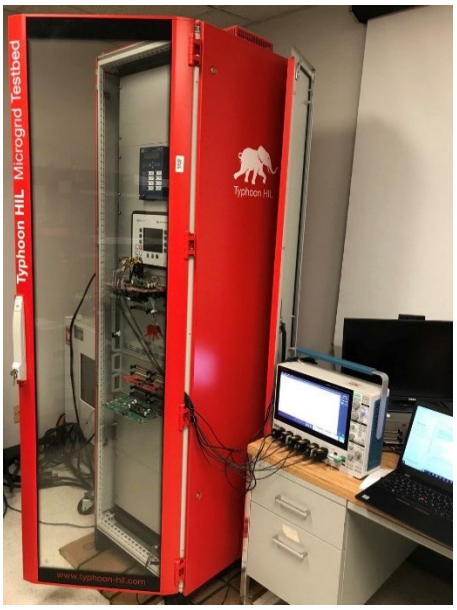

FIGURE 11. Typhoon HiL test bench.

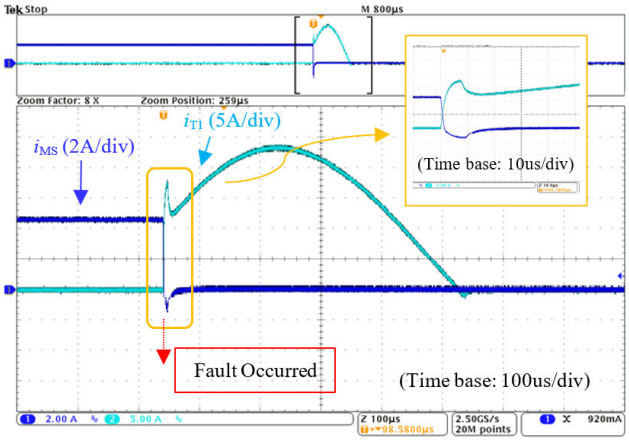

FIGURE 12. Current waveforms for the CB topology-I - based on experimental results with a response time of less than 20 us. Ch1 (blue) is the MS current. Ch2 (green) is thyristor T_1 current.

following 500 μs, the capacitor continues to discharge until the thyristor's (T_1) holding current is reached. Finally, T_1 turns off naturally once the capacitor current falls below its holding threshold.

Figure 13 displays the results of the voltages. The load voltage becomes zero after the fault is isolated (after the MS is open), and this occurs within several microseconds of the fault detection. The voltage across the coupled inductor's primary winding goes up to twice the input DC voltage due to the resonance operation, but it lasts only for a brief period.

2) TOPOLOGY-II WITH SIMPLE INDUCTOR

The experimental results for topology-II of the CB are presented in Figure 14 and Figure 15, which depict the current and voltage waveforms, respectively. As seen in the zoomed-in waveforms in Figure 13, the response time is

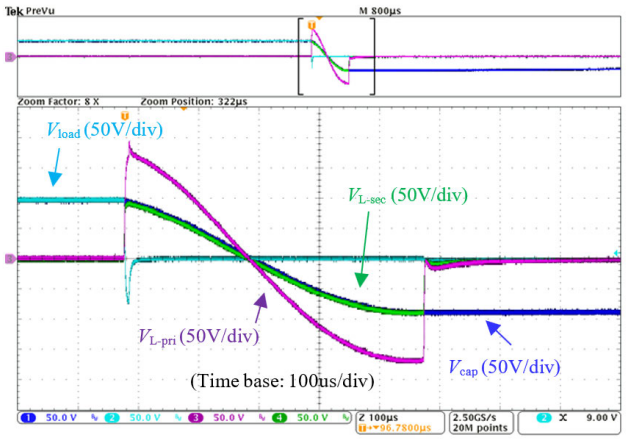

FIGURE 13. Voltage waveforms for the CB topology-I - based on experimental results. Ch1 (blue) is the capacitor voltage. Ch2 (green) is load voltage. Ch3 (purple) is coupled primary inductor voltage. Ch4 (green) is the coupled inductor secondary voltage.

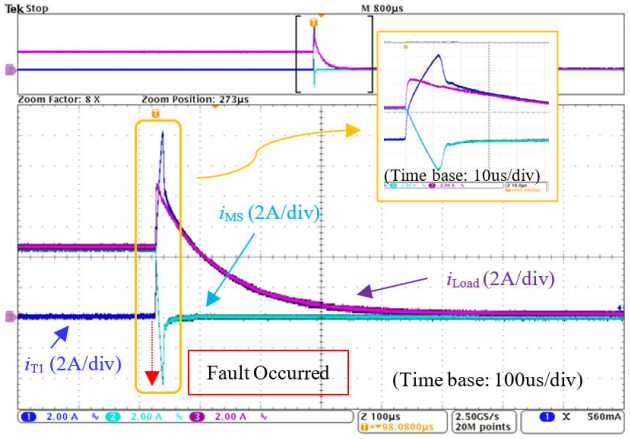

FIGURE 14. Current waveforms for the CB topology-II - based on experimental results with a response time of less than 20 us. Ch1 (blue) is the thyristor (T_1, T_2) current. Ch2 (green) is MS current. Ch3 (purple) is the load current.

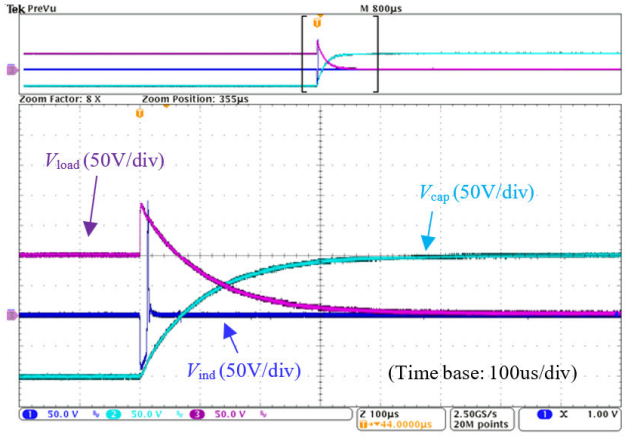

FIGURE 15. Voltage waveforms for the CB topology-II - based on experimental results. Ch1 (blue) is the inductor voltage. Ch2 (green) is capacitor voltage. Ch3 (purple) is load voltage.

roughly 20 μs while the total fault detection, isolation, and auxiliary circuit capacitor discharge time are around 500 μs. Figure 14 demonstrates that, upon the occurrence of a fault,

the capacitor C instantly begins discharging through R_B, T_1, and T_2 to counteract the entire fault current, as the inductor L prevents an immediate change in the current. The current flowing through T_1 and T_2 decreases until it reaches the holding current of the thyristors, at which point both thyristors turn off naturally. These experimental results affirm the efficient operation of topology-II in terms of the commutation process, response time, and ease of implementation for MVDC systems, with a response time requirement ranging from tens of microseconds to less than 1 ms considering the time for fault detection, isolation, and post-isolation.

The experimental results obtained from the laboratory prototypes of both the proposed CB topologies with in-line inductors validate their smooth commutation process, high response speed, and simple implementation in a practical system. Both experimental and real-time HiL results affirm that the proposed topologies are suitable for MVDC systems with response time requirements ranging from a few microseconds to 1 ms, taking into account the time needed for fault event detection, isolation, and post-isolation.

IV. TOPOLOGY SELECTION

In this section, the proposed resonant network-based topologies are briefly discussed with a view of their potential adoption in SSCB and HCB applications in MVDC distribution (1 kV to 100 kV). Based on the technology development survey of DC circuit breakers presented in [1] and the literature reviewed, the resonant topologies proposed in this paper can be modified by replacing the main switch (MS) with other power switches, such as IGBTs, SiC FETs, GTOs, IGCTs, or a combination of solid-state devices along with a fast disconnect (HCB), to meet the system requirements. The fault current can be interrupted within tens of microseconds, thus reducing the challenges related to semiconductor devices' protection capabilities, voltage surge arrester requirements, etc. This approach results in a significant reduction in instantaneous fault energy in the different CB elements.

V. CONCLUSION

This paper presented two resonant hybrid circuit breaker topologies for medium voltage DC applications such as subsea drives for oil and gas production, shipboard or aircraft power distribution, etc. The proposed concepts with fast response speeds provide a simple way to efficiently handle faults in MVDC systems. The performance of the topologies was verified through Typhoon Hardware-in-the-Loop tests and laboratory experiments. Results showed that both topologies offer low response times (in μs) and high efficiencies ($>$99.9%) for MVDC systems. Additionally, the design size, cost, and complexity are reduced by eliminating the need for multiple power electronics switches connected to the main switch. The second proposed topology-II has a slightly higher peak fault current, but a smaller inductor size and lower voltage rating requirement for the main components.

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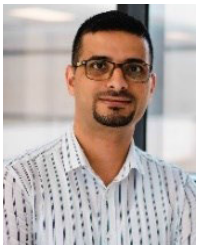

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