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RESEARCH ARTICLE

Evaluation and Performance of Three-Phase Inverter Using Multiple Bidirectional Choppers Intended for 1.5-kVdc PV Systems

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ABSTRACT This article focuses on the chopper-cell number of a novel three-phase inverter for utility-scale photovoltaic (PV) systems where multiple cascaded bidirectional chopper cells and a three-phase line-frequency transformer with a three-legged core are used. The inverter per phase is composed of a main converter, which is equivalent to the conventional bidirectional chopper, and an auxiliary converter, which is composed of multiple cascaded chopper cells. Although the inverter performance can be improved by increasing the chopper-cell number because of increased switching frequency and reduced voltage steps, the increased cell number may result in increased converter loss and cost. However, no paper has evaluated the chopper-cell number of the inverter to the best of the authors' knowledge. Further, no paper has carried out experimental verification of the inverter during the power faults. This article evaluates the inverter using two cells per phase (two-cell inverter) with the one using three cells per phase (three-cell inverter) under the same equivalent switching frequency in terms of converter loss, efficiency, and steady/transient state performance. The numerical analysis shows that the two-cell inverter shows superiority over the three-cell inverter in converter efficiency. Further, the experiments using a 1.5-kW downscaled model verify the inverter performance under the normal and fault conditions.

INDEX TERMS Low-voltage ride-through (LVRT), modular multilevel cascade converters (MMCCs), utility-scale PV systems.

I. INTRODUCTION

Owing to the accelerated development of the photovoltaic (PV) generation systems [1], [2], [3], [4], [5], [6], [7], [8], [9], [10], [11], [12], [13], an increasing number of utility-scale PV systems have been connected to the power grids. However, the conventional two- or three-level three-phase grid-connected inverters are facing challenges because the increased ac voltage level, which is to decrease the loss, narrows the available range of maximum power point tracking (MPPT) in return [1], [5], [14]. Meanwhile, PV inverters based on the latest modular multilevel cascade converter (MMCC) topologies have drawn attention as the connection interface between the PV systems and the grids in recent years [15], [16], [17], [18]. With the MMCCs, the size of passive filter components for grid connection could be reduced. In addition, the inverter performance can be improved with the MMCCs because of increased equivalent switching frequency as well as reduced voltage steps.

The authors of this article have presented a three-phase inverter for 1.5-kVdc grid-connected utility-scale PV systems, the circuit configuration of which is shown in Fig. 1. The inverter is based on the technologies used in the MMCCs and the inverter of each phase is composed of a main converter and an auxiliary converter. The main converter is equivalent to the conventional bidirectional chopper and the auxiliary converter is composed of multiple cascaded bidirectional chopper cells, where the number of cells is $N = 3$ in the

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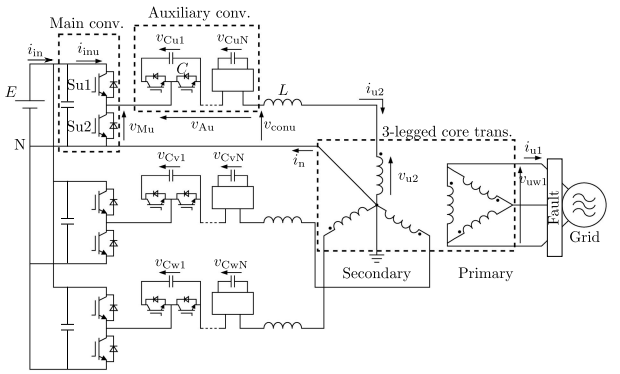


FIGURE 1. Circuit configuration of three-phase PV inverter based on multiple bidirectional choppers for utility-scale PV systems.

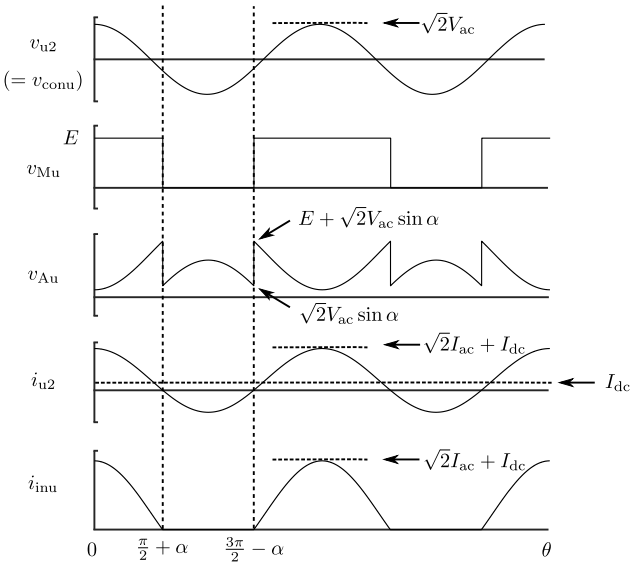


FIGURE 2. Ideal u-phase voltage and current waveforms of Fig. 1 circuit with ZCS.

previous works (three-cell inverter). The switching frequency of the main converter is 50 Hz, which is the same as the line frequency, whereas that of each chopper cell in the auxiliary converter is 7.2 kHz. When the phase-shifted PWM is applied, the equivalent switching frequency of the auxiliary converter is 21.6 kHz (= 7.2 kHz×3). The auxiliary converter functions as a power flow controller and an active power filter to reduce the high-frequency harmonic components. In addition, a three-phase line-frequency transformer with a three-legged core is used for grid connection so that the zero-sequence dc current can flow to the neutral point of the transformer without affecting transformer operation, which enables the boost operation of the inverter. Further, because of the direct connection between the negative terminal of the PV array and the ground, no high-frequency circulating current flows via the stray capacitance of the PV array, which reduces the difficulty of the parallel operation of the inverters. Consequently, a wider MPPT range and a smaller ac root-mean-square (RMS) current can be achieved simultaneously. The operation principles and control method of the inverter along with the efficiency comparison with that of the conventional two- and three-level inverters are provided in [1] with experimental verification using a 1.5-kW downscaled model.

Generally speaking, the selection of the cascaded cell (submodule) number of the MMCCs is crucial. When the MMCCs are applied to high-voltage applications such as high-voltage direct-current systems, the required cell number is mainly determined by the required voltage levels, and the number of cells can reach several hundreds, which eventually increases the cost and volume of the converter [15], [19]. A significant amount of research has been carried out to reduce the cost and volume of the MMCCs using new circuit topologies [20], the latest power devices [21], and the capacitor voltage oscillation reduction method [22]. On the other hand, the voltage level of the Fig. 1 circuit is 1.5 kVdc so it is not necessary to increase the cell number for increasing the voltage level. Instead, the cell number is increased to improve the inverter performance and to reduce the voltage/current harmonics for a smaller size of passive filter components. The minimum cell number per phase for enjoying the benefit of the MMCC technologies is two and it can be set to any higher number. However, the increased cell number may result in increased converter loss and cost. Hence, a detailed evaluation of the inverters with different cell numbers is required.

In addition, considering the potential damage to the power devices of MMCCs caused by the power faults [23], [24], the low-voltage ride-through (LVRT) capability of the proposed inverter circuit is also necessary to be verified, which has not been carried out in the authors' previous works. Even though a significant amount of research has been carried out for verifying the LVRT capability of various MMCC topologies [25], [26], [27], [28], there is no past research focusing on that of the proposed inverter circuit with experimental verification to the best of the authors' knowledge.

There are two main objectives in this article, following the authors' previous works [1], [2], [3]. The first objective is to evaluate the inverter using two cells per phase (two-cell inverter) with the one using three cells per phase (three-cell inverter) in terms of converter loss and efficiency. The reason for choosing the numbers two and three for evaluation is that two is the minimum number and three is the second minimum number that can contribute to cost reduction. It should be noted that no change occurs in the MPPT range under the condition of different cell numbers. For a fair comparison, the same equivalent switching frequency is assumed in both inverters while their dc-capacitor voltages are different. Further, the dynamic behaviors of both inverters under the steady and transient states are evaluated experimentally using a 1.5-kW downscaled model.

The rest of this article is organized as follows. Sections II and III describe the circuit configuration, operation principles, and control method of the proposed inverter. The theoretical loss and efficiency comparisons are presented in Section IV. Section V shows the comparisons of experimental waveforms between the two-cell inverter circuit and the three-cell inverter circuit in different operational cases, which contains the THD performance comparison.

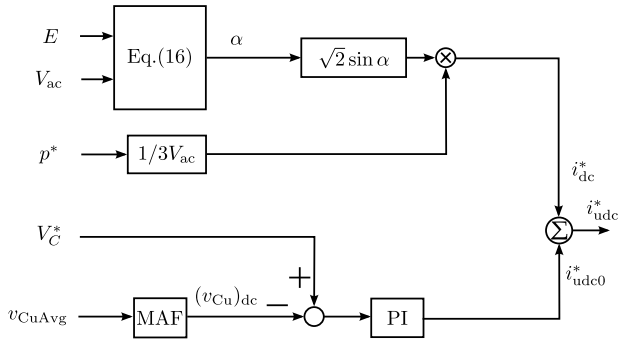


FIGURE 3. Block diagram of u-phase dc-capacitor voltage control when ZCS is achievable.

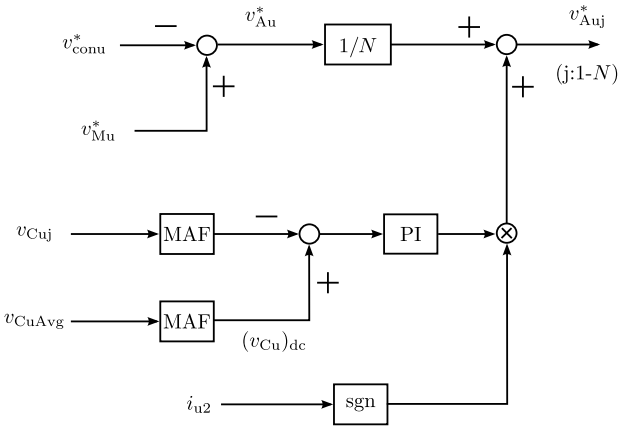


FIGURE 4. Block diagram of output voltage calculation for u-phase cells including individual balancing control.

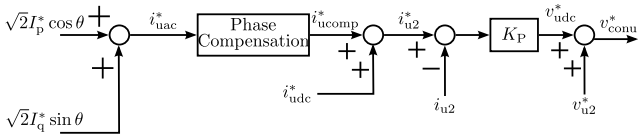


FIGURE 5. Block diagram of u-phase inductor current control.

II. CIRCUIT CONFIGURATION

The circuit configuration of the proposed three-phase PV inverter is shown in Fig. 1. The following explanation will focus on the u-phase inverter because the three phases have identical circuit configurations. The inverter is composed of a main converter and an auxiliary converter. The former is equivalent to the conventional bidirectional chopper and the latter is composed of multiple cascaded connected bidirectional choppers. The number of chopper cells per phase was set to $N = 3$ in [1], [2], and [3], whereas it was set to either $N = 2$ or $N = 3$ in this article. The ac (output) side of the inverter is connected to the secondary side of a three-phase transformer with a three-legged core via an ac-link inductor. The transformer has Δ-connected windings on the primary side and Y-connected windings on the secondary side, where the neutral point is connected to the negative terminal of the input dc voltage, N. The switching frequency of the main converter was set to 50 Hz to match the grid frequency. In contrast, the switching frequency of each chopper cell of the auxiliary converter was set to 7.2 kHz for the three-cell inverter and to 10.8 kHz for the two-cell inverter. In this case, the equivalent switching frequency of the two inverters is the same and it is 21.6 kHz in the following experiments. The phase-shifted PWM is applied to reduce harmonic voltage/current. This circuit is characterized in that a dc current flows to the neutral point of the transformer for boost operation, while it does not affect the transformer operation because it corresponds to the zero-sequence current in the three-phase circuit. The detailed explanation of the transformer operation is provided in [1] so that it is left out in this article. The grid faults are performed using a fault simulator that is connected between the grid and the transformer as shown in Fig. 1. The single-line-to-ground (SLG) fault is performed on u-phase and the three-phase (3P) fault is performed on three phases.

In Fig. 1, E is the input dc voltage corresponding to the PV array voltage, v_{Mu} is the main converter voltage, v_{Cu1} and v_{CuN} are the dc-capacitor voltages, v_{Au} is the auxiliary converter voltage, v_{conu} is the inverter line-to-neutral voltage, v_{u2} is the line-to-neutral secondary voltage of the transformer, v_{uw1} is the line-to-line transformer (i.e., grid) voltage, i_{inu} is the input dc current, i_n is the neutral current, i_{u1} is the grid current and i_{u2} is the inductor current. The phases of v_{uw1} and v_{u2} are the same with the assumption that an ideal transformer is used.

III. OPERATION PRINCIPLES AND CONTROL METHOD

Because the operation principles and the control method are explained in [1], only the important figures and equations which are necessary for the later explanation will be shown. It is noteworthy that the explanation of this section is based on the normal operation of the proposed inverter circuit, where only active power is transferred. Further, the operation principles are valid for the inverter with any cell number. First of all, the following assumptions are made.

1) The voltage of the inductor including the leakage inductance, the on-state voltage, and the resistance and inductance of the leading wires are zero;
2) The fundamental-frequency component in i_{u2} is in phase with that in v_{u2};
3) Switching-ripple components in v_{Au} and i_{u2} are zero.

The following equation is obtained when the first assumption holds true:

$$v_{Au} = v_{Mu} - v_{conu} = v_{Mu} - v_{u2}. \tag{1}$$

In (1), v_{u2} is given by

$$v_{u2} = \sqrt{2}V_{ac}\cos\theta = \sqrt{2}V_{ac}\cos 2\pi f_{SM}t, \tag{2}$$

where V_{ac} is the RMS value of the line-to-neutral secondary voltage and f_{SM} is the grid frequency (50 Hz). It is noteworthy that V_{ac} is obtained as

$$V_{ac} = V_d/\sqrt{3}, \tag{3}$$

where V_d is the d-axis component of the transformer secondary voltage. Further, V_{ac} is expressed as

$$V_{ac} = V_{grid}/(\sqrt{3}a), \tag{4}$$

where V_{grid} is the RMS value of the grid line-to-line voltage and a is the transformer voltage ratio. With the second assumption, the inverter could achieve unity-power-factor operation. The third assumption could be satisfied by increasing the chopper-cell number and/or switching frequency. The ideal voltage and current waveforms of the u-phase inverter are shown in Fig. 2 with the three assumptions mentioned above, where zero current switching (ZCS) is achieved in the main converter. On the other hand, the waveforms where ZCS is not achievable are shown in [1], and the explanation is left out in this article.

A. OPERATION PRINCIPLES OF MAIN CONVERTER

The main converter voltage, v_{Mu}, is a 50-Hz square-wave voltage, where the fundamental-frequency component is in phase with v_{u2} whereas their amplitudes are different from each other. Specifically, v_{Mu} is given by

$$v_{Mu} = \begin{cases} E & (0 \le \theta \le \frac{\pi}{2} + \alpha, \frac{3\pi}{2} - \alpha \le \theta \le 2\pi) \\ 0 & (\frac{\pi}{2} + \alpha < \theta < \frac{3\pi}{2} - \alpha), \end{cases} \tag{5}$$

where α is the turn-on (turn-off) angle of the main converter.

Furthermore, E and α should satisfy the following relationships [1]:

$$E \ge \sqrt{2}V_{ac}, \tag{6}$$

$$0 \le \alpha \le \frac{\pi}{2}. \tag{7}$$

B. OPERATION PRINCIPLES OF AUXILIARY CONVERTER

The relationship $v_{Au} \ge 0$ should always hold because a chopper cell can only produce a voltage that is equal to or larger than zero. According to (1), (2), and (5), v_{Au} is derived as

$$v_{Au} = \begin{cases} E - \sqrt{2}V_{ac}\cos\theta \ (0 \le \theta \le \frac{\pi}{2} + \alpha, \frac{3\pi}{2} \\ -\alpha \le \theta \le 2\pi) \\ -\sqrt{2}V_{ac}\cos\theta (\frac{\pi}{2} + \alpha < \theta < \frac{3\pi}{2} - \alpha). \end{cases} \tag{8}$$

It is obvious from (8) and Fig. 2 that the minimum dc-capacitor voltage, v_{minC}, should satisfy the following relationship:

$$v_{minC} \ge (E + \sqrt{2}V_{ac}\sin\alpha)/N, \tag{9}$$

where N is the number of chopper cells per phase. v_{Au} is the sum of the high-frequency component, $(v_{Au})_{ripple}$, the dc component, $(v_{Au})_{dc}$, and the fundamental-frequency component, $(v_{Au})_{50\,\mathrm{Hz}}$, which is shown as

$$v_{Au} = (v_{Au})_{ripple} + (v_{Au})_{dc} + (v_{Au})_{50\,\mathrm{Hz}}. \tag{10}$$

$(v_{Au})_{ripple}$ corresponds to the harmonic components included in v_{Mu}. In other words, the auxiliary converter works as a series-type active power filter to reduce the high-frequency components in v_{conu}. From (1) and (2), $(v_{Au})_{dc}$ is equal to the dc component included in v_{Mu}:

$$(v_{Au})_{dc} = \frac{1}{2\pi}\int_0^{2\pi} v_{Mu}\,d\theta = E(\frac{1}{2} + \frac{\alpha}{\pi}). \tag{11}$$

TABLE 1. Circuit parameters used for loss calculation.

DC input voltage	E	960 V
Secondary line-to-line voltage	$\sqrt{3}V_{ac}$	1150 V
Two-cell inverter dc-capacitor voltage	V_C	650 V
Three-cell inverter dc-capacitor voltage	V_C	420 V
Two-cell inverter carrier freq. (aux.conv.)	f_{SA}	3 kHz
Three-cell inverter carrier freq. (aux.conv.)	f_{SA}	2 kHz
Carrier freq. (main conv.)	f_{SM}	50 Hz

Meanwhile, $(v_{Au})_{50\,\mathrm{Hz}}$ is derived as

$$(v_{Au})_{50\,\mathrm{Hz}} = (\frac{2E}{\pi}\cos\alpha - \sqrt{2}V_{ac})\cos\theta. \tag{12}$$

Equations (2) and (12) imply that $(v_{Au})_{50\,\mathrm{Hz}}$ is in phase with v_{u2} or 180° out of phase with each other which depends on the values of E, α and V_{ac}.

C. DERIVATION OF α

As mentioned in Sections I and II, a dc current I_{dc} should flow for boost operation. Consequently, i_{u2} is expressed as

$$i_{u2} = \sqrt{2}I_{ac}\cos\theta + I_{dc}, \tag{13}$$

where I_{ac} is the RMS value of the fundamental-frequency component and I_{dc} represents the dc component. The value of α and I_{dc} could be calculated by solving the relationship $P_{in} = P_{out}$, where P_{in} and P_{out} are the dc input power and the ac output power per phase, respectively. P_{in} is calculated as [1]

$$\begin{aligned} P_{in} &= \frac{1}{2\pi}\int_0^{2\pi} E i_{inu}\,d\theta \\ &= \sqrt{2}EI_{ac}(\frac{\cos\alpha}{\pi} + \frac{\pi + 2\alpha}{2\pi}\sin\alpha), \end{aligned} \tag{14}$$

and P_{out} is obtained from (2) and (13) as

$$P_{out} = V_{ac}I_{ac}. \tag{15}$$

α and I_{dc} are obtained with the reasonable approximations of $\sin\alpha \cong \alpha$ and $\cos\alpha \cong 1 - \frac{\alpha^2}{2}$ as [1]

$$\alpha = \begin{cases} -\frac{\pi}{2} + \frac{1}{2}\sqrt{\pi^2 - 8 + 4\pi\frac{\sqrt{2}V_{ac}}{E}} \ \text{(ZCS achievable)} \\ 0 \ \text{(ZCS not achievable)}, \end{cases} \tag{16}$$

$$I_{dc} = \frac{2\pi I_{ac}}{\pi + 2\alpha}(\frac{V_{ac}}{E} - \frac{\sqrt{2}}{\pi}\cos\alpha). \tag{17}$$

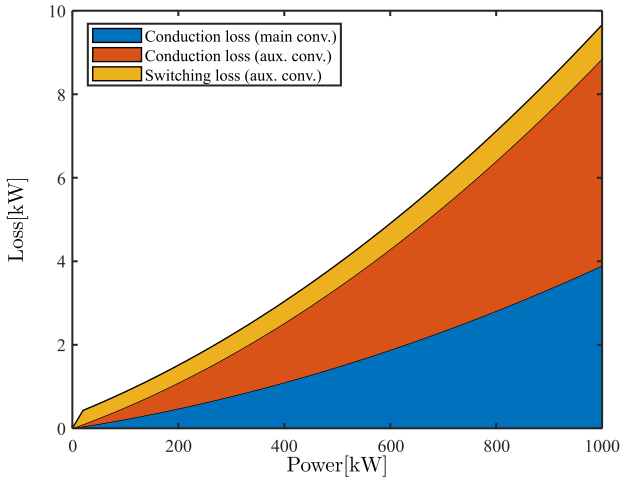
D. FEEDFORWARD CONTROL OF MAIN CONVERTER

The control of the main converter is composed of feedforward control of D_M, which is the duty ratio of the upper power devices (e.g., Su1 in Fig. 1), and it is common to all phases. The following relationship holds between D_M and α as

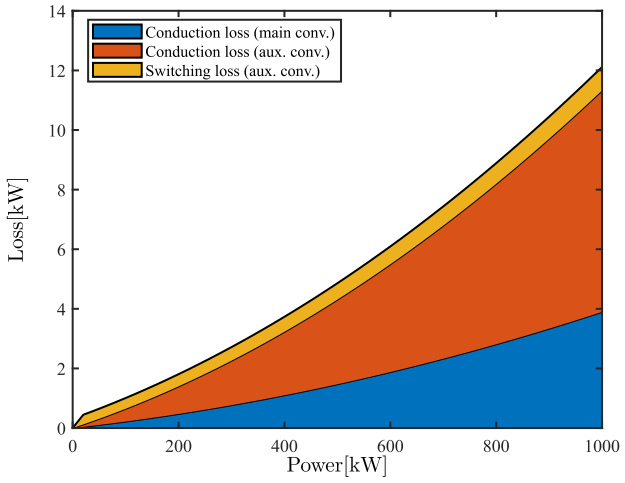
$$D_M = \frac{\pi + 2\alpha}{2\pi} = 0.5 + \alpha/\pi. \tag{18}$$

E. DC-CAPACITOR VOLTAGE CONTROL OF AUXILIARY CONVERTER

The dc-capacitor voltage control contains the following two parts:



(a)



(b)

FIGURE 6. Loss breakdown of proposed inverter: a) two-cell inverter circuit, b) three-cell inverter circuit.

TABLE 2. Parameters of proposed inverter used for comparison with same MPPT range.

DC input voltage	960 V	1100 V	1300 V
Two-cell inverter dc-capacitor voltage	650 V	680 V	730 V
Three-cell inverter dc-capacitor voltage	420 V	450 V	480 V
Secondary line-to-line voltage	1150 V		
MPPT range	960−1300 V		
Two-cell inverter carrier freq. (aux.conv.)	3 kHz		
Three-cell inverter carrier freq. (aux.conv.)	2 kHz		
Carrier freq. (main conv.)	50 Hz		

1) Phase dc-capacitor voltage control
2) Individual balancing control

Fig. 3 shows the control block diagram of the u-phase dc-capacitor voltage control when ZCS is achievable. i^*_{dc} is the reference value of I_{dc} shown in (17). v_{CuAvg} is the arithmetic average value of all the capacitor voltages in u-phase auxiliary converter which includes both dc and ac components. The role of the phase dc-capacitor voltage control is to regulate

TABLE 3. Two-cell inverter circuit parameters used for experiments.

Active power reference	p^*	1.5 kW
DC input voltage	E	85 V or 135 V
Nominal grid voltage	$V_{\rm grid}$	200 V
Voltage ratio of Tr.	a	$200/100 = 2$
Secondary voltage of Tr.	$V_{\rm ac}$	58 V
Inductor	L	0.21 mH
Leakage inductance of Tr.	l	0.27 mH
Chopper-cell count/phase	N	2
DC-capacitor voltage	$V_{\rm C}$	65 V or 75 V
Cell capacitor	C	4.4 mF
Carrier freq. (main conv.)	$f_{\rm SM}$	50 Hz
Carrier freq. (aux. conv.)	$f_{\rm SA}$	10.8 kHz
Fault duration	$t_{\rm F}$	100 ms

the dc component of v_{CuAvg}, $(v_{Cu})_{dc}$, to its reference value V^*_C using the dc component i^*_{udc0}. The moving average filter (MAF) with a frequency of 50 Hz is used to detect the dc component. Fig. 4 shows that of the individual balancing control. The function of the individual balancing control is to achieve the balancing of the dc-capacitor voltages used in each auxiliary converter since there could be differences between the dc-capacitor voltages even though $(v_{Cu})_{dc}$ is regulated to the reference value. Reference [1] provides a more detailed explanation of these control methods.

F. INDUCTOR CURRENT CONTROL

Fig. 5 shows the control block diagram for the u-phase inductor current control. With I^*_p and I^*_q, which are calculated from the reference values of active power, p^*, and reactive power, q^*, the reference value of the ac inductor current is given by

$$i^*_{uac} = \sqrt{2} I^*_p \cos\theta + \sqrt{2} I^*_q \sin\theta, \tag{19}$$

where θ is the phase angle of u-phase secondary side voltage obtained from the phase-locked loop. In the active power transfer operation mode, I^*_p equals I_{ac} and I^*_q equals zero. i^*_{ucomp} is the reference value of the u-phase ac component after the phase compensation, the detail of which is explained in [1].

The reference value of the u-phase inductor current, i^*_{u2}, is obtained as

$$i^*_{u2} = i^*_{dc} + i^*_{udc0} + i^*_{ucomp}. \tag{20}$$

Finally, the reference of the u-phase output voltage of the auxiliary converter, v^*_{Au}, is produced.

IV. LOSS AND EFFICIENCY COMPARISONS

The loss and efficiency analyses of the proposed three-cell inverter were carried out in [1] for comparisons with those of the conventional three-level inverter (i.e., T-type NPC inverter) [14]. The carrier frequency of the main converter in the three-cell inverter was set to 50 Hz, and that of each chopper cell was set to 2 kHz so that the equivalent carrier frequency became 6 kHz to match the normal carrier frequency

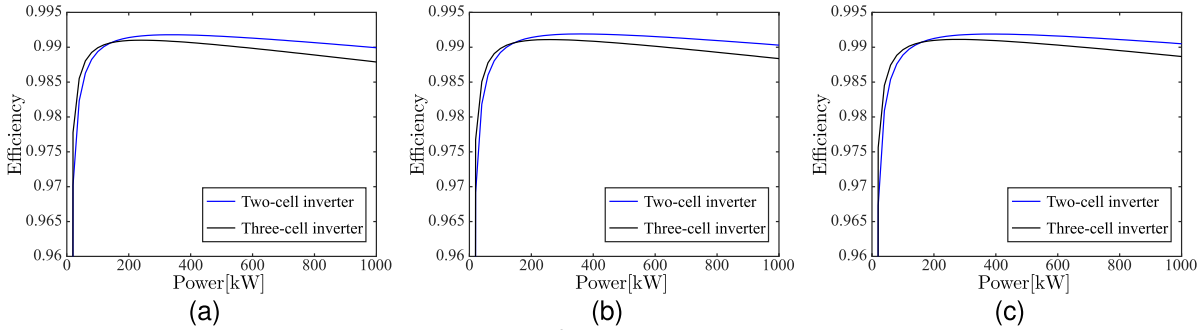


FIGURE 7. Efficiency comparisons of proposed inverter when $\sqrt{3}V_{ac} = 1150\,\mathrm{V}$ with MPPT range of $960 - 1300\,\mathrm{V}$: a) $E = 960\,\mathrm{V}$, b) $E = 1100\,\mathrm{V}$, 3) $E = 1300\,\mathrm{V}$.

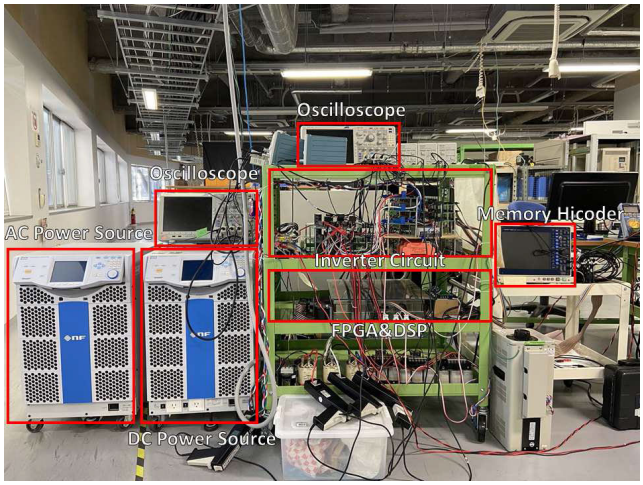


FIGURE 8. Photograph of 1.5-kW downscaled experiment system.

of the conventional three-level inverter [29], [30] for fair comparisons.

Following the works shown in [1], the loss breakdown of the two-cell inverter will be calculated, and the efficiency comparisons between the two-cell inverter and the three-cell inverter will be conducted in this section. In order to conduct fair comparisons, the loss in the transformer is not considered, which is similar to the previous work [1]. The switching and conduction loss of the auxiliary converter is taken into consideration. In contrast, only the conduction loss is considered for the main converter because ZCS is achieved in most cases, and the switching loss of the main converter with a carrier frequency of 50 Hz is negligible. It is noteworthy that the calculation in this section is based on active power control cases and the power factor is set to unity. To keep the consistency with the previous work [1], it is still assumed that the 3.3-kV IGBT modules 1MBI1000UG-330 from Fuji Electric are used in the main converters and the 1.2-kV IGBT modules CM1000DX-24T from Mitsubishi Electric are used in the auxiliary converters because the maximum dc-capacitor voltage is 730 V for the two-cell inverter and 480 V for the three-cell inverter. The parameters used for calculation are obtained from the official data sheets available on the manufacturer's homepage.

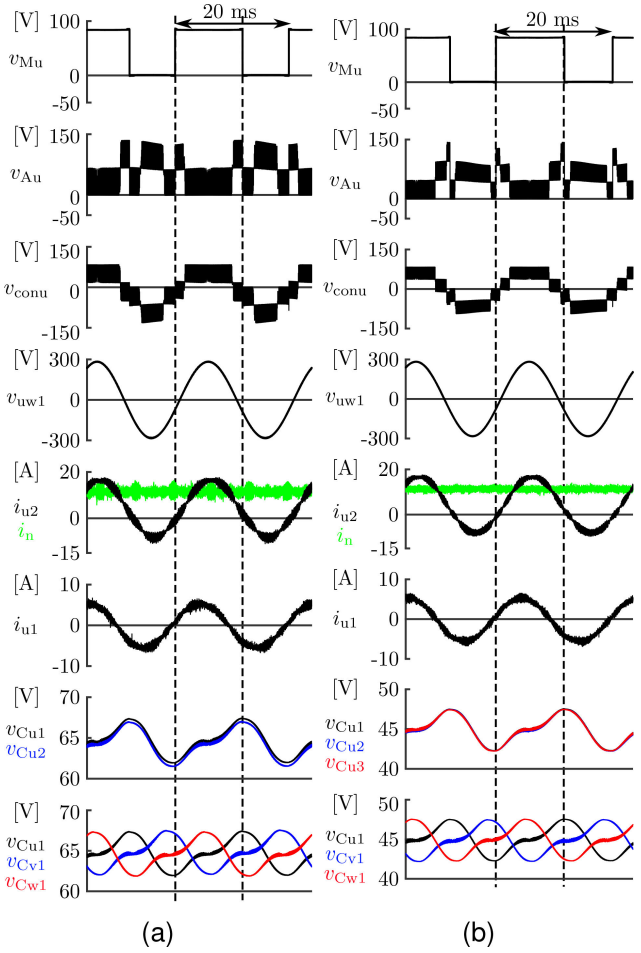


FIGURE 9. Experimental waveforms under steady state where $p^* = 1.5\,\mathrm{kW}$ and $E = 85\,\mathrm{V}$: a) two-cell inverter circuit, b) three-cell inverter circuit.

Table 1 shows the circuit parameters used for loss calculation. The carrier frequency of each cell in the auxiliary converter in the two-cell inverter was set to $f_{SA} = 3\,\mathrm{kHz}$ to achieve the same equivalent switching frequency of 6 kHz as that of the three-cell inverter calculated in [1]. The dc-capacitor voltages of the two inverters are different because of different cell numbers and they are determined according to (9). The loss calculation method is based on the methods shown in [31] and [32], and the results are shown in Fig. 6. From the comparison, it is obvious that the main

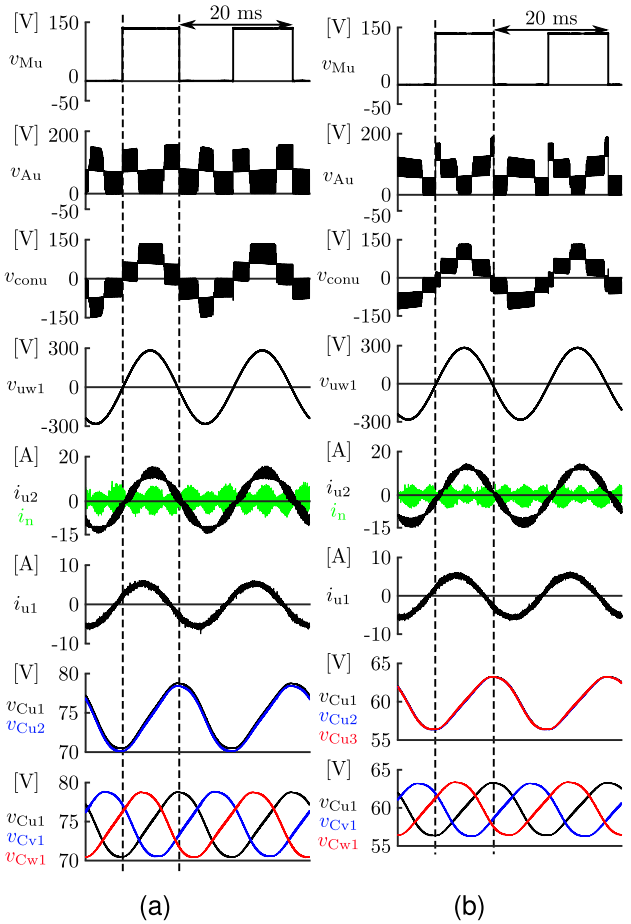


FIGURE 10. Experimental waveforms under steady state where $p^* = 1.5\,\text{kW}$ and $E = 135\,\text{V}$: a) two-cell inverter circuit, b) three-cell inverter circuit.

converter conduction loss of the two-cell inverter is the same as that of the three-cell inverter. However, the conduction loss of the auxiliary converter of the two-cell inverter is almost $\frac{2}{3}$ of that of the three-cell inverter at the output power of 1000 kW because the number of power devices used in the auxiliary converter of the two-cell inverter is $\frac{2}{3}$ that of the three-cell inverter. Even though the switching loss of the auxiliary converter of the two-cell inverter is larger than that of the three-cell inverter because of the increased dc-capacitor voltage, the total loss decreases as the output power increases compared with that of the three-cell inverter.

The following compares the efficiency of the two-cell and three-cell inverters with the same dc-input and ac-output voltages and the same MPPT range. The circuit parameters used for efficiency calculation are shown in Table 2 and the result of comparisons is shown in Fig. 7. According to Fig. 7, the two-cell inverter circuit has a higher efficiency in all of the three cases when the output power is higher than 200 kW, and the maximum efficiency is 99.2 %. In contrast, the efficiency of the three-cell inverter is higher when the output power is lower than 200 kW because the switching loss of the auxiliary converter is dominant in this region. Because the proposed inverter circuit is designed for applications in megawatt power level PV systems, the two-cell inverter circuit is better than the three-cell inverter circuit in terms of loss and efficiency.

TABLE 4. Three-cell inverter circuit parameters used for experiments.

Active power reference	p^*	1.5 kW
DC input voltage	E	85 V or 135 V
Nominal grid voltage	V_{grid}	200 V
Voltage ratio of Tr.	a	$200/100 = 2$
Secondary voltage of Tr.	V_{ac}	58 V
Inductor	L	0.21 mH
Leakage inductance of Tr.	l	0.27 mH
Chopper-cell count/phase	N	3
DC-capacitor voltage	V_{C}	45 V or 60 V
Cell capacitor	C	4.4 mF
Carrier freq. (main conv.)	f_{SM}	50 Hz
Carrier freq. (aux. conv.)	f_{SA}	7.2 kHz
Fault duration	t_{F}	100 ms

V. EXPERIMENT

A. EXPERIMENTAL CONDITIONS

The experimental verifications during the steady state, the SLG fault, and the 3P fault were carried out using the same 1.5-kW downscaled system used in [1], the photograph of which is shown in Fig. 8. The circuit parameters of the two-cell inverter and the three-cell inverter are summarized in Tables 3 and 4, respectively. The dc input voltage corresponding to the PV array voltage, E, was produced using the dc power source NF DP030RS. The grid voltage, which is the primary side voltage of the transformer was produced using the programmable ac power source NF DP045RT. The SLG fault (u-phase) and the 3P fault were performed on the primary side of the transformer shown in Fig. 1 using the sequence function of NF DP045RT. According to IEEE Std 1159-2019 [33], the fault duration, t_F, was set to 100 ms. The reference value of the active power was 1.5 kW, which means that the relationships $I_p^* = 8.66\,\text{A}$ and $I_q^* = 0\,\text{A}$ hold in (19). The reference value of the dc-capacitor voltage in the two-cell inverter was set to 65 V when the dc input voltage was 85 V and was set to 75 V when the dc input voltage was 135 V considering (9) except for Fig. 14, the reason of which will be explained later. Similarly, the reference value of the dc-capacitor voltage in the three-cell inverter was set to 45 V when the dc input voltage was 85 V and it was set to 60 V when the dc input voltage was 135 V, respectively. The deadtime was set to 4.0 µs for the main and the auxiliary converters. The voltage ratio of the transformer was set to $a = 2$ so that the secondary line-to-neutral (phase) RMS voltage was $V_{ac} = V_{grid}/(\sqrt{3}a) = 58\,\text{V}$.

The control system is composed of a digital signal processor unit utilizing Texas Instruments TMS320C6678 and a field programmable gate array unit utilizing Altera Cyclone IV. The voltage and current waveforms were

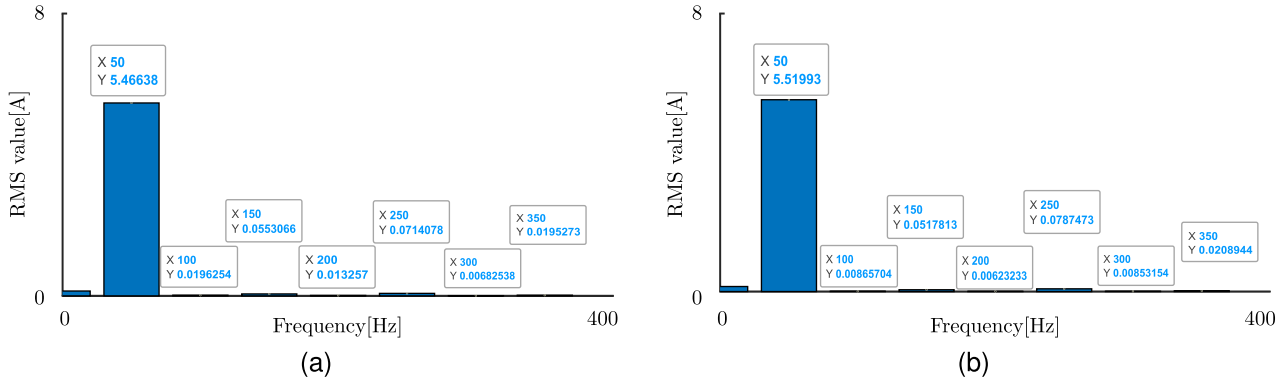


FIGURE 11. Spectrum of i_{u1}: a) two-cell inverter circuit, b) three-cell inverter circuit.

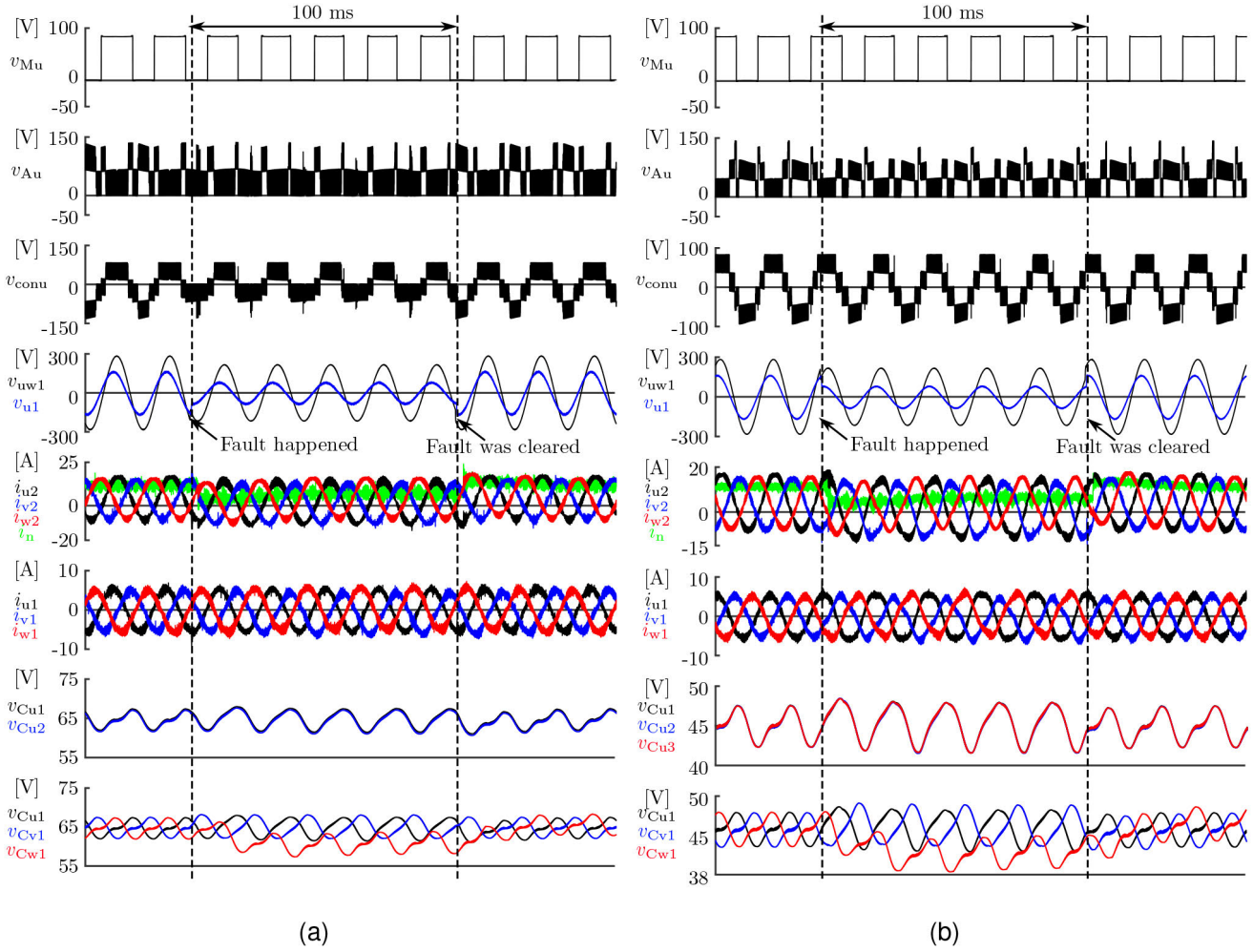


FIGURE 12. Experimental waveforms during SLG fault where $E = 85$ V and v_{u1} dropped by 50 %: a) two-cell inverter circuit, b) three-cell inverter circuit.

measured using Textronix DPO4104B-L with a frequency band of 1 GHz, Textronix MDO4104C with a frequency band of 1 GHz, and Hioki Memory Hicoder 8861-50.

Since the descriptions and the analyses regarding the voltage and current waveforms under the steady state of the three-cell inverter are provided in [1], the following mainly focuses on the behavior comparisons of the two-cell inverter and the three-cell inverter under the steady state and the fault condition. As mentioned in Section I, the detailed fault analysis will not be included in this section.

B. STEADY-STATE PERFORMANCE COMPARISONS

Fig. 9 shows the experimental waveforms comparison of the two-cell inverter and the three-cell inverter under a steady-state when $p^* = 1.5$ kW and $E = 85$ V. It corresponds to the low dc input voltage region where the ZCS

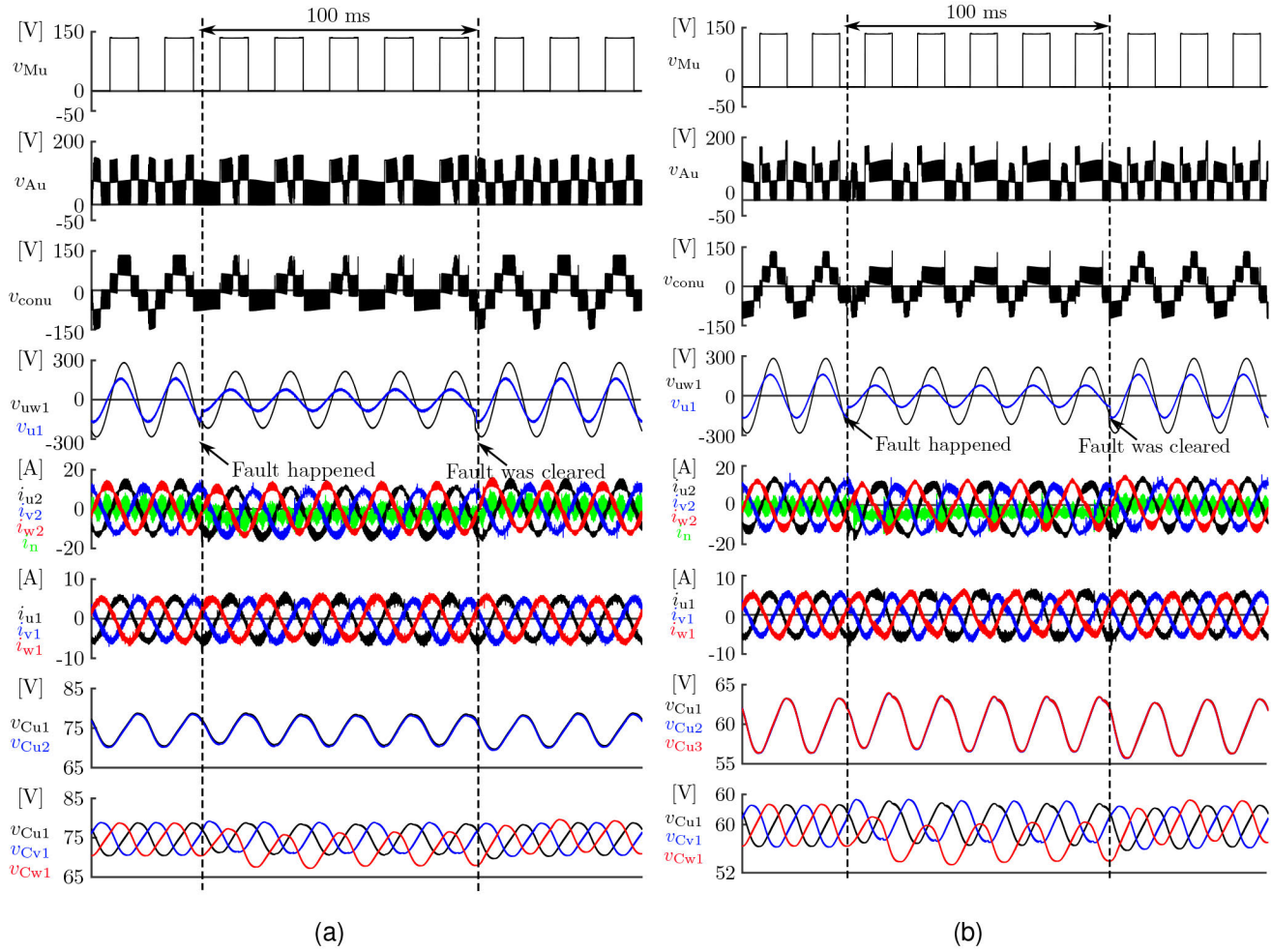


FIGURE 13. Experimental waveforms during SLG fault where $E = 135$ V and v_{u1} dropped by 50 %: a) two-cell inverter circuit, b) three-cell inverter circuit.

can be achieved as explained in [1]. Basically, the two-cell inverter and the three-cell inverter have similar experimental waveforms except for several differences. The auxiliary converter output voltage, v_{Au}, of the two-cell inverter has a three-level output waveform, whereas that of the three-cell inverter has a four-level output waveform. There are a few more harmonic components in i_{u1}, i_{u2}, and i_n of the two-cell inverter than those of the three-cell inverter. The reason for this phenomenon is that the active filter function of the auxiliary converter is weakened by reducing the cell number. In addition, the increased dc-capacitor voltage also increases the harmonic components in the two-cell inverter circuit. The dc-capacitor voltages are regulated to the reference value of 65 V and 45 V without any steady-state error in both inverter circuits, respectively. However, only two cells capacitor voltages need to be balanced per phase in the two-cell inverter, whereas there are three of them that need to be balanced per phase in the three-cell inverter. Fig. 10 shows the waveforms comparison of another experiment under a steady-state when $p^* = 1.5$ kW and $E = 135$ V. It corresponds to the high dc input voltage region where ZCS cannot be achieved in this region [1]. The waveforms comparison shows similar results as that of Fig. 9. In this case, the dc component included in the neutral current i_n is negative due to the increased E [1].

Further, the comparison of the THD values of the two-cell inverter and the three-cell inverter is carried out. The data of the u-phase grid current, i_{u1}, are used for calculation. The THD values are calculated using MATLAB, and up to the 40$^{\text{th}}$-order harmonic. The THD values of the 85 V steady-state cases of the two-cell inverter and the three-cell inverter are 2.735 % and 2.608 %, respectively. Meanwhile, the THD values of the 135 V steady-state cases of the two-cell inverter and the three-cell inverter are 1.956 % and 1.928 %, respectively. All of the THD values obtained above satisfy the requirement of IEEE std 519-2014 [34]. In addition, the comparison of the spectrum of i_{u1} of the two-cell inverter and the three-cell inverter in the 135 V steady-state case is shown in Fig. 11, where X stands for the frequency and Y stands for the RMS value. In Fig. 11, both spectrums are shown up to the 7$^{\text{th}}$-order harmonic because the RMS values of higher order harmonics are too small. It should be noted that the dc components shown in the spectrums were caused by the measurement equipment error. The THD performance of the two-cell inverter in Fig. 11a shows that the two-cell

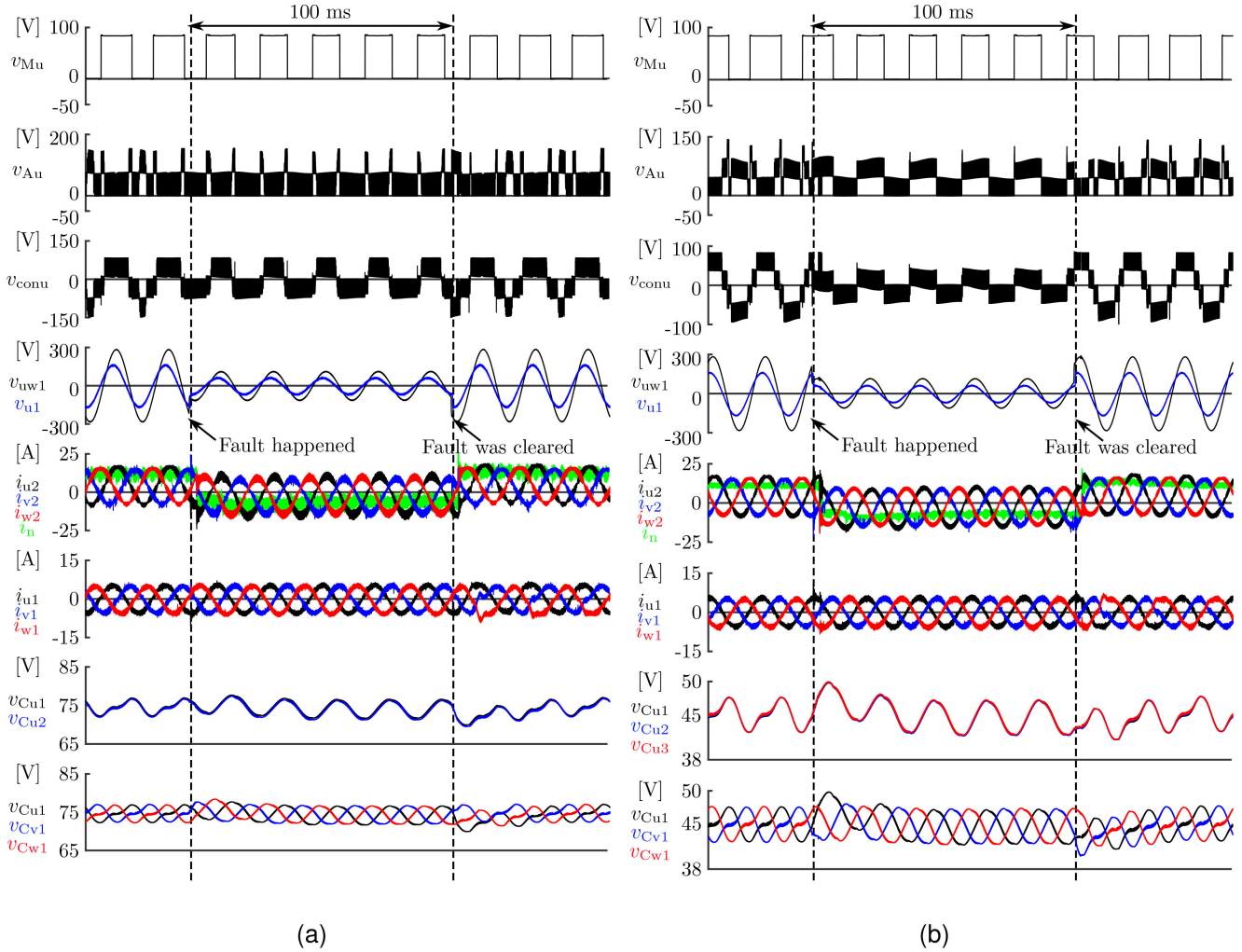


FIGURE 14. Experimental waveforms during 3P fault where $E = 85$ V and primary side line-to-neutral voltage dropped by 60 %: a) two-cell inverter circuit, b) three-cell inverter circuit.

inverter exhibits similar performance to that of the three-cell inverter.

C. LVRT CAPABILITY PERFORMANCE COMPARISONS DURING SLG FAULT

Fig. 12 shows the experimental waveforms comparison of the two-cell inverter and the three-cell inverter during an SLG fault (u-phase) where $E = 85$ V. During the SLG fault, the amplitude of v_{u1} dropped by 50 %, and a voltage dip and a phase jump occurred in v_{uw1} because of the Y-Δ connection of the transformer. Both inverters behaved similarly during the SLG fault. The value of the neutral line current i_n of both inverters decreased during the fault because several coefficients in (17) changed during the SLG fault. In addition, the currents of the two-cell inverter contained less low-order harmonic currents during the SLG fault than those of the three-cell inverter. The reason is that reduction of the cell number makes the capacitor voltage balancing control easier during the SLG fault, which increases the robustness and the LVRT capability of the proposed inverter. The dc-capacitor voltage unbalances occurred during the SLG fault and the dc-capacitor voltages of u-phase and v-phase increased slightly and that of w-phase decreased in both inverter circuits. However, the voltage variance of the two-cell inverter circuit is larger than that of the three-cell inverter circuit because the power unbalance caused by the SLG fault was imposed on only two cells. After the fault was cleared, the dc-capacitor voltages of both inverters were regulated to the reference values, respectively. Fig. 13 shows the waveforms comparison of another experiment during the SLG fault when $p^* = 1.5$ kW and $E = 135$ V. Similarly, the amplitude of v_{u1} dropped by 50 %, and a voltage dip and a phase jump occurred in v_{uw1}. Both inverters have similar performances as shown in Fig. 12.

D. LVRT CAPABILITY PERFORMANCE COMPARISONS DURING 3P FAULT

Fig. 14 shows the experimental waveforms comparison of the two-cell inverter and the three-cell inverter during a 3P fault where $E = 85$ V. The line-to-neutral voltage of the primary side of the transformer (grid) dropped by 60 % during the 3P fault. The operation principles during the 3P fault are similar

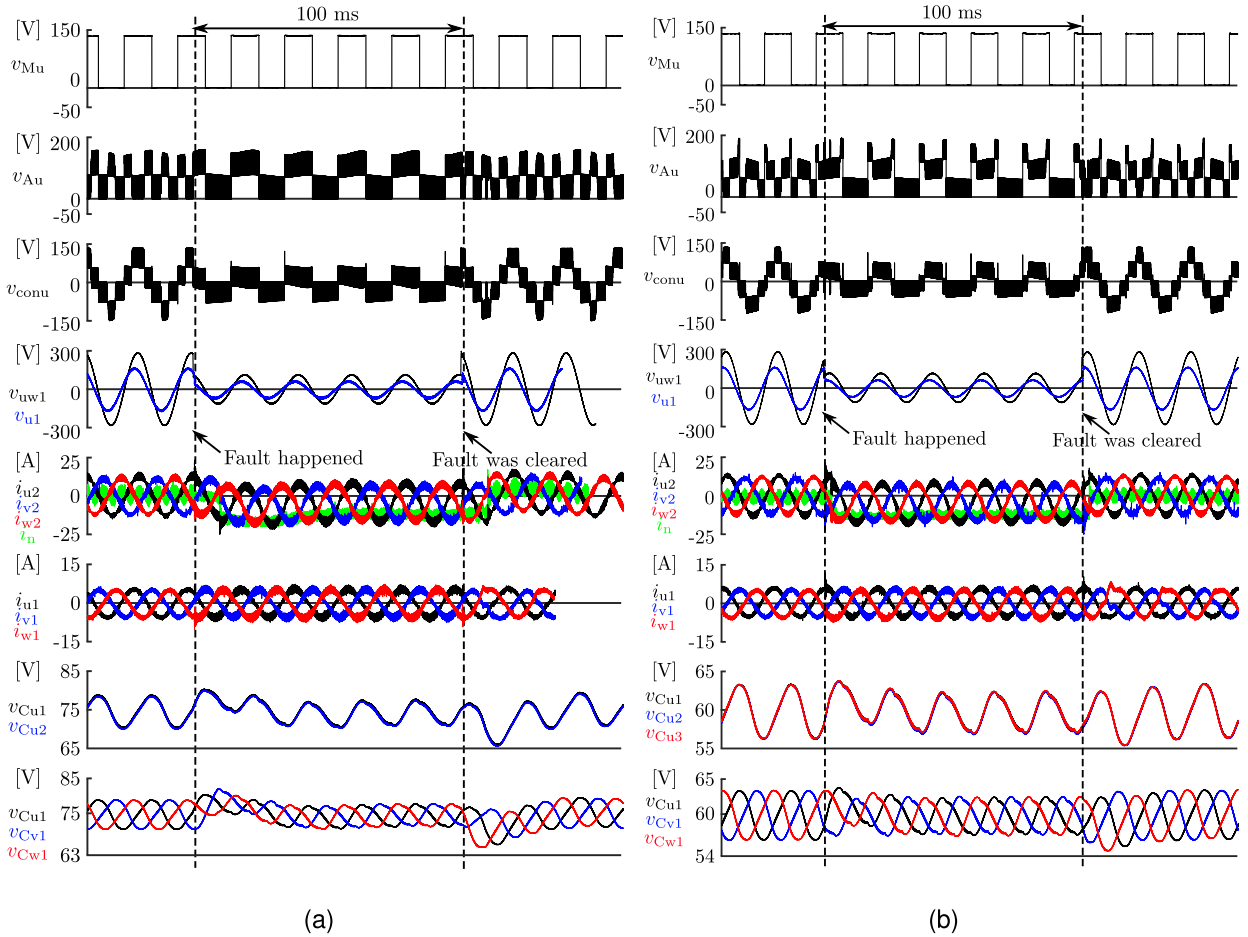


FIGURE 15. Experimental waveforms during 3P fault where $E = 135$ V and primary side line-to-neutral voltage dropped by 60 %: a) two-cell inverter circuit, b) three-cell inverter circuit.

to the ones of the 135-V normal condition [1], where $\alpha = 0$ and $\frac{V_{ac}}{E} < \frac{\sqrt{2}}{\pi}$. Therefore, i_n is negative during the 3P fault according to (17). The dc-capacitor voltage fluctuation of each phase when the fault occurred and was cleared is similar because of the symmetrical fault. Specifically, the capacitor voltages of all phases increased when the fault occurred and they decreased when the fault was cleared. However, the dc-capacitor voltage drop of the two-cell inverter when the fault was cleared broke the operational requirement (9) when the dc-capacitor voltage was set to 65 V. Therefore, it was set to 75 V in the experiment. The currents and the capacitor voltages were kept balanced during the 3P fault in both inverter circuits. Fig. 15 shows the waveforms comparison of another experiment during the 3P fault when $p^* = 1.5$ kW and $E = 135$ V. Similarly, the line-to-neutral voltage of the primary side of the transformer (grid) dropped by 60 % during the 3P fault and both inverters have similar performance as shown in Fig. 14. The larger voltage drop in v_{cw1} in Fig. 15a compared to that in Fig. 14a was caused by the different moments when the faults were cleared.

VI. CONCLUSION

This article has evaluated and compared the performance of the proposed two-cell and three-cell inverters in terms of loss, efficiency, THD performance, and experimental performance during steady and fault states to evaluate the chopper-cell number in the auxiliary converter. The comparisons have revealed that the two-cell inverter has lower total loss and higher efficiency in megawatt power-level applications. In addition, the power devices with the same voltage/current ratings can be applied to the two inverters. It has been shown that the THD performances of the two inverters are similar under the same equivalent switching frequency. The experimental verifications under the SLG and 3P faults have exhibited that the two-cell inverter shows superior performance than the three-cell inverter in terms of current and dc-capacitor voltage fluctuation.

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