IEEE Access
Multidisciplinary ⋮ Rapid Review ⋮ Open Access Journal

Received 24 February 2023, accepted 15 March 2023, date of publication 30 March 2023, date of current version 10 April 2023.

Digital Object Identifier 10.1109/ACCESS.2023.3261243

APPLIED RESEARCH

Third-Harmonic-Type Modulation Minimizing the DC-Link Energy Storage Requirement of Isolated Phase-Modular Three-Phase PFC Rectifier Systems

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This work has been partially supported by Silicon Austria Labs (SAL), owned by the Republic of Austria, the Styrian Business Promotion Agency (SFG), the Federal State of Carinthia, the Upper Austrian Research (UAR), and the Austrian Association for the Electric and Electronics Industry (FEEI).

ABSTRACT A three-phase ac-dc converter with high-frequency isolation can be realized as a phase-modular system by using three single-phase Power Factor Correction (PFC) rectifier modules with isolated dc-dc converter output stages, which advantageously allows to cover a wide input voltage range by module reconfiguration from a star-(Y)- to a delta-(Δ)-arrangement. However, the main limitation of a phase-modular topology is the fact that the input power of each PFC rectifier module pulsates at twice the mains frequency such that large dc-link capacitors are required. Recent literature predicts a substantial single-phase power pulsation reduction enabled by means of third-(3^{rd})-harmonic common-mode (CM) voltage (Y) or current (Δ) injection modulation. This paper experimentally verifies and extends the dc-link energy storage requirement reduction of the 3^{rd}-harmonic injection modulation concepts: In a first step, the derivation of the harmonic injection concept is recapitulated and suitable control methods are discussed for both CM voltage (Y) and CM current (Δ) injection. Further, an alternative CM voltage injection strategy with simplified reference generation based only on the instantaneous grid voltage measurements is presented and compared to the pure 3^{rd}-harmonic injection modulation. Measurement results obtained from a 6 kW prototype reveal a dc-link voltage variation and/or energy buffering reduction by up to 38.6 % enabled by the harmonic injection modulation compared to conventional operation without 3^{rd}-harmonic injection modulation.

INDEX TERMS AC-DC converter, three-phase, modular, harmonic injection, zero sequence, CM voltage injection, CM current injection.

I. INTRODUCTION

Three-phase ac-dc converter systems with High-Frequency (HF) isolation are commonly realized by combining a monolithic three-phase Power Factor Correction (PFC) rectifier with an isolated dc-dc converter stage [1], [2] as highlighted in **Fig. 1(a)**. There, the PFC rectifier (e.g., a two-level boost-type rectifier) generates sinusoidal grid currents i_a, i_b, i_c (with amplitude $\hat{I}_{ac}$) in phase with the respective grid voltages u_a, u_b, u_c (with line-to-neutral amplitude $\hat{U}_{ac}$). Advantageously, the instantaneous three-phase Low-Frequency (LF) input power sums up to a constant value which is processed by the isolated dc-dc converter stage (e.g., a Series-Resonant Converter (SRC) or a Dual-Active

The associate editor coordinating the review of this manuscript and approving it for publication was Sheldon S. Williamson.

Bridge (DAB) [3], [4]) such that the dc-link capacitor C_{dc} is only sized based on a HF and not an LF dc-link voltage criterion with typical capacitance values in the range of 10 μF/kW [5], [6], [7].

The monolithic three-phase rectifier front-end however, has two main limitations: First, for a given dc-link voltage U_{dc} a boost-type rectifier with standard modulation is limited to operation with grid voltage amplitudes $\hat{U}_{\mathrm{ac}} \leq (1-\epsilon)\frac{U_{\mathrm{dc}}}{2}$ where ϵ represents a typical dc-link voltage margin to maintain grid current controllability [2]. The tolerable grid voltage range is highlighted in **Fig. 2** for two dc-link voltage levels and is (for $\epsilon = 25\,\%$) limited to $U_{\mathrm{ac,max,M}} \approx 115\,\mathrm{V_{RMS}}$ for $U_{\mathrm{dc}} = 400\,\mathrm{V}$ in **Fig. 2(a)** and $U_{\mathrm{ac,max,M}} \approx 200\,\mathrm{V_{RMS}}$ for $U_{\mathrm{dc}} = 700\,\mathrm{V}$ in **Fig. 2(b)**. Second, in case a wide grid input voltage range is required, e.g., to allow for compatibility with different nominal mains voltages or to tolerate fluctuating mains voltages in weak grids, the rectifier front-end is subject to high current stresses and/or can only provide a limited output power. Typically, the tolerable RMS value $I_{\bar{\mathrm{j}}}$ of the rectifier input currents $i_{\bar{\mathrm{a}}}$, $i_{\bar{\mathrm{b}}}$, $i_{\bar{\mathrm{c}}}$ (here $I_{\bar{\mathrm{j}}} = I_{\mathrm{ac}}$) is limited by the dimensioning of the magnetic components or the power semiconductors and hence, the maximum transmittable power P_{max} presented in **Fig. 2** is proportional to the RMS grid voltage U_{ac} and is limited for the considered example to values below $P_{\mathrm{max}} \approx 3\,\mathrm{kW}$.

Converter reconfiguration is a well known concept to allow a wide ac input (and/or dc output) voltage range [8], [9], [10], but cannot be applied to the monolithic three-phase PFC rectifier front-end in **Fig. 1(a)**. However, the functionality of the converter in **Fig. 1(a)** can be achieved alternatively by combining three single-phase ac-dc PFC rectifier front-ends with individual isolated dc-dc converter stages [11], [12], [13], [14], [15] as highlighted in **Fig. 1(b)**. Here, the power modules can be advantageously configured in a star (Y)-arrangement (**Fig. 1(b.i)**) or a delta (Δ)-arrangement (**Fig. 1(b.ii)**), which allows to change the PFC rectifier front-end input voltage and current range [16]:

In Y-configuration (**Fig. 1(b.i)**) a boost-type rectifier with standard modulation is limited to $\hat{U}_{\mathrm{ac}} \leq (1-\epsilon)U_{\mathrm{dc}}$, i.e., an improvement by about a factor of two compared to the monolithic three-phase rectifier which is enabled by the bipolar-voltage capability and the full utilization of the dc voltage of the full-bridges in the single-phase PFC rectifier modules for generation of an ac voltage [17]. For $\varepsilon = 25\,\%$ the grid ac voltage amplitude is limited to $U_{\mathrm{ac,max,Y}} \approx 230\,\mathrm{V_{RMS}}$ for $U_{\mathrm{dc}} = 400\,\mathrm{V}$ in **Fig. 2(a)** and $U_{\mathrm{ac,max,Y}} \approx 400\,\mathrm{V_{RMS}}$ for $U_{\mathrm{dc}} = 700\,\mathrm{V}$ in **Fig. 2(b)**, corresponding to $P_{\mathrm{max}} \approx 6\,\mathrm{kW}$.

Note that in Y-configuration the rectifier input current stresses are (as for the monolithic rectifier in **Fig. 1(a)**) directly defined by the grid current and $I_{\bar{\mathrm{j}}} = I_{\mathrm{ac}}$. If the configuration is now changed to a Δ-arrangement of the modules as highlighted in **Fig. 1(b.ii)**, each module is subject to the grid line-to-line voltage with an amplitude of $\sqrt{3}\hat{U}_{\mathrm{ac}}$ and hence the module current stresses are reduced to $I_{\bar{\mathrm{j}}} = I_{\mathrm{ac}}/\sqrt{3}$ such that $P_{\mathrm{max}} \approx 6\,\mathrm{kW}$ can be achieved for lower grid voltage levels in **Fig. 2**. Here, the maximally tolerable grid voltage amplitude is limited to $\sqrt{3}\hat{U}_{\mathrm{ac}} \leq (1-\epsilon)U_{\mathrm{dc}}$, such that $U_{\mathrm{ac,max,}\Delta} \approx 130\,\mathrm{V_{RMS}}$ for $U_{\mathrm{dc}} = 400\,\mathrm{V}$ in **Fig. 2(a)** and $U_{\mathrm{ac,max,}\Delta} \approx 230\,\mathrm{V_{RMS}}$ for $U_{\mathrm{dc}} = 700\,\mathrm{V}$ in **Fig. 2(b)**, corresponding to $P_{\mathrm{max}} \approx 6\,\mathrm{kW}$.

Hence, the module configuration can be changed depending on the grid voltage level of the considered application which allows to cut the voltage or current stresses by a factor of $\sqrt{3}$ (see **Tab. 1**). Further, such a phase-modular realization features a high failure tolerance [13] and the system can continue operation with reduced output power in case one or even two converter modules fail. The main weakness of a phase-modular converter realization is, however, the fact that the input power of each PFC rectifier module pulsates at twice the mains frequency (which is inherent to single-phase power conversion) such that large dc-link capacitors C_{dc} are required, which may cover a large fraction of the overall converter volume and/or limit the system lifetime [18], [19].

Hence, several measures to reduce the dc-link power pulsation and/or the minimally required dc-link capacitance value of phase-modular three-phase PFC rectifier systems are investigated in literature: Active power pulsation buffers [10], [20], [21] allow a higher capacitor utilization, but require additional power components and result in elevated overall conversion losses compared to passive buffering with electrolytic capacitors [20]. Alternatively, as in sum the instantaneous grid input power is constant, the pulsating input power can be redistributed by the subsequent isolated dc-dc converter stages (see **Fig. 3(a)**) as investigated in [14], [15], and [22]. This approach, however, comes at the cost of elevated component stresses and conversion losses of the dc-dc converters and ideally the power pulsation is already reduced in the ac-dc front-ends. In [23] the power pulsation of a low power single-phase ac-dc converter is reduced by regulating a non-sinusoidal grid current, which comes at the cost of a high grid current distortion and therefore cannot be scaled to higher power levels. In contrast to a standalone single-phase ac-dc converter, the phase-modular realization of a three-phase ac-dc converter features an additional degree of freedom for the modulation given by the Common-Mode (CM) voltage u_{CM} (in Y-configuration, see **Fig. 3(a)**) or the CM current i_{CM} (in Δ-configuration, see **Fig. 3(e)**), that do not impact the grid currents (in contrast to [23] the grid currents remain fully sinusoidal) but allow to influence the distribution of the (instantaneously constant) overall three-phase input power flow to the three front-end single-phase PFC rectifier modules [1] and/or to shift the module input power pulsations to higher frequencies.

The concept of a power pulsation reduction by means of harmonic injection was investigated in [1] based on simulations only, and the main goal of this paper is to provide a hardware verification of the proposed modulation concept and the reduction of the dc-link energy buffering requirement based

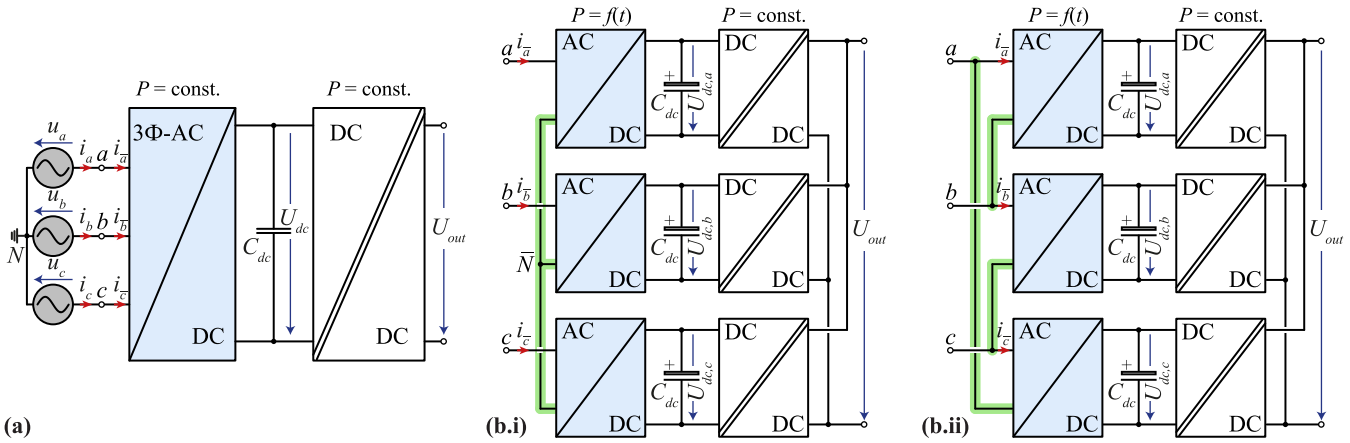

FIGURE 1. Converter concepts for the realization of a three-phase ac-dc converter systems with HF isolation: (a) Monolithic three-phase PFC rectifier front-end combined with an isolated dc-dc converter output stage, (b) phase-modular realization comprising three single-phase ac-dc PFC rectifier front-ends combined with individual isolated dc-dc converter stages. For the phase-modular approach the PFC rectifier front-ends can be configured in (b.i) a star (Y) or (b.ii) a delta (Δ) arrangement.

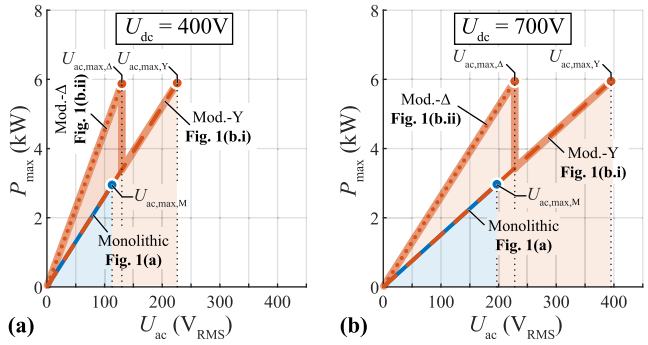

FIGURE 2. Maximum transmittable power P_{max} of a boost-type three-phase rectifier front-end as a function of the three-phase line-to-neutral grid voltage U_{ac} for (a) a dc-link voltage of U_{dc}400 V and a maximum rectifier input current of $I_{\bar{j}} = 8.7\ A_{RMS}$ (i.e., a nominal system power of 6 kW for an input voltage of $U_{ac} = 230\ V_{RMS}$), and (b) a dc-link voltage of $U_{dc} = 700$ V and a maximum rectifier input current of $I_{\bar{j}} = 5.0\ A_{RMS}$ (i.e., a nominal system power of 6 kW for an input voltage of $U_{ac} = 400\ V_{RMS}$). The considered rectifier front-end concepts are: the monolithic three-phase PFC rectifier from Fig. 1(a), and the phase-modular PFC rectifier in star (Y) or delta (Δ) arrangement from Fig. 1(b). The respective maximum tolerable input voltage (and power) operating point considering a grid current controllability voltage margin of $\epsilon = 25\%$ of each concept is highlighted by a round scatter point.

on a 6 kW hardware demonstrator (the main specifications are listed in **Tab. 1**) allowing both Y- and Δ-configuration of the modules.

The publication comprises two main Sections. First, **Section II** covers the Y-connected operation of the converter modules: The theoretical background of harmonic voltage injection and its impact on the module power flow is recapitulated. Further, harmonic injection by means of Space Vector Modulation (SVM) is considered. Then, a suitable control structure for PFC rectifier operation with harmonic voltage injection is presented. Last, details on the hardware prototype and experimental waveforms confirming the predicted energy buffering reduction are presented. Then, **Section III** covers all relevant aspects of the Δ-connected operation of the converter modules again including the experimental verification.

Last, **Section IV** summarizes the main findings of the paper and presents an outlook to further research on harmonic injection techniques for phase-modular three-phase isolated PFC rectifier systems.

TABLE 1. System specifications[1].

Design.	Description	Value
U_{ac}	Grid voltage (line-to-neutral)	$3\times230\ V_{RMS}$
I_{ac}	Grid current	$3\times8.7\ A_{RMS}$
f_{ac}	Grid frequency	50 Hz
P	Input power	3×2 kW
$I_{\bar{j}}$	LF input current (Y-config.)	$3\times8.7\ A_{RMS}$
$U_{dc,j}$	dc-link voltage (Y-config.)	400 V
$I_{\bar{j}}$	LF input current (Δ-config.)	$3\times5.0\ A_{RMS}$
$U_{dc,j}$	dc-link voltage (Δ-config.)	700 V

[1] $j \in \{a, b, c\}$

II. STAR-(Y)-CONNECTED PHASE-MODULAR CONVERTER

A. THEORY

The three single-phase isolated PFC rectifier modules in Y-configuration are shown in **Fig. 3(a)**, where the rectifier modules are realized with a totem pole structure [17], [24], [25], i.e., a fast-switching HF half-bridge is combined with an LF unfolder bridge-leg such that high conversion efficiency results. The grid voltages and currents of phase $j \in \{a, b, c\}$ are defined by

$$u_j = \hat{U}_{ac} \sin(\omega_{ac} t + \phi_j)$$
$$i_j = \hat{I}_{ac} \sin(\omega_{ac} t + \phi_j), \quad (1)$$

with the grid (line-to-neutral) voltage $\hat{U}_{ac}$ and current $\hat{I}_{ac}$ amplitude and the grid angular frequency $\omega_{ac} = 2\pi f_{ac}$ and phase angles $\phi_a = 0$, $\phi_b = -\frac{2\pi}{3}$ and $\phi_c = -\frac{4\pi}{3}$ (see **Tab. 1**).

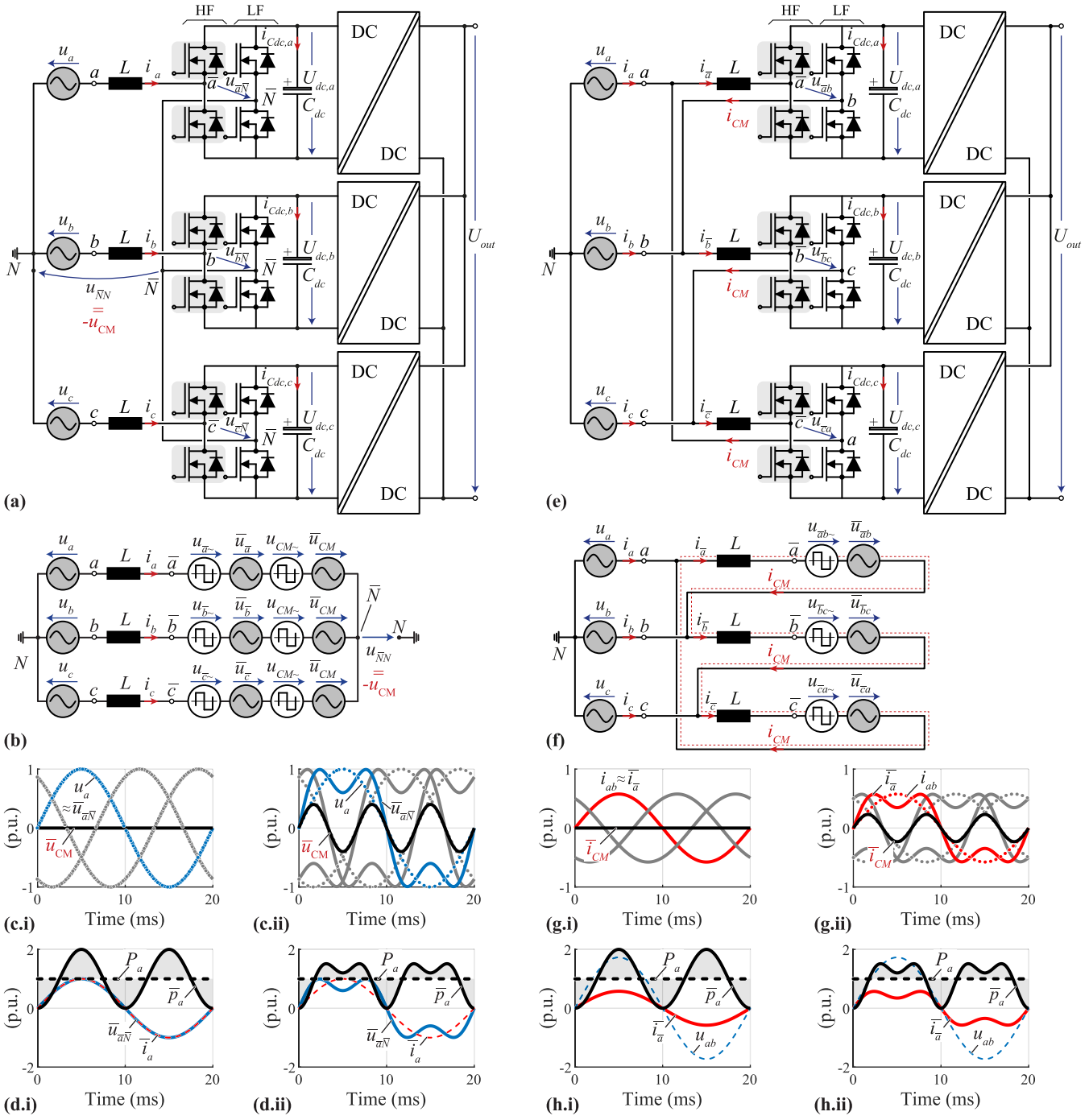

FIGURE 3. **(a) Phase-modular realization of the ac-dc converter employing a Y-connection of single-phase PFC rectifier modules with individual isolated dc-dc converter stages and dc-link voltages around 400 V for a typical peak grid line-to-neutral voltage of 325 V. (b) ac-side equivalent circuit of the converter shown in (a) with separate and high-frequency DM and CM module input voltage sources of the PFC rectifier switching stages. (c) Waveforms of the grid phase voltages and of the LF components of the input voltages of the rectifier switching stages and of the injected CM voltage for (c.i) $M_3 = 0$ and (c.ii) $M_3 = 0.4$. (d) Phase a switching stage LF input voltage $\bar{u}_{\bar{a}\bar{N}}$, current $\bar{i}_a$ and power $\bar{p}_a$ within one mains period for a 3rd harmonic voltage modulation index of (d.i) $M_3 = 0$ and (d.ii) $M_3 = 0.4$. Note, that the average input power P_a is represented by a dashed line and is not impacted by M_3. (e) Phase-modular realization of the ac-dc converter employing a Δ-connection of single-phase PFC rectifier modules with individual isolated dc-dc stages and dc-link voltages around 700 V. (f) ac-side equivalent circuit of the converter shown in (e) with separate LF and high-frequency equivalent input voltage sources of the PFC rectifier stages. (g) Waveforms of the grid phase currents and of the LF components of the input currents of the rectifier switching modules and of the CM current i_{CM} circulating inside the Δ-connection for (g.i) $M_3 = 0$ and (g.ii) $M_3 = 0.4$. (h) Phase a switching stage LF input voltage $\bar{u}_{\bar{a}\bar{N}}$, current $\bar{i}_a$ and power $\bar{p}_a$ within one mains period for a 3rd harmonic current modulation index of (h.i) $M_3 = 0$ and (h.ii) $M_3 = 0.4$. (Figure adapted from [1].)**

In **Fig. 3(a)** the module starpoint $\bar{N}$ is not connected to the grid starpoint N and therefore, the grid input currents i_a, i_b, i_c sum up to zero and are not impacted by a CM voltage $u_{\bar{N}N}$ in between $\bar{N}$ and N (note that CM voltage injection cannot be performed in a four-wire system where $\bar{N}$ and N are connected via a neutral conductor). CM voltage injection [26] was originally introduced to extend the linear operating range of motor drive inverters. However, the CM voltage offset can also employed to reduce the current stresses in Y-configured split-battery applications [27] or phase-modular isolated rectifier systems [1].

The ac-side equivalent circuit from [1] for the Y-configuration of the converter modules is shown in **Fig. 3(b)**. There the rectifier front-end switch-node voltages are decomposed into Differential-Mode (DM) / CM and LF / HF components, e.g., for phase module a the switch-node voltage $u_{\bar{a}\bar{N}}$ is represented by

- the HF DM voltage $u_{\bar{a}\sim}$,
- the LF DM voltage $\bar{u}_{\bar{a}} \approx u_a$,
- the HF CM voltage $u_{CM\sim}$, and,
- the LF CM voltage $\bar{u}_{CM}$,

with $u_{\bar{N}N} = -(\bar{u}_{CM} + u_{CM\sim})$ and $\bar{u}_{CM}$ is set by the harmonic injection modulation.

The considered single-phase converter module structure in **Fig. 3(a)** is a boost-type system [2], i.e., the condition for grid current controllability is given by

$$\bar{u}_{\bar{j}\bar{N}}(t) \leq U_{dc,j}(t), \tag{2}$$

thereby imposing a limit to the maximum module LF dc-link voltage fluctuation and/or a minimum dc-link capacitance value C_{dc} [28]. Further, C_{dc} needs to be sized such that the maximum dc-link voltage $U_{dc,max}$ is not exceeded, i.e.,

$$U_{dc,j}(t) \leq U_{dc,max}, \tag{3}$$

with $U_{dc,max}$ typically defined by the maximally tolerable semiconductor blocking voltage. For 600 V power semiconductors, typically $U_{dc,max} = 420\,\text{V}$ is employed corresponding to a 30 % blocking voltage margin to account for transient switch-node overvoltages.

The dc-link voltage $U_{dc,j}$ variation is a function of the LF module input power $\bar{p}_j$ which is defined by $\bar{u}_{\bar{j}\bar{N}}$ and the corresponding LF module input current $\bar{i}_{\bar{j}}$ as

$$\bar{p}_j(t) = \bar{u}_{\bar{j}\bar{N}}(t) \cdot \bar{i}_{\bar{j}}(t) = (\bar{u}_{\bar{a}}(t) + \bar{u}_{CM}(t)) \cdot \bar{i}_{\bar{j}}(t). \tag{4}$$

Hence, the module input power flow can be adjusted by means of setting a suitable LF CM voltage component $\bar{u}_{CM}$. Note that with $i_a + i_b + i_c = 0$ the CM voltage $\bar{u}_{CM}$ does not impact the overall power flow from the grid but redistributes power among the front-end single-phase rectifier modules.

In the following the main power flow quantities are derived, first, for conventional sinusoidal modulation (i.e., with $\bar{u}_{CM} = 0$) and, subsequently, for two CM voltage injection strategies, i.e., 3rd-harmonic and triangular CM voltage injection, and the improvement in energy buffering and dc-link voltage fluctuation are assessed. For simplicity, in the following all derivations are performed for the converter module a.

1) CONVENTIONAL MODULATION

The main ac-side terminal voltage waveforms for conventional modulation (i.e., with $\bar{u}_{CM} = 0$) are presented in **Fig. 3(c.i),(d.i)** where the LF module input power $\bar{p}_a$ according to (4) results to

$$\bar{p}_a(t) = \frac{1}{2}\hat{U}_{ac}\hat{I}_{ac}\,(1 - \cos(2\omega_{ac}t))\,, \tag{5}$$

and comprises the well known twice-mains-frequency single-phase grid power pulsation on top of the (assuming ideally lossless power conversion) constant module output power $P_a = \frac{1}{2}\hat{U}_{ac}\hat{I}_{ac}$. The difference of the fluctuating LF module input power $\bar{p}_a(t)$ and the output power P_a is covered by the dc-link capacitor C_{dc} with an energy balance

$$\begin{aligned} E_{dc,a}(t) &= \frac{1}{2}C_{dc}\,U_{dc,a}^2(t) \\ &= \int_0^t (\bar{p}_a(\tau) - P_a(\tau))d\tau \\ &= -\frac{\hat{U}_{ac}\hat{I}_{ac}}{4\omega_{ac}}\sin(2\omega_{ac}t) + E_{dc,a}(0), \end{aligned} \tag{6}$$

with $E_{dc,a}(0) = \frac{1}{2}C_{dc}U_{dc}^2$, and hence depends on the average dc-link voltage $U_{dc} = 400\,\text{V}$. The dc-link LF energy buffering requirement $\Delta E_{dc,a}$ (represented by the light-gray areas in **Fig. 3(d.i)**) is defined by the difference of the maximum and minimum value of $E_{dc,a}(t)$ within a mains period T_{ac} and results to

$$\begin{aligned} \Delta E_{dc,a} &= \max(E_{dc,a}(t)) - \min(E_{dc,a}(t)) \\ &= \frac{\hat{U}_{ac}\hat{I}_{ac}}{2\omega_{ac}}. \end{aligned} \tag{7}$$

With (6) the time-varying dc-link voltage $U_{dc,a}(t)$ is defined by the module input power $\bar{p}_a$ (cf., (5),(6))

$$\begin{aligned} U_{dc,a}(t) &= \sqrt{\frac{2}{C_{dc}}E_{dc,a}(t)} \\ &= \sqrt{\frac{2}{C_{dc}}\left(\frac{-\hat{U}_{ac}\hat{I}_{ac}}{4\omega_{ac}}\sin(2\omega_{ac}t) + E_{dc,a}(0)\right)}, \end{aligned} \tag{8}$$

and hence the peak-to-peak dc-link LF voltage fluctuation $\Delta U_{dc,a}$ results to

$$\begin{aligned} \Delta U_{dc,a} &= \sqrt{\frac{2}{C_{dc}}}\left(\sqrt{\max(E_{dc,a}(t)} - \sqrt{\min(E_{dc,a}(t)}\right) \\ &= \frac{\Delta E_{dc,a}}{C_{dc}U_{dc}} = \frac{\hat{U}_{ac}\hat{I}_{ac}}{2\omega_{ac}C_{dc}U_{dc}}, \end{aligned} \tag{9}$$

i.e., is proportional to the dc-link LF energy buffering requirement. The calculated values of $\Delta E_{dc,a}$ and $\Delta U_{dc,a}$ according to the considered converter specifications in **Tab. 1** and **Tab. 2** are provided in **Tab. 3**.

In the following, the voltage $\bar{u}_{\mathrm{CM}}$ is used to adjust the LF module input power $\bar{p}_{\mathrm{a}}$ such that the energy buffering requirement $\Delta E_{\mathrm{dc,a}}$ and the fluctuation of the dc-link voltage $\Delta U_{\mathrm{dc,a}}$ is reduced.

2) 3rd-HARMONIC CM VOLTAGE INJECTION

For 3rd-harmonic injection modulation, the LF CM voltage component is defined by

$$\bar{u}_{\mathrm{CM}}(t) = M_3 \hat{U}_{\mathrm{ac}} \sin(3\omega_{\mathrm{ac}} t + \varphi_3), \tag{10}$$

where $M_3 = \hat{U}_{\mathrm{CM}}/\hat{U}_{\mathrm{ac}}$ represents the 3rd-harmonic modulation index and φ_3 the corresponding phase angle. In **Fig. 3(c.ii,d.ii)** the characteristic waveforms of module a are illustrated for a 3rd-harmonic voltage injection with $M_3 = 0.4$. The LF module input power $\bar{p}_{\mathrm{a}}$ according to (4) results to (for $\varphi_3 = 0$),

$$\bar{p}_{\mathrm{a}}(t) = \frac{1}{2}\hat{U}_{\mathrm{ac}}\hat{I}_{\mathrm{ac}}\Big(1 - (1 - M_3)\cos(2\omega_{\mathrm{ac}} t) - M_3 \cos(4\omega_{\mathrm{ac}} t)\Big), \tag{11}$$

i.e., with increasing values of M_3 the twice-mains frequency power pulsation is shifted from $2f_{\mathrm{ac}}$ to $4f_{\mathrm{ac}}$. The 3rd-harmonic phase shift value φ_3 further allows to optimize the LF module input voltage $\bar{u}_{\bar{\mathrm{a}}\bar{\mathrm{N}}}$ with respect to the current controllability dc-link voltage margin (for more details please see [1]) and the module input power $\bar{p}_{\mathrm{a}}(t)$ results to

$$\bar{p}_{\mathrm{a}}(t) = \frac{1}{2}\hat{U}_{\mathrm{ac}}\hat{I}_{\mathrm{ac}}\Big(1 - \cos(2\omega_{\mathrm{ac}} t) + M_3 \cos(2\omega_{\mathrm{ac}} t + \varphi_3) - M_3 \cos(4\omega_{\mathrm{ac}} t + \varphi_3)\Big). \tag{12}$$

Combining (6) and (12) the energy stored in C_{dc} under 3rd-harmonic modulation results to

$$E_{\mathrm{dc,a}}(t) = \frac{1}{8\omega_{\mathrm{ac}}}\hat{U}_{\mathrm{ac}}\hat{I}_{\mathrm{ac}}\Big(-2\sin(2\omega_{\mathrm{ac}} t) + 2\,M_3 \sin(2\omega_{\mathrm{ac}} t + \varphi_3) - M_3 \sin(4\omega_{\mathrm{ac}} t + \varphi_3)\Big) + E_{\mathrm{dc,a}}(0). \tag{13}$$

Here, the analytic expression for the energy buffering requirement $\Delta E_{\mathrm{dc,a}}$ is rather involved and therefore omitted. However, $\Delta E_{\mathrm{dc,a}}$ can be easily calculated numerically from (13) and is provided in **Tab. 3**. Compared to conventional operation, i.e., with $M_3 = 0$ and $\Delta E_{\mathrm{dc,a}} = 6.4\,\mathrm{J}$ (depicted in **Fig. 3(d.i)**), the buffered energy $E_{\mathrm{dc,a}}$ for $M_3 = 0.4$ in **Fig. 3(d.ii)** is reduced by 30 % and $E_{\mathrm{dc,a}}$ can be further reduced by up to a factor of two for $M_3 = 1.0$ (which however would require a higher dc-link voltage level to maintain current controllability according to (2)).

Combining (6) and (11) the time-varying dc-link voltage $U_{\mathrm{dc,a}}(t)$ results to

$$U_{\mathrm{dc,a}}(t) = \Big(\frac{2}{C_{\mathrm{dc}}}\Big(\frac{1}{8\omega_{\mathrm{ac}}}\hat{U}_{\mathrm{ac}}\hat{I}_{\mathrm{ac}}\Big(-2\sin(2\omega_{\mathrm{ac}} t) + 2\,M_3 \sin(2\omega_{\mathrm{ac}} t + \varphi_3) - M_3 \sin(4\omega_{\mathrm{ac}} t + \varphi_3)\Big) + E_{\mathrm{dc,a}}(0)\Big)\Big)^{0.5}. \tag{14}$$

The peak-to-peak dc-link LF voltage fluctuation $\Delta U_{\mathrm{dc,a}}$ results again in an excessively long analytic expression, and is hence calculated numerically from (14).

3) TRIANGULAR CM VOLTAGE INJECTION

Aiming at a symmetric three-phase system, any CM voltage comprising voltage components at multiples of the triple-mains frequency $3f_{\mathrm{ac}}$ can be considered. Here, a triangular CM voltage is considered which is implicitly generated by Space Vector Modulation (SVM). The SVM concept originates from the field of motor drive inverter systems and here, the main benefit of SVM is the fact that – in contrast to the 3rd-harmonic injection modulation – no Phase-Locked Loop (PLL) is required to generate a CM voltage reference at multiples of $3f_{\mathrm{ac}}$: The triangular SVM LF CM voltage reference is generated solely based on the measured instantaneous module input voltages $u_{\bar{\mathrm{a}}\bar{\mathrm{N}}}$, $u_{\bar{\mathrm{b}}\bar{\mathrm{N}}}$, $u_{\bar{\mathrm{c}}\bar{\mathrm{N}}}$ and is defined as

$$\bar{u}_{\mathrm{CM}}(t) = -M_{\mathrm{SVM}}(\max(u_{\bar{\mathrm{a}}\bar{\mathrm{N}}}, u_{\bar{\mathrm{b}}\bar{\mathrm{N}}}, u_{\bar{\mathrm{c}}\bar{\mathrm{N}}}) + \min(u_{\bar{\mathrm{a}}\bar{\mathrm{N}}}, u_{\bar{\mathrm{b}}\bar{\mathrm{N}}}, u_{\bar{\mathrm{c}}\bar{\mathrm{N}}})), \tag{15}$$

with M_{SVM} the harmonic injection modulation index and $\max(\bar{u}_{\mathrm{CM}}) = \frac{1}{2}M_{\mathrm{SVM}}\hat{U}_{\mathrm{ac}}$. Note that the negative sign in (15) facilitates a decrease of the maximum instantaneous phase voltage and $M_{\mathrm{SVM}} = 0.5$ is traditionally employed in drive applications in order to maximize the dc-link voltage utilization similar to 3rd-harmonic injection modulation with $M_3 = 1/6$.

Due to the additional frequency components in $\bar{u}_{\mathrm{CM}}(t)$ the analytic expressions for $E_{\mathrm{dc,a}}(t)$, $\Delta E_{\mathrm{dc,a}}$, $U_{\mathrm{dc,a}}(t)$, and $\Delta U_{\mathrm{dc,a}}$ are rather involved. However 3rd-harmonic and triangular CM voltage injection can be compared qualitatively by considering the Fourier coefficient of the frequency decomposition of (15) which can be approximated by

$$b_{\mathrm{n}} = \frac{1}{2}M_{\mathrm{SVM}}\hat{U}_{\mathrm{ac}}\frac{8}{\pi^2}\frac{(-1)^{(\frac{n}{3}-1)/2}}{(\frac{n}{3})^2}, \tag{16}$$

with $n = 3, 9, 15, \ldots$ at multiples of $3f_{\mathrm{ac}}$. Hence, for $M_{\mathrm{SVM}} = 1.0$ the Fourier coefficient at $n = 3$ results to $b_3 \approx 0.4 \cdot \hat{U}_{\mathrm{ac}}$, and hence (when neglecting the impact of the additional frequency components at $n > 3$) the energy buffering reduction is similar to 3rd-harmonic voltage injection with $M_3 = 0.4$, which is confirmed by the calculated vales of $\Delta E_{\mathrm{dc,a}}$ and $\Delta U_{\mathrm{dc,a}}$ in **Tab. 3**.

B. CONTROL CONCEPT

Fig. 4 illustrates the cascaded control concept for the phase modular three ac-dc converter in Y-configuration (see **Fig. 3(a)**) with an outer low-bandwidth dc-link voltage controller RU_{dc} (regulating the average dc-link voltage value of the three modules) and two fast grid current controllers Ri_j ($j \in \{a, b\}$):

First, RU_{dc} defines an equal power reference P_{j} for all modules. Note that instability might occur in case of individual dc-link voltage controllers due to the three-phase coupling of the rectifier modules as highlighted in [1], [12], and [29].

Note that this control structure does not penalize a DM imbalance between the three dc-link voltages and it is assumed that the subsequent dc-dc stages assure dc-link voltage balancing in the modules. Alternatively, the dc-link balancing concept of [30] and [31] could be employed.

The power reference is then translated into sinusoidal current references i_j^* in phase with each respective grid voltages by using a grid conductivity reference G_j^*. Here, only the two grid currents i_a and i_b are actively controlled by means of a current controller Ri_j, whereas i_c is inherently defined due to the open module starpoint $\bar{N}$ implying $i_\mathrm{c} = -(i_\mathrm{a} + i_\mathrm{b})$. Hence, the inductor voltage reference of phase c is derived from the current controller signals of the phase module a and b with $u_{L,c}^* = -(u_{L,a}^* + u_{L,b}^*)$. The inductor voltage references $u_{L,j}^*$ is subtracted from the grid phase voltage feedforward term, u_j and, finally, the LF CM voltage reference $\bar{u}_\mathrm{CM}$ is added to obtain the LF switch-node voltage $u_\mathrm{ref,j}$. Finally, by dividing $u_\mathrm{ref,j}$ by the respective dc-link voltage $U_\mathrm{dc,j}$ the module duty-cycle $m_\mathrm{j} \in \{-1, 1\}$ is obtained, which is translated into a Pulse Width Modulation (PWM) signal for the HF bridge-leg and a binary switching state of the unfolder bridge-leg.

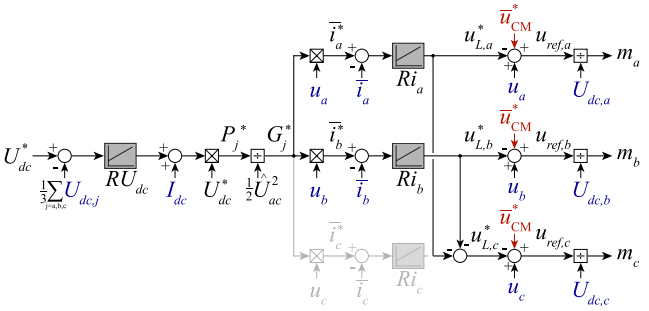

FIGURE 4. Block diagram of a cascaded control of the PFC rectifier input stages of Fig. 3(a) considering a 3rd harmonic CM voltage injection $\bar{u}_\mathrm{CM}^*$. (Figure adapted from [1].)

As a PLL is anyway required to generate a 3rd-harmonic CM voltage reference, the grid phase voltages u_j are calculated from the instantaneous PLL grid angle $\omega_\mathrm{ac}t$ and the (low-pass filtered) measured grid voltage amplitude $\hat{U}_\mathrm{ac}$ to avoid any undesired ringing or measurement noise originating from the grid voltage feedforward terms. The employed PLL is based on a Second-Order Generalized Integrator (SOGI) three-phase algorithm [32].

C. EXPERIMENTAL RESULTS

For this publication the 6 kW hardware demonstrator presented in **Fig. 5** was developed according to the specifications in **Tab. 1**. The system comprises three 2 kW single-phase PFC rectifier modules which can be freely reconfigured, thereby enabling the experimental investigation of the considered modulation strategies in Y-configuration and Δ-configuration (subject of **Section III**). Note that the prototype emulates the secondary isolated dc-dc converter stages (drawing a constant power P_j from the dc-link, see **Fig. 3a**) by three load resistors R_load during the experiments. For the considered operating points, the dc-link voltage fluctuation(and hence for a resistive load the dc current fluctuation) remains below ±10 %, such that R_load sufficiently approximates a constant-power load. Aiming at a flexible hardware demonstrator platform, the power module unfolder and HF bridge-leg semiconductors are realized with Silicon Carbide (SiC) Metal Oxide Semiconductor Field Effect Transistors (MOSFETs) rated to 1.2 kV [33] and further details on the main power components are listed in **Tab. 2**. It is worth highlighting that in an industrial system of course semiconductors with lower rated voltage, i.e., with 600 V for Y-configuration (and with 900 V for Δ-configuration) would be employed to maximize efficiency and minimize cost, whereas here the verification of the dc-link energy storage requirement reduction by a harmonic injection modulation is the main objective. The PWM switching frequency of the power semiconductors is selected to $f_\mathrm{s} = 48$ kHz such that advantageously only switching frequency harmonics of order four and above are subject to conducted electromagnetic emission limits starting from 150 kHz. Considering a higher switching frequency of, e.g., $f_\mathrm{s} = 72$ kHz could allow for a more compact realization of the ac inductors L which is, however, not the primary goal of this publication.

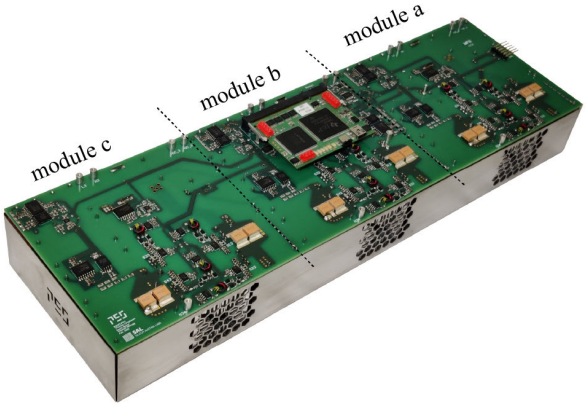

FIGURE 5. Phase-modular three-phase PFC rectifier hardware prototype which can be configured for Y- and Δ-connected operation of the modules as highlighted in Fig. 3. The system dimensions are 395 mm × 125 mm × 50 mm (15.6 in × 4.9 in × 2.0 in) and details on the main power components are listed in Tab. 2.

Measurement results for nominal power operation in Y-configuration are presented in **Fig. 6**. In case of conventional modulation (see **Section II-A1**) the CM voltage is set to $\bar{u}_\mathrm{CM} \approx 0$ and the module input voltages $\bar{u}_{\mathrm{j}\bar{\mathrm{N}}}$ in **Fig. 6(a.i)** are purely sinusoidal and the module input current $\bar{i}_\mathrm{a}$ is in phase with the respective grid voltage. **Fig. 6(a.ii)** further depicts the dc-link voltage of module a $U_\mathrm{dc,a}$ and the peak-to-peak dc-link voltage fluctuation results to $\Delta U_\mathrm{dc,a} = 66.5$ V corresponding to a buffered energy $\Delta E_\mathrm{dc,a} = 6.5$ J (obtained by

TABLE 2. Main power components of the hardware demonstrator.

Component	Nom. value	Details
Controller	$f_{\mathrm{clk}} = 150\,\mathrm{MHz}$	1 x TMS320C2834X
Semiconductors	$f_{\mathrm{s}} = 48\,\mathrm{kHz}$	12 x Infineon SiC IMZ120R030M1H 30 mΩ 1.2 kV (unfolder and HF bridge-leg)
Heatsink	$R_{\mathrm{th}} = 0.9\,\mathrm{K/W}$	3 x Fischer Elektronik LAM 4 75 12
ac inductor	$L = 600\,\mu\mathrm{H}$	3 x Changsung magnetic powder core LHEQ3626, 66 turns of 0.3 mm flat wire
dc-link capacitor	$C_{\mathrm{dc,LF}} = 240\,\mu\mathrm{F}$	6 x Kemet C4AQJBW5400M3LJ 40 µF, 700 V
	$C_{\mathrm{dc,HF}} = 1\,\mu\mathrm{F}$	2 x TDK Ceralink, 0.5 µF, 700 V
ac capacitor	$C_{\mathrm{ac}} = 4\,\mu\mathrm{F}$	4 x WE FTX2 890324026027, 1 µF, 275 $\mathrm{V_{RMS}}$
Load resistor	$R_{\mathrm{load}} = 80\,\Omega$	Y-configuration (see **Fig. 3(a)**)
Load resistor	$R_{\mathrm{load}} = 245\,\Omega$	Δ-configuration (see **Fig. 3(e)**)

TABLE 3. Measurement results for Y-configuration.

Modulation	ΔU_{dc} calc.	ΔU_{dc} meas.	ΔE_{dc} calc.	ΔE_{dc} meas.	THD meas.	η meas.
$M_3 = 0$ (conv.)	66.8 V	66.8 V	6.40 J	6.47 J (100 %)	1.39 %	98.6 %
$M_3 = 0.2$	55.0 V	55.4 V	5.27 J	5.23 J (80.8 %)	1.23 %	98.6 %
$M_3 = 0.4$	46.6 V	46.7 V	4.47 J	4.45 J (68.8 %)	1.64 %	98.7 %
$M_3 = 0.6$, $\varphi_3 = 11.4°$	41.0 V	43.6 V	3.94 J	4.03 J (62.3 %)	2.51 %	98.5 %
$M_{\mathrm{SVM}} = 0.5$	54.3 V	54.7 V	5.20 J	5.17 J (79.9 %)	1.17 %	98.6 %
$M_{\mathrm{SVM}} = 1.0$	45.8 V	46.3 V	4.39 J	4.38 J (67.7 %)	1.50 %	98.6 %

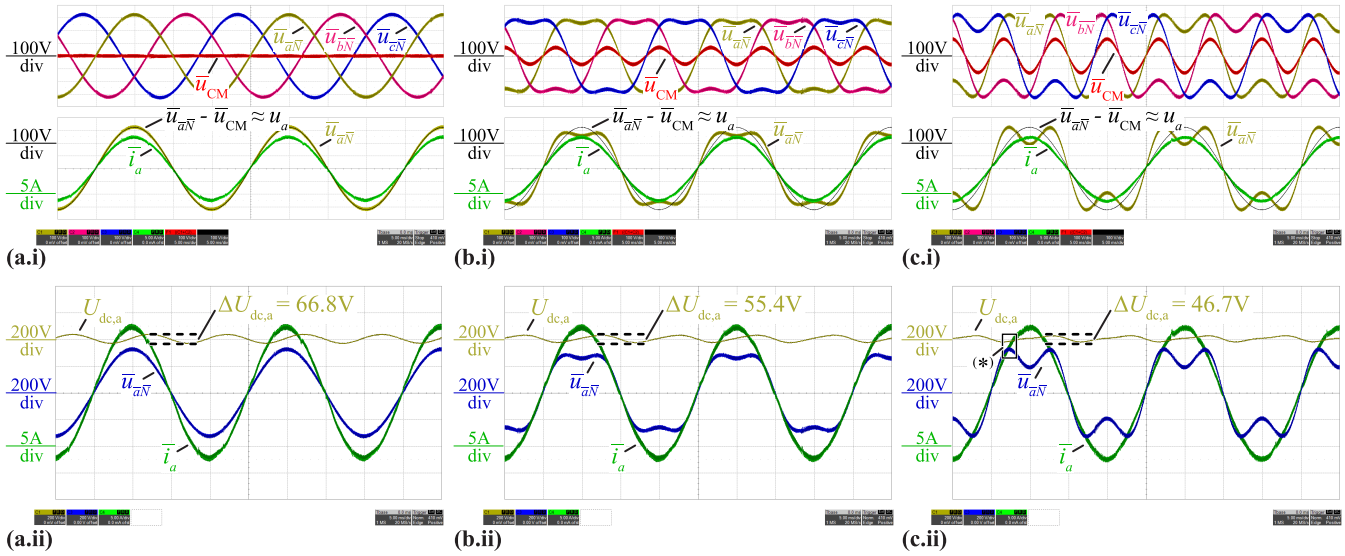

FIGURE 6. Experimental waveforms for nominal power operation in Y-configuration: (a.i)-(c.i) Input voltages $\bar{u}_{\bar{a}\bar{N}}$, $\bar{u}_{\bar{b}\bar{N}}$, $\bar{u}_{\bar{c}\bar{N}}$, CM voltage $\bar{u}_{\mathrm{CM}}$ and input current $\bar{i}_{\mathrm{a}}$ for a 3rd harmonic modulation index of (a.i) $M_3 = 0$, (b.i) $M_3 = 0.2$ and (c.i) $M_3 = 0.4$ in Y-configuration. (a.ii)-(c.ii) Input voltage $\bar{u}_{\bar{a}\bar{N}}$, input current $\bar{i}_{\mathrm{a}}$, dc-link voltage $U_{\mathrm{dc,a}}$ and dc-link voltage variation $\Delta U_{\mathrm{dc,a}}$ for a 3rd harmonic modulation index of (a.ii) $M_3 = 0$, (b.ii) $M_3 = 0.2$ and (c.ii) $M_3 = 0.4$ in Y-configuration. (*) The minimum dc-link voltage margin for current controllability of 58 V within a mains period is highlighted in (c.ii).

integrating the measured voltage $\bar{u}_{\bar{j}\bar{N}}$ and current $\bar{i}_{\mathrm{a}}$) which closely match the calculated values according to (9) and (7) provided in **Tab. 3**.

Next, operation with a 3rd-harmonic voltage injection index $M_3 = 0.2$ and $M_3 = 0.4$ is depicted in **Fig. 6(b)** and **(c)**, respectively. There, the module input current $\bar{i}_{\mathrm{a}}$ is not impacted by the injected CM voltage and remains fully sinusoidal and in phase with the grid voltage u_{a}. At the same time, the energy buffered by the dc-link $\Delta E_{\mathrm{dc,a}}$ is reduced by 19.2 % for $M_3 = 0.2$ and by 31.2 % for $M_3 = 0.4$ (see **Tab. 3**), and again closely matches the theoretical predictions of **Section II-A2**.

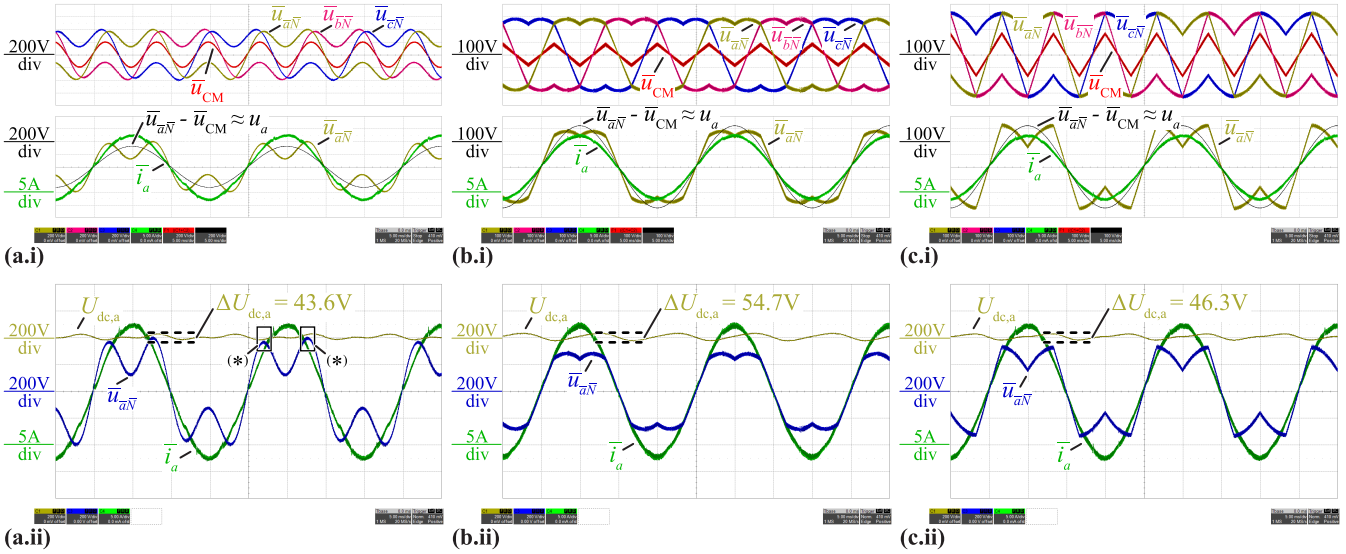

FIGURE 7. Experimental waveforms for nominal power operation in Y-configuration: (a.i-c.i) Input voltages $u_{\bar{a}\bar{N}}$, $u_{\bar{b}\bar{N}}$, $u_{\bar{c}\bar{N}}$, CM voltage u_{cm} and input current $\bar{i}_a$ for a 3rd harmonic modulation index of (a.i) $M_3 = 0.6$ and $\varphi_{CM} = 11.4°$, (b.i) SVM of $M_{SVM} = 0.5$ and (c.i) SVM of $M_{SVM} = 1$ in Y-configuration. (a.ii-c.ii) Input voltages $u_{\bar{a}\bar{N}}$, input current $\bar{i}_a$, dc-link voltage $U_{dc,a}$ and dc-link ripple voltage $\Delta U_{dc,a}$ for a 3rd harmonic modulation index of (a.ii) $M_3 = 0.6$ and $\varphi_3 = 11.4°$, (b.ii) SVM of $M_{SVM} = 0.5$ and (c.ii) SVM of $M_{SVM} = 1$ in Y-configuration. (*) The minimum dc-link voltage margin for current controllability of 20 V within a mains period is highlighted in (a.ii).

As highlighted in **Fig. 6(c.ii)** with (*) the dc-link voltage margin for current controllability (2) reduces to 58 V for $M_3 = 0.4$, and for the given dc-link capacitor value $C_{dc} = 240\ \mu$F a further increase of the harmonic injection to $M_3 = 0.6$ would require an elevated average dc-link voltage >400 V which is typically undesirable as this measure would inhibit the use of 600 V Gallium Nitride (GaN) power semiconductors with superior performance compared to devices of higher blocking voltage.

Alternatively, the 3rd-harmonic phase φ_3 can be utilized to separate in time the maxima of the LF module input voltage $\bar{u}_{\bar{a}\bar{N}}$ and the minima of the dc-link voltage $U_{dc,a}$ [1] such that the current controllability constraint (2) is respected. **Fig. 7(a)** presents experimental waveforms for a modulation index of $M_3 = 0.6$ and $\varphi_{CM} = 11.4°$, where a minimum dc-link voltage margin of 20 V (highlighted with (*)) is respected.

Fig. 7(b) and **(c)** further depict experimental waveforms for SVM operation with $M_{SVM} = 0.5$ and $M_{SVM} = 1$, respectively. Again, the input current is not impacted by the injected CM voltage which now contains additional frequency components compared to 3rd-harmonic voltage injection. As discussed in **Section II-A3**, the reduction of the dc-link voltage fluctuation $\Delta U_{dc,a}$ and the buffered energy $\Delta E_{dc,a}$ is almost identical for $M_{SVM} = 0.5$ and $M_3 = 0.2$, and for $M_{SVM} = 1$ and $M_3 = 0.4$ with the main advantage of the SVM operation given by the fact that no PLL is required to generate the CM voltage reference.

In summary, it can be stated that the predicted energy buffering and/or dc-link voltage fluctuation with harmonic voltage injection is verified with the prototype system (see **Tab. 3**). Alternatively, the dc-link voltage fluctuation can be kept constant for a reduced dc-link capacitor value by means of harmonic voltage injection. Note that **Tab. 3** also provides the measured grid current Total Harmonic Distortion (THD) and electrically measured conversion efficiency η where the harmonic injection has only a marginal impact on both performance metrics.

III. DELTA-CONNECTED PHASE-MODULAR CONVERTER

A. THEORY

The three single-phase-phase isolated PFC modules in Δ-configuration are shown in **Fig. 3(e)** with the grid voltage and current amplitude defined in **Tab. 1**. Here the modules are subject to the grid line-to-line voltages u_{jk} and currents i_{jk} which are defined as

$$u_{jk}(t) = \sqrt{3}\hat{U}_{ac}\sin(\omega_{ac}t + \phi_{jk}),$$
$$i_{jk}(t) = \frac{1}{\sqrt{3}}\hat{I}_{ac}\sin(\omega_{ac}t + \phi_{jk}), \quad (17)$$

with $j, k \in \{a, b, c\}$ and $j \neq k$, and phase angles $\phi_{ab} = 0, \phi_{bc} = -\frac{2\pi}{3}, \phi_{ca} = -\frac{4\pi}{3}$. Hence, the nominal module current in **Tab. 1** is advantageously reduced compared to Y-configuration. This, however, comes at the cost of an increased dc-link voltage with typically $U_{dc} = 700$ V, such that 900 V SiC and 900 V Silicon (Si) Super Junction (SJ) MOSFETs must be employed in the HF and unfolder bridge-legs of the converter modules, respectively. Compared to a standard monolithic boost-type three-phase PFC rectifier system [2] of the same power rating, the three single-phase PFC rectifier modules in Δ-configuration advantageously operate with reduced input currents amplitude and rms values.

The ac-side equivalent circuit from [1] for the Δ-configuration of the converter modules is shown in **Fig. 3(f)**. There the rectifier front-end switch-node voltages

are decomposed into DM/CM and LF/HF components, e.g., for phase module a the switch-node voltage $u_{\bar{a}b}$ is represented by

- the HF DM and CM voltage $u_{\bar{a}b\sim}$,
- the LF DM voltage $\bar{u}_{\bar{a}b} \approx u_{ab}$.

Note that in order to avoid LF grid current distortions, the rectifier front-end switch-node voltages must not generate an LF CM voltage component, as the modules directly connect to the grid line-to-line voltages.

However, in Δ-configuration three-phase grid currents i_a, i_b, i_c are formed by subtracting the line-to-line currents i_{ab}, i_{bc}, i_{ca} and accordingly a CM current i_{CM} can circulate in the Δ-connection and/or flow between the three single-phase PFC rectifier modules in **Fig. 3(e)** [34], [35] [36]. Hence, the module input current $i_{\bar{j}}$ can be decomposed into

- the HF DM input current $i_{\bar{a}\sim}$,
- the LF DM input current $\bar{i}_{\bar{a}b} \approx i_{ab}$,
- the HF CM input current $i_{CM\sim}$,
- the LF CM input current $\bar{i}_{CM}$,

and accordingly, the LF module input power $\bar{p}_a$ is defined by the LF DM voltage $\bar{u}_{\bar{a}b}$ and the corresponding LF module current $\bar{i}_{\bar{a}}$ as

$$\bar{p}_a(t) = \bar{u}_{\bar{a}b}(t) \cdot \bar{i}_{\bar{a}}(t) = \bar{u}_{\bar{a}b}(t) \cdot (\bar{i}_{\bar{a}b}(t) + \bar{i}_{CM}(t)). \quad (18)$$

Hence, the module input power can be – similar to Y-configuration – impacted by means of harmonic injection, however, here with a CM / zero-sequence current $\bar{i}_{CM}$

1) CONVENTIONAL MODULATION

The main ac-side terminal voltage waveforms for conventional modulation (i.e., with $\bar{i}_{CM} = 0$) are presented in **Fig. 3(g.i),(h.i)** where the LF module input power $\bar{p}_a$ according to (18) is equivalent to (5) and comprises the well known twice-mains-frequency single-phase grid power pulsation on top of the (assuming ideally lossless power conversion) constant module output power $P_a = \frac{1}{2}\hat{U}_{ac}\hat{I}_{ac}$. Similarly, the dc-link capacitor C_{dc} energy balance $E_{dc,a}(t)$ is defined by (6), and the dc-link LF energy buffering requirement $\Delta E_{dc,a}$ (highlighted with light-gray areas in **Fig. 3(h.i)**) by (7). Last, the time-varying dc-link voltage $U_{dc,a}(t)$ and the peak-to-peak dc-link LF voltage fluctuation $\Delta U_{dc,a}$ are described by (8) and (9), respectively.

In the following, the voltage $\bar{u}_{CM}$ is used to adjust the LF module input power $\bar{p}_a$ such that the energy buffering requirement $\Delta E_{dc,a}$ and the fluctuation of the dc-link voltage $\Delta U_{dc,a}$ is reduced.

2) 3rd-HARMONIC CM CURRENT INJECTION

In case of 3rd-harmonic current injection, the LF CM current reference value is defined as

$$i_{CM}(t) = M_3 \frac{1}{\sqrt{3}} \hat{I}_{ac} \sin(3\omega_{ac} t), \quad (19)$$

with the 3rd-harmonic modulation index $M_3 = \hat{I}_{CM}/(\sqrt{3}\hat{I}_{ac})$. Note that in contrast to 3rd-harmonic *voltage* injection, here, the selected value of M_3 has (in first approximation) no impact on the current controllability dc-link voltage margin (cf., (10)), such that no phase-shift angle (i.e., $\varphi_3 = 0$) is considered here. In **Fig. 3(g.ii,h.ii)** the characteristic waveforms of module a are illustrated for a 3rd-harmonic current injection with $M_3 = 0.4$. There, the LF module input power $\bar{p}_a$ according to (18) is described by (11) and with increasing values of M_3 the twice-mains frequency power pulsation is shifted from $2f_{ac}$ to $4f_{ac}$.

Again, the equations describing the dc-link energy and voltage waveform are (with the selected definition of the harmonic injection current (19)) equivalent to 3rd-harmonic voltage injection, i.e., the dc-link capacitors C_{dc} energy balance $E_{dc,a}(t)$ is defined by (13) and the time-varying dc-link voltage $U_{dc,a}(t)$ by (14). The numerically calculated dc-link LF energy buffering requirement $\Delta E_{dc,a}$ and the peak-to-peak dc-link LF voltage fluctuation $\Delta U_{dc,a}$ are provided in **Tab. 4**. Note that for a given value of M_3, $\Delta E_{dc,a}$ is identical for CM voltage injection (Y-configuration) and CM current injection (Δ-configuration), whereas $\Delta U_{dc,a}$ is reduced in Δ-configuration due to the elevated average dc-link voltage U_{dc} (cf., **Tab. 3**, **Tab. 4**).

B. CONTROL CONCEPT

The considered control concept presented in **Fig. 4** is similar to the Y-configuration (see **Sec. II-B**) and comprises the outer, low-bandwidth dc-link voltage controller (for all three converter modules) and the underlying current controllers. In contrast to Y-configuration, the module input currents in Δ-configuration no longer sum to zero and therefore three individual current controllers are required to ensure sinusoidal currents in all phases. Here the 3rd-harmonic CM current reference is added to the sinusoidal DM reference current values, i.e., the CM current reference is actively tracked by the current controllers.

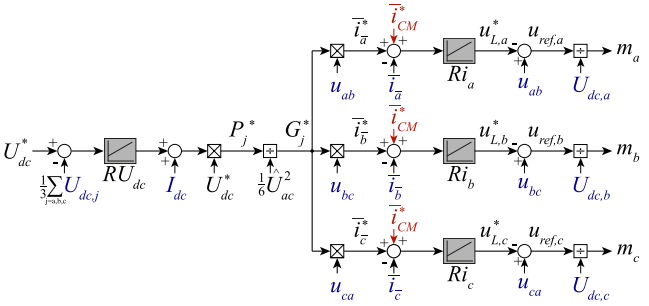

FIGURE 8. Block diagram of a cascaded control of the PFC rectifier input stages of Fig. 3(e) considering a 3rd harmonic CM current injection $\bar{i}^*_{CM}$.

C. EXPERIMENTAL RESULTS

Here, the hardware demonstrator of **Fig. 5** is reconfigured to a Δ-arrangement of the three single-phase PFC rectifier modules. Measurement results for nominal power operation are presented in **Fig. 9**. In case of conventional modulation (see **Section III-A1**) the CM current is set to $\bar{i}_{CM} \approx 0$ and the module input currents $i_{\bar{j}}$ in **Fig. 9(a.i)** are (apart from the HF current ripple) fully sinusoidal and in phase with

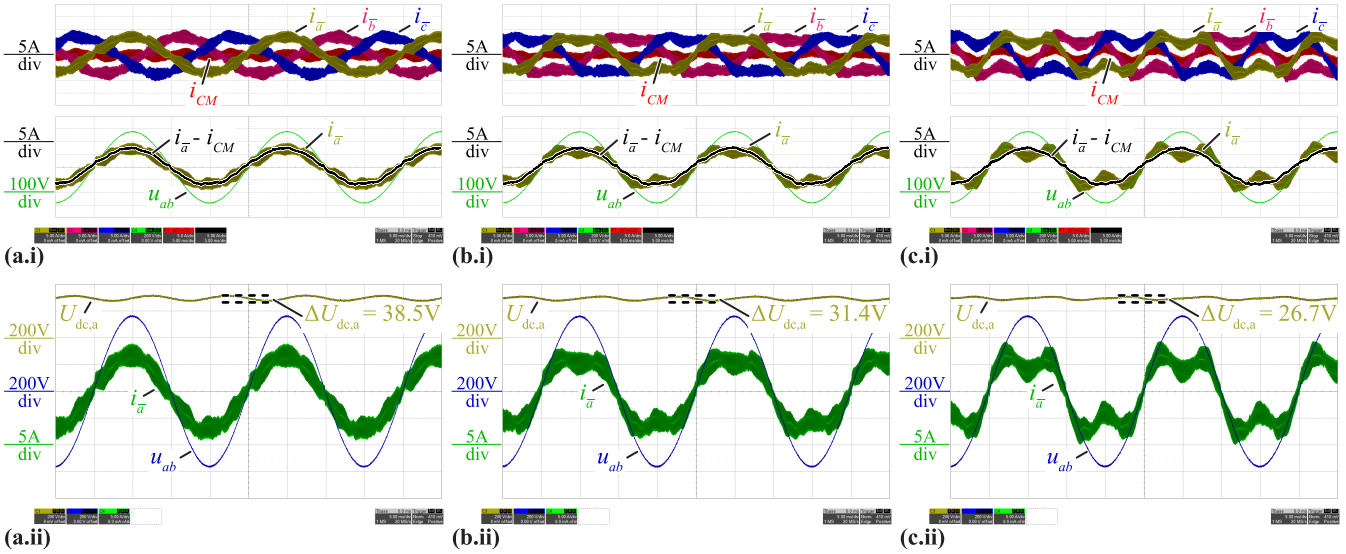

FIGURE 9. Experimental waveforms for nominal power operation in Δ-configuration: (a.i-c.i) Module input currents $i_{\bar{a}}$, $i_{\bar{b}}$, $i_{\bar{c}}$, CM current i_{CM} and grid line-to-line voltage u_{ab} for a 3rd harmonic modulation index of (a.i) $M_3 = 0$, (b.i) $M_3 = 0.2$ and (c.i) $M_3 = 0.4$. The sinusoidal LF DM current $i_{\bar{a}} - i_{CM}$ was extracted from the exported oscilloscope waveforms and added on top of the screenshots for illustration purposes. (a.ii-c.ii) Module input current $i_{\bar{a}}$, grid line-to-line voltage u_{ab}, dc-link voltage $U_{dc,a}$ and dc-link ripple voltage $\Delta U_{dc,a}$ for a 3rd harmonic modulation index of (a.ii) $M_3 = 0$, (b.ii) $M_3 = 0.2$ and (c.ii) $M_3 = 0.4$.

TABLE 4. Measurement results for Δ-configuration compromising the dc-link voltage ripple and the energy stored in the dc-link capacitors.

Modulation	ΔU_{dc} calc.	ΔU_{dc} meas.	ΔE_{dc} calc.	ΔE_{dc} meas.	THD meas.	η meas.
$M_3 = 0$ (conv.)	38.1 V	38.5 V	6.40 J	6.60 J (100 %)	4.70 %	99.2 %
$M_3 = 0.2$	31.4 V	31.4 V	5.27 J	5.37 J (81.4 %)	4.87 %	99.0 %
$M_3 = 0.4$	26.6 V	26.7 V	4.47 J	4.64 J (70.3 %)	4.72 %	99.0 %

the respective grid line-to-line voltage. **Fig. 9(a.ii)** further depicts the dc-link voltage of module a, $U_{dc,a}$, and the peak-to-peak dc-link voltage fluctuation results to $\Delta U_{dc} = 38.5$ V corresponding to a buffered energy $\Delta E_{dc} = 6.6$ J (obtained by integrating the measured voltage $\bar{u}_{\bar{a}b}$ and current $\bar{i}_{\bar{a}}$) which closely match the calculated values according to (9) and (7) provided in **Tab. 4**.

Next, operation with a 3rd-harmonic current injection index $M_3 = 0.2$ and $M_3 = 0.4$ is depicted in **Fig. 9(b)** and **(c)**, respectively. There, the module the module input currents $i_{\bar{j}}$ comprise an increasing CM component, and the grid current remains fully sinusoidal. At the same time, the dc-link voltage variation $\Delta U_{dc,a}$ is reduced by 18.6 % for $M_3 = 0.2$ and by 29.7 % for $M_3 = 0.4$, thereby verifying the predicted energy buffering and/or dc-link voltage fluctuation with harmonic current injection (see **Tab. 4**).

Here, in contrast to harmonic voltage injection, the current controllability is not affected by injected CM current. However, the module input current rms stresses increase with M_3, thereby causing additional conduction losses. Hence, the measured converter efficiency drops from $\eta = 99.2\,\%$ to $\eta = 99.0\,\%$ for the considered operating point. Note that the improved conversion efficiency in Δ-configuration compared to Y-configuration results as a 700 V dc-link better utilizes the employed 1200 V SiC MOSFETs of the hardware demonstrator and does not indicate a general superiority of the Δ-configuration over the Y-configuration.

IV. CONCLUSION

Phase-modular isolated three-phase Power Factor Correction (PFC) rectifiers comprising three front-end single-phase PFC rectifier modules show superior conversion efficiency compared to a standard monolithic three-phase rectifier system due to the lower dc-link voltage level and/or reduced current stresses of the power semiconductors. Further, reconfiguration from a star (Y)-arrangement to a delta (Δ)-arrangement of the PFC rectifier modules allows for wide input voltage ranges without compulsory over dimensioning of the main power components. However, each of the front-end single-phase PFC rectifier modules requires a large dc-link capacitor to buffer the single-phase twice-mains-frequency input power pulsation.

Recent literature proposes a power pulsation reduction by means of harmonic injection techniques and this paper provides an experimental verification of the proposed modulation concept. Both a Y-arrangement (i.e., with CM voltage

injection, see **Fig. 3(a)**) and a Δ-arrangement (i.e., with CM current injection, see **Fig. 3(e)**) of the three front-end single-phase PFC rectifier modules is considered. Measurement results obtained from a 6 kW prototype reveal a dc-link voltage variation and/or energy buffering reduction by up to 38.6 % enabled by the harmonic injection modulation compared to conventional operation, which is in line with the theoretical considerations.

In closing it is important to highlight, that future research could also investigate advanced modulation strategies to further minimize the dc-link energy buffering requirement and/or minimize the switching losses by means of clamping modulation [37], [38].

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