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RESEARCH ARTICLE

Dead-Time Impact on the Harmonic Distortion and Conversion Efficiency in a Three-Phase Five-Level Cascaded H-Bridge Inverter: Mathematical Formulation and Experimental Analysis

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ABSTRACT To avoid leg short-circuit in inverters, dead time must be introduced on leg gate signals. Dead time affects the inverter output voltage fundamental harmonic amplitude, voltage harmonic distortion and inverter efficiency by introducing additional voltage drops. In this regard, dead time effects have been widely investigated for traditional two-level three-phase voltage source inverters in the literature but not extensively for multilevel topology structures. This paper provides a detailed analysis of dead time impact on the harmonic distortion and efficiency of Cascaded H-Bridges Multilevel Inverters (CHBMIs). For this purpose, a general mathematical formulation to determine voltage drop due to dead time effects, also taking into account the adopted Multicarrier PWM strategy, has been provided and experimentally validated for a five-level three-phase CHBMI structure. As a comparison tool between expected and ideal inverter output voltage, the percentage voltage error $e_{\%}$ is introduced. In most of the cases, $e_{\%}$ is lower than 5%, and it starts increasing for very low amplitude modulation index or for specific working points where nonlinearities occur. Furthermore, several experimental investigations have been carried out to evaluate the CHBMI performance in terms of harmonic distortion and efficiency by changing, the values of dead time, modulation index and switching frequency for ten different multi-carried PWM strategies. Experimental results confirm the strong dependency between the dead time impact on the converter performance and the adopted Multi Carrier-PWM (MC-PWM) strategy: as a way of example, converter efficiency can be reduced from 80% to 60% when dead time is increased from 0.5 μs to 1.5 μs and Phase Shifted-PWM (PS-PWM) is adopted.

INDEX TERMS Dead time, harmonic distortion, efficiency, multilevel inverter, multi carrier PWM.

I. INTRODUCTION

Nowadays, energy saving and sustainable development play a key role in the mitigation of the expected catastrophic climate scenario; a way to reduce pollution emissions is the loss minimization or efficiency maximization of energy production and conversion systems.

In this contest, power converters represent one of the most widely used technologies employed in the energy framework especially in industrial applications, due to their high

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efficiency, low maintenance, compact size, robustness, and economical costs [1], [2]. In particular, Multilevel Inverters (MIs) represent an innovative and promising solution in the power conversion field for several applications such as energy transmission, distribution and electric drives, thanks to their improved performances. In detail, if compared with traditional VSIs, MIs present lower voltage THD and lower *dv/dt* on output voltage waveforms resulting in reduced switching devices voltage stress and lower EMIs [3], [4].

Among all topologies, CHBMI seems to be one of the most interesting in grid-connected applications [4], [5]: they find applications such as Flexible AC Transmission Systems (FACTS), static compensators (STATCOM), Dynamic Voltage Restorers (DVRs), Unified Power Flow Controllers (UPFC) [7], and photovoltaic energy generation [8], [9]. The modular structure allows for reaching high inverter output voltage and high-number of voltage levels starting by low voltage DC sources, reducing the Total Harmonic Distortion (THD) and avoiding bulky and expensive filters; in PV applications, the modular structure allows for avoiding the DC-DC conversion stage to execute the MPPT [10]. CHBMI is being adopted also in medium-voltage high-power industrial electric drives [11]. In detail, in the range of 4.16-13.8 kV, CHBMI-based electric drives result to be the most efficient, if compared with other MI topologies, regardless of the semiconductor technology. In this application, the main drawback is linked with the necessity of separated DC sources, which require a transformer with multiple secondary windings, which becomes increasingly costly and complicated to realize when the system rated voltage increases [12].

Recently, several studies in the literature have shown the advantages of using CHBMI in electric traction, electric mobility [13], [14], [15], [16] and aircraft [17]. In detail, CHBMI allows overcoming electric vehicle limits, such as limited power and energy density, and long recharging time, by increasing the total DC link voltage [18]. At the same time, it allows for maximizing performance and vehicle efficiency: lower voltage THD leads to a reduced torque ripple and lower iron losses, especially when switching frequency is reduced; the modular structure and required isolated DC sources allow simple integration between high-power and high-energy-density DC sources, such as batteries and supercapacitors, and their active control without DC-DC conversion stage [19]. According to [13], several challenges have to be faced: first, the converter weight and volume, and, as a consequence, the necessity of integration with the battery pack, in order to minimize the powertrain volume; second, the control complexity with respect to a traditional 2L-VSI; third, the converter impact on the battery module lifetime. In detail, the lack of an intermediate DC-DC converter between the inverter and the battery on a side can reduce the powertrain cost, weight, volume, and hardware complexity, but on the other side, can accelerate the reduction of the State of Health (SoH) of the battery, however, this is an open topic. In this analysis, it is necessary to consider that an increment in the CHBMI levels number, which results in better performances in terms of harmonic behavior and reliability, requires a huge increase in hardware resources. Therefore, for the aforementioned applications, the five-level three-phase CHBMI topology represents the most suitable topology in terms of the ratio between hardware resources and reachable benefits. In this context, new modulation strategies and control algorithms are extensively analyzed and proposed in the literature to further improve the CHBMI performance without increasing hardware resources [20]. For these reasons, the five-level three-phase structure is the most interesting and, thus, the most challenging.

The modulation strategy plays a key role in the performance optimization of CHBMI. Usually, Multicarrier Pulse Width Modulation (MC-PWM) modulation strategies are employed for CHBMI control purposes and they represent a natural evolution of traditional PWM modulation techniques. In detail, concerning traditional PWM, a higher number of triangular carriers is required, depending on the number of available output voltage levels. Carriers mutual disposition can be varied to obtain several modulation strategies [21], [22], [23].

Regardless of the adopted modulation strategy, control signals on the same converter leg must always be opposite, to avoid short circuits. Since switching devices are characterized by turn-on and turn-off delays, to avoid short-circuit conditions, Dead Time (DT) must be introduced. DT is defined as the time interval in which both devices on the same leg receive low gate signals. DT assumes a vital role in inverter reliability, it generates significant effects on both the inverter output voltage waveforms and the input quantities. Essentially, when both switches on an inverter leg are not conducting due to the DT, the load voltage depends on the direction of the load current, causing output voltage distortion. In detail, when the inverter output voltage and current have the same polarity, the inverter output voltage is reduced and vice versa. DT induces low-order harmonics on output voltage waveforms. Indeed, high switching frequencies and DT values generate a high distortion level of output voltage and an amplitude reduction of the fundamental harmonic. In grid-connected applications, such effects produce severe degradation of power quality. To improve power quality, LCL filters are adopted to mitigate PWM high-frequency harmonics.

DT impact effects have been widely investigated in the literature only for conventional two or three-level VSI, however, it is of considerable interest in the field of multilevel inverters although it has not been widely investigated yet. To reduce the injection into the grid of current harmonics, several DT compensation methods on conventional VSI have been developed in the literature. Compensation methods of DT non-linearities can be classified into two main categories [24]: in the first method, the average voltage drop over one period of the modulation signal is evaluated and added to the reference voltage; in the second, the voltage drop is evaluated on the current switching period and it is compensated at the next one.

This last method requires a very high computational cost and a very fast controller; thus, it is not commonly used. The first method is less accurate and the compensation signal depends on the current sign. Detection of current sign results to be difficult, especially on current zero-crossing.

According to the first strategy, the compensation signal is a square wave to be added to the modulating signal, whose amplitude is equal to the average voltage error during each switching period. Taking into account larger switching devices, (power rating PWM inverter for traction application reach hundreds of kilowatts) the error voltage waveshape seems to be closer to the trapezoidal wave: the classical compensation criterion produces an overcompensation and the snubber circuits must be considered [25].

Advanced control strategies have been developed, to compensate for low-frequency harmonics: Resonant Controllers are largely used in single-stage conversion in photovoltaic applications; they allow mitigating low-frequency harmonics but can trigger dangerous resonance phenomena. A new Repetitive Control is proposed in [26]: it can suppress selected low-frequency harmonics below the Nyquist frequency without bringing the system into instability. In [27], an alternative compensation scheme to minimize the zero-current clamping is proposed. The compensation voltage signal is piecemeal and has a trapezoidal wave shape. In addition, many small-signal models have been developed, to simulate the DT effects and implement a predictive model control for DT compensation. In [28] a VSI small-signal model including the dead time effects in DQ-frame is proposed: taking into account a three-phase RL passive load in DQ-frame, Z_{qq} impedance results to be more resistive than the Z_{dd} impedance due to the dead time, especially at low frequency. When the inverter feeds an electric motor, DT produces an increase in iron losses [29] and low-frequency harmonics produce torque ripple and other effects which depend on the specific electric drive. Taking into account an induction motor, as in [30], additional cross-coupling due to the DT is found. Moreover, open-loop V/Hz controlled induction motor drives exhibit small-signal instability in light load and low-speed conditions [31]. The oscillatory operating range is expanded with an increase of both DT and switching frequency. Finally, DT produces an increase in measured radiated emission and a shift in the lower-frequency range of resonant frequency [32]. On the source side, harmonics afflict source power quality, cause transformers to overheat, and increase the skin effect on wires. In [33], a DC link small-signal model is developed, to investigate the DT effects on the DC voltage and current. Oscillations on the inverter input current are observed.

In [34], a comparison between the output voltage waveforms of a Unipolar PWM-controlled H-Bridge and a PS-PWM-controlled Cascaded H-Bridge MI is carried out in the simulation environment. CHBMI is less afflicted by the DT effects since a lower THD is evaluated when the DT increases. In [35], [36], and [37], new DT compensation algorithms for CHBMI and NPCMI are proposed.

Regarding MIs, evaluation of the DT effects becomes more difficult, on one side due to the several and more complex available topologies, on the other due to the numerous available modulation strategies. Thus, an extended analysis of DT effects on CHBMI can be useful for CHBMI design and control purposes, and to define new compensation methods or mathematical models able to estimate the DT effects on converter electrical quantities.

Authors of this work have partially investigated the 3P-5L CHBMI behaviour: in [38] a preliminary analysis of CHBMI behaviour in terms of converter efficiency and voltage Total Harmonic Distortion (THD) as a function of switching frequency has been performed by considering some MC-PWM strategies. This analysis has been extended and deeply discussed in [23]. In detail, converter efficiency and voltage THD have been analyzed and discussed for ten different MC-PWM strategies, several CHBMI working conditions and switching frequency values. The DT effects have not been directly faced, however, these works represent the starting point for the DT analysis. Authors began the DT investigations in [39]; in detail, two strategies for the DT generation are proposed and the DT effects are analyzed on two MC-PWM strategies (PS-PWM and SCAMOD), taking into account voltage THD and converter efficiency. The results obtained are not adequate for extended analysis and provide only a partial overview of the DT impact on CHBMI behavior.

This paper aims to deeply extend the investigation of the DT impact on three-phase five-level Cascaded H-Bridge Multilevel Inverter (3P-5L CHBMI) performance begun in [39], taking into account all the MC-PWM strategies considered in [23], and providing a mathematical formulation to estimate the voltage drop on output voltage fundamental harmonic due to the DT. In detail, the voltage drop mathematical formulation can be applied to a generic number of voltage levels and to all the MC-PWM strategies considered in this work. Furthermore, to perform an extended analysis of the DT impact on CHBMI performance in terms of voltage distortion and conversion efficiency, several CHBMI working conditions have been considered. Working conditions are defined on the base of the adopted modulation strategy, switching frequency and DT values. In order to discriminate the DT effects on voltage waveforms in a much more accurate way, not only the previously used Total Harmonic Distortion (THD) is taken into account, but also several other distortion indexes, such as Partial Harmonic Distortion (PHD) and Low-Frequency Total Harmonic Distortion ($THD_{LF}\%$), are introduced. Therefore, distortion indexes and the converter efficiency are used as comparison tools, to compare experimental results associated with each considered working condition. Regarding modulation strategies, by combining five different carrier dispositions (three Level Shifted (LF), one Phase Shifted, and one hybrid strategy) and two modulating

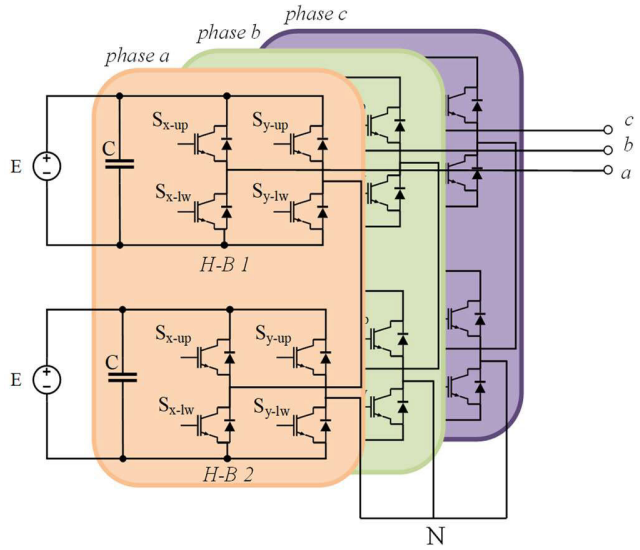

FIGURE 1. Circuit diagram of a three-phase five-level CHB.

signals groups (Sinusoidal and Switching Frequency Optimal), ten MC-PWM modulation strategies are obtained.

This work aims to provide a detailed analysis and experimental validation with respect to the CHBMI converters, which is actually missing in the literature. The output results can be imported and scaled for each system which employs a generical 3P-n_lL-CHBMI to provide guidelines for converters designers, thanks to the proposed mathematical model generalization.The paper is structured in the following sections: Section II presents the considered MC-PWM modulation strategies and their main features; Section III the voltage drop mathematical formulation due to dead time effects for the CHBMI inverter is described; Section IV presents the test bench set-up, the CHBMI prototype and its control implementation on SOM sbRIO-9651 control board; Section V presents the experimental investigations carried out and the results obtained. The abbreviations used throughout the paper are listed in Table I.

II. MULTICARRIER-PWM: A SUMMARY

Multicarrier Pulse Width Modulation (MC-PWM) schemes and their impact on 3P-5L CHBMI efficiency and THD have been deeply analyzed as a function of switching frequency values in [23]. To evaluate DT effects on the same converter topology and modulation schemes for various DT values, MC-PWM schemes are briefly analyzed.

In Figure 1 the 3P-5L CHBMI circuit diagram is presented. Each phase of 3P-5L CHBMI is composed of two series-connected traditional single-phase H-Bridge. This converter topology is characterized by a modular structure which allows easy maintenance in case of switching devices fault, redundancy of states which leads to high reliability, and a reduced number of circuital passive components in comparison to other MI topologies; it requires isolated DC sources per each H-Bridge.

Gate control signals are generated through the comparison of modulating signals and carrier triangular signals. In detail, concerning traditional PWM strategies, the number of modulating signals depends on the number of phases, and the number of carriers n_c depends on the number of MI voltage levels per each phase, according to relation (1):

$$n_c = n_l - 1 \tag{1}$$

where n_l is the number of available voltage levels per phase, which depends on the converter topology. Thus, for a five-level converter, four carrier signals are required.

MC-PWM strategies are classified as Level Shifted (LS) and Phase Shifted (PS). About LS-PWM, carriers are characterized by the same peak-to-peak amplitude, a mutual amplitude shift such that no carrier's superpositions appear, and a mutual phase shift. Depending on the mutual phase shift, LS-PWM can be classified as:

- Phase Disposition (PD): all carriers are in phase;
- Phase Opposition Disposition (POD): carriers are in phase two-by-two;
- Alternative Phase Opposition Disposition (APOD): adjacent carriers are in phase opposition.

When CHBMI is controlled by LS-PWM strategies, output voltage harmonics are centered around the switching frequency and its multiples. Moreover, each H-Bridge leads a different active power than the other bridges in the same phase, depending on the assigned carriers of each H-Bridge and depending on the amplitude modulation index. As a way of example, when the amplitude modulation index is less than 0.5, the H-Bridge controlled by an external couple of carriers does not switch at all.

About PS-PWM, carriers are characterized by the same peak-to-peak amplitude, the same average value, equal to zero, and a mutual phase shift that depends on the relation (2):

$$\varphi_i = \frac{(i-1)\cdot 180}{N} \tag{2}$$

where i is the i^{st} H-Bridge per phase considered, and N is the number of series connected H-Bridge per phase. When CHBMI is controlled by PS-PWM strategy, each H-Bridge is controlled with a classical Unipolar PWM strategy, in this way all the H-Bridges on the same phase lead the same active power independently by the amplitude modulation index, allowing a uniform utilization of each converter. Output voltage harmonics are centered around multiples of switching frequency, according to relation (3).

$$f_h = (n_l - 1)\cdot f_{sw} \tag{3}$$

where f_{sw} is the switching frequency. The quantity f_h is called virtual switching frequency. In a 3P-5L CHBMI, harmonics are centered around $4f_{sw}$ and its multiples. A high virtual switching frequency allows an easy filtration of current harmonics, but at the same time, higher switching losses occur.

According to [38] and [40], a hybrid modulation strategy, called Suppressed Carrier Arrangement Modulation

TABLE 1. List of important abbreviations used throughout the paper in alphabetical order.

Abbreviation	Definition	Abbreviation	Definition
APOD	Alternative Phase Opposition Disposition	PHD	Partial Harmonic Distortion
CHBMI	Cascaded H-Bridge Multilevel Inverter	POD	Phase Opposition Disposition
DPF	Displacement Power Factor	PS	Phase Shifted
DSP	Digital Signal Processor	PV	Photo-Voltaic
DT	Dead Time	PWM	Pulse Width Modulation
DVR	Dynamic Voltage Restorer	S	Sinusoidal
EMI	Electro Magnetic Interference	SCAMOD	Suppressed Carrier Arrangement Modulation
FACTS	Flexible AC Transmission Systems	SFO	Switching Frequency Optimal
FPGA	Field Programmable Gate Array	SOH	State of Health
GUI	Graphical User Interface	SOM	System on Module
LF	Low Frequency	STATCOM	Static Compensator
MC	Multicarrier	SV	Space Vector
MI	Multilevel Inverters	THD	Total Harmonic Distortion
MPPT	Maximum Power Point Tracking	THD_{LF}	Low-Frequency Total Harmonic Distortion
NPCMI	Neutral Point Clamped Multilevel Inverter	UPFC	Unified Power Flow Controller
PD	Phase Disposition	VSI	Voltage Source Inverter

(SCAMOD) is considered. In this application, SCAMOD is arranged with the same number of carriers than the previously analyzed modulation schemes. It consists of couples of carriers characterized by the same average value, equal peak-to-peak amplitude, and a mutual phase shift equal to 180°. When CHBMI is controlled by the SCAMOD strategy, all the H-Bridges on the same phase lead the same active power independently by the amplitude modulation index, allowing a uniform utilization of each converter. Output voltage harmonics are centered around multiples of switching frequency, according to relation (4):

$$f_h = \frac{(n_l - 1) \cdot f_{sw}}{2} \tag{4}$$

In this case, the virtual switching frequency is half the PS virtual switching frequency. In a 3P-5L CHBMI, harmonics are centered around $2f_{sw}$ and its multiples. It represents a compromise between harmonic content and switching losses.

About modulating signals, in a generical three-phase system, three sinusoidal modulating signals are employed for gate signals generation, since they guarantee the lower output voltage harmonic content. In order to extend the inverter linear operating range, modulating signals can be modified by introducing an offset signal v_{offset}, defined as:

$$v_{offset} = \frac{\max(v_a, v_b, v_c) + \min(v_a, v_b, v_c)}{2} \tag{5}$$

where v_a, v_b, v_c are the sinusoidal modulating signals. In this way, Switching Frequency Optimal (SFO) modulating signals v_a^*, v_b^*, v_c^* can be obtained by combining the offset signal and each sinusoidal modulating signal as follow:

$$\begin{cases} v_a^* = v_a - v_{offset} \\ v_b^* = v_b - v_{offset} \\ v_c^* = v_c - v_{offset} \end{cases} \tag{6}$$

It should be noted that the SFO-based PWM schemes allow obtaining similar performance of Space Vector (SV) PWM modulation, in terms of harmonic content, as described in [41].

Combining the previously defined carrier and modulating signal arrangements, the ten MC-PWM schemes presented in Figure 2 are obtained.

III. DEAD TIME VOLTAGE DROP: MATHEMATICAL FORMULATION FOR CHBMI

As previously described, the aim of this work is to investigate the DT effects on CHBMI performance. In detail, in this section, the DT impact on the output voltage fundamental harmonic is considered; the goal is to analytically estimate the fundamental harmonic voltage drop ΔV due to the DT effects, for a generic n_l-level CHBMI, taking into account the adopted MC-PWM strategy. In order to carry out the voltage drop mathematical formulation, the CHBMI is treated as the composition of several elementary converter cells, known as Half-Bridge converters, whose schematic is shown in Figure 3 (a). The H-Bridge converter legs (called X-leg and Y-leg) can be treated as two independently controlled paralleled Half Bridges. The Half bridge is controlled by a traditional PWM modulation scheme. In detail, Figure 3(b) shows one period of the triangular carrier signal and one sample of the modulating signal u (black horizontal line). In order to introduce a DT, the ideal modulating signal is split into two signals $u+k$ (blue horizontal line) and $u-k$ (red

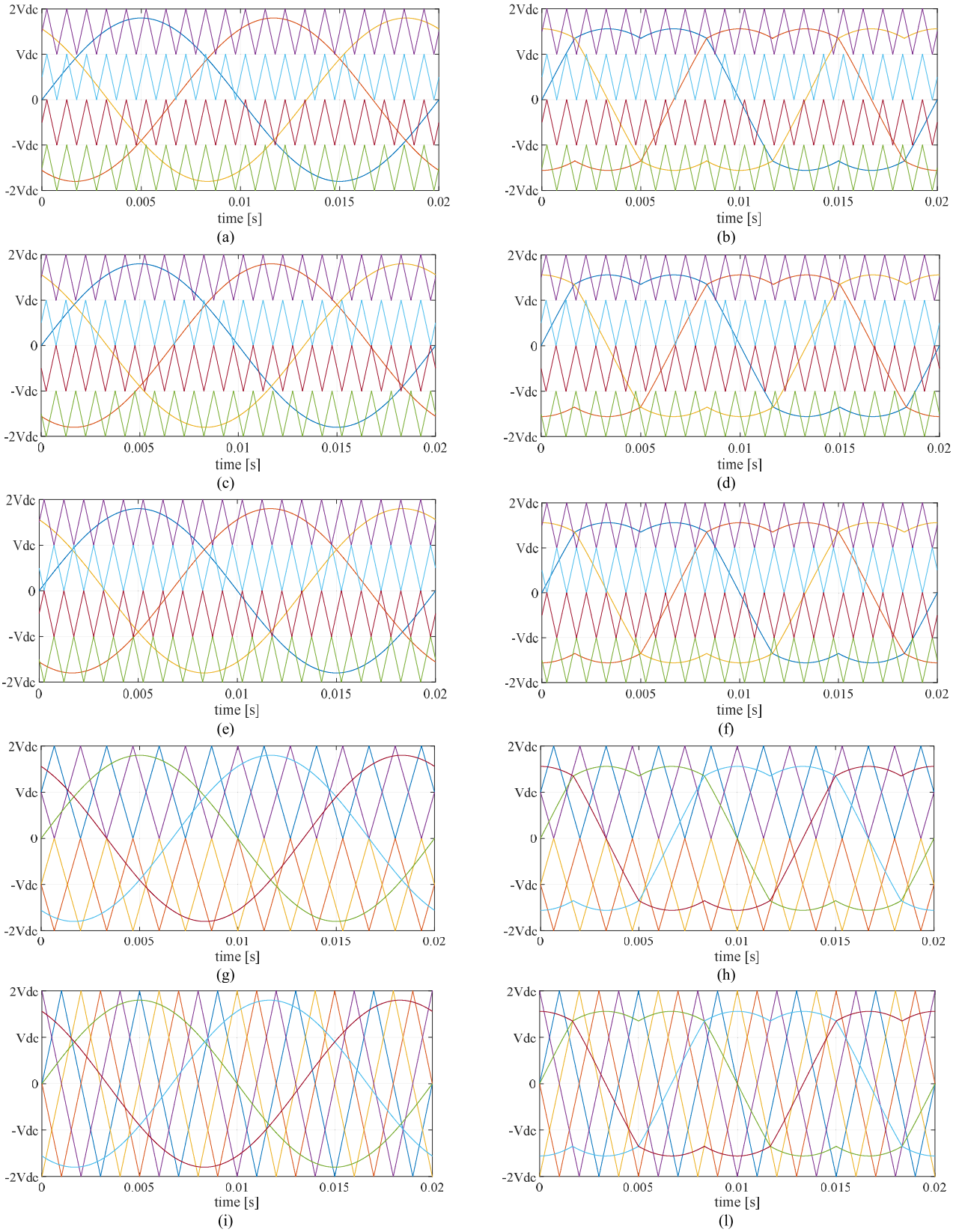

FIGURE 2. Magnetization as a Carrier patterns: (a) Sine Phase Disposition – SPD; (b) SFO Phase Disposition – SFOPD; (c) Sine Phase Opposition Dis-position – SPOD; (d) SFO Phase Opposition Disposition – SFOPOD; (e) Sine Alternative Phase Opposition Disposition – SAPOD; (f) SFO Alternative Phase Opposition Disposition – SFOPOD; (g) Sine Phase Shifted – SPS; (h) SFO Phase Shift-ed – SFOPS; (i) Sine Suppressed Carrier Arrangement – SSCA; (l) SFO Suppressed Carrier Arrangement – SFOSCA.

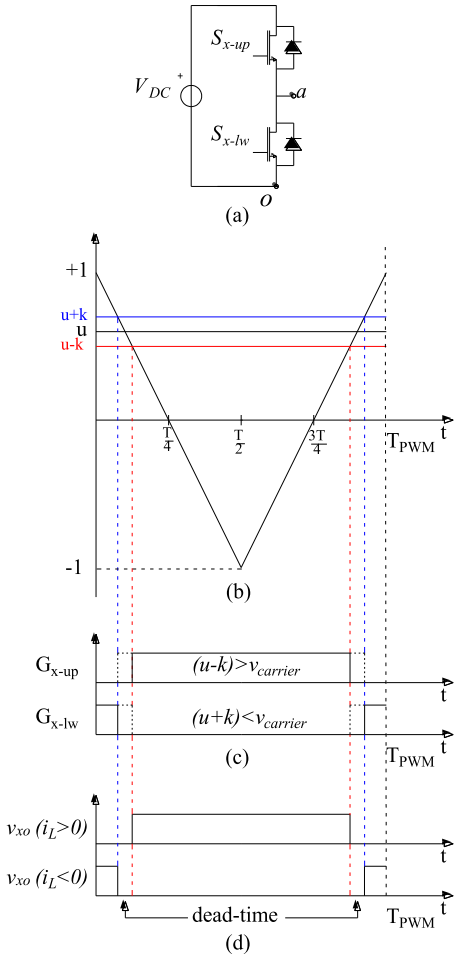

FIGURE 3. (a) Half-Bridge module; (b) PWM control scheme, composed of one period of the carrier signals, ideal modulating sample u (black) and real modulating samples $u+k$ and $u-k$, split due to the dead time; (c) gate command G_{x-up} and G_{x-lw} in the ideal case (dash line) and real case (continuous) when dead-time is applied; (d) half-bridge output voltage v_{xo} when the load current i_L is positive and negative.

horizontal line), where k is a dead time factor defined as in [39]; the split modulating signals u-k and u+k are assigned to the upper and lower devices of each Half Bridge, respectively. Through the modulating and carriers signals comparison, the Half Bridge gate control signals G_{x-up} and G_{x-lw}, reported in figure 3(c), are generated. In detail, the ideal control signals (with DT = 0) are identified with a dashed line, and the real control signals are identified by the continuous line. DT leads to an output voltage width variation, with respect to the ideal case, which depends on the current sign. In detail, in each switching period T_{sw}, the Half-Bridge output voltage impulse v_{xo}, with respect to the theoretical case, is larger when the current is negative and it is shorter when the current is positive, as shown in Figure 3(d). This behaviour depends on whether the diodes are involved in the current circulation path.

According to [20], neglecting the devices turn-on and turn-off times, the mean voltage drop ΔV on a switching period T_{sw} can be expressed as follow:

$$\Delta V(t) = \begin{cases} -\dfrac{t_{dt}}{T_{sw}} V_{DC}, & i_{inv}(t) > 0 \\ +\dfrac{t_{dt}}{T_{sw}} V_{DC}, & i_{inv}(t) < 0 \end{cases} = -\,|\Delta V| \cdot \mathrm{sign}[i_L(t)] \tag{7}$$

where t_{dt} is the dead-time, i_L is the load current, V_{DC} is the DC-link voltage, and $|\Delta V|$ is the voltage drop module, which can also be expressed as:

$$|\Delta V| = \frac{t_{dt}}{T_{sw}} V_{DC} = t_{dt} f_{sw} V_{DC}. \tag{8}$$

Considering the fundamental harmonic $v^1_{xo}(t)$, due to the DT effects, it is modified as:

$$v^1_{xo}(t) = v^1_{xo,id}(t) - |\Delta V| \cdot \mathrm{sign}(i_L) \tag{9}$$

where $v^1_{xo,id}(t)$ is the output voltage fundamental harmonic in the ideal case with no DT applied. According to equation (9), the output voltage fundamental harmonic is distorted by the superposition of a square wave, whose amplitude depends on the DC link voltage, on the chosen DT and the switching frequency, and whose sign depends on the current sign and consequently on the power factor. When the current is positive, the fundamental harmonic is decreased, when negative, increased.

Considering the H-Bridge converter, it is composed of two legs (named X-leg and Y-leg) which correspond to two Half-Bridges. Each leg can be independently controlled by the assignment of independent carrier signals. In this case, the adopted PWM strategy is the traditional Unipolar PWM strategy, whose modulation scheme and gate signals in a switching period T_{sw} are shown in Figure 4.

The H-Bridge output voltage v_{xy}(t) can be expressed as:

$$v_{xy}(t) = v_{xo}(t) - v_{yo}(t). \tag{10}$$

In order to evaluate the DT effects on the H-Bridge output voltage fundamental harmonic v^1_{xy}, combining equations (9) and (10), v^1_{xy} can be expressed as:

$$v^1_{xy}(t) = v^1_{xy,id}(t) - 2\,|\Delta V| \cdot \mathrm{sign}(i_L) \tag{11}$$

where $v^1_{ab,id}$(t) is the output voltage fundamental harmonic in the ideal case with no DT applied. With respect to Figure 4, in a switching period T_{sw}, each leg changes state once, moreover, this behavior does not change if the converter works in the linear region. Now, phase a of the 3P-5L CHBMI, whose schematic is reported in Figure 1, is considered. The phase voltage v_{aN}(t) with respect to the neutral point N can be expressed as:

$$v_{aN}(t) = v_{xy,HB1}(t) + v_{xy,HB2}(t) \tag{12}$$

where $v_{xy,HB1}$(t) and $v_{xy,HB2}$(t) are the output voltage of the two cascaded H-Bridges, respectively. Each H-Bridge per phase is powered by the voltage source E. The CHBMI total DC-link voltage V_{DC} can be expressed as the sum of each

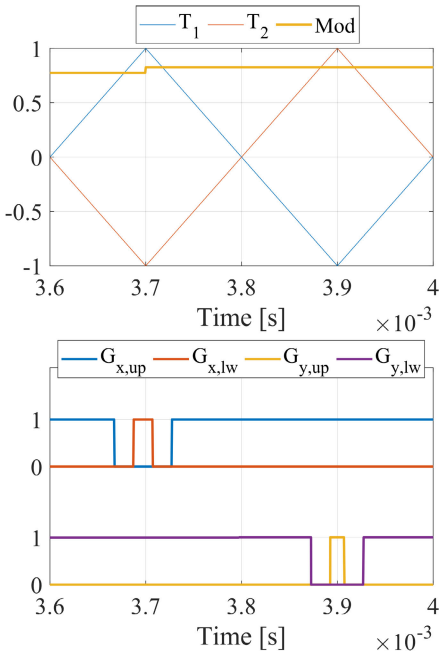

FIGURE 4. Traditional Unipolar PWM modulation strategy for single-phase H-Bridge and gate signals in a switching period T_{sw}.

H-Bridge DC-link voltage source E, applied at each series-connected H-Bridge, according to the following relation:

$$V_{DC} = \sum_{k=1}^{N} E_i = NE \tag{13}$$

which is valid for Symmetric CHBMI topology. The voltage drop module $|\Delta V|_{HBk}$ on one leg of the *k-th* cascaded H-Bridge in a phase can be expressed as:

$$|\Delta V|_{HBk} = t_{dt} f_{sw} E. \tag{14}$$

Considering the output voltage fundamental harmonic $v^1_{aN}(t)$, combining equations (11) and (12), v^1_{aN}(t) can be expressed as:

$$v^1_{aN}(t) = v^1_{aN,id}(t) - 4\,|\Delta V|_{HBk} \cdot \text{sign}(i_L) \tag{15}$$

where $v^1_{aN,id}$(t) is the output voltage fundamental harmonic in the ideal case with no DT applied. For a generic n_l-level CHBMI, relations (12) and (13) can be generalized as:

$$v_{aN}(t) = \sum_{k=1}^{N} v_{xy,HBk}(t) \tag{16}$$

$$v^1_{aN}(t) = v^1_{aN,id}(t) - 2N\,|\Delta V|_{HBk} \cdot \text{sign}(i_L) \tag{17}$$

where N is the number of cascaded H-Bridges converters per phase. Replacing the relation (14) in (17) and considering relation (13):

$$v^1_{aN}(t) = v^1_{aN,id}(t) - 2 \cdot t_{dt} f_{sw} V_{dc} \cdot \text{sign}(i_L). \tag{18}$$

The second term in equation (18) represents the total voltage drop due to the dead time on the phase voltage. It can be noted that the voltage drop in relation (18) coincides with the voltage drop in equation (11). It means that, for fixed dead time t_{dt}, fixed switching frequency f_{sw} and fixed total DC link voltage V_{DC}, the total voltage drop module on CHBMI phase voltage is the same of the traditional single-phase H-Bridge. This result can be explained as follow: although CHBMI is characterized by a higher number of commutations in the considered T_{sw}, each of them causes a little voltage drop since each H-Bridge is powered by a fraction of the total DC link voltage V_{DC}. It must be underlined that relation (18) is valid only if each cascaded H-Bridge per phase (and so each Half Bridge) has the same behaviour in terms of commutations number per T_{sw}. In this context, the adopted MC-PWM strategy plays a key role, thus it must be considered. In Figure 5 carriers, modulating signals and gate control signals of one phase of 3P-5L CHBMI in a T_{sw} are represented. It can be noted that, when PS PWM is adopted, each H-Bridge on a phase is controlled as a traditional Unipolar PWM-controlled single-phase H-Bridge (HB), so the relation (18) is valid. Taking into account a PD-PWM strategy, according to the generated gate signals in a T_{sw} reported in Figure 5, only one Half-Bridge per T_{sw} changes its state, which means that Half Bridge modules are not working in the same way in the considered T_{sw}, and so relation (18) must be modified.

For a generic n_l-level CHBMI, when PD-PWM is adopted, only one Half-Bridge per phase changes its state in a T_{sw}, this means that $2N$ fewer commutations occur in the considered period, thus, taking into account relations (13) and (14), equation (18) must be modified as follow:

$$\begin{aligned} v^1_{aN}(t) &= v^1_{aN,id}(t) - \frac{1}{2N} 2 \cdot t_{dt} f_{sw} V_{dc} \cdot \text{sign}[i_L(t)] \\ &= v^1_{aN,id}(t) - t_{dt} f_{sw} E \cdot \text{sign}[i_L(t)]. \end{aligned} \tag{19}$$

In this case, the voltage drop due to DT is independent of the number of series connected H-Bridges, since only one Half-bridge is switching per T_{sw}. According to (19), when LS-PWM is adopted, the voltage drop is $2N$-times lower than the voltage drop with the PS-PWM strategy. Such considerations are also valid for other LS-PWM strategies (POD, APOD) since the mutual carriers phase shift does not have such influence on the number of commutations per T_{sw}.

When SCAMOD is adopted, according to Figure 5, two commutations per T_{sw} occur. This behaviour is independent of the number of cascaded H-Bridges per phase since the modulating signal can intercept only two of n_l-1 carriers signals, thus only two half bridges are switching. Taking into account such considerations, relation (18) must be modified as:

$$\begin{aligned} v^1_{aN}(t) &= v^1_{aN,id}(t) - \frac{1}{N} 2 \cdot t_{dt} f_{sw} V_{dc} \cdot \text{sign}[i_L(t)] \\ &= v^1_{aN,id}(t) - 2 \cdot t_{dt} f_{sw} E \cdot \text{sign}[i_L(t)] \end{aligned} \tag{20}$$

According to (20), when SCAMOD is adopted, the voltage drop is N-times lower than the voltage drop with the PS-PWM strategy.

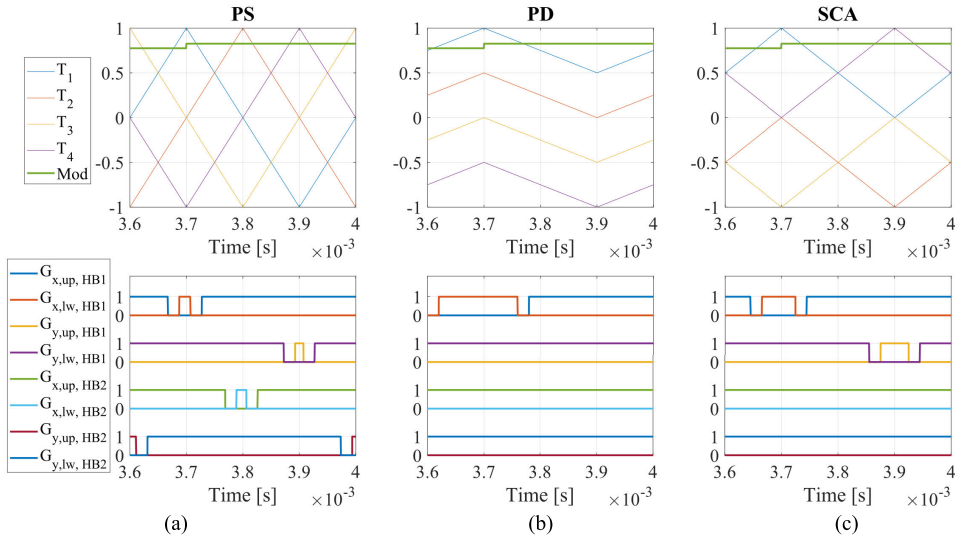

FIGURE 5. (a) MC-PWM control schemes, and gate control signals of one phase of 3P-5L CHBMI in one T_{sw}, $m_a = 0.9$: (a) Phase Shifted (b) Phase Disposition, (c) SCA-PWM.

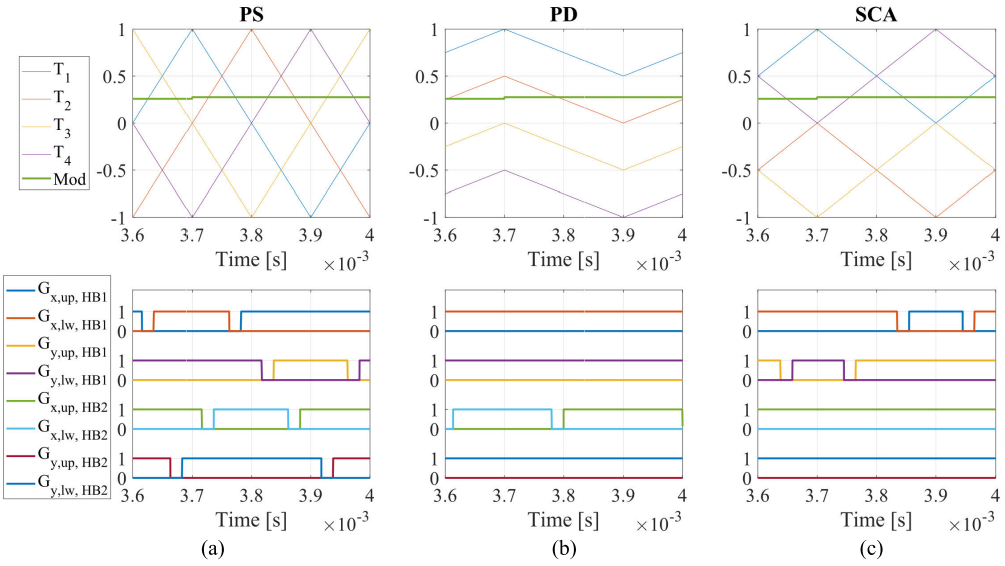

FIGURE 6. (a) MC-PWM control schemes, and gate control signals of one phase of 3P-5L CHBMI in one T_{sw}, $m_a = 0.3$: (a) Phase Shifted (b) Phase Disposition, (c) SCA-PWM.

Unless the converter works in the linear region, all the previous considerations are independent by the amplitude modulation index m_a, as can be noted in Figure 6, where carriers, modulating signals, and gate control signals of one phase of 3P-5L CHBMI in a T_{sw} are represented for $m_a = 0.3$.

In conclusion, according to equations (18), (19) and (20), the phase voltage drop $|\Delta V|_{MC}(t)$ and the CHBMI phase output voltage $v^1_{aN}(t)$ for the considered MC-PWM strategies can be expressed as follow:

$$\Delta V_{MC}(t) = C_{MC} \cdot t_{dt} f_{sw} E \cdot \text{sign}[i_L(t)] \tag{21}$$

$$v^1_{aN}(t) = v^1_{aN,id}(t) - \Delta V_{MC}(t) \tag{22}$$

where C_{MC} is a constant parameter which allows considering the adopted MC-PWM strategy; in detail, $C_{MC} = 1$ when LS-PWM is adopted, $C_{MC} = 2$ when SCA-PWM is adopted, and $C_{MC} = 2N$ when PS-PWM is adopted. In detail, for 3P-5L CHBMI, $C_{MC} = 4$ when PS-PWM is adopted.

Looking at equation (22), it can be noted that the term $|\Delta V|_{MC}(t)$ causes a distortion of the fundamental harmonic $v_{aN1}(t)$; for this reason, to analyze only the effect on the fundamental harmonic, the voltage drop fundamental harmonics $|\Delta V|_{1x}$ must be considered. Moreover, with respect to the test bench, which will be introduced in the next section, each output phase voltage is measured with respect to the neutral star load point n, because it represents the load phase voltage.

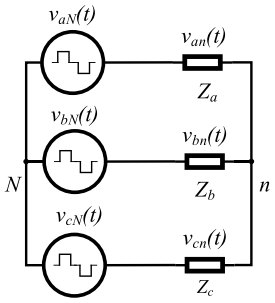

FIGURE 7. Electrical scheme of CHBMI and three-phase load.

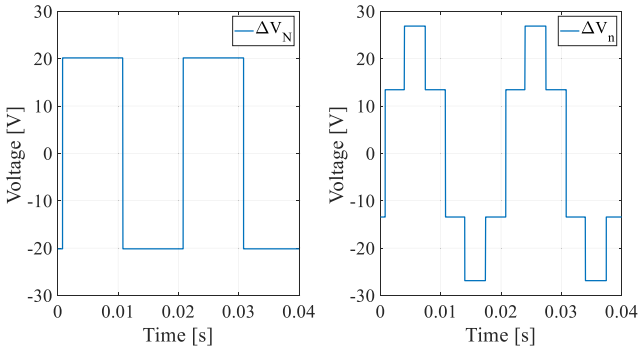

FIGURE 8. Voltage drop $|\Delta V|_{MC,N}(t)$ and $|\Delta V|_{MC,n}(t)$ with PS-PWM modulation strategy, switching frequency $f_{sw} = 70$ kHz, DT $= 1.5\ \mu$s.

Therefore, it is necessary to find an equation equivalent to the (22) but related to the three-phase load neutral point n.

With respect to the schematic in Figure 7, which represent the CHBMI with a symmetrical three-phase passive load, it is possible to link the three output-phase voltage, $v_{aN}(t)$, $v_{bN}(t)$, and $v_{cN}(t)$ with the load phase voltage $v_{an}(t)$, $v_{bn}(t)$, and $v_{cn}(t)$ according to equation (23):

$$\begin{cases} v_{an}(t) = v_{aN}(t) - v_{nN}(t) \\ v_{bn}(t) = v_{bN}(t) - v_{nN}(t) \\ v_{cn}(t) = v_{cN}(t) - v_{nN}(t) \end{cases} \tag{23}$$

where $v_{nN}(t)$ represents the voltage between the converter neutral point N and the three-phase load neutral point n.

Adding member to member equations in (23), since $v_{aN}(t) + v_{bN}(t) + v_{cN}(t) = 0$, the relation (24), which links $v_{nN}(t)$ with the three output phase voltage, $v_{aN}(t)$, $v_{bN}(t)$, and $v_{cN}(t)$, is obtained:

$$v_{nN}(t) = \frac{v_{aN}(t) + v_{bN}(t) + v_{cN}(t)}{3}. \tag{24}$$

By replacing equation (24) in (23), and sorting equations into matrices:

$$\begin{bmatrix} v_{an}(t) \\ v_{bn}(t) \\ v_{cn}(t) \end{bmatrix} = \frac{1}{3} \begin{bmatrix} 2 & -1 & -1 \\ -1 & 2 & -1 \\ -1 & -1 & 2 \end{bmatrix} \begin{bmatrix} v_{aN}(t) \\ v_{bN}(t) \\ v_{cN}(t) \end{bmatrix} \tag{25}$$

In a compact form, equation (25) becomes:

$$[v_n(t)] = [T]\,[v_N(t)] \tag{26}$$

where $[v_n(t)]$ is the load voltages column vector, $[T]$ is the link matrix, and $[v_N(t)]$ is the converter phase voltage column vector. The load voltages fundamental harmonics are now considered by taking into account equation (22):

$$\begin{aligned} \left[v_n^1(t)\right] &= \left[v_{n,id}^1(t)\right] - \left[\Delta V_{MC,n}(t)\right] \\ &= [T]\left[v_{N,id}^1(t)\right] - [T]\,[\Delta V_{MC}(t)] \end{aligned} \tag{27}$$

where $[v_n^1(t)]$ is the column vector of the load voltages fundamental harmonics, $[v_N^1(t)]$ is the converter phase voltage fundamental harmonics column vector, and $[\Delta V_{MC,n}(t)]$ is the voltage drop on the load phase voltage, which can be expressed as follow, according to equations (21) and (27) as:

$$\begin{cases} \Delta V_{MC,an}(t) \\ \quad = C_{MC} \cdot t_{dt} f_{sw} E \\ \quad \dfrac{2 \cdot \mathrm{sign}[i_a(t)] - \mathrm{sign}[i_b(t)] - \mathrm{sign}[i_c(t)]}{3} \\ \Delta V_{MC,bn}(t) \\ \quad = C_{MC} \cdot t_{dt} f_{sw} E \\ \quad \dfrac{-\mathrm{sign}[i_a(t)] + 2 \cdot \mathrm{sign}[i_b(t)] - \mathrm{sign}[i_c(t)]}{3} \\ \Delta V_{MC,cn}(t) \\ \quad = C_{MC} \cdot t_{dt} f_{sw} E \\ \quad \dfrac{-\mathrm{sign}[i_a(t)] - \mathrm{sign}[i_b(t)] + 2 \cdot \mathrm{sign}[i_c(t)]}{3} \end{cases} \tag{28}$$

As previously discussed, $|\Delta V|_{MC}(t)$ causes a distortion of the fundamental harmonic $v_{aN}^1(t)$; similarly, $|\Delta V|_{MC,n}(t)$ causes a distortion of the fundamental harmonic $v_{an}^1(t)$; for this reason, in order to detect the DT effects on the fundamental harmonic of acquired signals, the voltage drop $|\Delta V|_{1x,n}$ has been considered. Since the CHBMI output voltages system is symmetrical and the load is balanced, the voltage drop fundamental harmonics represent symmetric and direct tern too. As a way of example, with respect to phase a, the theoretical voltage drop $|\Delta V|_{MC,N}(t)$ and $|\Delta V|_{MC,n}(t)$ with PS-PWM modulation strategy, switching frequency $f_{sw} = 70$ kHz, DT $= 1.5\ \mu$s are reported in Figure 8.

Both waveforms are characterized by an odd and quarter-wave symmetry. Therefore, the even-order harmonics are absent, while the odd-order harmonics have the following amplitudes:

$$\begin{aligned} &\Delta V_{hx,t,N} \\ &\quad = \frac{4}{\pi} \left|\Delta V_{1,MC,N}\right| \int_0^{\pi/2} \sin(h\omega t) d(\omega t) \\ &\quad = \frac{4\left|\Delta V_{1,MC,N}\right|}{h\pi} \\ &\Delta V_{hx,t,n} \\ &\quad = \frac{4}{\pi} \frac{2\left|\Delta V_{1,MC,N}\right|}{3} \end{aligned} \tag{29}$$

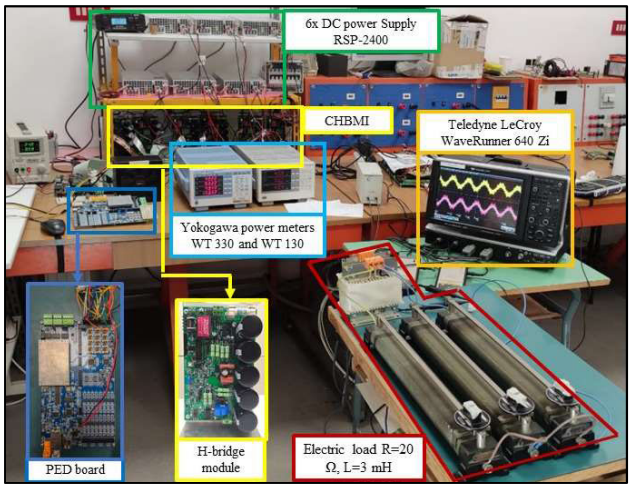

FIGURE 9. Test rig.

$$\cdot \left\{ \int_0^{\pi/3} \sin(h\omega t) d(\omega t) + 2 \int_{\pi/3}^{\pi/2} \sin(h\omega t) d(\omega t) \right\}$$
$$= \frac{8 \left| \Delta V_{1,MC,N} \right|}{3h\pi} \left[1 + \cos\left(h \frac{\pi}{3} \right) \right] \quad (30)$$

where h is the harmonic order ($h = 1, 3, 5\ldots$). With respect to the fundamental harmonic, it results:

$$\Delta V_{1x,t,N} = \Delta V_{1x,t,n} = \frac{4 \left| \Delta V_{1,MC,N} \right|}{\pi} \quad (31)$$

Looking at equation (31), it results that voltage drop fundamental harmonics $|\Delta V|_{1x,t,N}$ and $|\Delta V|_{1x,t,n}$ are characterized by the same amplitude. This result confirms that is possible to use equations (21) and (22) also on voltages measured with respect to the point n.

IV. TEST RIG

For experimental investigation purposes, a test rig, shown in Figure 9, has been assembled at SDESLab of the University of Palermo. It is composed by:

- a three-phase five-level CHBMI MOSFET-based inverter prototype composed of six 5 kW H-bridges whose main nameplate data are reported in Table II;
- six programmable DC power supplies RSP-2400 with rated DC voltage equal to 48 V, whose nameplate data are reported in Table III;
- a control board, commercially named PED-board, equipped with System on Module (SOM) sbRIO 9651 composed of an ARM Cortex-A9 processor and an Artix-7 FPGA unit, whose main features are reported in [23] and summarized in Tables IV and V;
- three constantan rheostats and a three-phase inductive load series connected with resistance and inductance equal to 20 Ω and 3 mH, respectively;
- a Teledyne LeCroy WaveRunner Oscilloscope 640Zi, whose main data are reported in table VI; it is equipped with two Yokogawa 700924 differential voltage probes and two Yokogawa 701933 current probes, whose main data are summarized in Tables VII and VIII, respectively;
- two Yokogawa power meters (WT 330 and WT 130), whose technical data are reported in Table IX.

TABLE 2. CHBMI MOSFET IRFB4115PBF technical data.

Symbol	Quantity	Value
V_{dss}	Voltage	150 V
R_{dSon}	Resistance	9.3 mΩ
I_D	Current	104 A
T_{Don}	Turn on delay	18 ns
T_R	Rise time	73 ns
T_{Doff}	Turn off delay	41 ns
T_F	Fall time	39 ns
T_{RR}	Reversal Recovery	86 ns

TABLE 3. DC power supply RSP- 2400 technical data.

Symbol	Quantity	Value
V_{out}	Rated output voltage	48 V
I_{out}	Rated output current	50 A
P_N	Rated power	2400 W
ΔV	Ripple	200 $mV_{p\text{-}p}$
V_{in}	Input voltage range	180 ~ 264 VAC
$cos\varphi$	Power factor	0.95
η	Efficiency	91.5 %
I_{in}	Input current	12 A/230 Vac

In order to accurately evaluate the DT impact on CHBMI performance in terms of electric quantities harmonic contents and CHBMI efficiency, particular attention was paid to instruments choice and their acquiring features. For this purpose, the experimental investigations have been carried out by acquiring both input and output electrical quantities of CHBMI with a fixed R-L load value that results in a fixed value of displacement power factor (DPF) by varying modulation strategies and its parameters such as modulation index value and dead time value. Since the input CHBMI electrical quantities present continuous waveforms with negligible harmonic content, the input CHBMI power is measured by two conventional power analyzers (Yokogawa WT 330 and WT 130) with a sampling frequency equal to 100 kS/s. Whereas, since the CHBMI output electrical quantities present a larger harmonic continent, the CHBMI output quantities are acquired and analyzed by a Teledyne LeCroy WaveRunner Oscilloscope 640Zi equipped with Yokogawa 701933 current and Yokogawa 700924 voltage probes.

For accurate CHBMI output power detection, a sampling frequency and time window equal to 10 MS/s and 1 s have been chosen, respectively. This measurement setup ensures an accurate analysis of CHBMI electrical quantities in the frequency domain, with a resolution of 1 Hz, and accurate detection of CHBMI active power quantities. Discussed modulation strategies are implemented on sbRIO 9651 System on Module controller. It consists of an FPGA unit, which is

TABLE 4. SoM sbRIO 9651 technical data.

Quantity	Value
Type	Xilinx Zynq-7000 SoC
Architecture	ARM Cortex A-9
Speed	667 MHz
Cores	2
Logic Cells	85000
Flip-flops	106400
LUTs	53200
DSP slices	220

TABLE 5. PED board technical data.

Hardware	Features
PWM Channels	30x, 0-5V or 0-15 V selectable voltage
14 bit-ADC,	2x8 Channels, Simultaneous Sampling up to 600 kS/s, -5 - +5V or 0-10V
10 bit- ADC,	1x8 Channels, Up to 200 kS/s, 0-5 V inputs
12 bit-DAC,	1x4 Channels, 10 µs settling time
Digital I/O	46x3.3V standard
Ethernet	1x RS485

TABLE 6. Teledyne LeCroy WaveRunner 640Zi technical data.

Quantity	Value
Analog Bandwidth	4 GHz @ 50 Ω, 500 MHz @ 1MΩ
Maximum sampling rate	40 GS/s
Input Channels	4
Vertical Resolution	8-bits; up to 11-bits with enhanced resolution (ERES)
Sensitivity	50 Ω: 1 mV/div–1 V/div, fully variable 1 MΩ: 1 mV/div–10 V/div, fully variable

TABLE 7. Yokogawa 700924 voltage probes technical data.

Quantity	Value
Frequency bandwidth	DC to 100 MHz (-3dB)
Input type	Balancing difference input
Attenuation ratio	Switched ratios of 100:1 and 1000:1
Input resistance/capacity	4 MΩ/10 pF each side to ground
Differential allowable voltage (between + and – terminals)	±350 V (DC +ACpeak) or 250 Vrms at 100:1 attenuation
Max CMV	±1400 V (DC +ACpeak) or 1000 Vrms
Max input voltage	±1400 V (DC +ACpeak) or 1000 Vrms
CMRR (typical)	60 Hz: less than −80 dB; 1 MHz: less than −50 dB
Output voltage	±3.5 V (DC + ACpeak) (R_{in}=50 kΩ or higher)

TABLE 8. Yokogawa 701933 current probes technical data.

Quantity	Value
Frequency bandwidth	DC to 50 MHz (-3dB)
Maximum continuous input range	30 Arms
Maximum peak current value	50 Apeak (discontinuous)
Output voltage rate	0.1 V/A
Amplitude accuracy	0 to 30 Arms: ±1% of rdg ±1 mV To 50 Apeak: ±2% of rdg (DC, and 45 to 66 Hz)
Noise	Equivalent to 2.5 mArms or less (for 20 MHz band measuring instrument)

TABLE 9. Yokogawa WT 330 & WT 130 power meters technical data.

Quantity	WT 330	WT 130
Instantaneous maximum allowable input voltage (1 s)	Peak value of 2kV or RMS value of 1.5kV, whichever is less	Peak value of 2kV or RMS value of 1.5kV, whichever is less
Instantaneous maximum allowable input current (1 s)	Peak value of 150A or RMS value of 40A, whichever is less.	Peak value of 150A or RMS value of 40A, whichever is less.
Continuous maximum allowable input voltage	Peak value of 1.5kV or RMS value of 1kV, whichever is less.	Peak value of 1.5kV or RMS value of 1kV, whichever is less.
Continuous maximum allowable input current	Peak value of 100A or RMS value of 30A, whichever is less.	Peak value of 100A or RMS value of 30A, whichever is less.
A/D conv resolution	16 bits	12 bits
Maximum conversion rate	10 µs	22 µs
Bandwidth	Up to 100 kHz	Up to 50 kHz
Accuracy	±(0.1% of reading +0.2% of range)	±(0.2% of reading +0.2% of range)

used for high-frequency time-critical control operations, and a DSP, where non-time-critical operations are implemented. Both units can be independently programmed in the LabVIEW environment with graphical language, which allows an easy implementation for rapid prototyping system purposes. The algorithm structure has been deeply described in [23], here it is briefly summarized. On the FPGA module, time-critical operations, such as carriers and modulating signals generation and comparison, and PWM gate signals generation, are implemented. The FPGA algorithm is split into a high-frequency loop and a low-frequency loop. With respect to the first loop, carriers are generated by four up-down counters, which main parameters such as starting point, counting direction and maximum and minimum counting values can be varied according to the adopted MC-PWM strategy and switching frequency. With respect to the second, modulating signals are generated by acceding to a pre-allocated memory, which consists in a period of a sinusoidal signal. The access to the memory is managed by three reset counters (one per phase), whose output represents the addresses to elements of the memory. If SFO modulating signals are adopted, modulating signals are combined according to equations (5) and (6). These operations must require an execution time lower than a T_{sw} period.

On the Real-Time module, ancillary operations, such as counters parameters calculation, dead-time to dead-ticks conversion, and Graphical user interface (GUI) management are implemented. In detail, the GUI allows monitoring carriers and modulating signals, modifying switching frequency and dead time. Computational costs are widely discussed in [23].

V. EXPERIMENTAL RESULTS

As described above, this work aims to investigate the DT impacts on CHBMI performance through an experimental approach. Thus, in this section experimental results are reported and discussed. In detail, the DT impacts on the voltage drop on fundamental amplitude, global harmonic distortion, low-frequency analysis, and conversion efficiency have been investigated. Several tests have been conducted as a function of DT value. In detail, DT is varied in the range 0.5 -1.5 μs, with a step of 0.5 μs; the minimum dead time value is chosen according to MOSFETs turn-on and turn-off times. In each test, the 3P-5L CHBMI has been controlled with each of the ten previously described MC-PWM strategies and the switching frequency f_{sw} has been varied in the range 10-70 kHz with a step of 10 kHz. For fixed switching frequency, tests are carried out for four amplitude modulation index values, 0.3, 0.6, 0.9 and 1.15. Per each test, phase output voltage waveforms and phase currents are measured, according to the scheme discussed in the previous section. The acquired electrical quantities are post-processed in the MATLAB environment. In the following subsections, all experimental results and relative considerations have been reported.

A. VOLTAGE DROP ON FUNDAMENTAL AMPLITUDE

In this subsection, the DT effect on the fundamental amplitude in terms of the voltage drop is analyzed. In detail, the goal is to validate the voltage drop mathematical formulation discussed in section III. Several analyses are carried out on measured voltage and current signals in the MATLAB environment.

The first analysis consists in the comparison between the theoretical voltage drop first harmonic $|\Delta V|_{1x,t}$ and the voltage drop first harmonic $|\Delta V|_{1x,m}$ obtained from the experimental data. In detail, the term $|\Delta V|_{1x,t}$ is evaluated by extracting the first harmonic amplitude from the spectrum of the theoretical voltage drop $|\Delta V|_{MC}$, evaluated according to relation (21). The term $|\Delta V|_{1x,m}$ is evaluated by extracting the first harmonic amplitude from the difference:

$$\Delta V_m(t) = v^1_{an,t}(t) - v^1_{an,m}(t) \tag{32}$$

where $v^1_{an,m}(t)$ is the fundamental harmonic of the measured phase voltage on one phase of CHBMI, $v^1_{an,t}(t)$ is the theoretical fundamental harmonic of the CHBMI phase voltage, which depends on the amplitude modulation index m_a and on the total DC link voltage V_{dc} as follow:

$$v^1_{an,id}(t) = m_a V_{dc} \cos(2\pi f_1 t + \phi_{1,m}) \tag{33}$$

TABLE 10. Theoretical Voltage drop range for PD, POD, and APOD-PWM schemes.

Dead Time [μs]	Voltage Drop $\|\Delta V\|_{1x,t}$ [V]		
	PD-PWM	*POD-PWM*	*APOD-PWM*
0,5	$0.3 \leq \Delta V \leq 2.15$	$0.3 \leq \Delta V \leq 2.15$	$0.3 \leq \Delta V \leq 2.15$
1	$0.6 \leq \Delta V \leq 4.28$	$0.6 \leq \Delta V \leq 4.28$	$0.6 \leq \Delta V \leq 4.28$
1,5	$0.9 \leq \Delta V \leq 6.40$	$0.9 \leq \Delta V \leq 6.40$	$0.9 \leq \Delta V \leq 6.40$

where $\phi_{1,m}$ represents the measured voltage phase. In Figure 10, a comparison between the theoretical voltage drop first harmonic $|\Delta V|_{1x,t}$ and the voltage drop first harmonic from the experimental data $|\Delta V|_{1x,m}$ is presented. In detail, for each modulation scheme and different DT values (0.5μs, 1.0μs, and 1.5μs) the theoretical voltage drop $|\Delta V|_{1x,t}$ is compared with the corresponding voltage drop obtained by using Sinusoidal $|\Delta V|_{1x,m,S}$ and SFO $|\Delta V|_{1x,m,SFO}$ as modulation signals.

Taking into account LS-PWM (PD, POD, and APOD) modulation strategies, they lead to the lowest voltage drop as shown in Figures 10 (a)-(i), if compared with other MC-PWM strategies. In detail, the theoretical voltage drop range of variation is summarized in Table X, for different values of the dead time considered.

It can be noted that by increasing the switching frequency or the DT, the voltage drops increase. Moreover, for fixed switching frequency and DT, the analytical voltage drop value is the same, independently of the chosen LS-PWM strategy, since the instantaneous triangular mutual orientation has a negligible effect on the voltage drop.

Regarding experimental results, some considerations must be made: when the amplitude modulation index increases, also the experimental voltage drop increases. This phenomenon can be justified by taking into account the switching devices behavior: in detail, when the amplitude modulation index increases, the load current increases, and consequently the voltage drop on the conducting switching devices, which can be considered as resistances, increases too. However, the difference between the theoretical and measured voltage never exceeds 1 V, except when SFO modulating signals are adopted and $m_a = 0.6$. In this specific case, non-linearities occur. In detail, with respect to Figure 11 (a), a fraction of the modulating signal period, around the instant $t = T_{sw}/4$, is taken into account: let's consider the ideal case with DT = 0, the modulating signal falls between two adjacent carriers signals, and the ideal control signals are generated. As shown, according to the previous considerations, control signals are sent only to one Half-bridge at a time. Moreover, with respect to a single Half Bridge, both *upper* and *lower* control signals change state in the considered T_{sw}.

Regarding the case with DT$\neq$0, in order to introduce a DT, the ideal modulating signal is split into two signals *Mod+k* and *Mod-K*, where k is a dead time factor defined as in [39]; the split modulating signals *Mod+k* and *Mod-K* are assigned to the upper and lower devices of each Half

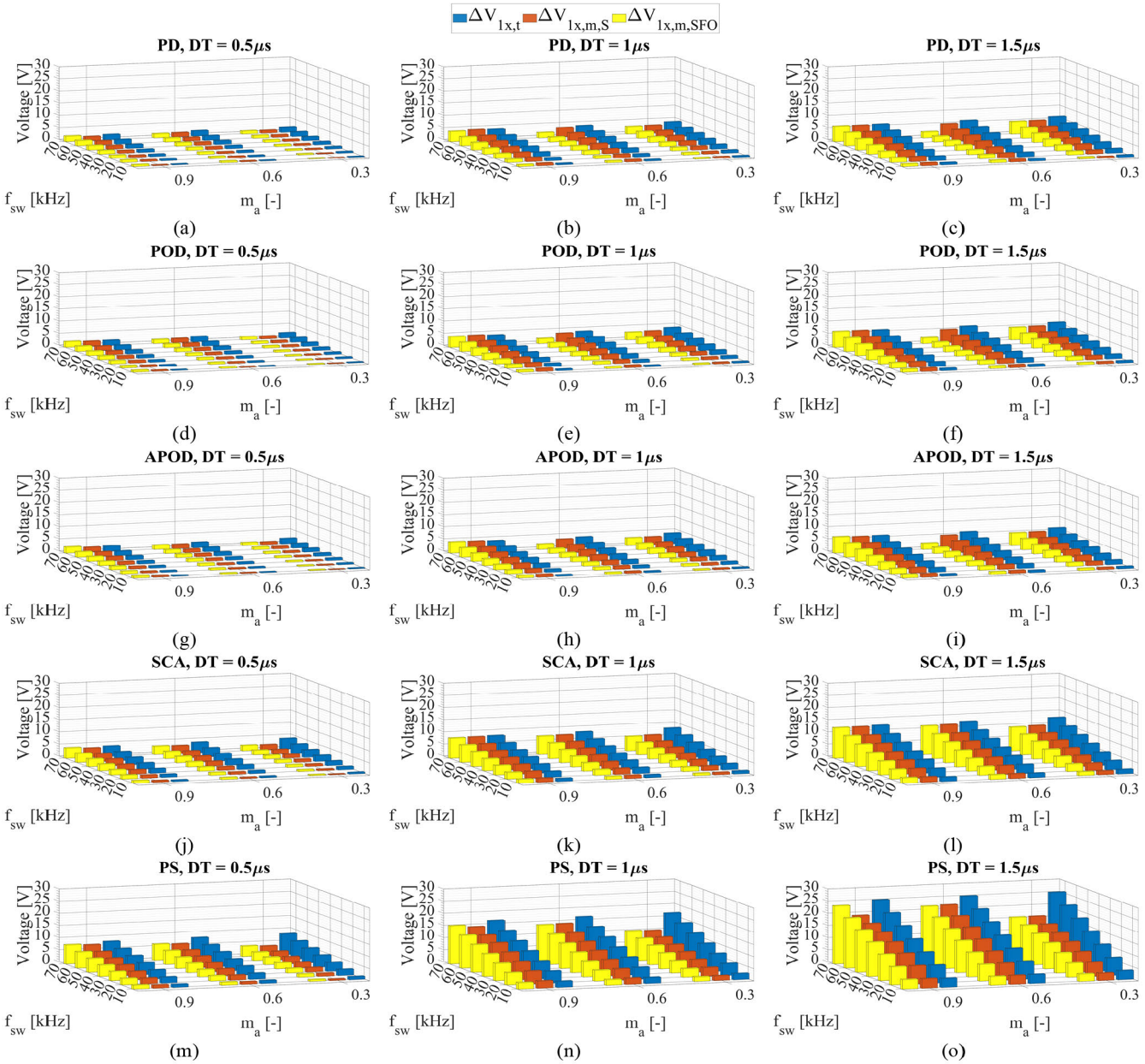

FIGURE 10. Comparison between the theoretical voltage drop first harmonic $|\Delta V|_{1x,t}$ (blue bars) and the voltage drop first harmonic from the experimental data $|\Delta V|_{1x,m}$(red bars for Sine modulation signal and yellow bars for SFO modulation signals).

Bridge, respectively. In this context, due to the modulating and carriers signals comparison, very small amplitude gate control signals should be ideally produced, but, if the dead time is larger than the gate control signal impulse, the signal impulse is not produced at all.

Due to the DT effects, the gate signals result to be very different with respect to the ideal case; in detail, the split modulating signals are producing gate signals sent to upper and lower devices of different half bridges. This behaviour causes a saturation effect on the output voltage, as can be seen in Figure 11 (b). In detail, PD-PWM is chosen and the output phase voltage v_{an}(t) is reported under two working conditions obtained with switching frequency $f_{sw} = 10$ kHz, dead time DT $= 0.5$ μs and switching frequency $f_{sw} = 70$ kHz, dead time DT $= 1.5$ μs. In the first working condition, which is the least severe condition in the working range, the dead time effect is negligible and no saturation can be observed; in the second working condition, which is the most severe in the working range, the DT causes a saturation effect, such that the CHBMI stop switching in some fractions of the fundamental period and the output voltage is constant. This behavior leads on one side to a reduced voltage drop, since a reduced number of commutations occurs, on the other, it causes an increment of harmonic distortion, as will be discussed in the following

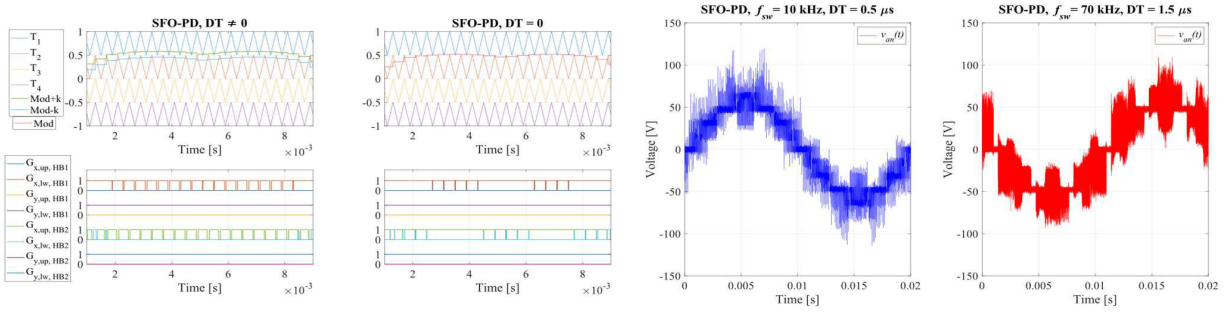

FIGURE 11. (a) Comparison between 3P-5L CHBMI control signals with DT = 0 and DT≠0; (b) phase voltage under different test conditions, saturation effect due to dead time.

TABLE 11. Theoretical Voltage drop range for SCA-PWM and PS-PWM schemes.

Dead Time [μs]	Voltage Drop $\|\Delta V\|_{lx,t}$ [V]	
	SCA-PWM	*PS-PWM*
0,5	$0.6 \leq \Delta V \leq 4.3$	$1.2 \leq \Delta V \leq 8.6$
1	$1.2 \leq \Delta V \leq 8.56$	$2.4 \leq \Delta V \leq 17.12$
1,5	$1.8 \leq \Delta V \leq 12.80$	$3.6 \leq \Delta V \leq 25.60$

sections. Since the working region around $m_a = 0.6$ is not linear, in this region, the relations (21) and (22) are not valid anymore; high dead time and switching frequency values result in a wider non-linear operating region around $m_a = 0.6$. It must be noted that a similar situation occurs when sinusoidal modulating signals are chosen and $m_a = 0.5$.

This behavior is not visible in Figure 10 because tests have not been carried out in this specific condition. Moreover, this phenomenon occurs only when a LS-PWM strategy is adopted, since it depends on the mutual carriers disposition; it does not occur when SCA and PS are chosen, as it will be illustrated below. When PS-PWM and SCA-PWM schemes are considered, the theoretical voltage drop is doubled and quadrupled, respectively. In detail, the variation range of analytical voltage drop is summarized in Table XI, for different values of the dead time considered, and SCA-PWM and PS-PWM strategies.

Considerations about PS and SCA theoretical and experimental voltage drops partly coincide with previous considerations relating to LS-PWM strategies. In this case, the maximum difference between the theoretical and measured voltage drop reaches less than 5 V and 10 V in SCA and PS, respectively. In this case, the coincidence between voltage drops with sinusoidal and SFO modulating signals is more evident, as the previously described non-linearity phenomenon does not occur when $m_a = 0.6$, due to the different carriers disposition. It can be noted that the difference between theoretical and measured voltage drops increases when the switching frequency increases and the amplitude modulation index decreases. The theoretical voltage drop calculation leads to an overestimation, as it is confirmed in [25].

The second analysis consists in the comparison between the ideal output phase voltage $v^1_{an,id}(t)$ with no dead time applied to the inverter, which is evaluated according to equation (33), and the expected output phase ideal voltage $v^1_{an,ex}(t)$, which is evaluated, according to equation (22), as follows:

$$v^1_{an,ex}(t) = v^1_{an,m}(t) + \Delta V_{MC}(t) \tag{34}$$

where $v^1_{an,m}(t)$ is the fundamental harmonic of the measured output voltage and $|\Delta V|_{MC}(t)$ is the theoretical voltage drop, evaluated according to equation (21).

The term $v^1_{an,ex}(t)$ is distorted due to the dead time voltage drop, so the fundamental harmonic is extracted through the FFT algorithm. In order to carry out this comparison, the relative percentage error $e_{\%}$ is defined as:

$$e_{\%} = \frac{V^1_{an,id} - V^1_{an,ex}}{V^1_{an,id}} \cdot 100 \tag{35}$$

where $V^1_{an,ex}$ is the fundamental harmonic amplitude of the expected output phase voltage, and $V^1_{an,id}$ is the fundamental harmonic amplitude of the ideal output phase voltage. In Figure 12 the relative percentage error $e_{\%}$ in all the considered working range is reported. Taking into account LS-PWM strategies, the maximum $e_{\%}$ magnitude occurs when $f_{sw} = 70$ kHz, DT $= 1.5$ μs, $m_a = 0.6$ and SFO modulating signal is chosen and $e_{\%}$ magnitude is equal to 8%.

This specific working condition has been previously discussed, in all the other working conditions $e_{\%}$ magnitude is always lower than 4%, and in most cases is lower than 1%. Taking into account LS-PWM strategies, the maximum $e_{\%}$ magnitude occurs when $f_{sw} = 70$ kHz, DT $= 1.5$ μ s, $m_a = 0.6$ and SFO modulating signal is chosen and $e_{\%}$ magnitude is equal to 8%. This specific working condition has been previously discussed, in all the other working conditions $e_{\%}$ magnitude is always lower than 4%, and in most cases is lower than 1%. Taking into account PS-PWM, the maximum $e_{\%}$ magnitude occurs when $f_{sw} = 70$ kHz, DT $= 1.5$ μs, $m_a = 0.3$ and $e_{\%}$ magnitude is equal about to 30%. The error sign confirms that when the amplitude modulation index is very low, a voltage drop overestimation occurs. The percentage

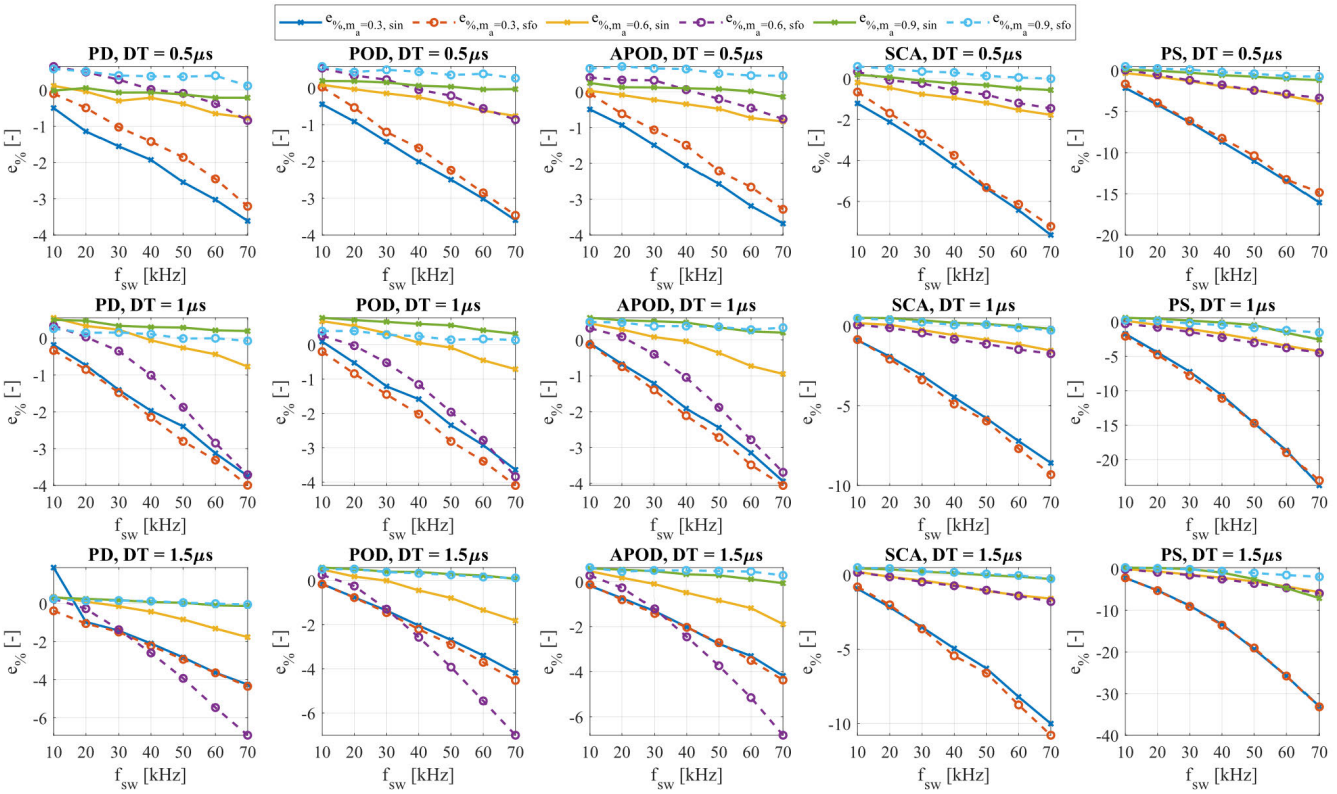

FIGURE 12. Percentage error e% under various test conditions.

error is drastically reduced when the amplitude modulation index increases, and it does not exceed 5%. Similar considerations can be applied to the SCA-PWM, although the maximum amplitude error is lower than in the previous case, about 10%. Also, in this case, the worst approximation occurs when m_a is very low.

The goal of this analysis is to underline the MC-PWM modulation strategies impact on the DT effects with respect to the 3P-5L CHBMI structure. In detail, in this subsection, the DT effect on the fundamental harmonic has been analyzed. Experimental results confirm the DT effects strong dependency on the selected MC-PWM strategy. Indeed, from the comparison between analytical and experimental results, the voltage drop mathematical formulation allows predicting quite well the DT effect on the voltage fundamental harmonic for higher values of the modulation index (in the range from 0.5 to 1.15). Nevertheless, an overestimation phenomenon occurs for lower values of the modulation index. Thus, this phenomenon must be considered in all cases where a voltage compensation algorithm is employed.

B. GLOBAL HARMONIC DISTORTION ANALYSIS

In this subsection, the DT impact on the global voltage harmonic distortion, among the considered MC-PWM strategies, is discussed. In this context, the Total Harmonic Distortion (THD) index is used as a comparison tool of the converter performance, it is expressed according to [42] as follows:

$$THD\% = \sqrt{\frac{V_{rms}^2 - V_{rms,1}^2}{V_{rms,1}^2}} \cdot 100 \tag{36}$$

where V_{rms} and $V_{rms,1}$ are the root mean square (RMS) value of the voltage waveform and the RMS value of the fundamental harmonic, respectively. Figure 13 shows the global THD% values obtained for each modulation scheme and for different values of the DT. In detail, the THD% values have been reported as a function of the modulation index and switching frequency. By considering THD% values, obtained with LS-PWM-based schemes, shown in Figure 13 (a)-(f), it should be noted that the DT effect is negligible in all working points where the modulation index is higher than 0.5. Indeed, the THD% presents the same values. While, in all working points where the modulation index is lower than 0.5, the THD% values are higher, since the converter works in three voltage levels mode, instead of five. Moreover, higher DT values result in higher THD% values, especially when the amplitude modulation index is very low. When PS-PWM is adopted, as illustrated in Figure 13 (g) and (h), the DT generates an increment of the THD% values. In this case, the DT effect is visible for modulation index values up to 0.6. Instead, the DT effect is less visible for higher values of the modulation index.

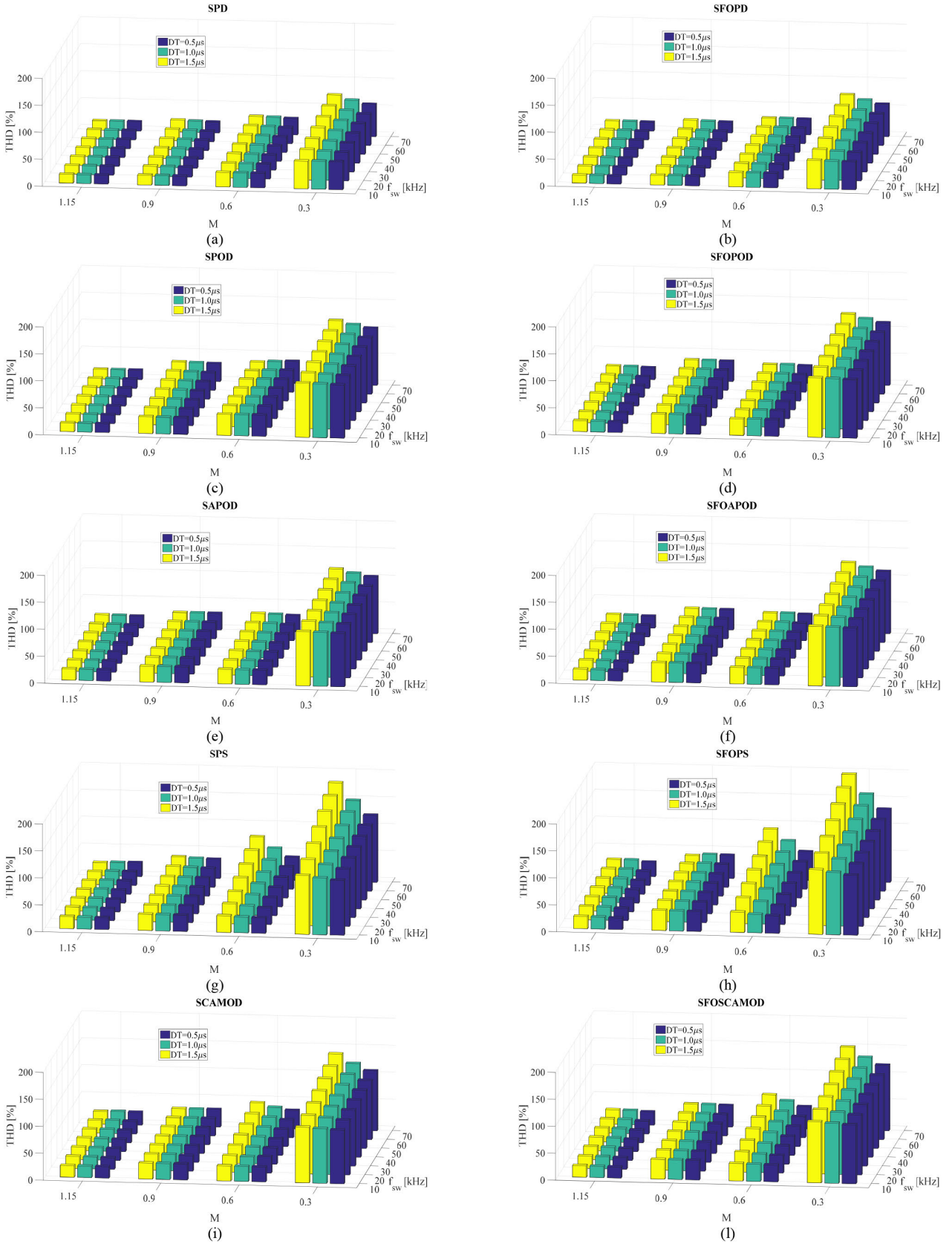

FIGURE 13. Experimental global THD% values: (a) S PD; (b) SFO PD; (c) S POD; (d) SFO POD; (e) S APOD; (f) SFO APOD; (g) S PS; (h) SFO PS; (i) SCA; (l) SFO SCA.

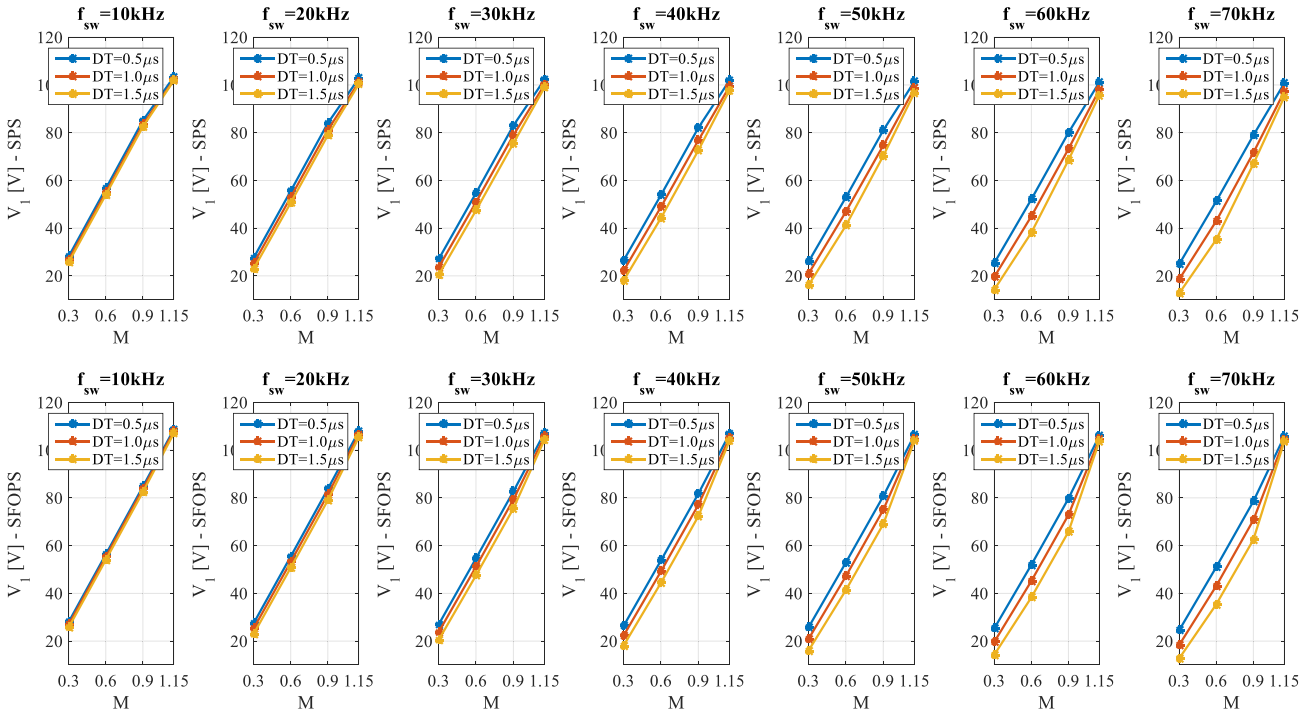

FIGURE 14. Experimental 1st voltage harmonic vs. modulation index obtained with SPS and SFOPS schemes.

This phenomenon can be explained by comparing the first voltage harmonic values, obtained with SPS and SFOPS schemes, with respect to the modulation index and for different values of the switching frequency, in the three cases of the DT considered, as shown in Figure 14. Indeed, when switching frequency and DT increase, the reduction of the first voltage harmonic becomes more evident; this reduction causes a THD% increase, according to equation (36). This result is coherent with the previous discussion on the voltage drop: in detail, the PS-PWM strategy causes the highest voltage drop on the fundamental harmonic voltage amplitude, which is responsible for the THD% increment. The THD% values obtained with SCAMOD and SFOSCAMOD are shown in Figure 13 (i) and (l), respectively. In this case, the DT effect on the THD% is mitigated if compared to the case of PS-PWM based THD%, due to a lower reduction of the fundamental harmonic voltage amplitude as the DT increase, as can be seen in Figure 15. Also in this case, the phenomenon can be justified by looking at the voltage drop: in detail, SCA-PWM determines an intermediate fundamental harmonic voltage drop, with respect to the LS and PS PWM strategies, which causes a lower THD% increment as the DT increases, with respect to the PS-PWM.

According to [42], the THD index allows considering the overall harmonic content in a voltage or current waveform without providing information on the real distribution in the harmonic spectra and the contribution of each harmonic in the frequency domain. Moreover, the expression (36) allows measuring the overall distortion, although it does not allow distinguishing harmonics from inter-harmonics or low-frequency components by high-frequency components. The knowledge of the real distribution of the harmonic components and their amplitudes in the frequency domain, for example, can be used in the filter design process for grid-connected applications or to estimate the torque ripple and iron losses for electrical drive applications. In this context, in order to compare and analyze the DT impacts in the frequency domain, in terms of the distribution and amplitude of a harmonics group, a Partial Harmonic Distortion (PHD) has been used as a comparison tool. The PHD% index has been defined as:

$$PHD\% = \frac{\sqrt{\sum_{h=k_h f_{sw}-B_{sw}}^{k_h f_{sw}+B_{sw}} V_h^2}}{V_{DC}} \cdot 100 \tag{37}$$

where V_h is the generic voltage harmonic of *h-th* order, f_{sw} is the switching frequency, k_h is a constant integer number, and B_{sw} is the bandwidth which allows to consider the sideband harmonics around the frequency $k_h f_{sw}$; in detail, B_{sw} is equal to 2 kHz. Moreover, the PHD values are expressed as a percent of the total DC voltage V_{dc}, which is equal to the sum of each H-Bridge DC source E in one phase of the converter, according to equation (13). In this way, the PHD allows the evaluation of the DT impacts in the frequency domain providing information about the distribution and amplitude of the main high-frequency harmonics without considering the previously described first harmonic reduction effect.

As previously discussed, each MC-PWM strategy allows placing harmonic groups differently in the frequency domain.

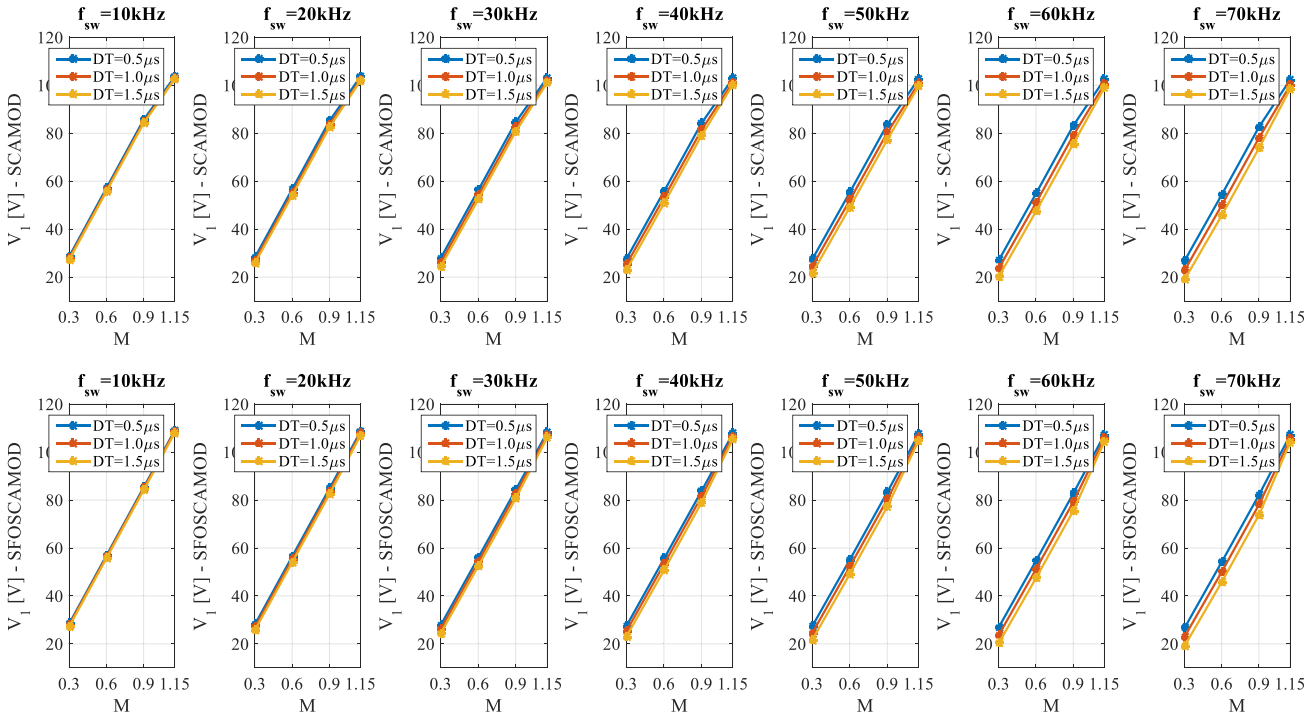

FIGURE 15. Experimental 1st voltage harmonic vs. modulation index obtained with SCAMOD and SFOSCAMOD schemes.

TABLE 12. PHD evaluated in frequency domain.

Modulation schemes	PHD% evaluation points in the frequency domain - $k_h f_{sw}$				
LS-PWM (PD, POD and APOD)	f_{sw}	$2f_{sw}$	$3f_{sw}$	$4f_{sw}$	$5f_{sw}$
PS-PWM	$4f_{sw}$	$8f_{sw}$	$12f_{sw}$	$16f_{sw}$	$20f_{sw}$
SCAMOD	$2f_{sw}$	$4f_{sw}$	$6f_{sw}$	$8f_{sw}$	$10f_{sw}$

In order to take into account only the more significant harmonics group, the PHD% index is evaluated in function of the switching frequency f_{sw} and an integer multiplier factor k_h which depend on the adopted modulation schemes. PHD% evaluation points in the frequency domain are summarized in Table XII.

From the elaboration of the experimental data, by fixing the values of the DT and switching frequency, it emerges that the PHD% values do not vary over the modulation index. Thus, the PHD% values only for amplitude modulation index $m_a = 0.9$ are reported.

By considering all cases summarized in Table III, for the LS-PWM strategies (PD, POD and APOD), the comparison of PHD trends with respect to the switching frequency, evaluated for three DT values, with sinusoidal and SFO modulation signals, are shown in Figure16 and Figure 17, respectively.

With respect to the schemes with sinusoidal modulation signals (Figure 16), it is interesting to note that the DT effect is evident only for SPD in the harmonic group centered at the switching frequency ($k_h = 1$). In detail, it is possible to observe a stronger increase in the PHD values for higher values of the switching frequency. Whereas, the DT effect is negligible in other analyzed cases. With respect to SFO modulating signals, the DT effect is evident in the harmonics centered at twice ($k_h = 2$) of the switching frequency in all adopted LS-PWM strategies. In this case, the DT effect generates a stronger increase in the PHD values for higher values of the switching frequency. Moreover, an interesting effect has been observed in the harmonics group centered at three times ($k_h = 3$) of the switching frequency, when SFOPD is adopted. In detail, a reduction of the PHD values has been observed when the switching frequency is increased. Figure 18 shows the PHD trends with respect to the switching frequency obtained with SPS and SCAMOD schemes. For these modulation schemes, the DT effect is more evident with respect to the LS-PWM-based schemes. In detail, the DT effect generates a reduction of the PHD values in the first harmonic groups centered at four ($k_h = 4$) and two ($k_h = 2$) times of the switching frequency for SPS and SCAMOD, respectively. Moreover, the DT generates an increase in the PHD values in other harmonic groups and, in detail, for the SPS scheme in the harmonic groups centered at eight ($k_h = 8$) and twelve ($k_h = 12$) times of the switching frequency. For the SCAMOD scheme, the DT effect is negligible for the other harmonic group, from $k_h = 4$ to $k_h = 10$, where the PHD values are similar.

Figure 19 shows the PHD trends vs. switching frequency obtained with SFOPS and SFOSCAMOD. It should be noted that also in this case the DT impact generates a benefic effect on the first harmonic groups by reducing the PHD values as the DT increase. Instead, an increase in the PHD values has

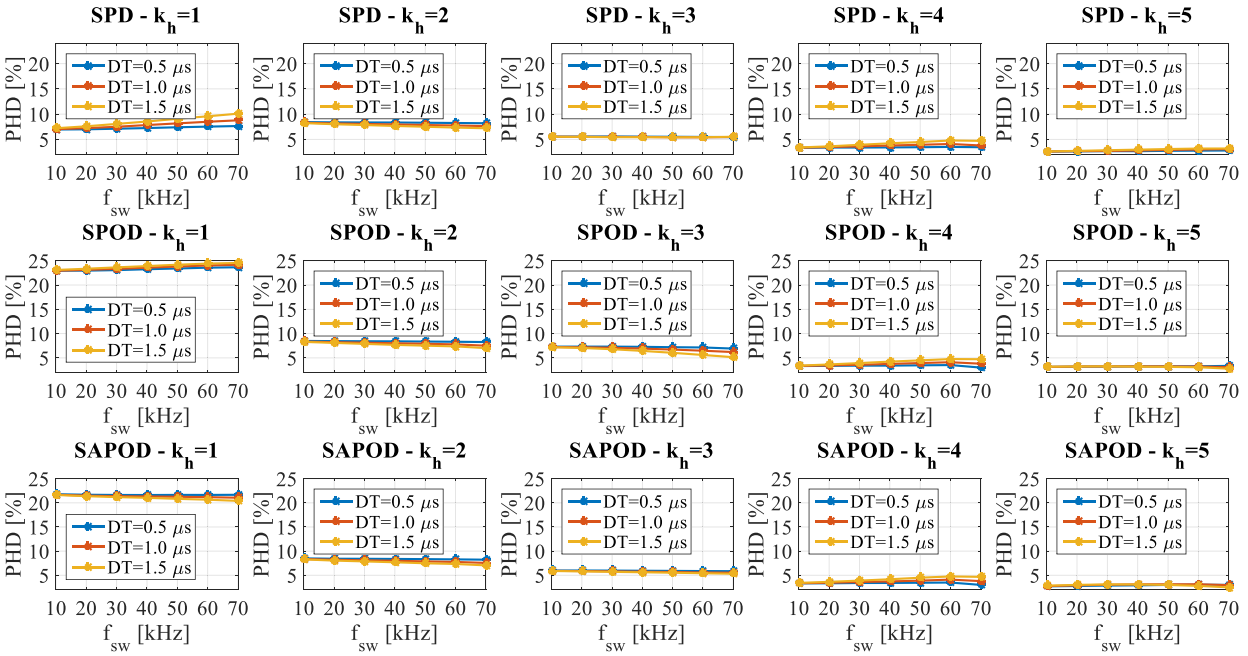

FIGURE 16. PHD values vs. switching frequency obtained with LS-PWM-based schemes and sinusoidal modulation signals (SPD, SPOD and SAPOD).

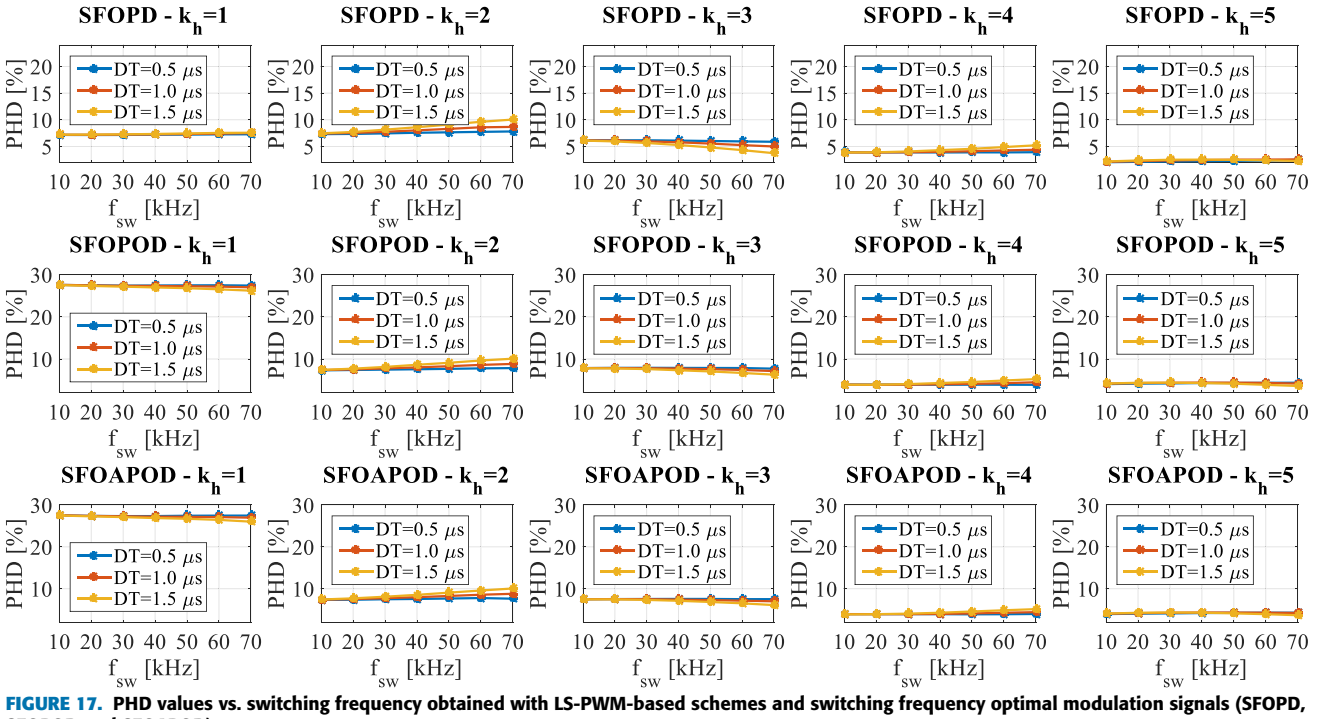

FIGURE 17. PHD values vs. switching frequency obtained with LS-PWM-based schemes and switching frequency optimal modulation signals (SFOPD, SFOPOD and SFOAPOD).

been observed in the second harmonic groups $k_h = 8$ and $k_h = 4$ for SFOPS and SFOSCAMOD, respectively. In other cases the DT effect is negligible.

In conclusion, the PHD allows to analyse the DT impact on the high-frequency harmonic components. In detail, it emerged that the LS-PWM-based schemes are insensible on the DT effect showing a negligible result of the PHD values. The DT effect is evident for PS-PWM and SCAMOD schemes. In particular, the DT generates a benefit in the first harmonic group by reducing the PHD values. Whereas, the DT generates a more evident increase in the PHD values for the second harmonic groups. In the next subsection, the low-frequency DT effect is discussed.

C. LOW-FREQUENCY HARMONIC DISTORTION ANALYSIS

As well known, the DT generates low-order harmonics in the output voltages of the converter. By analyzing the harmonic spectra in the frequency domain, only the odd harmonics,

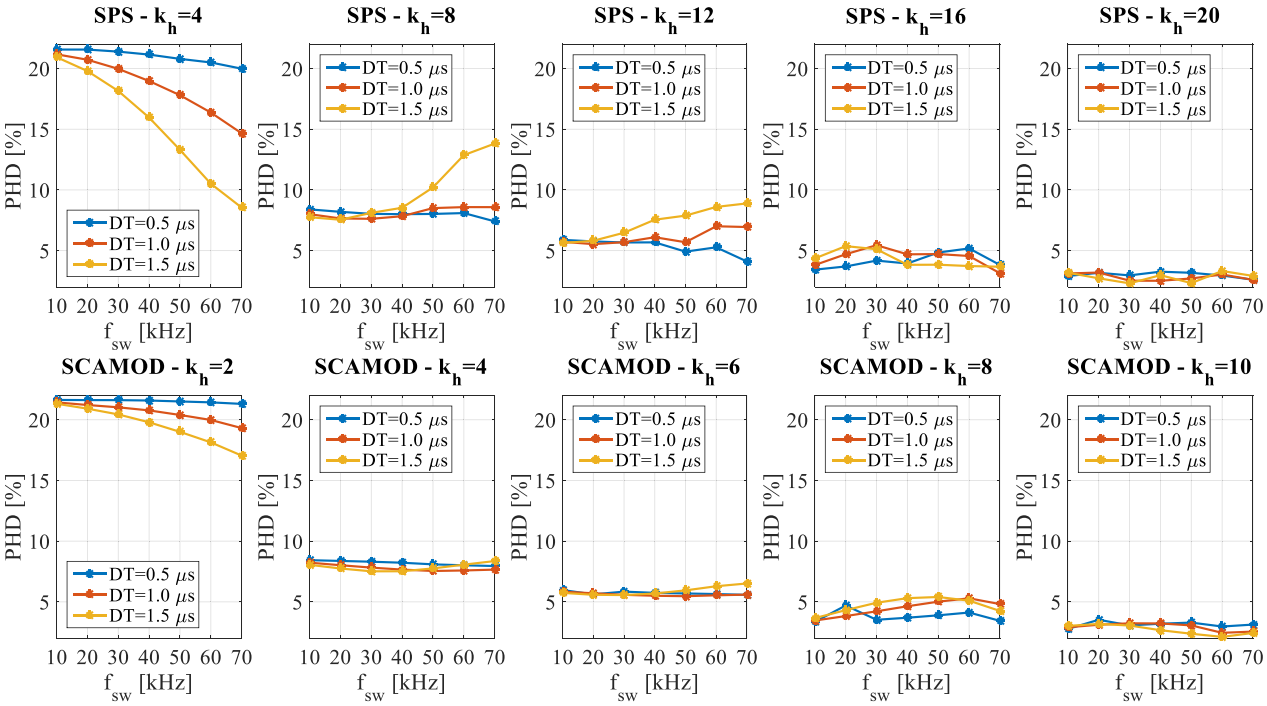

FIGURE 18. PHD values vs. switching frequency obtained with SPS and SCAMOD schemes.

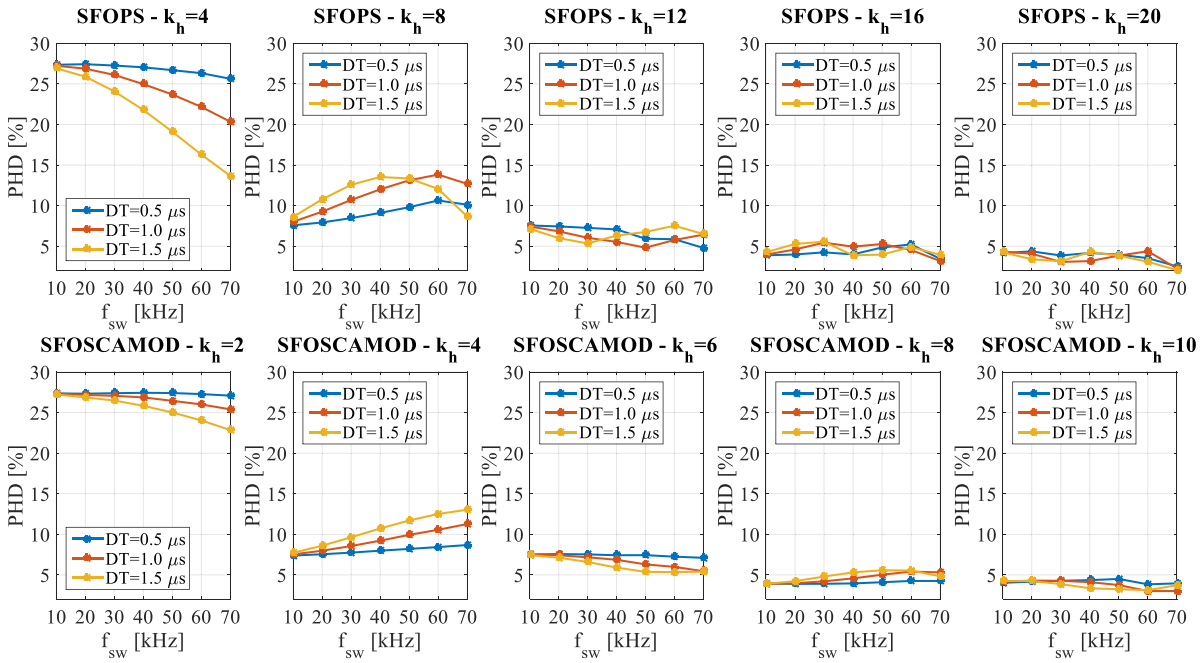

FIGURE 19. PHD values vs. switching frequency obtained with SFOPS and SFOSCAMOD schemes.

from the fifth to twenty-third components, result predominantly with respect to the other high-frequency harmonics, in all modulation techniques considered. In detail, a random variability of the harmonics amplitude has been observed for low values of the DT and switching frequency. For this reason, a low frequency total harmonic distortion ($THD_{LF}\%$) index, evaluated by considering harmonics from the 5^{th} to 23^{rd} expressed in percent with respect to the fundamental harmonic, has been used as a comparison tool. The $THD_{LF}\%$ is expressed as:

$$THD_{LF}\% = \frac{\sqrt{\sum_{h=5}^{23} V_h^2}}{V_1} \cdot 100 \tag{38}$$

where V_h is the peak value of the voltage harmonic of order h and V_1 is the peak value of the first harmonic.

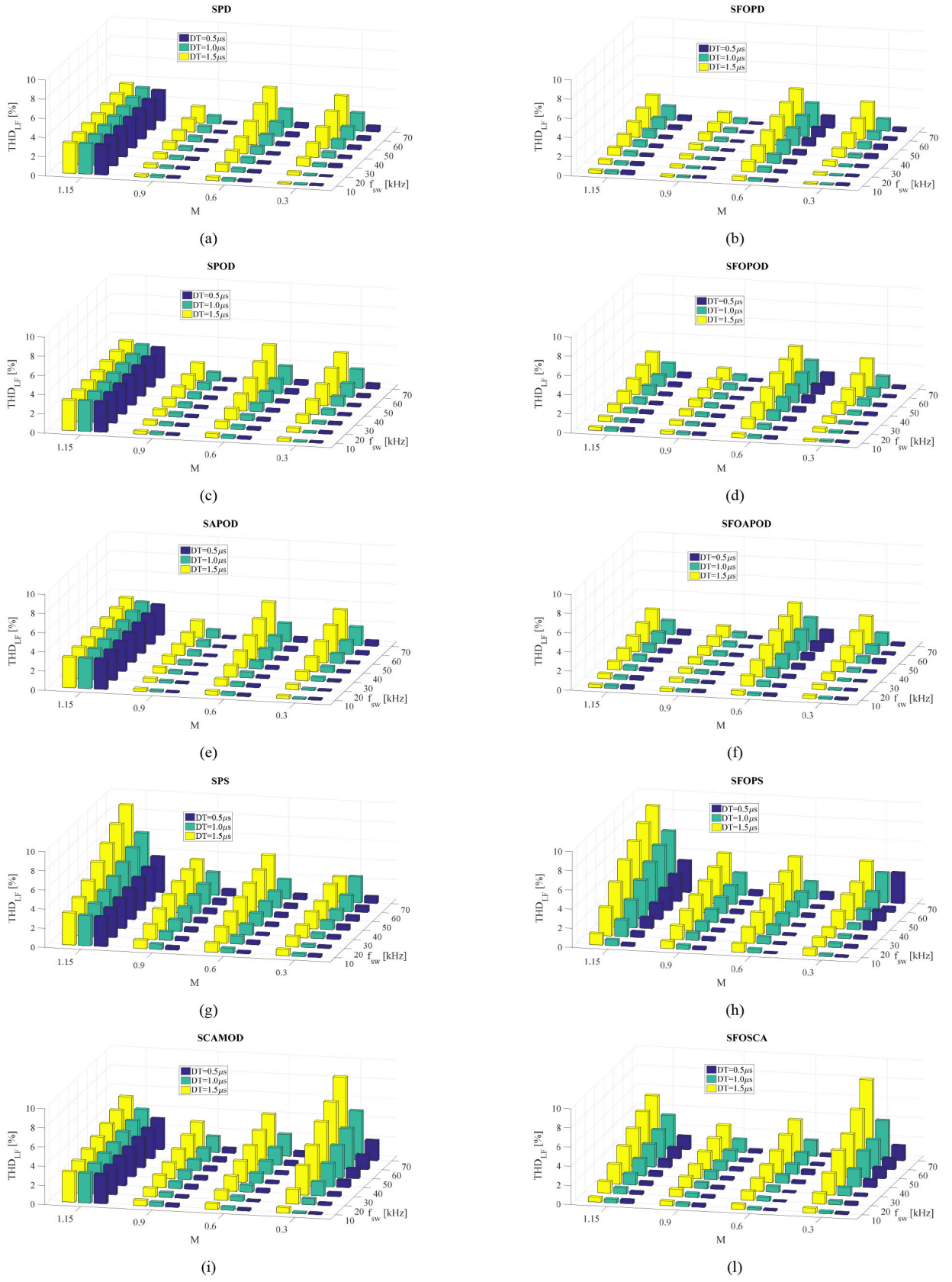

FIGURE 20. Experimental THD_{LF}% values: (a) SPD; (b) SFOPD; (c) SPOD; (d) SFOPOD; (e) SAPOD; (f) SFOAPOD; (g) SPS; (h) SFOPS; (i) SCAMOD; (l) SFOSCAMOD.

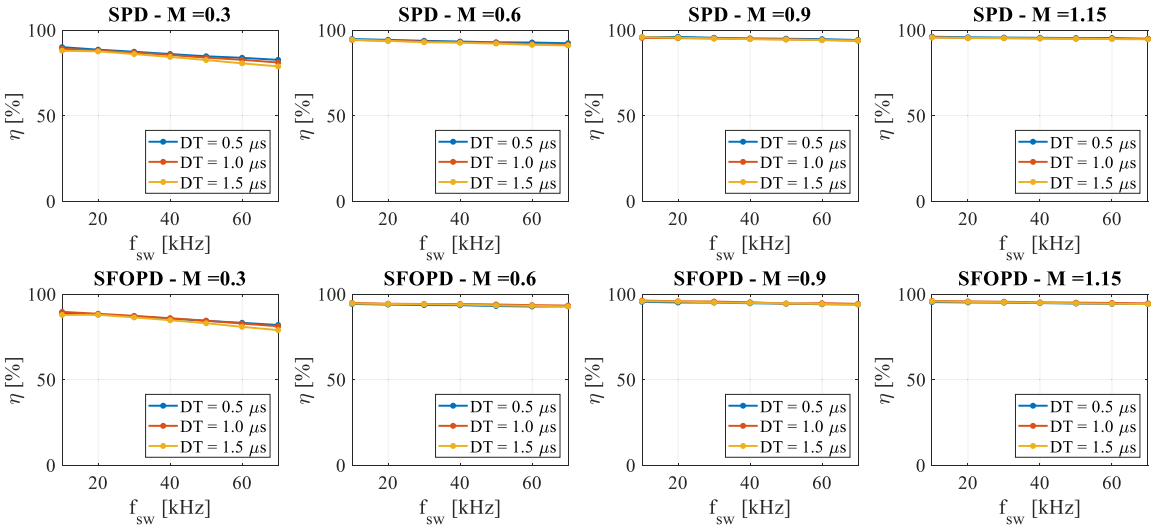

FIGURE 21. SPD and SFOPD experimental conversion efficiency vs. switching frequency for different values of the DT.

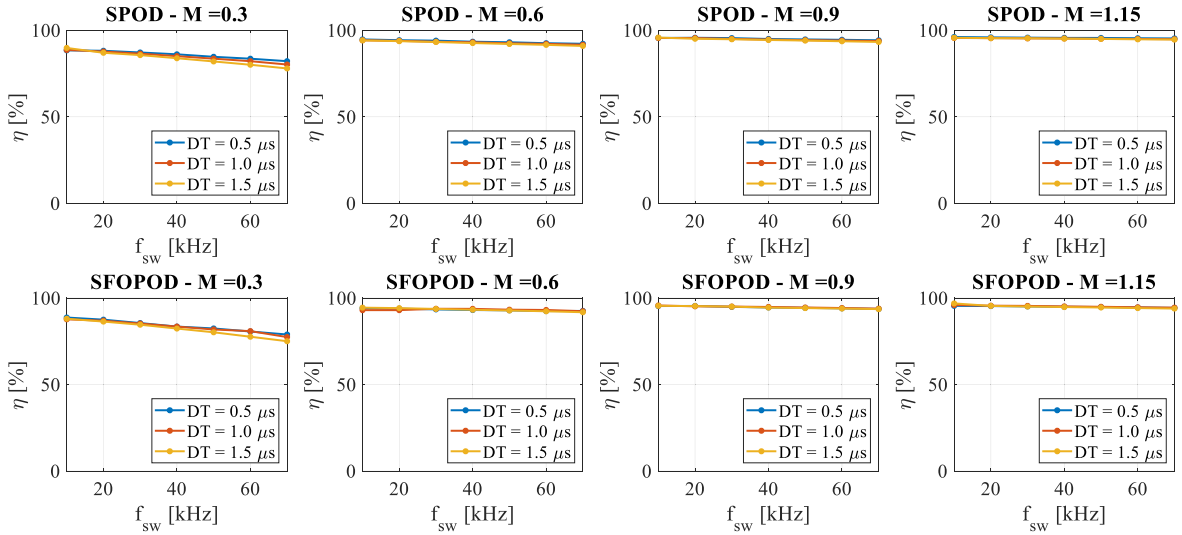

FIGURE 22. SPOD and SFOPOD experimental conversion efficiency vs. switching frequency for different values of the DT.

It must be underlined that the $THD_{LF}\%$ allows to investigate the overall low-frequency voltage harmonics distortion by providing information about the DT impact without considering the real harmonics distribution in the frequency domain.

Figure 20 shows the $THD_{LF}\%$ values with respect to the modulation index and switching frequency evaluated for DT equal to $0.5\mu s$, $1\mu s$ and $1.5\mu s$ for each modulation scheme considered. As previously noted, the DT impact is similar among the LS-PWM-based schemes, as shown in Figure 20 (a) – (f). In detail, the $THD_{LF}\%$ values increase as the switching frequency increases; this growth is emphasized when the modulation index is equal to 0.6. Instead, the DT effect is mitigated in the over-modulation region, when sinusoidal modulating signals are adopted.

It is interesting to note that the DT effect is lower in the overmodulation region where SFOs are employed as modulation signals. This phenomenon occurs since the SFO signals allow extending linear modulation region up to 1.15. Thus, it is possible to claim that the modulation schemes with SFO as modulation signals present the best results in terms of $THD_{LF}\%$.

Figure 20 (g) and (h) show the $THD_{LF}\%$ results obtained with SPS and SFOPS schemes, respectively. In this case, the DT effect is evident in all working points considered, showing similar numeric impact, and in detail, the $THD_{LF}\%$ increases as the switching frequency increases. Moreover, the introduction of the SFO as modulation signals allows for the reduction of the $THD_{LF}\%$ values only for lower values of the switching frequency with respect to the sinusoidal signals employed. Finally, the $THD_{LF}\%$ results for SCAMOD and SFOSCAMOD are depicted in Figure 20 (i) and (l), respectively. In this case, it should be noted that the DT effect is more evident for lower values of the modulation index and for higher values of the modulation index. This phenomenon is present both where sinusoidal and SFO are adopted as the

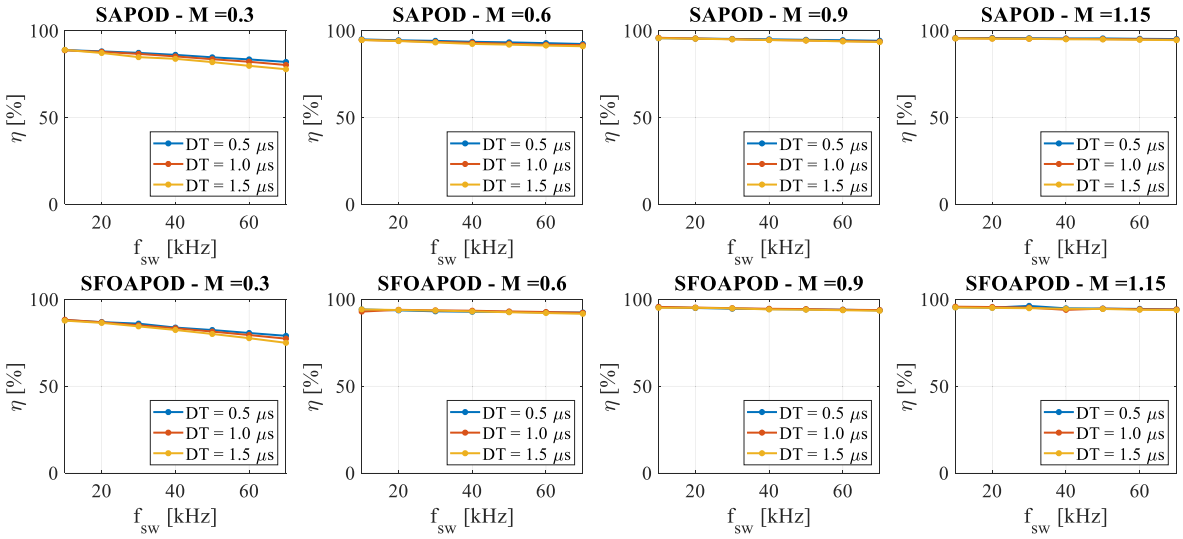

FIGURE 23. SAPOD and SFOAPOD experimental conversion efficiency vs. switching frequency for different values of the DT.

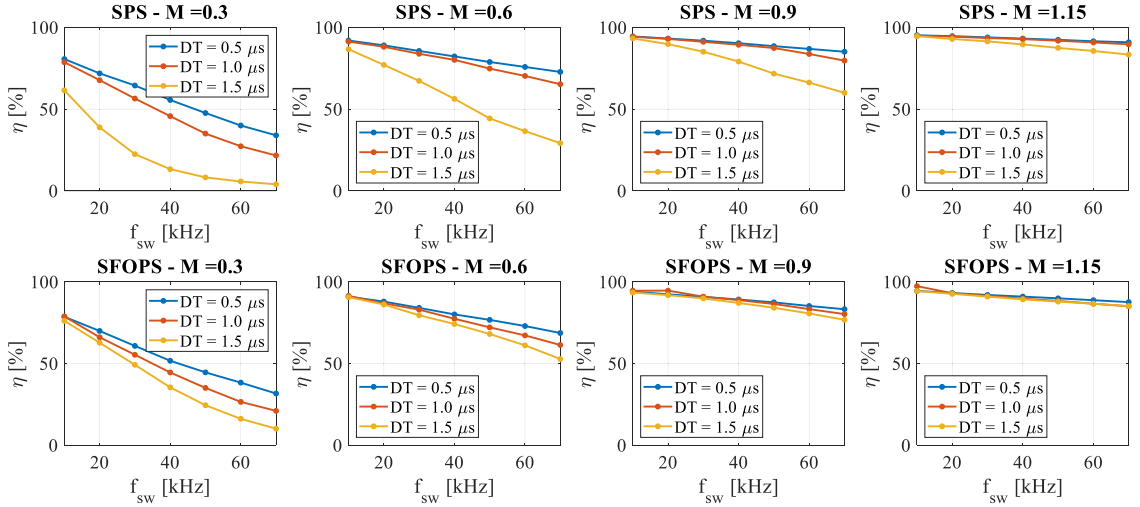

FIGURE 24. SPS and SFOPS experimental conversion efficiency vs. switching frequency for different values of the DT.

modulation signals. Anyhow, also, in this case, the SFO allow reducing the DT effect, especially for switching frequency from 10 kHz to 30 kHz, with respect to the sinusoidal signals used.

D. CONVERTER EFFICIENCY ANALYSIS

In this subsection, the DT impacts on the conversion efficiency have been presented for each modulation technique considered and for different values of the DT. The main goal is to analyze the effect of the DT in all working points of the converter defined by the values of the modulation index and switching frequency. In this context, the conversion efficiency has been used as a comparison tool and expressed as:

$$\eta_{\%} = \frac{P_{AC}}{\sum_{i=1}^{n_{HB}} P_{DC,i}} \cdot 100 \tag{39}$$

where P_{AC} is the active output power of the converter, $P_{DC,i}$ is the i^{th} DC input power of the corresponding H-Bridge, and n_{HB} is the H-Bridges overall number of the converter.

Figure 21 shows the comparison of conversion efficiency trends vs. switching frequency, obtained with SPD and SFOPD schemes, for different values of DT and each modulation index value considered.

As shown in Figure 21, it is interesting to note that the effect of the DT on conversion efficiency is absent. Indeed, only the efficiency reduction, due to the increase of the switching frequency, is evident in particular for lower values of the modulation index. Also in the case of POD and APOD-based schemes, the DT impact is absent, as shown in Figure 22 and Figure 23, respectively. Moreover, for all LS-PWM schemes, it is evident that similar results have been obtained by comparing the values with sinusoidal and SFO modulation signals. Thus, it is possible to claim that the DT impact is absent in conversion efficiency values obtained with LS-PWM schemes.

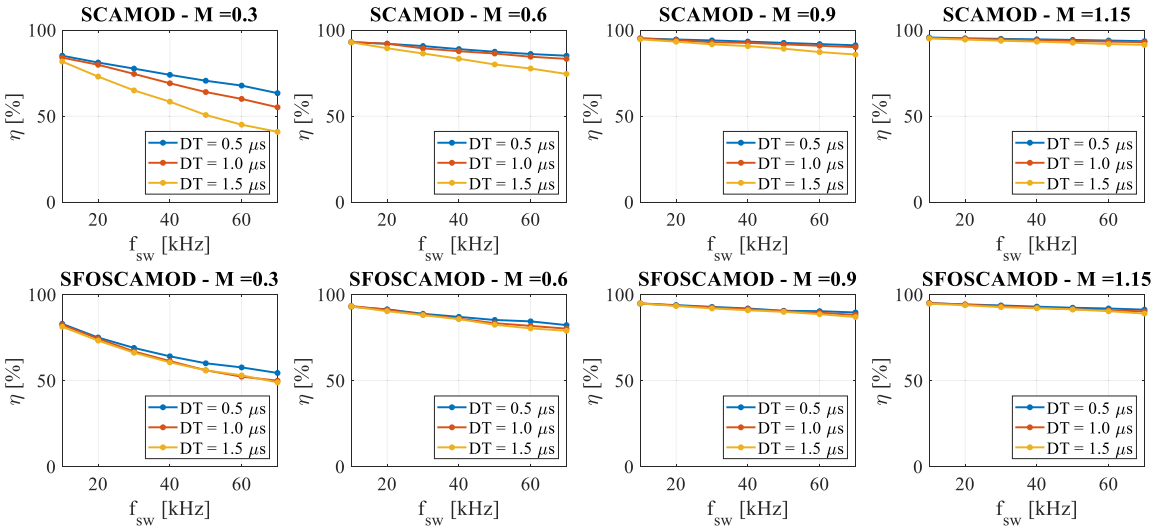

FIGURE 25. SCAMOD and SFOSCAMOD experimental conversion efficiency vs. switching frequency for different values of the DT.

Different results have been obtained for PS and SCAMOD-based schemes. Figure 24 shows the conversion efficiency trend vs. switching frequency for different values of the DT and each modulation index value considered. In detail, the DT generates an evident reduction of the conversion efficiency that is highlighted for higher values of the switching frequency where there is a combination of the effects produced by the switching frequency and DT. Anyhow, by comparing the results obtained with Sinusoidal and SFO modulation signals, it is interesting to note that the best results have been obtained with the SFOPS scheme.

Finally, also the SCAMOD-based scheme presents a reduction of the conversion efficiency produced by the DT, as shown in Figure 25. Anyhow, DT impact is less evident with respect to the PS-based schemes. Indeed, only for lower values of the modulation index, the DT generates a significant reduction of the conversion efficiency. Moreover, it is interesting to note that the SFOSCAMOD scheme results are less sensible regarding the DT impact in terms of conversion efficiency. In conclusion, from the previous analysis, it emerged that the PS-based scheme is more sensible at the DT impact presenting a significant reduction of the conversion efficiency, with respect to the other modulation techniques taken into account. Also, SCAMOD-based schemes emerged that are sensible at the DT impact but the effect is less obvious. Moreover, in the SFOSCAMOD scheme, the effect of the DT is negligible. While, in the case of LS-PWM schemes (SPD, SFOPD, SPOD, SFOPOD, SAPOD, and SFOAPOD) the effect of the DT is absent in all working points considered.

VI. CONCLUSION

This paper deals with the experimental investigation of the DT impacts on 3P-5L CHBMI performance, taking into account commonly used MC-PWM strategies. The analysis deal with the DT impact on the fundamental harmonic voltage drop, on the voltage spectrum, and on the converter efficiency. In the first part of the paper, the fundamental harmonic voltage drop mathematical formulation is presented. In detail, the proposed mathematical approach for the fundamental harmonic voltage drop estimation has been generalized for a generic 3P-n_lL-CHBMI, for any amplitude modulation index m_a, for any switching frequency f_{sw}, and for any of the MC-PWM strategies proposed in this work, which represent the most commonly adopted modulation strategies for the CHBMIs. Indeed, a general mathematical formulation of the fundamental amplitude voltage drop taking into account the adopted MC-PWM schemes is missing in the literature. According to the proposed mathematical approach, by increasing the switching frequency or the DT, the voltage drop increase: the voltage drop variation rate is strongly correlated with the adopted MC-PWM strategy. When LS-PWM (PD, POD, APOD) strategies are adopted, it can be noted that, for fixed DT and switching frequency value, the evaluated voltage drops are quite the same, which means that the mutual carriers orientation has a negligible effect on voltage drops. When SCA-PWM is adopted, the voltage drop is doubled. In both cases, the voltage drop is independent of the number of H-B modules per phase. When PS-PWM is adopted, the voltage drop is 2N-times higher, whit respect to the LS-PWM case, in the same working conditions. According to the proposed model, it emerges a very strong correlation between the fundamental harmonic voltage drop and the adopted modulation strategy. These results represent powerful tools for MIs design purposes, especially when the number of H-B modules per phase must be chosen or when the appropriate MC-PWM strategy must be adopted.

Experimental tests have been carried out in order to validate the proposed mathematical approach. The experimental tests have been conducted by fixing a specific working condition characterized by the value of the modulation index, DT, and switching frequency. Thus, the DC and AC electric quantities (voltages and currents) have been acquired and elaborated in the Matlab environment. The first analysis deal with the comparison between the theoretical voltage drop

first harmonic $|\Delta V|_{1x,t}$ and the voltage drop first harmonic $|\Delta V|_{1x,m}$ obtained from the experimental data. It can be noted that when the amplitude modulation index increases, also the experimental voltage drop increases. This phenomenon is not considered in the proposed mathematical approach and can be justified by taking into account the switching devices conduction resistance, which causes a progressively increasing voltage drop, as the current increases. However, when LS-PWM strategies are considered, the difference between the theoretical and measured voltages never exceeds 1 V, except when SFO modulating signals are adopted and $m_a = 0.6$. In this specific case, some nonlinearities, which have been deeply discussed in section V, occur. When SCA and PS-PWM are considered, the maximum difference between the theoretical and measured voltage drop reaches less than 5 V and 10 V in SCA and PS, respectively. In this case, the theoretical voltage drop calculation leads to an overestimation, especially when the amplitude modulation index is very low. The second analysis consists in the comparison between the fundamental harmonic amplitude of the expected output phase voltage $V^1_{an,ex}$ and the fundamental harmonic amplitude of the ideal output phase voltage. $V^1_{an,id}$. As a comparison tool, the relative percentage error $e_{\%}$ is introduced. Taking into account LS-PWM strategies, $e_{\%}$ magnitude is always lower than 4%, and in most cases is lower than 1%, excluding cases where nonlinearities occur. Taking into account PS-PWM, the maximum $e_{\%}$ magnitude occurs when $f_{sw} = 70$ kHz, DT $= 1.5$ μs, $m_a = 0.3$ and $e_{\%}$ magnitude is equal about to 30%. The percentage error is drastically reduced when the amplitude modulation index increases, and it does not exceed 5%. Similar considerations can be applied to the SCA-PWM, although the maximum amplitude error is lower than in the previous case, about 10%.

Anyhow, experimental results confirm that the voltage drop mathematical formulation allows predicting very well the DT effect on the voltage fundamental harmonic in the range from 0.5 to 1.15. Nevertheless, an overestimation phenomenon occurs for lower values of the modulation index. This analysis can be of relevant interest when a CHBMI advanced mathematical model is implemented for analysis purposes, or when a DT compensation algorithm must be implemented on a controller.

In the second part of the paper, DT impact on the voltage spectrum, and on the converter efficiency is analyzed. With respect to the voltage spectrum analysis, several indexes, i.e., the THD%, the PHD% and THD_{LF}% are adopted and applied to the measured voltages. In detail, in order to evaluate the global effect of the DT on the voltage spectrum, the traditional THD% index is adopted. A common behaviour has been observed among MC-PWM strategies, i.e. the THD% increases as the DT increases; DT impact results more relevant when the amplitude modulation index is very low. This behaviour is emphasized when PS-based schemes are adopted. This behaviour can be justified by a progressive reduction of the fundamental harmonic when the DT increase, which causes an increment of THD%.

In order to evaluate the local DT impact on the voltage spectrums, the PHD% has been adopted. It is interesting to note that, taking into account how PHD% is defined, it is independent by the fundamental harmonic, which is affected by a reduction due to the DT; therefore, it allows investigation of the distorting effect of the DT.

Results show that, when LS-PWM strategies are adopted, the PHD% values do not vary considerably over the modulation index for fixed values of the DT and switching frequency. The DT effect becomes evident when PS-PWM and SCAMOD are adopted. It is interesting to note that in the first group of the harmonics centered at four ($k_h = 4$) and two ($k_h = 2$) times of the switching frequency, respectively, the DT generates a beneficial effect by reducing the PHD% values. In other harmonic groups, the DT generates an increase in the PHD% values.

Subsequently, also the effect of the DT on the low-frequency harmonics has been investigated. From the analysis of the harmonic spectrums, it emerged that odd harmonics from the 5^{th} to the 23^{rd} result predominant with respect to the other high-frequency harmonics, in all modulation techniques considered; however, it is not possible to recognize a pattern in harmonics amplitude variation in this range. For this reason, a low-frequency THD has been defined by considering harmonics from the 5^{th} to the 23^{rd}. It allows to investigate the overall low-frequency voltage harmonics distortion by providing information about the DT impact without considering the real harmonics distribution in the frequency domain. In this case, in the low-order harmonics, the DT impact is evident in all modulation schemes considered. In particular, it emerged that low-order harmonics amplitude is mitigated when SFO modulating signals are adopted. Moreover, the worst results have been obtained with SCAMOD-based schemes where the DT impact is more evident also for lower values of the modulation index.

Finally, the effect of the DT has been studied also in the conversion efficiency. From the experimental results emerged that in the LS-PWM-based schemes, the DT impact is negligible in all working points considered. When the SPS modulation scheme is adopted, the DT effect is responsible for a drastic reduction of the converter efficiency. When SCA-PWM is adopted, DT impact is less evident with respect to the PS-based schemes. Indeed, only for lower values of the modulation index, the DT generates a significant reduction of the conversion efficiency. By employing SFO as modulation signals the DT effects on the converter efficiency can be reduced, as shown in the experimental tests.

Exactly as the voltage drop analysis, also the spectra and efficiency analysis confirm the strong correlation between the main modulation strategy parameters, i.e. the chosen MC-PWM scheme, the switching frequency and the DT, with the converter performance, in terms of voltage harmonic content and converter efficiency. Thus, these results represent complementary tools, with respect to the DT fundamental harmonic voltage drop estimation, and allow to expand the range of analysis and choice tools in CHBMI design. These

tools allow to satisfy several goals, which depends on the specific application, such as the power quality in the grid-connected application, or to improve motor performance and efficiency in electric drive applications.

In future works, the authors will exploit the analysis carried out and the voltage drop formulation proposed for the definition of innovative DT compensation strategies. In detail, the study will focus on a generical approach suitable for all CHBMI topological structures defined as a function of voltage levels number and by considering both symmetrical and asymmetrical structures.

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REFERENCES

[1] J. I. Leon, S. Kouro, L. G. Franquelo, J. Rodriguez, and B. Wu, "The essential role and the continuous evolution of modulation techniques for voltage-source inverters in the past, present, and future power electronics," *IEEE Trans. Ind. Electron.*, vol. 63, no. 5, pp. 2688–2701, May 2016.

[2] M. Zand, M. A. Nasab, H. R. Hanif, M. R. Ghahri, S. Padmanaban, and B. Khan, "A hybrid scheme for optimal performance of photovoltaic system converters with multilayer structure," *J. Eng.*, vol. 2023, no. 1, pp. 1–10, Jan. 2023.

[3] W. Choi, W. Lee, D. Han, and B. Sarlioglu, "New configuration of multifunctional grid-connected inverter to improve both current-based and voltage-based power quality," *IEEE Trans. Ind. Appl.*, vol. 54, no. 6, pp. 6374–6382, Nov./Dec. 2018.

[4] S. Choudhury, M. Bajaj, T. Dash, S. Kamel, and F. Jurado, "Multilevel inverter: A survey on classical and advanced topologies, control schemes, applications to power system and future prospects," *Energies*, vol. 14, no. 18, p. 5773, Sep. 2021.

[5] S. Shuvo, E. Hossain, T. Islam, A. Akib, S. Padmanaban, and M. Z. R. Khan, "Design and hardware implementation considerations of modified multilevel cascaded h-bridge inverter for photovoltaic system," *IEEE Access*, vol. 7, pp. 16504–16524, 2019.

[6] A. Bughneda, M. Salem, A. Richelli, D. Ishak, and S. Alatai, "Review of multilevel inverters for PV energy system applications," *Energies*, vol. 14, no. 6, p. 1585, Mar. 2021.

[7] T. H. Nguyen, K. Al Hosani, M. S. El Moursi, and F. Blaabjerg, "An overview of modular multilevel converters in HVDC transmission systems with STATCOM operation during pole-to-pole DC short circuits," *IEEE Trans. Power Electron.*, vol. 34, no. 5, pp. 4137–4160, May 2019.

[8] A. I. Elsanabary, G. Konstantinou, S. Mekhilef, C. D. Townsend, M. Seyedmahmoudian, and A. Stojcevski, "Medium voltage large-scale grid-connected photovoltaic systems using cascaded H-bridge and modular multilevel converters: A review," *IEEE Access*, vol. 8, pp. 223686–223699, 2020.

[9] Y. Yu, G. Konstantinou, B. Hredzak, and V. G. Agelidis, "Power balance optimization of cascaded H-bridge multilevel converters for large-scale photovoltaic integration," *IEEE Trans. Power Electron.*, vol. 31, no. 2, pp. 1108–1120, Feb. 2016.

[10] B. L. Xiao, L. Hang, C. Riley, L. M. Tolbert, and B. Ozpineci, "Modular cascaded H-bridge multilevel PV inverter with distributed MPPT for grid-connected applications," *IEEE Trans. Ind. Appl.*, vol. 51, no. 2, pp. 1722–1731, Mar. 2015.

[11] B. Singh, R. Kumar, and P. Kant, "Adjustable speed induction motor drive fed by 13-level cascaded inverter and 54-pulse converter," *IEEE Trans. Ind. Appl.*, vol. 58, no. 1, pp. 890–900, Jan./Feb. 2022.

[12] A. Marzoughi, R. Burgos, and D. Boroyevich, "Investigating impact of emerging medium-voltage SiC MOSFETs on medium-voltage high-power industrial motor drives," *IEEE J. Emerg. Sel. Topics Power Electron.*, vol. 7, no. 2, pp. 1371–1387, Jun. 2019.

[13] F. Chang, O. Ilina, M. Lienkamp, and L. Voss, "Improving the overall efficiency of automotive inverters using a multilevel converter composed of low voltage Si MOSFETs," *IEEE Trans. Power Electron.*, vol. 34, no. 4, pp. 3586–3602, Apr. 2019.

[14] V. Patel, M. Tinari, C. Buccella, and C. Cecati, "Analysis on multilevel inverter powertrains for E-transportation," in *Proc. IEEE 13th Int. Conf. Compat., Power Electron. Power Eng. (CPE-POWERENG)*, Apr. 2019, pp. 1–6.

[15] V. Patel, C. Buccella, A. M. Saif, M. Tinari, and C. Cecati, "Performance comparison of multilevel inverters for E-transportation," in *Proc. Int. Conf. Electr. Electron. Technol. Automot.*, Jul. 2018, pp. 1–6.

[16] A. Poorfakhraei, M. Narimani, and A. Emadi, "A review of multilevel inverter topologies in electric vehicles: Current status and future trends," *IEEE Open J. Power Electron.*, vol. 2, pp. 155–170, 2021.

[17] C. Buccella, C. Cecati, M. G. Cimoroni, A. Damiano, S. Korjani, M. Porru, and A. Serpi, "A cascade multilevel configuration for commercial transport aircraft," in *Proc. AEIT Int. Annu. Conf.*, Oct. 2018, pp. 1–5.

[18] A. Poorfakhraei, M. Narimani, and A. Emadi, "A review of modulation and control techniques for multilevel inverters in traction applications," *IEEE Access*, vol. 9, pp. 24187–24204, 2021.

[19] L. Liu, H. Li, S.-H. Hwang, and J.-M. Kim, "An energy-efficient motor drive with autonomous power regenerative control system based on cascaded multilevel inverters and segmented energy storage," *IEEE Trans. Ind. Appl.*, vol. 49, no. 1, pp. 178–188, Jan./Feb. 2013.

[20] M. Ahmed, "General mathematical solution for selective harmonic elimination," *IEEE J. Emerg. Sel. Topics Power Electron.*, vol. 8, no. 4, pp. 4440–4456, Dec. 2020.

[21] E.-J. Lee, S.-M. Kim, and K.-B. Lee, "Modified phase-shifted PWM scheme for reliability improvement in cascaded H-bridge multilevel inverters," *IEEE Access*, vol. 8, pp. 78130–78139, 2020.

[22] S.-M. Kim, J.-S. Lee, and K.-B. Lee, "A modified level-shifted PWM strategy for fault-tolerant cascaded multilevel inverters with improved power distribution," *IEEE Trans. Ind. Electron.*, vol. 63, no. 11, pp. 7264–7274, Nov. 2016.

[23] A. Busacca, A. O. Di Tommaso, R. Miceli, C. Nevoloso, G. Schettino, G. Scaglione, F. Viola, and I. Colak, "Switching frequency effects on the efficiency and harmonic distortion in a three-phase five-level CHBMI prototype with multicarrier PWM schemes: Experimental analysis," *Energies*, vol. 15, no. 2, p. 586, Jan. 2022.

[24] U. Abronzini, C. Attaianese, M. D'Arpino, M. Di Monaco, and G. Tomasso, "Steady-state dead-time compensation in VSI," *IEEE Trans. Ind. Electron.*, vol. 63, no. 9, pp. 5858–5866, Sep. 2016.

[25] Z. Zhang and L. Xu, "Dead-time compensation of inverters considering snubber and parasitic capacitance," *IEEE Trans. Power Electron.*, vol. 29, no. 6, pp. 3179–3187, Jun. 2014.

[26] Y. Yang, K. Zhou, H. Wang, and F. Blaabjerg, "Harmonics mitigation of dead time effects in PWM converters using a repetitive controller," in *Proc. IEEE Appl. Power Electron. Conf. Exposit. (APEC)*, Mar. 2015, pp. 1479–1486.

[27] M. A. Herran, J. R. Fischer, S. A. Gonzalez, M. G. Judewicz, and D. O. Carrica, "Adaptive dead-time compensation for grid-connected PWM inverters of single-stage PV systems," *IEEE Trans. Power Electron.*, vol. 28, no. 6, pp. 2816–2825, Jun. 2013.

[28] S. Ahmed, Z. Shen, P. Mattavelli, D. Boroyevich, and K. J. Karimi, "Small-signal model of voltage source inverter (VSI) and voltage source converter (VSC) considering the DeadTime effect and space vector modulation types," *IEEE Trans. Power Electron.*, vol. 32, no. 6, pp. 4145–4156, Jun. 2017.

[29] S. M. Dehghan and K. Fujisaki, "Impact of dead-time on iron losses in inverter-fed magnetic materials," in *Proc. IEEE Energy Convers. Congr. Exposit.*, Sep. 2013, pp. 3166–3171.

[30] A. Guha and G. Narayanan, "Small-signal stability analysis of an open-loop induction motor drive including the effect of inverter deadtime," *IEEE Trans. Ind. Appl.*, vol. 52, no. 1, pp. 242–253, Jan./Feb. 2016.

[31] A. Guha and G. Narayanan, "Impact of undercompensation and overcompensation of dead-time effect on small-signal stability of induction motor drive," *IEEE Trans. Ind. Appl.*, vol. 54, no. 6, pp. 6027–6041, Nov./Dec. 2018.

[32] J. Bacmaga, R. Blecic, F. Pareschi, G. Setti, and A. Baric, "Impact of dead times on radiated emissions of integrated and discrete DC–DC converter," in *Proc. 12th Int. Workshop Electromagn. Compat. Integr. Circuits (EMC Compo)*, Oct. 2019, pp. 266–268.

[33] A. Guha and G. Narayanan, "Impact of dead-time on inverter input current, DC-link dynamics and light-load instability in rectifier-inverter-fed induction motor drives," in *Proc. Int. Symp. Power Electron., Electr. Drives, Autom. Motion (SPEEDAM)*, Jun. 2016, pp. 1249–1254.
[34] J. Patel and V. K. Sood, "Impact of dead-band time on the harmonic spectrum of power converters," in *Proc. IEEE Electric Power Energy Conf. (EPEC)*, Nov. 2020, pp. 1–7.
[35] A. Mora, J. Juliet, A. Santander, and P. Lezana, "Dead-time and semiconductor voltage drop compensation for cascaded h-bridge converters," *IEEE Trans. Ind. Electron.*, vol. 63, no. 12, pp. 7833–7842, Dec. 2016.
[36] B. Li, J. Xu, J. Ye, H. Wang, S. Huang, Y. Li, and A. Shen, "A new model-based dead-time compensation strategy for cascaded H-bridge converters," *IEEE Trans. Ind. Electron.*, vol. 70, no. 4, pp. 3793–3802, Apr. 2023.
[37] N. Diao, X. Sun, C. Song, Q. Zhang, and Z. Zhang, "A multimodulation times SVPWM for dead-time effect elimination in three-level neutral point clamped converters," *IEEE Trans. Ind. Electron.*, vol. 68, no. 7, pp. 5476–5485, Jul. 2021.
[38] G. Schettino, C. Nevoloso, R. Miceli, A. O. Di Tommaso, G. Scaglione, C. Cecati, and C. Buccella, "Experimental comparative analysis of efficiency and THD for a three-phase five-level cascaded H-bridge inverter controlled by several MC-PWM schemes," in *Proc. 47th Annu. Conf. IEEE Ind. Electron. Soc.*, Oct. 2021, pp. 1–6.
[39] G. Schettino, C. Nevoloso, R. Miceli, A. O. Di Tommaso, G. Scaglione, F. Viola, C. Buccella, and M. G. Cimoroni, "Experimental evaluation of dead-time impacts on the efficiency and THD for a three-phase five-level cascaded H-Bridge inverter," in *Proc. IEEE 21st Medit. Electrotechnical Conf. (MELECON)*, Jun. 2022, pp. 1091–1096.
[40] C. Nevoloso, G. Schettino, G. Scaglione, A. O. Di Tommaso, R. Miceli, F. Viola, and A. Busacca, "Implementation on NI-SOM sbRIO-9651 and experimental validation of multi-carrier PWM techniques for three-phase five level cascaded H-bridge inverter," in *Proc. 10th Int. Conf. Renew. Energy Res. Appl. (ICRERA)*, Sep. 2021, pp. 276–281.
[41] G. Holmes and T. A. Lipo, *Pulse Width Modulation for Power Converters: Principle and Practice*. Piscataway, NJ, USA: IEEE Press, 2003.
[42] A. Arranz-Gimon, A. Zorita-Lamadrid, D. Morinigo-Sotelo, and O. Duque-Perez, "A review of total harmonic distortion factors for the measurement of harmonic and interharmonic pollution in modern power systems," *Energies*, vol. 14, no. 20, p. 6467, Oct. 2021.

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