IEEE Access
Multidisciplinary ⋮ Rapid Review ⋮ Open Access Journal

Received 3 March 2023, accepted 17 March 2023, date of publication 27 March 2023, date of current version 30 March 2023.

Digital Object Identifier 10.1109/ACCESS.2023.3262307

RESEARCH ARTICLE

A 50-1600 MHz Wide-Range Digital Duty-Cycle Corrector With Counter-Based Half-Cycle Delay Line

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This work was supported by the Institute of Information & communications Technology Planning & Evaluation (IITP) grant funded by the Ministry of Science and ICT (MSIT) under Grant 2020-0-01300 and Grant 2022-0-01013.

ABSTRACT Duty-cycle distortion may occur due to variations in the process, voltage, and temperature, or if the clock signal passes through clock buffers. To compensate duty-cycle distortion, a digital duty-cycle corrector (DCC) with counter-based half-cycle delay line (HCDL) is introduced. The HCDL of conventional edge combiner type DCC requires a large area and make the DCC unsuitable for applications that operate in a wide-range frequency. The proposed counter-based HCDL reduces the silicon cost by repeating the delay line, while maintaining the performance of conventional DCC. A prototype chip fabricated in a 65nm CMOS process has an area of 0.0064mm^2 and consumes 2.1mW at 1.6GHz. The measurement results show that the duty-cycle error is less than 0.89% over an input duty-cycle range of 20-80% for 50-1600MHz.

INDEX TERMS Memory interface, ADC interface, digital duty-cycle corrector (DCC), half-cycle delay line (HCDL).

I. INTRODUCTION

The ratio between the pulse width and the period of the clock signal is called duty-cycle. In various applications, performance is affected by the duty-cycle of the clock signal [1]. Double data-rate (DDR) and quad data-rate (QDR) architectures are now common for dynamic random access memory (DRAM). As the internal clock frequency is reduced, the power consumption and the timing margin are relaxed. These structures require an accurate duty-cycle of the clock for data sampling or transmitting [2]. Similar approaches have been taken in analog-to-digital converters (ADCs). Double-sampling techniques are used in various ADCs to reduce power consumption [3]. Also, these techniques are used in pipelined ADCs to share op-amps, which can bring advantage to the area [4]. Double-sampling techniques and shared op-amps use clock rising and falling edges, making the duty-cycle of the clock important.

The duty-cycle can become distorted inside the applications because of process, voltage and temperature variation. And this distortion is likely to be larger for a more complicated clock tree. As the clock duty-cycle distortion affects circuit performance, it is necessary to compensate for the duty-cycle distortion. For this reason, these applications such as the DRAM and the ADC introduce DCC for accurate duty-cycle of the clock signal [5]. The operating frequency of the DRAMs is at the GHz level, and the ADCs mostly use the MHz clocks. Therefore, DCC can be operational in wide-range frequency to be compatible with various applications.

DCC is divided into analog [6], [7] and digital [1], [8], [9], [10], [11], [12] types according to the method of detecting the duty-cycle of the signal. Since analog DCC detects the duty-cycle by using capacitors, it takes a long time to settle and may cause duty fluctuations due to leakage current [11]. Thus, digital DCC is preferred in various applications, which

The associate editor coordinating the review of this manuscript and approving it for publication was Poki Chen.

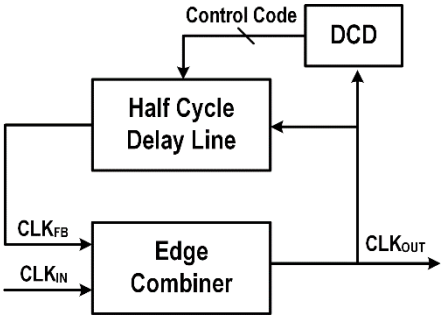


FIGURE 1. Block diagram of the conventional DCC with HCDL.

is advantageous for maintaining duty-cycle corrected information, considering standby mode or power down mode [12]. In digital DCCs, there are methods using phase interpolation (PI) [8], [9] and HCDL [1], [10], [11], [12]. The conventional PI method consists of tied two inverters with an output capacitor. However, the interpolation capacity is a trade-off with operating frequency, and PI performance varies for each frequency range [8]. Therefore, DCC using PI may not be suitable for wide-range applications.

Another digital DCC is a scheme that adjusts the duty-cycle using HCDL. Fig. 1 shows the block diagram of conventional DCC with HCDL. HCDL delays the rising edge of CLK_{OUT} by as much as half a cycle of the current operating frequency. In the case of DCC with conventional HCDL, the HCDL should be able to cover the delay of half-period of the lowest operating frequency. As mentioned before, in order to use DCC in various applications, wide-range frequency operation from several MHz frequency bands to GHz must be possible. However, the area of HCDL in DCC increases to cover the low-frequency-range. Therefore, the silicon cost of HCDL can be a burden when applying it to various applications. In addition, as the area of the delay line increases, the training time to find the accurate duty-cycle may also increase.

To overcome the drawbacks described above, we propose a counter-based HCDL to solve the above disadvantage in digital DCC using HCDL. Through the counter-based HCDL, DCC can operate in a wide frequency range while resolving area requirements. The operation of the proposed DCC is divided into training operation and normal operation. In the training operation, the repeating times, DCDL, and intrinsic delay are adjusted to satisfy the half-cycle delay. To reduce power and area cost, a method of training using the bang-bang duty-cycle detector is proposed [13]. However, this method has a long lock time when used in wide-range operation. Therefore, we apply the binary search method, which helps minimize the lock time. In normal operation, these parameters are used to correct the duty-cycle of the clock signal.

The rest of this paper is organized as follows: in Section II we describe overall architecture of the proposed DCC with counter-based HCDL and training operation; in Section III we present measurement results, and in Section IV we draw conclusions.

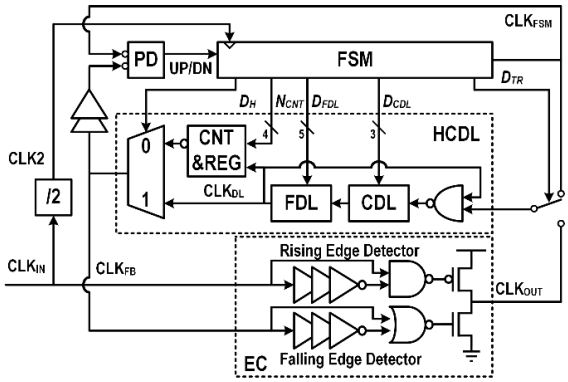


FIGURE 2. Overall architecture of the proposed DCC with counter-based HCDL.

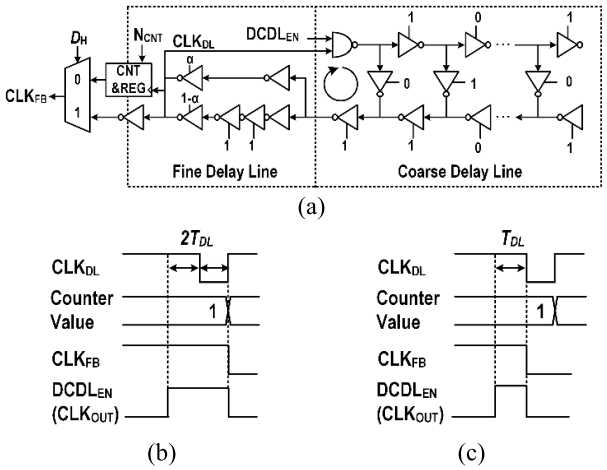


FIGURE 3. Block diagram of (a) the counter-based HCDL and conceptual timing diagram of the half-delay mode (b) off (D_H =0) and (c) on (D_H =1).

II. PROPOSED DUTY-CYCLE CORRECTOR

A. OVERALL DCC ARCHITECTURE

Fig. 2 is a block diagram of the proposed DCC, which consists of an edge combiner (EC), a counter-based HCDL, a switch, a divider, a phase detector (PD), and a finite state machine (FSM). In the EC, a pMOS pull-up transistor is driven by a rising edge detector, and an nMOS pull-down transistor is driven by a falling edge detector. The counter-based HCDL consists of a NAND gate, a coarse delay line (CDL), a fine delay line (FDL), a counter with register (CNT & REG), and a 2:1 multiplexer (MUX).

In order to compensate for drawbacks of the conventional DCC, HCDL is constructed using counter-based HCDL. Fig. 3(a) is a block diagram of our counter-based HCDL. The counter-based HCDL consists of a DCDL and a counter with register. DCDL can be 8-bit controlled, and the counter can count up to 16 to allow for wide-range frequency operation. The counter counts the rising edge of the DCDL and sends this counter value to the register. Then the register compares this value with a 4-bit N_{CNT}. The N_{CNT}, which specifies the number of times the DCDL should be repeated and is obtained through a training operation. If the counter value and N_{CNT} value are the same, the register generates a falling edge to EC. Fig. 3(b) is the timing diagram of when N_{CNT}

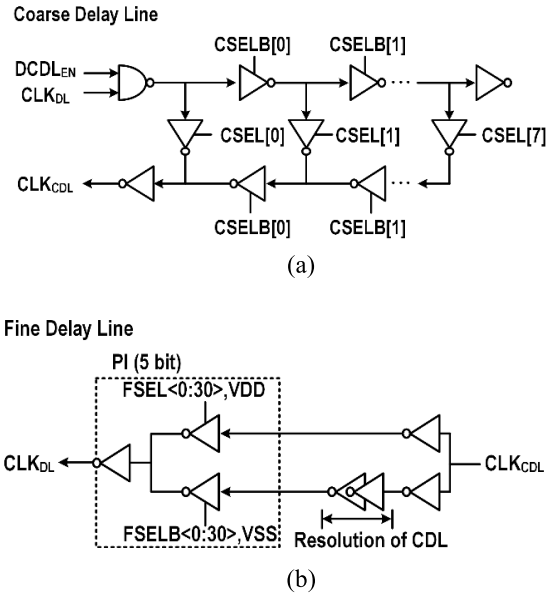


FIGURE 4. Conceptual lock diagram of (a) coarse delay line, (b) fine delay line, and (c) example of the counter-based HCDL.

is 1. For the counter value to be the same as N_{CNT}, the clock signal must pass through the DCDL twice. Once this happens, a falling edge is output to the CLK_{FB} signal. The D_H signal adjusts the half-delay mode because the amount delayed twice may limit the high frequency operation. In the half-delay mode, the D_H signal of Fig. 3(a) is turned on and the DCDL is directly connected to CLK_{FB} without counting. Fig. 3(c) shows the timing diagram when the half-delay mode is on. In this mode, the input clock passes through DCDL only once, enabling the counter-based HCDL to operate as if N_{CNT} is 0.5.

The CDL is constructed as shown in Fig. 4(a). Since the counter counts the rising edge of the DCDL, the data changes every DCDL cycle through NAND gate. The CDL is designed to be 3-bit controllable, and 1 unit of CDL is composed of two stage tri-state inverters. It is possible to adjust up to 8-stage by converting 3-bit into a thermometer code. The accuracy of the DCC is determined by the resolution of the DCDL. To increase the accuracy of DCC, fine adjustment is possible through FDL. The FDL is composed of PI, as shown in Fig. 4(b). In PI operation, one of the two inputs is delayed by about 1 unit of CDL, and the number of tri-state inverters is adjusted according to the selected bits. The PI is designed to be 5-bit controllable and is adjusted through the binary-to-thermometer converter inside the PI. Based on the post-simulation, the resolution of FDL was about 6 ps.

During the training operation, the CLK2 signal generated by the divider is used as a reference clock because obtaining a pulse width of half-period from the duty-cycle distorted input clock can be challenging. Therefore, the CLK2 signal, which changes its value at every rising edge of the input signal, provides a stable reference for the training operation. The PD and the FSM determine the N_{CNT} and the digital codes D_{CDL} and D_{FDL}, which control the delay of the coarse and fine delay

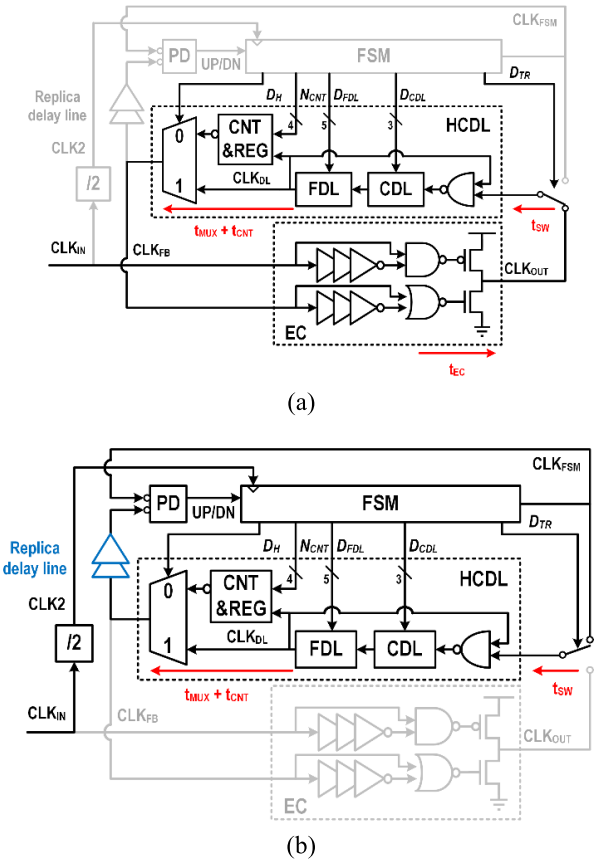


FIGURE 5. Block diagram of the proposed DCC with counter-based HCDL (a) used in normal operation and (b) used in training operation.

lines. In normal operation, the counter counts the number of rising edges of the CLK_{DL} signal, and the register compares this value with N_{CNT}. If the counter value reaches N_{CNT}, the register creates a falling edge to CLK_{FB}.

B. TRAINING OPERATION

For wide-range operation, it is necessary to detect the current operating frequency. The FSM block detects the operating frequency through the training operation. The delay of the counter-based HCDL is then adjusted based on the detected frequency. Fig. 5(a) highlights only the block diagram used in the normal operation. The counter-based HCDL and intrinsic delay, which should be adjusted to half-cycle based on Fig. 5(a), are expressed as follows:

$$0.5T_{REF} = t_{EC} + 2N_{CNT}t_{DL} + t_{CNT} + t_{MUX} + t_{SW} \quad (1)$$

where T_{REF} is the period of CLK_{IN}, and t_{SW}, t_{CNT}, t_{MUX} and t_{EC} marked red in Fig. 5(a) are the intrinsic delay of the switch, the CNT with REG, the 2:1 MUX and the EC, respectively. The variable N_{CNT} determines the number of times that the delay is repeated, and t_{DL} is the sum of the delay provided by CDL and FDL. The counter counts the rising edge of CLK_{DL}, which is the output signal of DCDL. Therefore, the t_{DL} multiplied by 2 goes into the above equation. The values of N_{CNT} and t_{DL} required to satisfy (1) are obtained during the training operation.

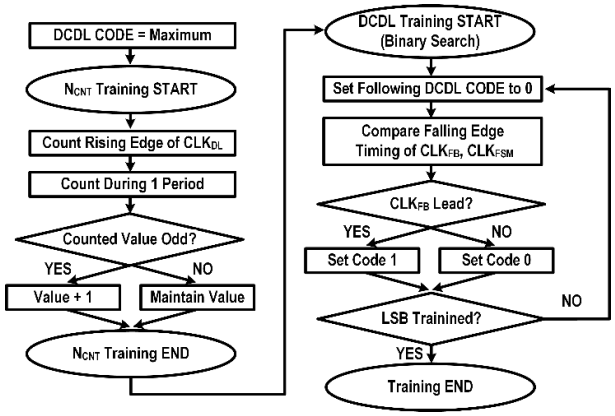
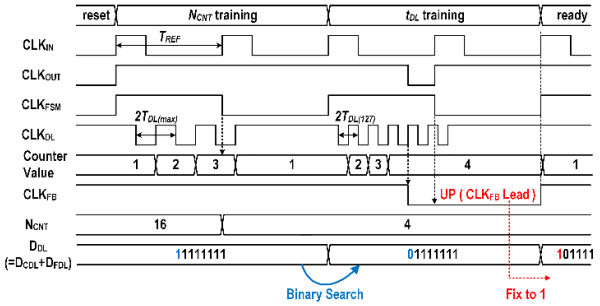
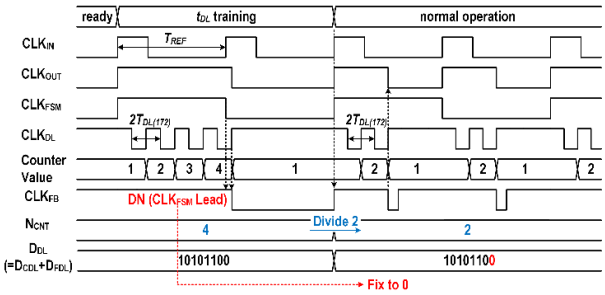


FIGURE 6. Algorithm of the proposed DCC.



(a)



(b)

FIGURE 7. Timing diagram of the proposed DCC with counter-based HCDL (a) N_{CNT} and DCDL training, (b) Normal operation.

During the training operation, a reference signal is required to detect the period of the input signal, but obtaining a pulse width of $0.5T_{REF}$ from a duty-cycle distorted input signal can be challenging. Therefore, the divider creates the CLK2 signal by inverting the data from each rising edge of the input clock. As a result, CLK2 signal has the pulse width of T_{REF}. The FSM block then generates a CLK_{FSM} signal that duplicates the CLK2 signal and uses it as a reference signal. As shown in Fig. 5(b), CLK_{FSM} is divided into two paths. One path creates a standard delay of T_{REF}, while the other goes through a delay of counter-based HCDL used as a training loop. In the training operation, the delay of the training loop should be set to T_{REF}. The delay used in the training loop is expressed as follows:

$$T_{TR} = 2N_{CNT}t_{DL} + t_{CNT} + t_{MUX} + t_{SW} \quad (2)$$

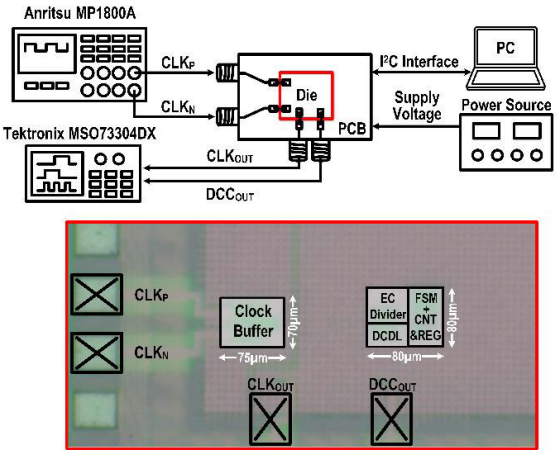


FIGURE 8. Measurement setup and die micrograph.

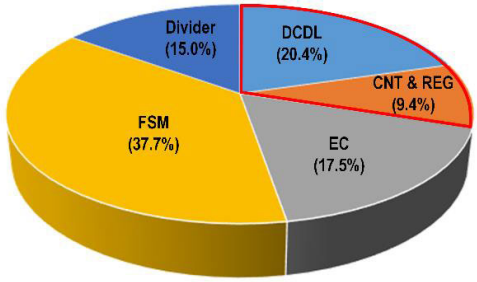


FIGURE 9. Area breakdown of the proposed DCC.

where T_{TR} is the delay of training loop. For accurate training, the mismatch must be removed between the loops used in the training and normal operation. When comparing (1) multiplied by 2 and (2), the delay components of $2N_{CNT}t_{DL}$, t_{SW}, t_{CNT}, t_{MUX} and $2t_{EC}$ in (2) are missing in the training loop. $2N_{CNT}t_{DL}$ is canceled by obtaining the $2N_{CNT}$ value in training operation and applying half the N_{CNT} value in normal operation. To compensate for the remaining intrinsic delays, an additional replica delay line is placed between the FSM and the counter-based HCDL.

Training is preceded to detect operating frequency when the device is turned on or when a reset signal is received. The training algorithm of the proposed DCC is shown in Fig. 6. When the training begins, the DCDL is reset to a digital code with a maximum delay, and N_{CNT} training, a value that repeats the delay, starts. The number of rising edges of CLK_{DL} during the pulse width of CLK_{FSM} is counted, and the counter value is checked at the falling edge of CLK_{FSM}. If N_{CNT} is an odd number other than 1, then it is incremented by 1 to divide N_{CNT} in half in normal operation. If the N_{CNT} value is 1, the D_H signal is turned on, allowing for high-frequency operation by operating in the half-delay mode. After the N_{CNT} value has been fixed, DCDL training starts by changing the digital code of the DCDL to determine the value of t_{DL}. To reduce the locking time of the DCDL, the binary search method is used for t_{DL} training. DCDL training is divided into two phases: a t_{DL} training phase comparing the timing and a ready phase determining the bit value. In the

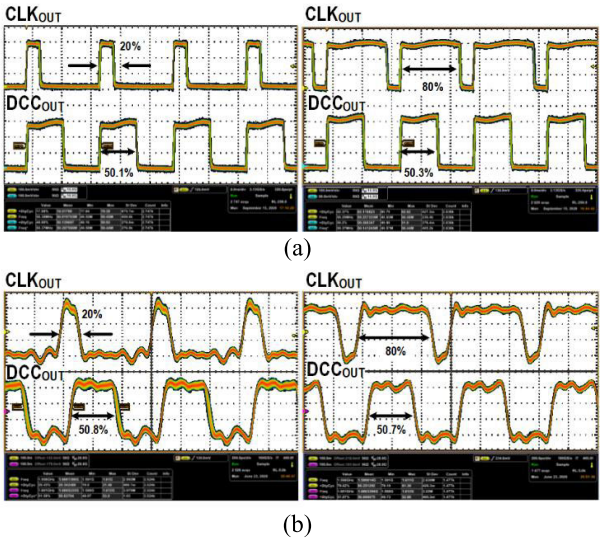


FIGURE 10. Measured input and output clock waveform of proposed DCC at (a) minimum frequency (50MHz) and (b) maximum frequency (1.6GHz).

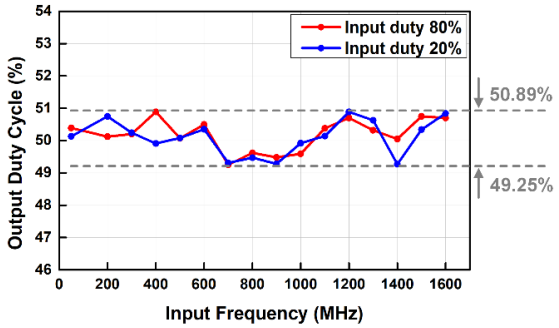


FIGURE 11. Measured results of the duty-cycle every 100MHz.

t_{DL} training phase, PD compares the delay amount of T_{REF} and training loop after changing the MSB of the DCDL code to 0. The delay amount can be compared with the timing of CLK_{FSM} and CLK_{FB}, where CLK_{FSM} has the pulse width of T_{REF}, and CLK_{FB} is delayed by the training loop. In the ready phase, according to the following (3) and (4), the bit previously converted to 0 is determined as 0 or 1.

$$T_{REF} > 2t_{EC} + 4N_{CNT}t_{DL} + 2t_{CNT} + 2t_{MUX} + 2t_{SW} \quad (3)$$

$$T_{REF} < 2t_{EC} + 4N_{CNT}t_{DL} + 2t_{CNT} + 2t_{MUX} + 2t_{SW} \quad (4)$$

The meaning of (3) is that the timing of CLK_{FB} leads the timing of CLK_{FSM}, and in the case of (4), CLK_{FSM} leads. Since the delay of the DCDL should increase when CLK_{FB} leads, the PD sets the previous bit to 1 when the UP signal is generated and keeps it at 0 when the DN signal is generated. The t_{DL} training continues until the LSB is compared. After the LSB training is completed, the overall training operation is finished.

Based on the input signal, N_{CNT} training requires 2 cycles, and DCDL training requires 4 cycles per 1-bit, resulting in a total of 34 cycles for the entire training operation. Fig. 7(a) shows the timing diagram of the training to obtain N_{CNT}, and the value of the MSB. For example, if the counter value is 3,

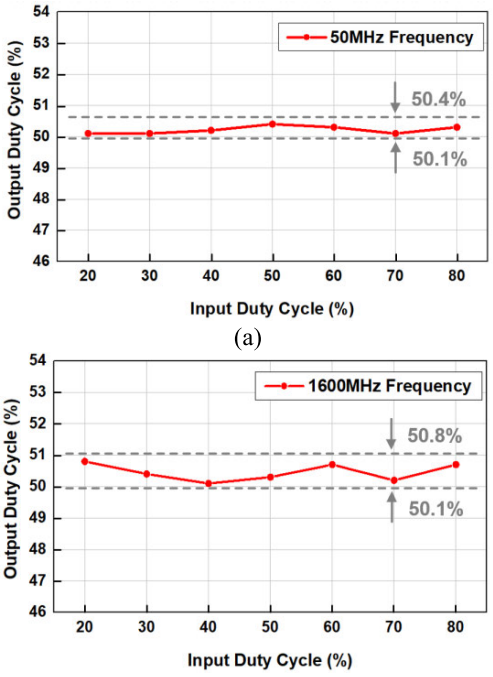


FIGURE 12. Measured results of the output duty-cycle while sweeping input duty-cycle (a) 50MHz and (b) 1.6GHz.

1 is added to make N_{CNT} an even number. After completing N_{CNT} training, the t_{DL} training begins. The MSB value is changed to 0, and the timing of CLK_{FSM} and CLK_{FB} is compared. It is observed that CLK_{FB} is leading, so it is fixed to 1.

C. NORMAL OPERATION

Fig. 5(a) highlights the blocks used during normal operation. As mentioned earlier, the block diagram shows the delay components that are involved in normal operation, including the intrinsic delay. During normal operation, the EC generates a rising edge of the CLK_{OUT} by detecting the rising edge of the CLK_{IN} and then enters the DCDL. After repeating DCDL as many times as N_{CNT}, the counter-based HCDL generates a falling edge to CLK_{FB} and the EC generates the falling edge to CLK_{OUT}. When the counter-based HCDL needs to generate a short delay for high-frequency operation, the D_H signal makes the first falling edge of CLK_{DL} using the MUX.

The timing diagram in Fig. 7(b) shows that the DCC enters normal operation after LSB training. When entering normal operation, the value of N_{CNT} is halved because the counter-based HCDL requires a delay of $0.5T_{REF}$ instead of T_{REF}. Since the N_{CNT} value was set to an even number during the training operation, it is divided by 2 and normal operation proceeds. As shown in the timing diagram, the N_{CNT} value is initially set to 4 during the training operation and is then changed to 2 during normal operation. The digital codes of the DCDL, which were determined during the t_{DL} training, remain unchanged during normal operation.

TABLE 1. Performance summary and comparison with other digital DCC designs.

	[8]	[1]	[10]	[11]	[12]	This Work
Types	PI	HCDL	HCDL	HCDL	HCDL	Counter-based HCDL
Process (nm)	55	65	180	90	130	65
Supply voltage (V)	1	1	1.8	1	1.2	1
Frequency (MHz)	333~1000	262~1020	400~2000	75~734	350~1000	50~1600
Input duty-cycle range (%)	20 ~ 80	14~86	20~80	9 ~ 86	10 ~ 90	20 ~ 80
Max. output duty-cycle Error (%)	1.4	1.6	3.5	1.78	1.4	0.89
RMS jitter (ps)	-	3.23 @1020MHz	3.5 @1000MHz	4.11 @734MHz	2.901 @1000MHz	2.23 @1600MHz
Pk-Pk jitter (ps)	12.53 @1000MHz	23.64 @1020MHz	28.45 @1000MHz	27.13 @734MHz	20.5 @1000MHz	14.8 @1600MHz
Power consumption (mW)	2.09 @1000MHz	6.5 @ 1020MHz	1.76 @400MHz 3.6 @2000MHz	0.9 @75MHz 4.59 @734MHz	5.6 @1000MHz	2.1 @1600MHz
[a]Normalized power (mW)	3.95	10.20	0.32	7.23	3.11	2.1
Area (mm^2)	0.0186	0.01	0.025	0.0289	0.059	0.0064

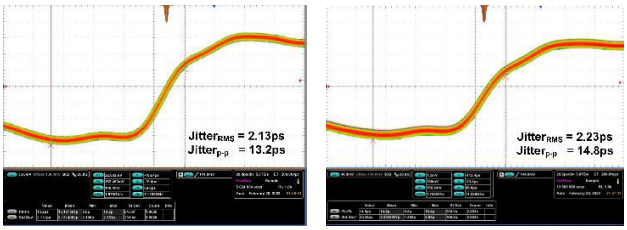
[a] $NP = P \times \left(\frac{0.65}{Technology}\right) \times \left(\frac{1.0}{VDD}\right)^2 \times \frac{1600}{F_{max}}$

III. MEASUREMENT RESULTS

The proposed DCC is fabricated in CMOS 65nm process and operated with a supply voltage of 1 V. Fig. 8 shows the die micrograph and the measurement setup. A power source generates the supply voltage for the chip. The differential clock signal CLK_P and CLK_N are supplied by a clock source (Anritsu MP1800A). The clock source intentionally distorts the duty-cycle of the differential clock signal to verify the performance of our DCC. Either of these signals is measured as CLK_{OUT} before entering the DCC with only the clock buffer passed through. The DCC_{OUT} signal is the output signal from the proposed DCC, and it is measured using an oscilloscope (Tektronix MSO733404DX).

The area breakdown of the DCC is shown in Fig. 9. The total area of the proposed DCC is 0.0064mm^2 without clock buffer. The DCDL accounts for 20.4% of the total area, with 29.8% of it including the counter with register. By setting the maximum value of N_{CNT} to 16, the proportion of area of the delay line could be reduced by about 32 times.

The following Fig. 10 shows the output clock signal through an oscilloscope when the input clock has a duty-cycle of 20 or 80% at the minimum and maximum frequency. In the upper figure of Fig. 10(a), the duty-cycle of the clock signal with a frequency of 50 MHz that has passed through the clock buffer is distorted. The results of the duty-cycle are compensated to 50.1% and 50.3%, as shown in the below figure. The measured waveforms of the input and the output duty-cycle at 1.6 GHz frequency are shown in Fig. 10(b). Based on the results of the training operation, the duty-cycle of the output clock signal is adjusted to within 0.8%.



(a) (b)

FIGURE 13. Jitter histogram of (a) the input clock and (b) the proposed DCC at 1.6GHz.

Fig. 11 shows the measured output clock duty-cycle of the proposed DCC for input clock duty-cycles of 20% and 80% at different frequencies ranging from 50 MHz to 1.6 GHz. The results show that the DCC is able to correct the duty-cycle with an error of up to 0.89%.

Fig. 12 shows the results of sweeping the input duty-cycle from 20% to 80% in steps of 10%, and measuring the output duty-cycle at the minimum and maximum operating frequencies. The graph shows that the DCC can correct duty-cycle errors up to 30%, with a maximum error of only 0.8%, regardless of frequency.

Fig. 13 shows the measured jitter of the input clock and the output clock at 1.6GHz, which is the maximum frequency of the DCC. As shown in Fig. 13(a), the RMS and peak-to-peak jitter of the input clock are measured as 2.13ps_{rms} and 13.2ps_{pp}. The jitters of the output clock slightly increase to 2.23ps_{rms} and 14.8ps_{pp}, respectively, as shown in Fig. 13(b).

Table 1 compares the proposed DCC with other digital DCCs. Our circuit offers a wider operating frequency range compared to other DCCs when comparing the maximum and

minimum frequency ratios. By using Counter-based HCDL, it is possible to minimize area cost. For fair performance comparison, the normalized power (NP) is inserted with reference to [11]. Digital DCC [10] showed good performance in terms of NP. However, due to its coarse-tuning, it can be seen that it is not as effective in output duty-cycle errors.

IV. CONCLUSION

A 50-1600 MHz digital DCC with counter-based HCDL is presented. By using counter-based HCDL, it was able to correct a wide-range of input frequency while consuming less silicon cost. The total area of the proposed DCC is 0.0064mm^2, and the proportion of area occupied by DCDL can be reduced with the counter-based HCDL. Also, according to the training operation, it can settle in various operating frequencies within 34-cycle. A prototype implementation of our DCC corrected duty-cycle errors to within 0.89% of 50% over operating frequencies ranging from 50 MHz to 1.6 GHz, consuming 2.1 mW at 1.6 GHz.

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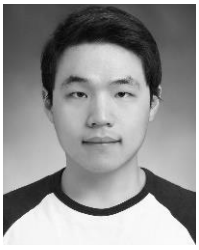

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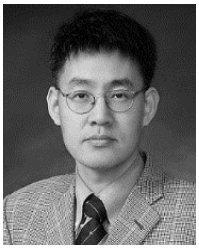

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