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TOPICAL REVIEW

Design and Implementation of Hybrid DC-DC Converter: A Review

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ABSTRACT The advancement in Power Management Integrated Circuit (PMIC) has driven the dc-dc conversion technology into a System-on-Chip (SoC) solutions, leveraging CMOS technology scaling from 180nm to 22nm and on-chip passive element integration. Concurrently, as the applications demand smaller form factor solution towards device portability with optimized power qualities, switched-capacitor-inductor hybrid architectures with fully-integrated passives have become a popular choice for a compact and high efficiency converter solution, in contrast to bulky and discrete component based alternatives. This article reviews the latest advancements in hybrid dc-dc topologies, specifically for low-power applications to address the downsides such as charge sharing loss, high current ripple, limited conversion ratio, low-power density, and efficiency. An overview of capacitor and inductor technology is discussed in terms of on-chip parasitic losses, and miniaturization. A comprehensive comparison in the state-of-the-art hybrid dc-dc converter work is tabulated with power density and efficiency as the primary performance metrics, highlighting their operability in low-power applications. Moreover, a discussion is included with quantified benchmarks to justify the viability of converters, along with the future recommendation of realizing ultra-high switching frequency for smaller footprint inductor and design approach to resolve the current tradeoff bottlenecks.

INDEX TERMS Power management integrated circuit (PMIC), system-on-chip (SoC), hybrid DC-DC converters, power efficiency, power density, transient response.

I. INTRODUCTION

Power Management technology is advancing exponentially due to the elevated demand of diverse applications ranging from high-power electric vehicles (EVs) to ultra-low-power wearable electronic devices. This suggests the power electronic technology needs a versatility of Power Management Integrated Circuit (PMIC) implementation in the context of multiple configuration such as fully discrete, partial-integrated, and fully-integrated solution. However, integrated solution have drawn favorable attention due to the advantage of small form factor by embedding on-chip integration to reduce the implementation cost and area in a System-on-Chip (SoC) modules [1]. Nevertheless, capacitors are more favorable in a miniaturized fully-integrated technology for diversified applications such as Internet of Things (IoT) [2]. Alternatively, applications toward high switching frequency to relieve the area penalty is dominated by on-chip inductor integration. The co-design of voltage regulator and dc-dc converter improves the performance significantly with the respective size scaled down adopting strategic design techniques and topologies. Generally, functional circuits such as

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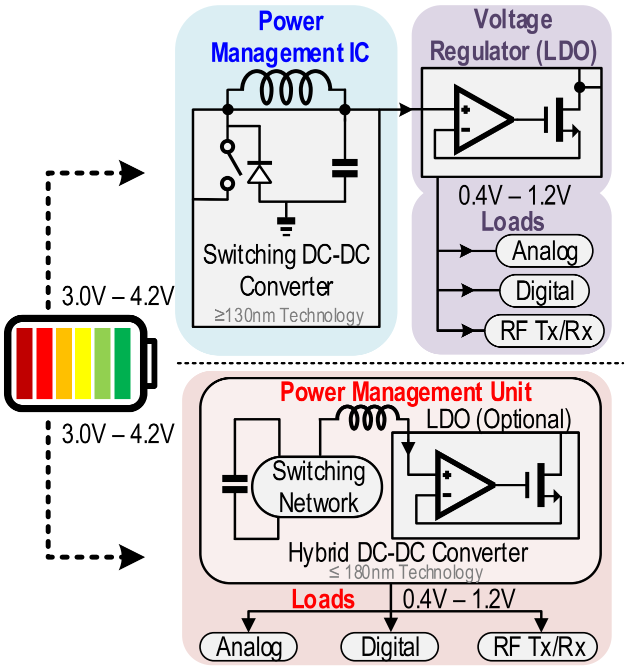

FIGURE 1. Conventional PMIC & PMU architecture in SoC technology.

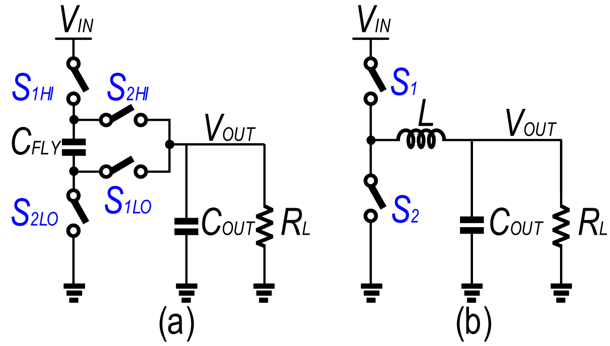

FIGURE 2. Fundamental switching DC-DC converters. (a) switched-capacitor (SC) converter (b) Switched-Inductor (SI) converter.

Radio-Frequency (RF) front end, processors, memory, and control unit operate in the range of 0.4V to 1.2V in a SoC enabled from a 3.0V to 4.2V lithium battery (Fig. 1). The dc-dc converter steps up or down the supply voltage level based on various application prior in delivering the power directly to the loads. Most of the SoC design consists of point-of-load voltage regulators to optimize each voltage domain independently. Hence, the research and development of a fully-integrated power converter has drawn enormous attention in terms of topological design, control scheme and performance enhancement.

The key performance index in the power converter design consists three major parameters, which is the efficiency, transient response, and power density [3]. In compromise of performance tradeoffs, fully-integrated dc-dc converter plays a vital role in SoC with a small form factor in providing a regulated voltage for point-of-load application [4], [5]. Among the dc-dc converter architectures, hybrid dc-dc converter topology shows superior balance in high efficiency and power density with an optimized tradeoff in favorable degree among the linear and switching topology. The hybrid converter is associated with the inductor and flying capacitor to realize the soft-charging, hence alleviating charge sharing loss, commonly suffered by Switched-capacitor (SC) and resonant SC converters. In addition, the flying capacitor transfers the charge from the input source while the inductor extends the voltage conversion ratio (VCR) with a proper duty-cycle. This realizes a smaller footprint inductor with lower dc resistance (DCR) [4].

Typically, a low-dropout (LDO) regulator is widely used as a point-of-load regulator due to fast transient response and excellent noise rejection with compact area implementation at the cost of low efficiency, especially when the VCR is low [6]. Meanwhile, switching regulators exploit energy storing devices such as capacitors, inductors, or transformers to store the input source periodically and transfer the desired voltage level to the output based on the design specification. SC converter (Fig. 2(a)) inherits the property of multiple VCRs but deteriorates in power density and efficiency due to the increase in component counts and charge sharing loss [7]. Alternately, the switched-inductor (SI) converter (Fig. 2(b)), commonly known as buck-boost converter is capable of operating with high efficiency over a dynamic range of VCR; unlike the SC converter which only exhibits high efficiency at a particular VCR. Pulse-width modulation (PWM) controls switches by modifying the switching frequency, duty-cycle, D and defining the operation states. Specifically, the VCR can be fully controlled by varying the duty-cycle in continuous conduction mode (CCM). However, off-chip inductors used in SI converters with high Q-factor degrade power density due to area constraint. Therefore, the SC converter shows high popularity in fully-integrated solutions due to its small form factor, but the extension of VCR requires additional flying capacitors. In short, dc-dc converters suffer from an inherent tradeoff between power density and efficiency.

Hybrid topology of dc-dc power converters exploit the benefits of both the SC and SI converters have been gaining popularity in recent years [4]. Specifically, the configuration of flying capacitor in SC topology reduces voltage stress on the switching transistors while transferring the charge to the output node. Meanwhile, inductor in SI topology generates a low output voltage ripple and high efficiency with wide scalable VCR by modifying the duty-cycle of PWM. As the effective switching frequency generated from the inductor-capacitor (LC) circuit configuration achieves soft switching, the charge sharing loss in the flying capacitor can be alleviated. Therefore, the size of the integrated on-chip inductor can be scaled down under a soft charging mechanism.

This article provides an overview of hybrid dc-dc converters especially for fully-integrated implementation in CMOS technology. Section II introduces several mainstream hybrid dc-dc converters with their respective design

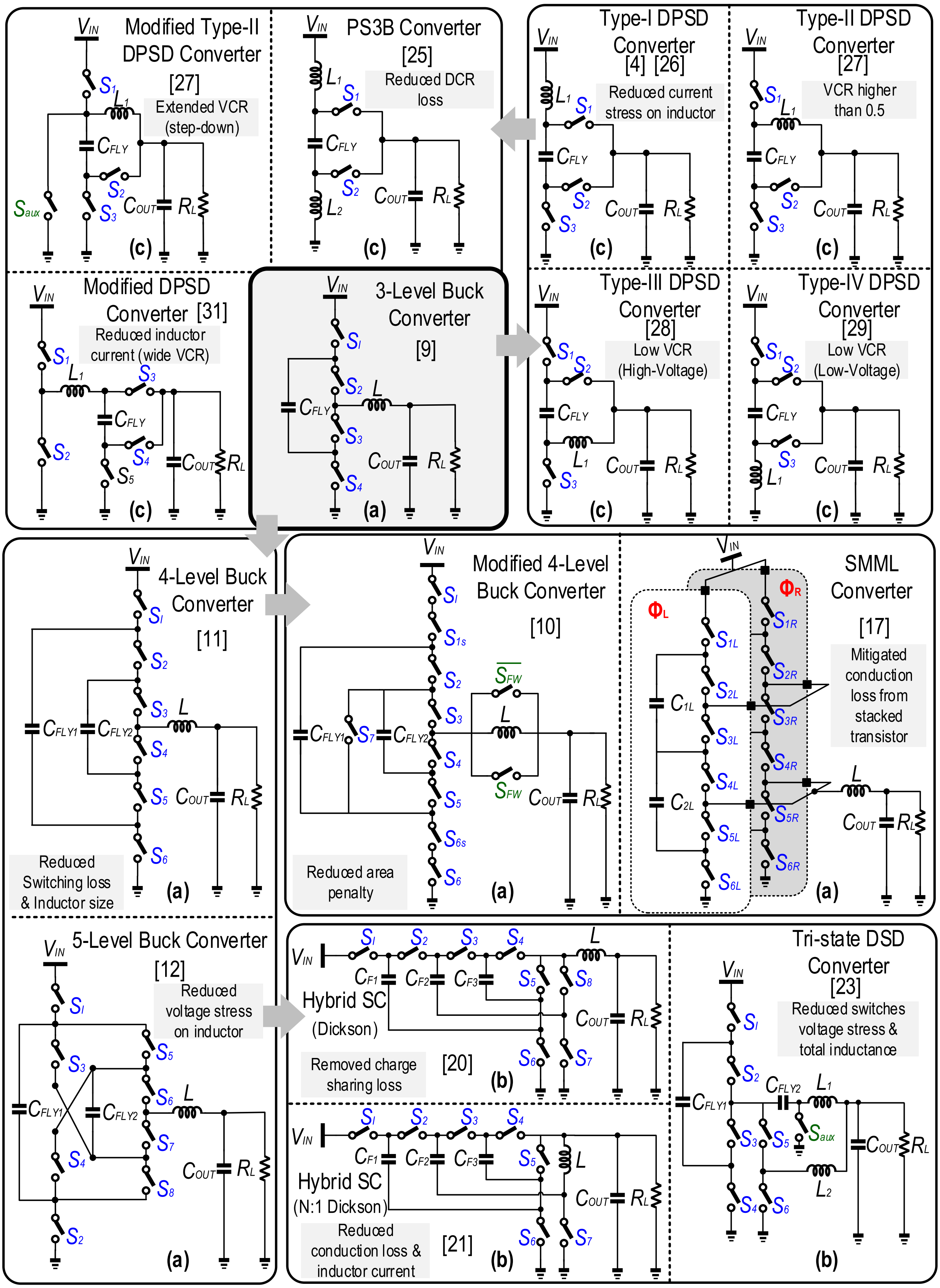

FIGURE 3. State-of-the-art hybrid DC-DC converter topologies: (a) FCML topology (b) Hybrid SC topology (c) dual-path topology. The flow depicts the advancement of the topology.

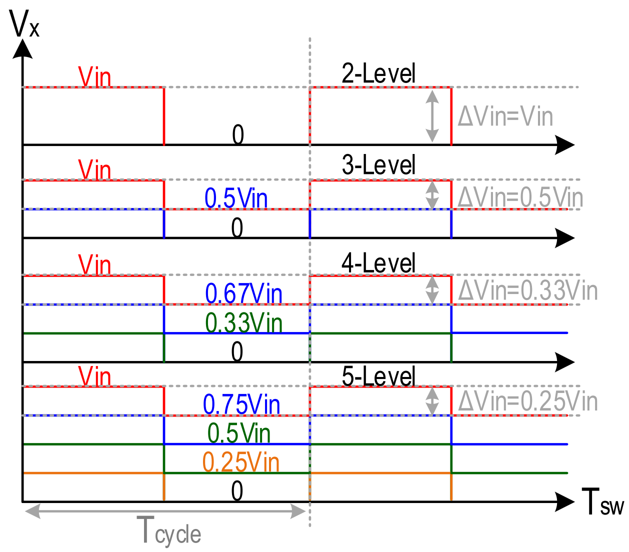

FIGURE 4. Switching node voltage waveforms of FCML.

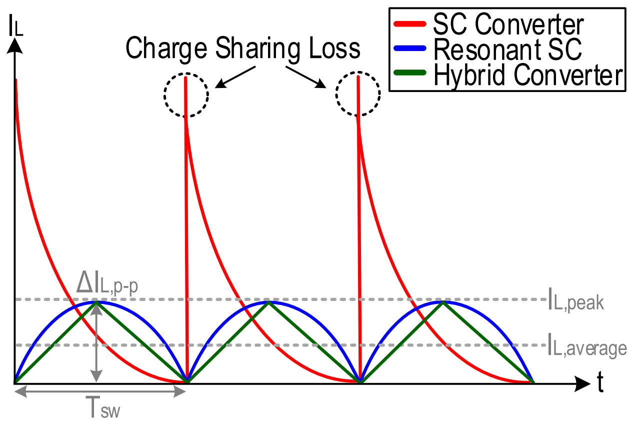

FIGURE 5. Inductor current at various topologies.

motivation, power loss analysis, and passive element technology. Section III discusses the transient response and regulation in improving the load response and charge (discharge) balancing. Section IV presents the comparison of recently published state-of-the-art hybrid dc-dc converter. Lastly, section V presents the conclusion of the review.

II. HYBRID DC-DC CONVERTER ARCHITECTURES

The trend in merged architecture of hybrid dc-dc converter has broadened the research direction for power management and conversion, which enables the development of IoT, energy harvesting, telecommunication industry for 4G/5G that supports bandwidth as wide as hundreds of MHz, and compatible battery storage. These applications necessitate high power density and efficiency across a wide dynamic range of VCRs to ensure a well-functioning system throughout the power conversion under different load conditions [8]. As illustrated in Fig. 3, the hybrid dc-dc architecture offers a favorable tradeoff strategy to overcome the research gap associated with the corresponding topology. Furthermore, the three classified topologies shown in Fig. 3 are flying capacitor multilevel (FCML), hybrid SC, and dual-path (DP) topologies. Typically, FCML topology (Fig. 3(a)) reduces the voltage stress of the devices, while hybrid SC topology (Fig. 3(b)) realizes soft charging of capacitor, and DP topology (Fig. 3(c)) reduces current stress on inductor. In this section, these topologies will be further discussed along with the brief concept, contributions, and the advancements of the topology.

In the FCML topology, the flying capacitor in SI converter reduces the voltage stress of the switching transistors. It establishes numerous switching paths to realize multilevel voltage domains. Furthermore, it ensures a smaller amplitude of voltage swing at the switching node as the level increases as shown in Fig. 4. The scaled-down voltage at the switching node is associated with an LC low-pass filter, which generates a small output ripple. Therefore, the inductor size can be reduced for higher power density while maintaining the system efficiency. In [9], a typical 3-level buck converter with a small on-chip spiral inductor of 1nH is proposed at the cost of the increased effective switching frequency. With a flying capacitor and 4-phase interleaved switching, the load current ripple is reduced, thus improving the power density and efficiency. However, there is a trend to further increase the level of FCML with higher VCR by stacking transistors and adding flying capacitors. In recently published work, a modified hybrid 4-level converter in [10] has improved the area penalty by 47% respective to a 4-level converter in [11] by reducing 33% of voltage stress on flying capacitor with the aid of auxiliary switches to enable additional switching mode. However, the increased number of power transistors results in higher junction capacitance, but the reduced flying capacitance offsets the parasitic capacitance loss.

Similarly, a 5-level buck converter proposed in [12] has ripple current. However, a higher level translates into higher parasitic resistance, which offsets the advantage due to higher switching loss. In short, FCML converters enable a lower voltage amplitude than V_{IN} at the switching node, minimizing the voltage stress of transistors, making the FCML topology viable in low-power applications. Multi-phasing techniques are employed to resolve the issue of low current density [13], [14], [15]. However, this technique requires more passive components and results in a significant conduction loss due to metal trace of the inductors [16]. Nevertheless, a symmetric modified multilevel (SMML) converter proposed in [17] mitigates conduction loss from the stacked transistor during the power stage by sharing the same current path between right and left channels with the symmetrical flying capacitors to charge and discharge alternately, allowing it to balance naturally at a minimum voltage rating of $0.33V_{IN}$. Alternatively, [18], [19] utilized cross-connected flying capacitor configuration to resolve the imbalanced C_{FLY}, avoiding the implementation of current sensing technique.

A hybrid switched-capacitor based dc-dc converter is a merged structure of SC architecture and inductors. The hybrid SC converter is inspired by FCML topology, where the additional inductor enables soft charging of capacitor in SC architecture such as in Dickson, series-parallel and ladder network. A hybrid Dickson SC converter in [20] achieves high power density and efficiency by split-phase control technique to remove the charge sharing loss. However, the additional flying capacitors and switches increase the complexity of the capacitor-voltage balancing controller and the gate driver, respectively. Consequently, [21] proposed an N:1 hybrid Dickson SC converter, which replaces one of the switches with an inductor respective to [20], establishing a shared path for the SC stage to reduce the inductor current and hence the conduction loss is effectively minimized by 41%. Furthermore, the proposed solution does not require pre-charge or capacitor-voltage balancing. In [22], a reconfigurable capacitive-sigma Dickson buck converter is proposed to further enhance the efficiency over wide VCR by shunting the current from high and low-side converters. However, hybrid switched-capacitor based converter requires more passive components and high-voltage rating devices to withstand a high-voltage supply over a large conversion ratio. Typically, double step-down (DSD) converter functions similarly to a hybrid SC converter that processes high voltage at large conversion ratios such as 48V/24V/12V to 1V. However, the DSD generally utilizes two inductors to reduce the current stress and voltage ripple, consequently enhancing the conversion efficiency. In [23], a tri-state DSD converter with a capacitor-voltage balancing scheme is proposed to merge the structural merit of 3-level and conventional DSD converters. It further reduces the voltage stress on switches to $0.25V_{IN}$ at discharging path by the secondary flying capacitor, C_{FLY2}. It improves power density due to reduced total inductance, eventually extending the on-time duty-cycle. This mechanism also reduces conduction loss and enables high switching operation with low-voltage rating devices. Accordingly, [24] proposed a symmetrical DSD converter to improve the limitation of DSD converters where the VCR range is capped at 0.25. The proposed converter exploits an additional 1/3× mode, interchanging with 1/4× mode to extend the VCR range to 0.33.

Conventionally, the size of the power inductor in SI converter is usually bulky and implemented as an off-chip component. This also implies that the inductor has low DCR, $R_{L,DCR}$, and parasitic coupling, providing a higher degree of freedom in the design. However, on-chip inductors have attracted favorable attention in fully-integrated systems achieving smaller form factor but suffering from limited Q-factor, increased parasitic loss, and high DCR. Therefore, several published works have emphasized an alternative solution to relieve inductor stress. For instance, dual-path step-down (DPSD) topology has an additional power path to reduce the current stress of the inductor by relocating the inductor to the input path. The work [25] proposed a passive-stacked third-order buck (PS3B) converter with one inductor connected between the input source and flying capacitor, and the other between flying capacitor and ground to reduce the inductor stress and DCR conduction loss. Thus, the inductor size at the input and ground nodes can be optimized to 240nH. The solution achieves a high power density of 0.7W/mm^2 with the input capacitor removed. Similarly, in [4], a Type-I dual-path step-down switching inductor-capacitor (SIC) converter is proposed, realizing a high power density of 0.73W/mm^2 while maintaining a favorable efficiency of 74.6% by reducing the current stress on the inductor. The relocation of the inductor has inspired the transformation of DPSD topology, in which the relocated inductor at different nodes have been classified into Type-I [4], [26], Type-II [27], Type-III [28], and Type-IV [29], respectively. The evolution has become the baseline in DPSD converters for the designers. A typical Type-II DPSD converter inherits higher VCR of more than 0.5. Hence [27] added an auxiliary switch was to extend the VCR for further step-down ratio at the cost of efficiency. In contrast, Type-III and Type-IV exhibit low VCR, with Type-III being suitable for high-voltage and Type-IV for low-voltage applications, respectively. However, the mitigation of high DCR due to a smaller on-chip inductor, as emphasized in [30], [31], and [32] have proposed a modified DPSD, reducing the inductor current across a wide range conversion ratio. In short, DPSD topology enables a smaller size of on-chip inductor but suffers from switching loss due to hard switching, and the significance of DCR loss has to be considered.

A. POWER LOSSES ANALYSIS

The power efficiency of a power converter is defined by the ratio of output power to input power as described in equation (1).

$$\eta = \frac{P_{out}}{P_{out} + P_{TotalLoss}} \tag{1}$$

In the preliminary structure of hybrid dc-dc converter, the inductor is required to soft charge the flying capacitor to reduce the charge sharing loss. However, on-chip inductor integration has increased the complexity of the circuit [33]. Stacked transistors are commonly used circuit techniques to withstand high voltage stress at the expense of increased conduction loss due to the turn-on resistance of the transistor. In short, most of the aforementioned solutions and techniques significantly enhance the circuit performance, but the trade-offs in power consumption and power losses are inevitable. Therefore, several significant power loss factors in hybrid power converters are analyzed as follows:

1) CONDUCTION LOSS

Conduction loss arises from the on-resistance of switching transistors, inductors, and flying capacitors. However, the resulting parasitic resistance expression varies according to circuit topologies and operation modes. Generally, the inductor geometry in hybrid topology directly reflects the converter performance, as the parasitic resistance limits the efficiency [4]. Furthermore, the inductance has a direct impact on the induct current or load current ripple, where a higher inductance leads to a lower current ripple. As a result, the inductor in hybrid converter plays a vital role in conduction loss. Hence, the conduction loss of the inductor and the load current ripple can be expressed as follows:

$$P_{conduction} = \left(I_{Load}^2 + \frac{\Delta I_{Load}^2}{12}\right) R_{parasitic} \tag{2}$$

$$\Delta I_{Load} = \frac{V_{out}\left[1-(N-1)\,VCR\right]}{f_{sw}L_{out}\,(N-1)} \tag{3}$$

The expression in equation (2) is valid under continuous-conduction mode (CCM) operation in which the output inductor current or load current, I_{Load} is represented as triangular waveform (Fig. 5). Besides, the load current ripple, ΔI_{Load} shown in equation (3) is highly dependent on N-level of the FCML topology and also the inductance, where N is the number of level of the FCML topology, $f_{sw}$is the switching frequency, $L_{out}$is the output inductance, and VCR is the voltage conversion ratio. Also, the relationship between switching frequency and DCR loss of the inductor concludes that switching at a lower frequency leads to higher resistive loss and vice versa. The conduction loss of on-resistance is due to the source-drain channel of the transistor during turn-on period, where it is highly dependent on the process parameters of the adopted CMOS technology, which is expressed in equation (4).

$$R_{on} = \frac{1}{\mu_n C_{ox}\frac{W}{L}(V_{GS}-V_{TH})} \tag{4}$$

The technology constant μ_n and C_{ox} is the mobility of charge and capacitance of gate oxide, respectively, W/L is the ratio of channel width over length, and V_{GS}-V_{TH} is the overdrive voltage. Body-biasing techniques are widely employed to scale the threshold voltage dynamically, V_{TH} [34], [35] to minimize conduction loss at low-voltage applications.

2) SWITCHING LOSS

Switching loss occurs during the switching transition of the transistor due to the charging and discharging of parasitic capacitance. Hence, the switching loss can be expressed as follows:

$$P_{switch} = V_{in}^2 f_{sw} C_{Eff} \tag{5}$$

$$C_{Eff} = k\left(\alpha C_{gsw} + \beta C_{par}\right) \tag{6}$$

In equation (5), C_{Eff} is the total effective gate switching capacitance per unit width C_{gsw}, and bottom-plate capacitance of the flying capacitor C_{par}. The sensitivity of switching loss is directly proportional to the switching frequency. At the same time, the effective parasitic capacitance in the power stage is correlated to the sizing of transistors and flying capacitor. Furthermore, the parasitic capacitance model can be computed based on Miller Coupling Factor (MCF) [36]. In equation (6), the coefficient factors, α, β, and k represent the number of switching cycles, bottom-plate capacitance loss and multilevel improvement factor, respectively. Regardless, the switching loss is inversely proportional to conduction loss, as shown in equation (7). Total power dissipation within the power level can be described as the sum of switching loss and conduction loss as described in equation (8).

$$P_{switch} \propto \frac{1}{P_{conduction}} \tag{7}$$

$$P_{TotalLoss} = P_{switch} + P_{Conduction} \tag{8}$$

B. POWER LOSSES REDUCTION AND OPTIMIZATION

In recent state-of-the-art hybrid dc-dc converters, various methodologies and design strategies are adopted to reduce power loss. As highlighted in equations (2) and (5), the conduction and switching loss are functions of switching frequency. Thus, the selection of switching frequency with an appropriate topology is crucial. Several literature review exploits different design strategy in reducing the power loss either by establishing a parallel path for load current flow [37], multi-phase interleaved technique [38], [39], relocating inductor to the low current path [26], [27], [28], [29], and more. Moreover, inductors with low DCR are an alternative to minimize conduction loss. In a tradeoff of low DCR, the inductor size is bulky, which translates to the degradation of power density [25].

Besides, closed-loop regulation is the simplest method for load regulation at different loading conditions to avoid unnecessary power loss. Conventionally, voltage-mode control, such as PWM is commonly used to control the switching period of the transistors, but it limits the bandwidth and is prone to stability issues. The current sensing technique is suitable for high switching frequency operation but highly sensitive to the RC network. Hysteretic control enables high transient response, but the large output voltage ripple contributes to conduction loss. In [40], a real-time voltage-mode control V_{CF} calibration scheme was proposed to regulate V_{CF} to $0.5V_{IN}$ continuously. This work enables bandwidth extension and effectively reduces the output ripple resulting in minimized conduction loss.

Furthermore, the charging and discharging of the gate terminal cause switching loss due to the gate bias voltage required in driving the transistor, resulting in the adoption of thin-oxide transistor, which is commonly used for minimal gate parasitic capacitance [1], [41]. Additionally, the intrinsic loss in hybrid topology due to control timing mismatch and parasitic resistance affects the imbalance charging (discharging) of flying capacitor [42]. Hence, adjusting the transistor width achieves an identical on-resistance r_{on} for both PMOS and NMOS [10]. Furthermore, the work [5] presented a duty-cycling scheme with dynamic load current using two NMOS footer transistors to minimize the power loss at various loads (i.e. light or heavy) by alternately activating and deactivating the oscillators. The transistor sizing optimization is essential to reduce the conduction loss by the on-resistance of the cross-coupled switch. The switching loss is negligible when the switching frequency of the footer transistor is lower than

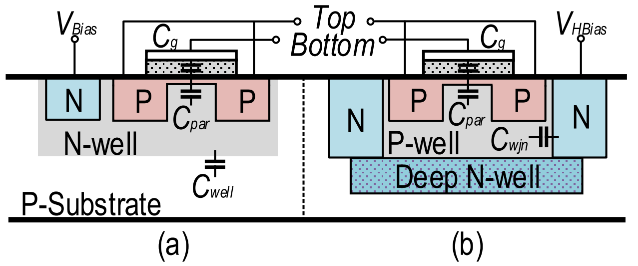

FIGURE 6. Parasitic capacitance within MOS capacitor (a) PMOS capacitor and (b) PMOS capacitor with high N-well bias [52].

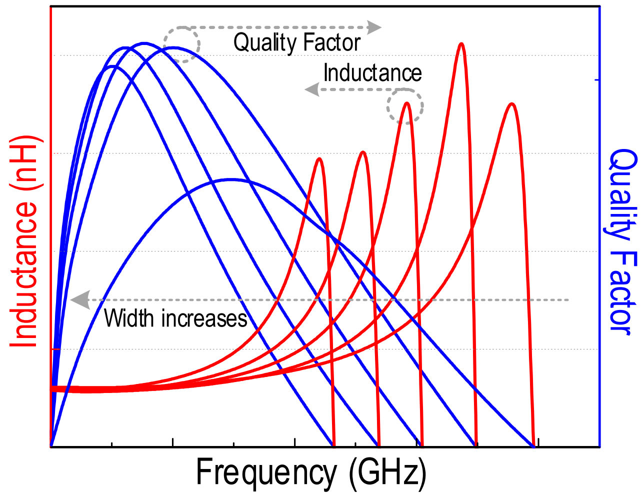

FIGURE 7. Inductance and quality factor versus frequency under width variation.

the resonant frequency [5]. Also, appropriate sizing of PMOS and NMOS alleviates the tradeoff between switching and conduction loss at a ratio of 2:1 [43]. Proper gate biasing techniques assist in forward conduction and leakage loss [44], [45]. The power loss reduction technique discussed are summarized as follows:

1. Inductor stress can be reduced by adding current path or relocating to low current path. However, it may require additional switching control and balancing technique.
2. On-chip inductor DCR can be reduced at the cost of increased silicon area.
3. Transistors size can be optimized with an appropriate ratio; its gate is biased using advanced dynamic gate biasing technique.
4. A closed-loop feedback system can be employed to minimize signal mismatches, charge balance etc.
5. Low parasitic technology or technique can be adopted, which will be further discussed in the subsequent section.

C. PARASITIC CAPACITOR TECHNOLOGY

Flying capacitor technology is indispensable for a fully-integrated solution in hybrid architecture of dc-dc converters. It establishes a scalable VCR with gate controller design and reduces voltage stress on switches to prevent internal breakdown. An ideal characteristic for an on-chip capacitor is a negligible parasitic loss and high capacitance density. As a result, Metal-Oxide-Metal (MOM) capacitors and Metal-Insulator-Metal (MIM) capacitors are notable capacitor technology for their low parasitic properties. Generally, the MOM capacitor is often used in advanced process with multi-metal layers stacking to enhance the capacitance [46]. MIM capacitor is formed between metal layers, and the capacitance density is dependent on the dielectric thickness [47].

Additionally, capacitance density (nF/mm^2) affects the on-chip size. Metal-Oxide-Semiconductor (MOS) based capacitors are well-suited to achieve high capacitance density [48], [49]. The fundamental configuration of the MOS capacitor is modified from the CMOS process with shorted drain and source terminal and with the gate terminal configured as the connecting node.

The equivalent capacitance within the MOS capacitor can be computed as the sum of the junction capacitance between each layer (Fig. 6). C_{par} is the capacitance between the drain-source and well, C_{well} is the capacitance between the well and substrate. The parasitic capacitance is affected by the doping concentration [1]. Besides that, Silicon-On-Insulator (SOI) technology is an alternative approach to reduce parasitic capacitance, such as in [50], where a deep trench capacitor in the SOI CMOS process is implemented, with the penalty of additional fabrication cost. Alternatively, another methodology for parasitic improvement is proposed in [51], [52], and [53], in which a high value of the resistor is adapted to bias the node at N-well with a high voltage V_{NM}, so that the C_{par} and C_{well} are virtually open to AC ground. As an example, [51] adopts the conventional N-well and the series parasitic capacitance is higher than top plate gate capacitance C_g, while the work [53] adopts a deep N-well in which parasitic capacitance is lower than gate capacitance C_g. For the method proposed in [52], a high bias voltage $V_{HBias}$is employed to the N-well by an on-chip voltage doubler to reduce the well-junction parasitic capacitance C_{wjn}.

Practical implementation includes MOM and MOS combination capacitors or MIM and MOS combination capacitors, further strengthening the popularity and benefits of MOS capacitors. References [53] and [54] employed MOM and MOS capacitors with high capacitance density. It reduces switching loss due to parasitic capacitance at 450MHz [4], where the thick oxide property of the MOS capacitor also minimizes parasitic coupling by pushing the bias voltage, as highlighted in [55]. However, the thick oxide MOS capacitor occupies a larger silicon area than the MOM capacitors [56]. The implementation of MIM and MOS capacitors can also be referred to [10], [57], [58], and [59]. The work [57] demonstrates a high density stacked MIM and MOS capacitor, effectively reducing 52% of the capacitance by grounding the bottom plate of the synchronous bootstrap capacitor. Also, the spatial area is reduced due to high capacitance density, which exhibits

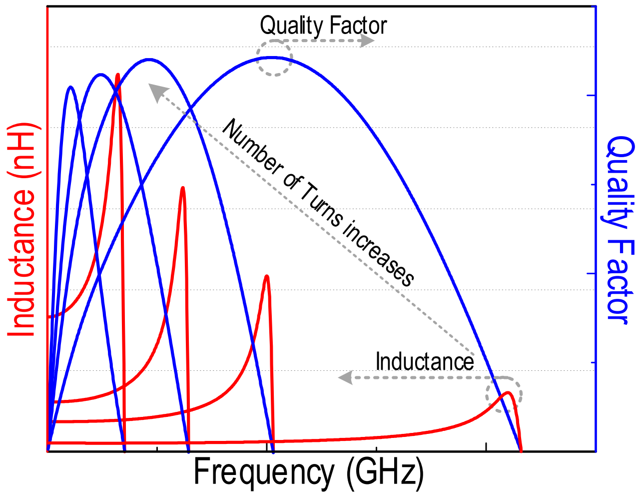

FIGURE 8. Inductance and quality factor versus frequency under number of turns variation.

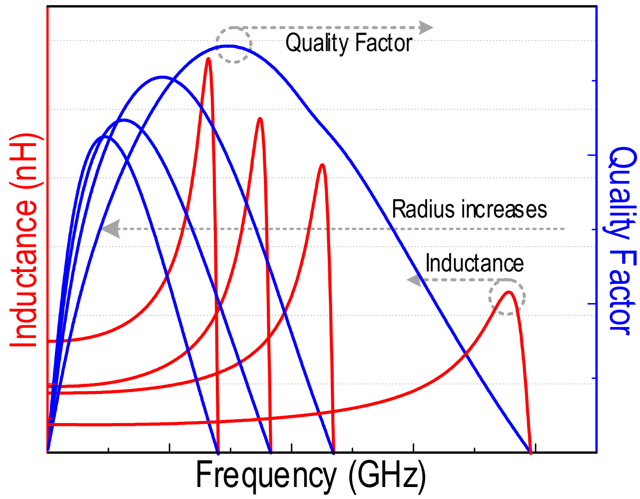

FIGURE 9. Inductance and quality factor versus frequency under radius variation.

low slow switching limit resistance (R_{SSL}) and parasitic loss [59].

D. INTEGRATION OF INDUCTOR AND OPTIMIZATION

For an on-chip inductor, balancing the desired Q-factor and the silicon area consumed is crucial. In the advances of high power density and efficiency application, the integration of on-chip inductor plays a crucial role in performance improvement [60]. Generally, on-chip inductors suffer from inherent low Q-factor due to the DC resistance of metal at low frequency. However, the current crowding effect becomes significant as the frequency increases to more than 1GHz. In addition, the inductor current resonates with the lossy substrate, generating eddy currents due to electromagnetic coupling to the substrate [61]. Particularly in the scaled CMOS process, the top metal is closer to the substrate incurring extra loss, thereby exacerbating the Q-factor and channel effect [62]. Therefore, an innovative strategy is necessary to enhance the quality of on-chip architecture.

There are several proposed techniques for improving the inductor performance and concurrently suppressing the parasitic coupling effect to push the Q-factor higher and decrease the AC losses. Patterned ground shield (PGS) is commonly adopted to isolate the parasitic coupling, minimizing the induced eddy current from the lossy substrate [63], [64]. However, the shielding technique increases the substrate capacitance as an offshoot, producing higher switching loss and degrading power efficiency. The work [3] utilized a co-planar ground shield to improve the Q-factor of the coupled on-chip transformer by 0.32, achieved by reducing the substrate loss from the induced eddy current between the edge of the metal trace. Subsequently, the work in [58] proposed a new direction of merged LC resonators for passive integration. Compared to the conventional use of spiral inductor, a single MIM capacitor is embedded as a single LC structure which establishes capacitive ballasting to reduce

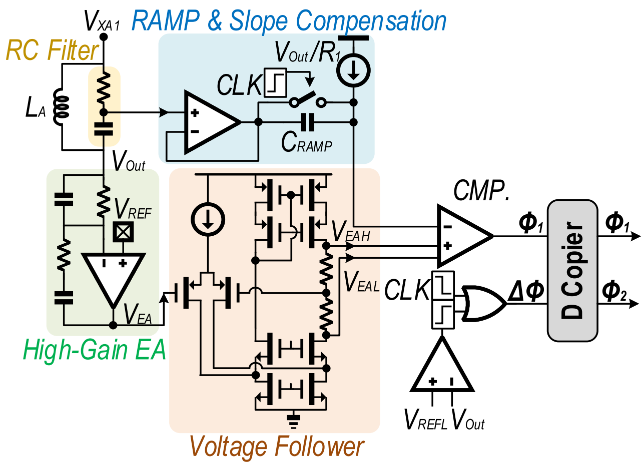

FIGURE 10. Schematic of synchronized hysteretic controller [69].

current crowding by pulling current to the outer trace due to concentrated magnetic flux at the inner trace. As a result, the current crowding effect is reduced.

Moreover, the geometrical design of an on-chip inductor or transformer regulates several fundamental design rules to achieve a reasonable inductance, Q-factor, frequency, and coupling coefficient. The width of the metal trace should be widened according to the design perspective [65], increasing area consumption and a proportional DCR decreases leading to a higher Q-factor [66]. However, the skin and proximity effect become significant at a specific frequency, and the DCR gradually worsens (Fig. 7). Furthermore, narrow conductor spacing provides higher effective inductance due to a stronger concentrated magnetic field. As the number of turns increases, especially in the transformer, the coupling effect is further strengthened, enhancing the capability of energy transferring with higher mutual inductance in the context of the coupling coefficient [67]. Also, the increase in inductance respective to the higher number of turns results in a reduced

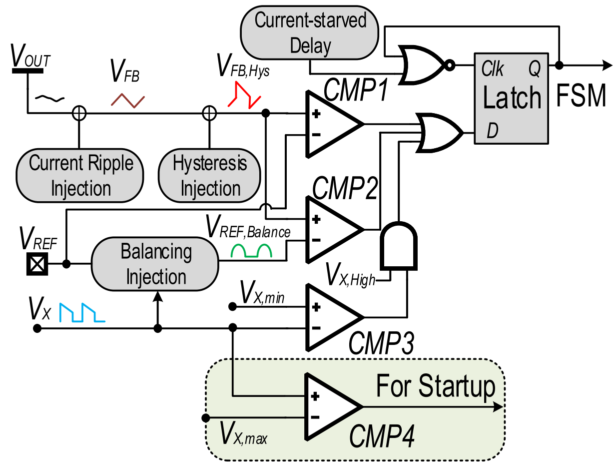

FIGURE 11. Ripple-injection control [68] with phase-skipping technique [71].

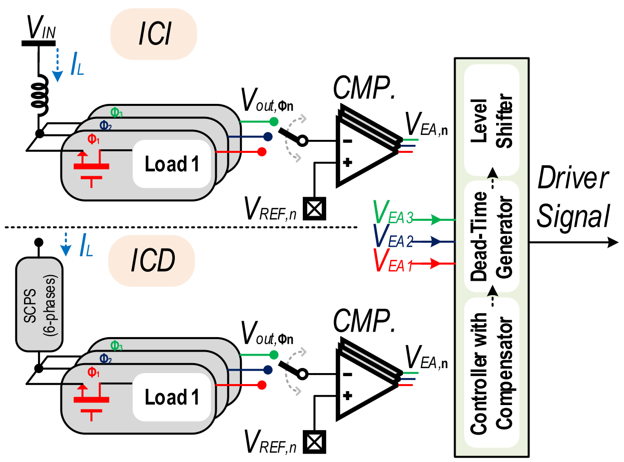

FIGURE 12. ICI and ICD modes control in steady-state operation [72].

self-resonant frequency (Fig. 8). The Q-factor also increases proportionally to the inner radius. Therefore, as the self-inductance increases, but at the cost of increased eddy current, parasitic coupling, and higher area consumption, resulting in reduced bandwidth of resonant frequency along with the degradation of Q-factor (Fig. 9). In short, the desired design objectives can be optimized by varying the number of turns, metal width and inner radius. Each parameter has its respective sensitivity towards the overall performance.

III. TRANSIENT RESPONSE AND REGULATIONS

Transient specifies the high computation performance in the point-of-load voltage regulator for microprocessors. In power converter, it is important to generate the desired output with high conversion efficiency, especially for dynamic voltage scaling over an extended operating time. An erratic or unstable behavior can occur due to a poor transient response [68]. Conventionally, PWM is often implemented to reduce the overshoot or undershoot during transient, while filter such as Type-II or Type-III compensator is used to sustain the loop

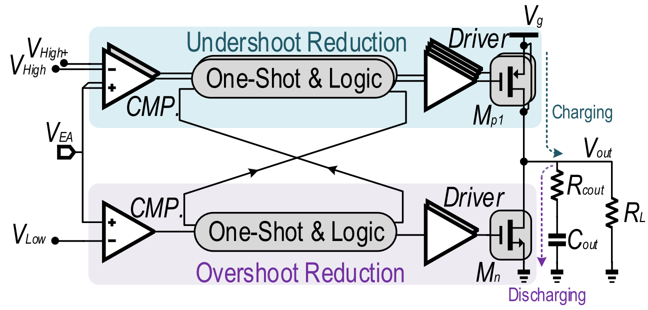

FIGURE 13. Undershoot and overshoot reduction hybrid scheme [73].

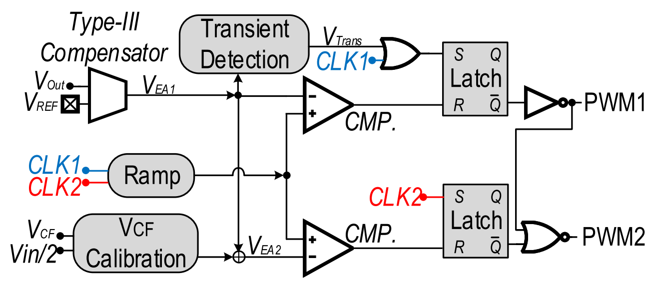

FIGURE 14. Delay-insensitive technique with Type-III compensator [75].

stability by extending the loop gain bandwidth. Therefore, various works have improved and extended the regulation techniques based on the conventional method. For instance, the work [69] proposed a synchronized hysteretic controller to charge a capacitor faster between the two phases during load transient (Fig. 10). The duty-cycle is more than 0.5 for better transient performance and to alleviate ringing in the form of accumulated error. In addition, [69] proposed a D-copier to balance the capacitor voltage by duplicating the output PWM signal with desired phase shift for complementary switching to generate an identical duty-cycle without overlapping. The proposed Flying Capacitor Cross-Connected (CCC) converter is an improved topology from the DSD but with additional charging and discharging path, which increases of component count with compromised performance. Besides, a shared bootstrap capacitor scheme is proposed to reduce the area constraint. It achieves a minimum efficiency of 84.6% at Vo=0.9V and a peak efficiency of 89.3% at Vo=1.8V.

In [70], a fast transient response of 1V/10μs line regulation was achieved while maintaining more than 80% of peak efficiency by implementing augmented ripple-injection control (Fig. 11). The control system consists of three comparator, which provide real-time (RT) cycle by cycle control for capacitor voltage imbalance issue by adjusting the duration of switching states while regulating the output voltage simultaneously. Further, self-start up is achieved when switching node voltage, V_X reaches a minimum threshold voltage, $V_{X,min}$ to trigger the comparator, thus terminating the charging or discharging, preventing pre-charge and fault conditions at start up.

TABLE 1. Transient response of hybrid DC-DC converters.

Ref.	[69]	[70]	[71]	[72]	[73]	[74]	[75]
Topology	DSD	5Level FCML	Hybrid Cascaded SC	SIMO Hybrid	Hybrid Buck	Hybrid SIBO	CCC
CMOS Process	180nm BCD	180nm	180nm	180nm	130nm	350nm	180nm BCD
Input Voltage	12V/24V	5.5V	4V -6V	1.8V	3.3V	2.7V - 4.5V	12V
Output Voltage	1V	0.4V - 1.2V	0.4V - 1.2V	0.4V - 1.6V	1.8V	5.3V -4.7V	0.9V - 1.8V
Max Current	4A	1.4A	1A	0.45mA	1.25A	350mA	4A
Inductance	2x 1.8µH	240nH	240nH	4.7µH	90nH	10µH	2x 0.74µH
Flying Capacitance	4.7µF	3x 4.7µF	2x 4.7µF + 10µF	2x 1.5µF + 3µF	2x 0.47µF	4.7µF	2x 2.2µF
Control Technique	Voltage Mode (PWM)	Augmented Ripple Injection (Integrated)	Ripple Injection with phase skipping technique	Dual Switching Frequency (PWM)	Voltage Mode + Type-III Compensator	Voltage Mode + Type-II compensator	Synchronized Hysteretic
Peak Efficiency (CR)	88.3%/83.5%	92.4% (4.58)	96.9% (4.2)	87.50%	90.70%	89.30%	89.30%
Max CR (Peak Eff)	NA	13.75 (80.2%)	12.5 (85.5%)	NA	NA	NA	NA
Power Density	NA	0.103W/mm2	0.10W/mm2	0.369W/mm2*	1.875W/mm2*	0.951W/mm2	0.857W/mm2*
Transient Response (Settling Time)	56mV (0.9µs)	58mW (2.5µs)	32mV (1µs)	20mV (2µs)	36mV (125ns)	3mV (55µs)	110mW (1.5µs)
	3A (20ns)	1A (250ns)	1A (1µs)	140mA (2µs)	1.25A (2ns)	320mA (1.3µs)*	4A (20ns)

* Estimated from given specification and data.

In [71], a cascaded hybrid SC converter with a faster self-startup time of 10 μs was proposed compared to [70]. The modified ripple-injection control (MRIC) achieves capacitor voltage balancing and output voltage regulation similar to [70] (Fig.11). However, an addition of a phase-skipping technique is adopted to the controlling scheme. The phase-skipping scheme triggers during the startup mode for rapid charging and balancing transient. This ensures the secondary flying capacitor undergoes charging only by generating a gate driving signal to skip the discharge phase from the finite state machine (FSM). The proposed circuit can achieve at least 85.5% efficiency (VCR=12.5) and a full-load transient of 1A/μs.

In [72], a dual switching frequency scheme between 500 kHz and 100 MHz is proposed to obtain a fast response speed and low cross-regulation. The controlling scheme is implemented with PWM control to regulate the inductor current. Hence it switches between the inductor current increasing (ICI) and inductor current decreasing (ICD) modes (Fig. 12). ICD mode occurs when V_{out} is higher than V_{REF}, and the power stage is switching in six-interleaves of 100 MHz each. The switching node is charged up to 3.8V during ICD mode to generate a smaller duty-cycle based on a higher slew rate of the inductor current. Similarly, ICD and ICI modes reduce switching loss at 500 kHz during ICI mode. Additionally, both ICI and ICD mode shortens the response time between high and low load variation.

In [73], a voltage-mode controller with type-III compensator and delay-compensated ramp with hybrid scheme was proposed to enhance load transient response (Fig. 13). Firstly, near-optimal transient response is achieved by prompting the compensator to saturate the duty-cycle to 1 and optimize the PWM control with unity-gain bandwidth (UGF) when the load varies spontaneously. Furthermore, the hybrid scheme bounded by the threshold voltage of ramp signal as the detector window optimizes the load transient at different load step by using the output voltage, V_{EA} from the type-III compensator. As the V_{EA} swing exceeds V_{High}, the

TABLE 2. Comparison of State-of-the-arts hybrid DC-DC converters.

Ref	Year	Process (nm)	Topology	Freq. (MHz)	Vin (V)	Vout (V)	Ind. (nH)	Flying Cap. (nF)	Max Load Current (mA)	Area (mm^2)	Power Density (W/mm^2)	Eff. @ Peak (%)
[4]	2021	65	Dual-Path	450	1.2	0.6 - 0.9	0.85	4.82	533	0.65	0.73	74.6 @ 78
[5]	2021	180	Coupled Class-D	1250	1 - 3.6	0.4 - 1.6	7.8 coupled	2 x 0.229	138	1.61	0.21	65.2 @ 67
				2500	1 - 3	0.4 - 1.3	3.1 coupled	2 x 0.076	NA	0.37	0.88	57.5 @ 58.1
[10]	2019	28	FCML	200	2.8 - 4.2	0.6 - 1.2	3	2 x 5	12	1.5	0.267	50.5 @ 78
[16]	2019	130	SIC	1.8 - 2.3	9	3 - 4.2 6 - 8.4	522	2 x 22000 4 x 10000	3400 (4200)	7.37$^{\%}$	0.00166* 0.00433*	90.8 @ 94.3 96.5 @ 97.4
[17]	2020	180	SMML	3 - 5	3 - 5	0.3 - 1.2	220	4 x 1000	2500	5.5	0.52	89.5 @ 90
[19]	2020	350	DSD	2	2 - 4.4	9-20	2 x 3300	2 x 470	250	0.86	2.325*	91.7 @ 93.5
[22]	2022	180	Hybrid Reconfig.	1-2	4 - 5.5	0.4 - 1.2	400	3 x 2200 2 x 10000	2000	5.8*	0.414*	79$^{\#}$ @ 98.4
[23]	2021	180	DSD	0.2 - 5	12 (24)	1	2x 560	2x 1000	3000	6.3	0.476	86.7 @ 92.1 83 @ 88.3
[24]	2022	65	SDSD	3	2.7 - 4.2	0.5 - 0.8	2 x 4700	2 x 470	500	1.53	0.268*	86.5 @ 86.5
[25]	2019	180	Dual-Path	6.5	1.8	0.5 - 1.5	2 x 240	470	2500	1.85	0.7	86.6 @ 94
[27]	2019	180	Dual-Path	1	4.5	0.8 - 4	4700	2 x 10000	1600	3.24$^{\%}$	0.395*	91$^{\#}$ @ 96.2
[32]	2022	65	CPL Buck	2	3 - 4.2	1.2	470	2 x 4700	1200	2.72	0.3*	90$^{\#}$ @ 92.9
[37]	2022	180	Hybrid SCR	2 - 5	1.8 - 4.2	5 - 24	4700	8 x 4700	250	135$^{\%}$	0.044*	86$^{\#}$ @ 93.2
[38]	2018	65	FCML	10 - 40	1.2	0.1 - 1.1	5.8	2 x 2.2	100	2.34	0.047	88 @ 93.2
[39]	2022	28	MP-Buck	400	1.2	0.45 - 0.9	6 x 1	6	1800	1.31	1.23	77$^{\#}$ @ 83.7
[40]	2018	65	FCML	50	5	0.6 - 4.2	100	5	700	2.313$^{\%}$	1.297	NA @ 90
[48]	2021	180	Hybrid SC	120	1.2 - 2.7	1.45 (3.2)	20 + 30	0.66	25 (50)	0.84	0.195*	>52 @ 77
[57]	2021	180	FCML	1.4 - 1.6	4 - 6	0.4 - 1.2	240	2 x 4700	1000	7.82	0.1	90$^{\#}$ @ 96.9
[58]	2020	180	ReSC	47.5	2.4 - 4.4	1 - 2.2	7.7 coupled	2 x 1.7	520	8.93	0.097	74.5 @ 85.5
[69]	2022	180	CCC	2	12	0.9 - 1.8	2 x 740	2 x 2200	4000	2.8$^{\%}$	0.857*	81$^{\#}$ @ 86.8
[75]	2022	180	DSD	1	12 (24)	1	2 x 1800	4700	4000	9.6$^{\%}$	0.323*	NA @ 83.5 NA @ 88.3

* Calculated from given specification and data. $^{\#}$ Estimated from measured waveforms and graphs.
$^{\%}$ The system is integrated on PCB and observed from the measured die micrograph.

undershoot reduction scheme will be activated, whereas when V_{EA} swings below V_{Low}, the overshoot reduction scheme will be activated. The work achieves a minimum efficiency of 83.6% and a peak efficiency of 90.7% at an output of 1.2V and 2.4V, respectively.

In [74], a hybrid SIBO converter with floating negative output and shunt regulators was proposed to drive a quality active-matrix organic light-emitting diode (AMOLED) with fast load transient response, low output ripple and low-power consumption. The proposed shunt regulator is used to tune the positive output voltage, Vp with the ripple of near-zero and the conduction loss is negligible. The fine-tuned Vp is fed into the type-II PWM controller for negative output voltage, Vn regulation. The proposed circuit has a peak efficiency of 89.3% at 1.1W output power with the maximum power can go up to 3.5W. The achieved load transient response is around 250mA/μs, with negligible undershoot and overshoot voltage.

Alternatively, [75] presents a DSD topology with a similar charging concept in [69] but with an additional auxiliary switch, enabling dual-phase charging to enhance the inductor current slew rate. Nevertheless, the proposed voltage-mode

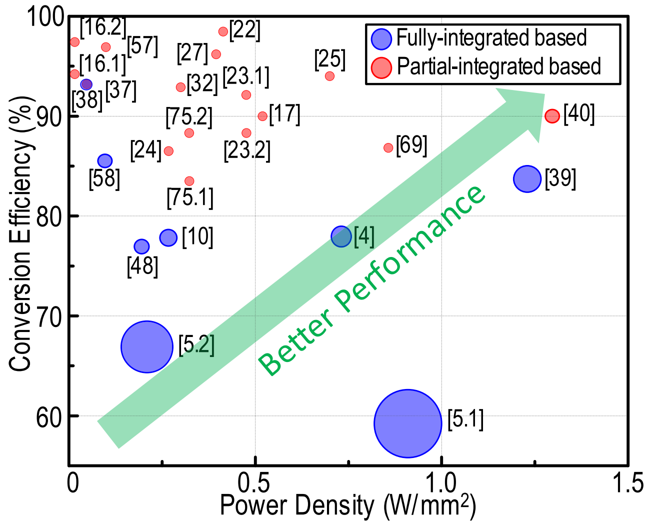

FIGURE 15. Power efficiency versus power density of state-of-the-art hybrid DC-DC converters. The size of the circle depicts the operating range of switching frequency.

control with delay-insensitive technique, as shown in Fig. 14 is optimized to enhance the transient response by employing two feedback loops. The feedback loops are configured as PWM controllers, generating two duty-cycle signals for the respective phase. Therefore, the loop responds if the transient event occurs within on-time of phase-1. Otherwise, the massive delay will cause a large undershoot. Hence, the delay-insensitive technique is used to detect and respond to the load transient without the need of waiting for the next clock cycle.

In summary, different topologies to achieve fast transient response and voltage regulation are described in Table 1. Several techniques are presented to increase the slew rate of the inductor current, including multi-phasing charging, switching frequency modulation etc. In addition, voltage-mode controlled converters are commonly used and optimized with a compensator to accelerate the transient response. The uprising trend of fast transient is shown in numerous results due to the collective contribution of previous works.

IV. DISCUSSION OF STATE-OF-ARTS HYBRID CONVERTER

The hybrid dc-dc converters topology has shown potential for a smaller form factor realization and to adopt the favorable trends towards system on-chip solution while maintaining a power density above 1W/mm^2 and more than 80% efficiency, making it well-suited for low-power conversion with high performance. Also, it counterbalances the performance tradeoffs, offering extended opportunity in advanced power converter design especially for low-voltage application. The recent state-of-the-art hybrid dc-dc converters are tabulated in Table 2. Also, Fig. 15 illustrates the power efficiency versus power density of recent reported work on hybrid dc-dc converters, with the size of the circles signifying the operating switching frequency.

Generally, most hybrid power converter architecture have capped the switching frequency under 10 MHz to steer clear

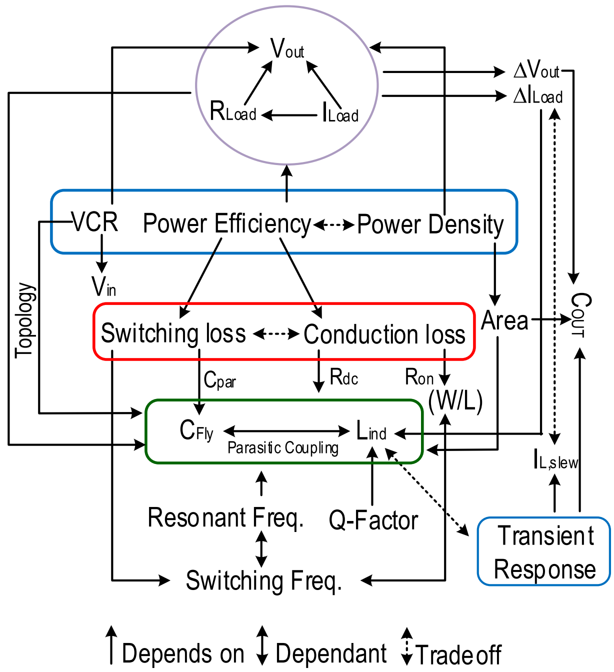

FIGURE 16. Hybrid DC-DC converters design considerations.

the switching loss from dominating the power matrix as described in Table 2. However, work published in [4], [5], [10], [39], and [48] propels the operating switching frequency up to hundreds of megahertz and gigahertz. This allows reduced inductance in proportion to an on-chip inductor footprint to achieve high power density. However, corresponding strategy for loss reduction is required by exploiting topological advantage to alleviate the intrinsic loss. For an example, [5] implemented stacked Class-D voltage-controlled oscillator (VCO) to exhibit the nature of gigahertz oscillation, while the voltage swing is boosted up to 3.3 times of V_{DD}. However, the solution requires two complementary on-chip transformers which adversely impact the active chip area. Correspondingly, the oscillation frequency is doubled up to 2.5 GHz which results in high power density of 0.88 W/mm^2, with the tradeoff in efficiency degradation. Nonetheless, this has unveiled a design approach by adopting VCO in advanced future dc-dc power converter design.

On the other hand, partial-integrated converter exhibits higher power efficiency due to off-chip passive component which eases the constraint on core design, however the PCB footprint is inevitable. Nevertheless, fully-integrated converters have been gradually adopted by designers in recent years, while the discrete implementation methodology edges up for maximum efficiency. Although in [40] a highly compromised result in high power density of 1.297 W/mm^2 with peak efficiency of 90% is demonstrated, but only the core area is considered (air core inductor is excluded). It is more challenging to achieve high power density than efficiency as the power density of recent reported works is more diverged (Fig. 15), with the power efficiency is often the preliminary consideration in benchmarking the performance. Therefore, a fully-integrated design outlays room for improvement by exploiting the advantage of hybrid topology and packaging technology. For instance, a fully-integrated based converter deviates across the lower boundary (Fig. 15) due to the limitation of on-chip passive elements. Consequently, in [39] an exceptional tradeoff is shown by implementing bond-wires as inductance which is an alternative substitution for a monolithic inductor.

In the design interest, CMOS technology of 180 nm is widely used based on the benchmarking in Table 2. As the CMOS technology scales down, it offers faster speed, higher capacitance density, and lower gate parasitic [76]. Nevertheless, scaled CMOS processes with shorter channel length tend to have low-voltage rating, which implies the necessity of stacking transistors for high-voltage input. Thus, scaled CMOS process is recommended for ultra-low-voltage application. A hybrid dc-dc converter design consideration with the associated tradeoff is shown in Fig. 16. The performance index is highly dependent on the core passive elements, which induces soft-charging, parasitic coupling, as well as power loss. For example, higher inductance reduces current ripple, but the transient response and the area consumption is limited. Fig. 16 provides a design considerations chart to determine the design objective with the associated tradeoff. In summary, the development of integrated hybrid dc-dc converters is evolving rapidly as it inherits the characteristics of reduced inductor current ripple, soft-switching, and diverged voltage stress on switches. These demonstrate the need of an exemplary solution for current technology with challenging criteria such as dynamic VCR, fast transient, high efficiency, high power density, and small form factor. Regardless, partial-integrated based hybrid converter is still dominating the current design trend, providing great research opportunity in fully-integrated architecture.

V. CONCLUSION

In conclusion, the revolution of SoC specifies that low-power applications are striving for high power efficiency, high power density, and fast transient response. This article classifies the types of hybrid dc-dc converters from the existing hybrid architecture such as FCML, hybrid SC, and dual-path topology. The power loss analysis and reduction technique are discussed with the design strategy and equations proposed in recently reported works. In addition, the capacitor technology and integration of inductors are discussed from the viewpoint of a fully-integrated solution for a thorough understanding of the passive component selection and implementation for hybrid dc-dc converter design. A comparison to the state-of-the-art hybrid dc-dc converters in terms of power specification, design parameter, on-chip process, and area consumption is reviewed. In the benchmarking of power density and efficiency as the primary performance metrics, the FCML topology shows the most promising outcomes, as it not only employs higher switching frequency to reduce the size of inductor but also maintains a high level of conversion efficiency. For instance, the reported work in [40] has achieved a better performance by employing a switching frequency of 50MHz compared to other hybrid dc-dc converter designs with a power density of 1.297 W/mm^2 and a peak efficiency of 90%. Although there are several proposed work that have shown higher peak efficiency of more than 90%, but the tradeoff in power density has hindered the architecture from being desirable. Furthermore, a new research area has been reviewed and discussed to realize the novel concept of hybrid dc-dc converter architecture for future works. Evidently, the tradeoff between power density and power efficiency is inevitable, thus optimization is always required to determine the desired design quality from different hybrid architectures.

REFERENCES

[1] J. Jiang, X. Liu, W.-H. Ki, P. K. T. Mok, and Y. Lu, "Circuit techniques for high efficiency fully-integrated switched-capacitor converters," *IEEE Trans. Circuits Syst. II, Exp. Briefs*, vol. 68, no. 2, pp. 556–561, Feb. 2021, doi: 10.1109/TCSII.2020.3046514.

[2] M. H.-W. Loo, H. Ramiah, K.-M. Lei, C. C. Lim, N. S. Lai, P.-I. Mak, and R. P. Martins, "Fully-integrated timers for ultra-low-power Internet-of-Things nodes—Fundamentals and design techniques," *IEEE Access*, vol. 10, pp. 65936–65950, 2022, doi: 10.1109/ACCESS.2022.3183995.

[3] X. Liu, "Session 18 overview: DC–DC converters," in *Proc. IEEE Int. Solid-State Circuits Conf. (ISSCC)*, vol. 65, Feb. 2022, pp. 296–297, doi: 10.1109/ISSCC42614.2022.9731632.

[4] N. Tang, W. Hong, B. Nguyen, Z. Zhou, J.-H. Kim, and D. Heo, "Fully integrated switched-inductor-capacitor voltage regulator with 0.82-A/mm^2 peak current density and 78% peak power efficiency," *IEEE J. Solid-State Circuits*, vol. 56, no. 6, pp. 1805–1815, Jun. 2021, doi: 10.1109/JSSC.2020.3036394.

[5] A. Novello, G. Atzeni, J. Kunzli, G. Cristiano, M. Coustans, and T. Jang, "A 1.25-GHz fully integrated DC–DC converter using electromagnetically coupled class-D LC oscillators," *IEEE J. Solid-State Circuits*, vol. 56, no. 12, pp. 3639–3654, Dec. 2021, doi: 10.1109/JSSC.2021.3112129.

[6] G. K. Kumar, T. Kobaku, S. Sahoo, B. Subudhi, D. Elangovan, and F. Blaabjerg, "An overview of fully integrated switching power converters based on switched-capacitor versus inductive approach and their advanced control aspects," *Energies*, vol. 14, no. 11, p. 3250, Jun. 2021, doi: 10.3390/en14113250.

[7] M.-K. Law, Y. Jiang, P.-I. Mak, and R. P. Martins, "Miniaturized energy harvesting systems using switched-capacitor DC–DC converters," *IEEE Trans. Circuits Syst. II, Exp. Briefs*, vol. 69, no. 6, pp. 2629–2634, Jun. 2022, doi: 10.1109/TCSII.2022.3168307.

[8] C.-H. Chan, L. Cheng, W. Deng, P. Feng, L. Geng, M. Huang, H. Jia, L. Jie, K. M. Lei, X. Liu, and X. Liu, "Trending IC design directions in 2022," *J. Semiconductors*, vol. 43, no. 7, 2022, Art. no. 071401, doi: 10.1088/1674-4926/43/7/071401.

[9] W. Kim, D. Brooks, and G.-Y. Wei, "A fully-integrated 3-level DC–DC converter for nanosecond-scale DVFS," *IEEE J. Solid-State Circuits*, vol. 47, no. 1, pp. 206–219, Jan. 2012, doi: 10.1109/JSSC.2011.2169309.

[10] S. S. Amin and P. P. Mercier, "A fully integrated Li-ion-compatible hybrid four-level DC–DC converter in 28-nm FDSOI," *IEEE J. Solid-State Circuits*, vol. 54, no. 3, pp. 720–732, Mar. 2019, doi: 10.1109/JSSC.2018.2880183.

[11] C. Schaef, S. Weng, B. Choi, W. Lambert, K. Radhakrishnan, K. Ravichandran, J. Tschanz, and V. De, "A 93.8% peak efficiency, 5 V-input, 10 A max ILOAD flying capacitor multilevel converter in 22 nm CMOS featuring wide output voltage range and flying capacitor precharging," in *IEEE Int. Solid-State Circuits Conf. (ISSCC) Dig. Tech. Papers*, Feb. 2019, pp. 146–148, doi: 10.1109/ISSCC.2019.8662475.

[12] A. Abdulslam, F. El-Sehrawy, and Y. Ismail, "Five-level hybrid DC–DC converter with enhanced light-load efficiency," in *Proc. IEEE Int. Symp. Circuits Syst. (ISCAS)*, May 2016, pp. 217–220, doi: 10.1109/ISCAS.2016.7527209.

[13] Y. Lu, J. Jiang, and W.-H. Ki, "A multiphase switched-capacitor DC–DC converter ring with fast transient response and small ripple," *IEEE J. Solid-State Circuits*, vol. 52, no. 2, pp. 579–591, Feb. 2017, doi: 10.1109/JSSC.2016.2617315.

[14] P.-Y. Wang, Y.-W. Huang, and T.-H. Kuo, "A reconfigurable transient optimizer applied to a four-phase buck converter for optimizing both DVS and load transient responses," *IEEE Trans. Circuits Syst. II, Exp. Briefs*, vol. 67, no. 1, pp. 52–56, Jan. 2020, doi: 10.1109/TCSII.2019.2904308.

[15] L. Zhao, J. Tang, and C. Huang, "A fully in-package 4-phase fixed-frequency DAB hysteretic controlled DC–DC converter with enhanced efficiency, load regulation and transient response," in *Proc. IEEE Custom Integr. Circuits Conf. (CICC)*, Apr. 2022, pp. 01–02, doi: 10.1109/CICC53496.2022.9772798.

[16] C. Hardy, Y. Ramadass, K. Scoones, and H.-P. Le, "A flying-inductor hybrid DC–DC converter for 1-cell and 2-cell smart-cable battery chargers," *IEEE J. Solid-State Circuits*, vol. 54, no. 12, pp. 3292–3305, Dec. 2019, doi: 10.1109/JSSC.2019.2944837.

[17] A. Abdulslam and P. P. Mercier, "A symmetric modified multilevel ladder PMIC for battery-connected applications," *IEEE J. Solid-State Circuits*, vol. 55, no. 3, pp. 767–780, Mar. 2020, doi: 10.1109/JSSC.2019.2957658.

[18] C. Wang, Y. Lu, M. Huang, and R. Martins, "A two-phase three-level buck converter with cross-connected flying capacitors for inductor current balancing," *IEEE Trans. Power Electron.*, vol. 36, no. 12, pp. 13855–13866, Dec. 2021, doi: 10.1109/TPEL.2021.3084218.

[19] M. Huang, Y. Lu, T. Hu, and R. P. Martins, "A hybrid boost converter with cross-connected flying capacitors," *IEEE J. Solid-State Circuits*, vol. 56, no. 7, pp. 2102–2112, Jul. 2021, doi: 10.1109/JSSC.2020.3044062.

[20] P. Assem, W.-C. Liu, Y. Lei, P. K. Hanumolu, and R. C. N. Pilawa-Podgurski, "Hybrid Dickson switched-capacitor converter with wide conversion ratio in 65-nm CMOS," *IEEE J. Solid-State Circuits*, vol. 55, no. 9, pp. 2513–2528, Sep. 2020, doi: 10.1109/JSSC.2020.3004256.

[21] C. Chen, J. Liu, and H. Lee, "A 92.7%-efficiency 30A 48V-to-1V dual-path hybrid Dickson converter for PoL applications," in *Proc. IEEE Energy Convers. Congr. Expo. (ECCE)*, Oct. 2021, pp. 1989–1994, doi: 10.1109/ECCE47101.2021.9595635.

[22] X. Yang, L. Zhao, M. Zhao, Z. Tan, L. He, Y. Ding, W. Li, and W. Qu, "A 5V input 98.4% peak efficiency reconfigurable capacitive-sigma converter with greater than 90% peak efficiency for the entire 0.4∼1.2V output range," in *IEEE Int. Solid-State Circuits Conf. (ISSCC) Dig. Tech. Papers*, Feb. 2022, pp. 108–110, doi: 10.1109/ISSCC42614.2022.9731550.

[23] K. Wei, Y. Ramadass, and D. B. Ma, "Direct 12V/24V-to-1V tri-state double step-down power converter with online V_{CF} rebalancing and in-situ precharge rate regulation," *IEEE J. Solid-State Circuits*, vol. 56, no. 8, pp. 2416–2426, Aug. 2021, doi: 10.1109/JSSC.2021.3053457.

[24] J. Huang, C. S. Lam, Y. Lu, and R. P. Martins, "A symmetrical double step-down converter with extended voltage conversion ratio," *IEEE Trans. Circuits Syst. I, Reg. Papers*, vol. 62, no. 12, pp. 1–13, Aug. 2022, doi: 10.1109/TCSI.2022.3197356.

[25] A. Abdulslam and P. P. Mercier, "A passive-stacked third-order buck converter with inherent input filtering achieving 0.7-W/mm^2 power density and 94% peak efficiency," *IEEE Solid-State Circuits Lett.*, vol. 2, no. 11, pp. 240–243, Aug. 2019, doi: 10.1109/LSSC.2019.2935563.

[26] N. Tang, B. Nguyen, Y. Tang, W. Hong, Z. Zhou, and D. Heo, "Fully integrated buck converter with 78% efficiency at 365mW output power enabled by switched-inductor capacitor topology and inductor current reduction technique," in *IEEE Int. Solid-State Circuits Conf. (ISSCC) Dig. Tech. Papers*, Feb. 2019, pp. 152–154, doi: 10.1109/ISSCC.2019.8662530.

[27] Y. Huh, S.-W. Hong, and G.-H. Cho, "A hybrid structure dual-path step-down converter with 96.2% peak efficiency using 250-mΩ large-DCR inductor," *IEEE J. Solid-State Circuits*, vol. 54, no. 4, pp. 959–967, Apr. 2019, doi: 10.1109/JSSC.2018.2882526.

[28] K. Hata, Y. Yamauchi, T. Sai, T. Sakurai, and M. Takamiya, "48V-to-12V dual-path hybrid DC–DC converter," in *Proc. IEEE Appl. Power Electron. Conf. Expo. (APEC)*, Mar. 2020, pp. 2279–2284, doi: 10.1109/APEC39645.2020.9124077.

[29] S. Zhen, R. Yang, D. Wu, Y. Cheng, P. Luo, and B. Zhang, "Design of hybrid dual-path DC–DC converter with wide input voltage efficiency improvement," in *Proc. IEEE Int. Symp. Circuits Syst. (ISCAS)*, May 2021, pp. 1–5, doi: 10.1109/ISCAS51556.2021.9401442.

[30] J.-Y. Ko, Y. Huh, M.-W. Ko, G.-G. Kang, G.-H. Cho, and H.-S. Kim, "A 4.5V-input 0.3-to-1.7V-output step-down always-dual-path DC–DC converter achieving 91.5%-efficiency with 250 mΩ-DCR inductor for low-voltage SoCs," in *Proc. Symp. VLSI Circuits*, Jun. 2021, pp. 1–2, doi: 10.23919/VLSICircuits52068.2021.9492478.

[31] X. Zhang, Q. Ma, Y. Jiang, M.-K. Law, P.-I. Mak, and R. P. Martins, "A 12V-to-1V switched-capacitor-assisted hybrid converter with dual-path charge conduction and zero-voltage switching," *IEICE Electron. Exp.*, vol. 18, no. 22, Nov. 2021, Art. no. 20210382, doi: 10.1587/elex.18.20210382.

[32] G. Cai, Y. Lu, and R. Martins, "A battery-input sub-1V output 92.9% peak efficiency 0.3A/mm^2 current density hybrid SC-parallel-inductor buck converter with reduced inductor current in 65 nm CMOS," in *IEEE Int. Solid-State Circuits Conf. (ISSCC) Dig. Tech. Papers*, Feb. 2022, pp. 312–314, doi: 10.1109/ISSCC42614.2022.9731576.

[33] A. Abdulslam, S. H. Amer, A. S. Emara, and Y. Ismail, "Evaluation of multi-level buck converters for low-power applications," in *Proc. IEEE Int. Symp. Circuits Syst. (ISCAS)*, May 2016, pp. 794–797, doi: 10.1109/ISCAS.2016.7527360.

[34] G. Tochou, A. Cathelin, A. Frappe, A. Kaiser, and J. Rabaey, "Impact of forward body-biasing on ultra-low voltage switched-capacitor RF power amplifier in 28 nm FD-SOI," *IEEE Trans. Circuits Syst. II, Exp. Briefs*, vol. 69, no. 1, pp. 50–54, Jan. 2022, doi: 10.1109/TCSII.2021.3088996.

[35] I. Bhattacharjee and G. Chowdary, "A 0.3 nW, 0.093%/V line sensitivity, temperature compensated bulk-programmable voltage reference for wireless sensor nodes," *IEEE Trans. Very Large Scale Integr. (VLSI) Syst.*, vol. 30, no. 9, pp. 1281–1293, Sep. 2022, doi: 10.1109/TVLSI.2022.3178735.

[36] M. Ghoneima and Y. Ismail, "Accurate decoupling of capacitively coupled buses," in *Proc. IEEE Int. Symp. Circuits Syst.*, vol. 4, May 2005, pp. 4146–4149, doi: 10.1109/ISCAS.2005.1465544.

[37] C. Chen, J. Liu, and H. Lee, "A 2-5 MHz multiple DC output hybrid boost converter with scalable CR boosting scheme achievi 1 ng 91% efficie 1 ncy at a conversion ratio of 12," in *IEEE Int. Solid-State Circuits Conf. (ISSCC) Dig. Tech. Papers*, vol. 65, Feb. 2022, pp. 1–3, doi: 10.1109/ISSCC42614.2022.9731710.

[38] A. Abdulslam, B. Mohammad, M. Ismail, P. P. Mercier, and Y. Ismail, "A 93% peak efficiency fully-integrated multilevel multistate hybrid DC–DC converter," *IEEE Trans. Circuits Syst. I, Reg. Papers*, vol. 65, no. 8, pp. 2617–2630, Aug. 2018, doi: 10.1109/TCSI.2018.2793163.

[39] J.-H. Cho, D.-K. Kim, H.-H. Bae, Y.-J. Lee, S.-T. Koh, Y. Choo, J.-S. Paek, and H.-S. Kim, "A 1.23 W/mm^2 83.7%-efficiency 400 MHz 6-phase fully integrated buck converter in 28 nm CMOS with on-chip capacitor dynamic re-allocation for inter-inductor current balancing and fast DVS of 75 mV/ns," in *IEEE Int. Solid-State Circuits Conf. (ISSCC) Dig. Tech. Papers*, Feb. 2022, pp. 1–3, doi: 10.1109/ISSCC42614.2022.9731726.

[40] X. Liu, C. Huang, and P. K. T. Mok, "A high-frequency three-level buck converter with real-time calibration and wide output range for fast-DVS," *IEEE J. Solid-State Circuits*, vol. 53, no. 2, pp. 582–595, Feb. 2018, doi: 10.1109/JSSC.2017.2755683.

[41] Q. Liu, Z. Mu, C. Liu, L. Zhao, L. Chen, Y. Yang, X. Wei, and W. Yu, "Gate-all-around MOSFET built on void embedded silicon on insulator substrate," *IEEE Electron Device Lett.*, vol. 42, no. 5, pp. 657–660, May 2021, doi: 10.1109/LED.2021.3066171.

[42] A. Stillwell, E. Candan, and R. C. N. Pilawa-Podgurski, "Active voltage balancing in flying capacitor multi-level converters with valley current detection and constant effective duty cycle control," *IEEE Trans. Power Electron.*, vol. 34, no. 11, pp. 11429–11441, Nov. 2019, doi: 10.1109/TPEL.2019.2899899.

[43] K. K. P. Churchill, G. Chong, H. Ramiah, M. Y. Ahmad, and J. Rajendran, "Low-voltage capacitive-based step-up DC–DC converters for RF energy harvesting system: A review," *IEEE Access*, vol. 8, pp. 186393–186407, 2020, doi: 10.1109/ACCESS.2020.3028856.

[44] J. K. Yong, H. Ramiah, K. K. P. Churchill, G. Chong, S. Mekhilef, Y. Chen, P.-I. Mak, and R. P. Martins, "A 0.1-V VIN subthreshold 3-stage dual-branch charge pump with 43.4% peak power conversion efficiency using advanced dynamic gate-bias," *IEEE Trans. Circuits Syst. II, Exp. Briefs*, vol. 69, no. 9, pp. 3929–3933, Sep. 2022, doi: 10.1109/TCSII.2022.3182344.

[45] A. C. C. Chun, H. Ramiah, and S. Mekhilef, "Wide power dynamic range CMOS RF-DC rectifier for RF energy harvesting system: A review," *IEEE Access*, vol. 10, pp. 23948–23963, 2022, doi: 10.1109/ACCESS.2022.3155240.

[46] D. Yang, Y. Ding, and S. Huang, "A 65-nm high-frequency low-noise CMOS-based RF SoC technology," *IEEE Trans. Electron Devices*, vol. 57, no. 1, pp. 328–335, Jan. 2010, doi: 10.1109/TED.2009.2034994.

[47] W. S. Sul and S. G. Pyo, "RF characteristic analysis model extraction on the stacked metal–insulator–metal capacitors for radio frequency applications," *IEEE Trans. Electron Devices*, vol. 61, no. 8, pp. 3011–3013, Aug. 2014, doi: 10.1109/TED.2014.2330842.

[48] S. Dam and P. Mandal, "A hybrid, fully-integrated, dual-output DC–DC converter for portable electronics," *IEEE Trans. Power Electron.*, vol. 36, no. 4, pp. 4360–4370, Apr. 2021, doi: 10.1109/TPEL.2020.3019273.

[49] H. Meyvaert, T. Van Breussegem, and M. Steyaert, "A 1.65W fully integrated 90nm bulk CMOS capacitive DC–DC converter with intrinsic charge recycling," *IEEE Trans. Power Electron.*, vol. 28, no. 9, pp. 4327–4334, Sep. 2013, doi: 10.1109/TPEL.2012.2230339.

[50] T. M. Andersen, F. Krismer, J. W. Kolar, T. Toifl, C. Menolfi, L. Kull, T. Morf, M. Kossel, M. Brändli, and P. A. Francese, "A 10W on-chip switched capacitor voltage regulator with feedforward regulation capability for granular microprocessor power delivery," *IEEE Trans. Power Electron.*, vol. 32, no. 1, pp. 378–393, Jan. 2017, doi: 10.1109/TPEL.2016.2530745.

[51] H. Le, J. Crossley, S. R. Sanders, and E. Alon, "A sub-ns response fully integrated battery-connected switched-capacitor voltage regulator delivering 0.19 W/mm^2 at 73% efficiency," in *IEEE Int. Solid-State Circuits Conf. (ISSCC) Dig. Tech. Papers*, Feb. 2013, pp. 372–373, doi: 10.1109/ISSCC.2013.6487775.

[52] J. Jiang, Y. Lu, C. Huang, W.-H. Ki, and P. K. T. Mok, "A 2-/3-phase fully integrated switched-capacitor DC–DC converter in bulk CMOS for energy-efficient digital circuits with 14% efficiency improvement," in *IEEE Int. Solid-State Circuits Conf. (ISSCC) Dig. Tech. Papers*, Feb. 2015, pp. 1–3, doi: 10.1109/ISSCC.2015.7063078.

[53] N. Butzen and M. S. J. Steyaert, "Design of soft-charging switched-capacitor DC–DC converters using stage outphasing and multiphase soft-charging," *IEEE J. Solid-State Circuits*, vol. 52, no. 12, pp. 3132–3141, Dec. 2017, doi: 10.1109/JSSC.2017.2733539.

[54] M. Lee, Y. Choi, and J. Kim, "A 500-MHz, 0.76-W/mm power density and 76.2% power efficiency, fully integrated digital buck converter in 65-nm CMOS," *IEEE Trans. Ind. Appl.*, vol. 52, no. 4, pp. 3315–3323, Jul. 2016, doi: 10.1109/TIA.2016.2541079.

[55] N. Tang, B. Nguyen, R. Molavi, S. Mirabbasi, Y. Tang, P. Zhang, J. Kim, P. P. Pande, and D. Heo, "Fully integrated buck converter with fourth-order low-pass filter," *IEEE Trans. Power Electron.*, vol. 32, no. 5, pp. 3700–3707, May 2017, doi: 10.1109/TPEL.2016.2593049.

[56] C. Kim, S. Ha, J. Park, A. Akinin, P. P. Mercier, and G. Cauwenberghs, "A 144-MHz fully integrated resonant regulating rectifier with hybrid pulse modulation for mm-sized implants," *IEEE J. Solid-State Circuits*, vol. 52, no. 11, pp. 3043–3055, Nov. 2017, doi: 10.1109/JSSC.2017.2734901.

[57] Z. Xia and J. T. Stauth, "A cascaded hybrid switched-capacitor DC–DC converter capable of fast self startup for USB power delivery," *IEEE J. Solid-State Circuits*, vol. 57, no. 6, pp. 1854–1864, Jun. 2022, doi: 10.1109/JSSC.2022.3162166.

[58] P. H. McLaughlin, Z. Xia, and J. T. Stauth, "A monolithic resonant switched-capacitor voltage regulator with dual-phase merged-*LC* resonator," *IEEE J. Solid-State Circuits*, vol. 55, no. 12, pp. 3179–3188, Dec. 2020, doi: 10.1109/JSSC.2020.3023884.

[59] Y. Jiang, M.-K. Law, Z. Chen, P.-I. Mak, and R. P. Martins, "Algebraic series-parallel-based switched-capacitor DC–DC boost converter with wide input voltage range and enhanced power density," *IEEE J. Solid-State Circuits*, vol. 54, no. 11, pp. 3118–3134, Nov. 2019, doi: 10.1109/JSSC.2019.2935556.

[60] C. Schaef and J. T. Stauth, "A 3-phase resonant switched capacitor converter delivering 7.7 W at 85% efficiency using 1.1nH PCB trace inductors," *IEEE J. Solid-State Circuits*, vol. 50, no. 12, pp. 2861–2869, Dec. 2015, doi: 10.1109/JSSC.2015.2462351.

[61] R. Ondica, D. Arbet, M. Kovac, and V. Stopjakova, "Investigation of inductor-based fully on-chip boost converter," in *Proc. 28th Int. Conf. Mixed Design Integr. Circuits Syst.*, Jun. 2021, pp. 115–119, doi: 10.23919/MIXDES52406.2021.9497548.

[62] R. Huang, H. Wu, J. Kang, D. Xiao, X. Shi, X. An, Y. Tian, R. Wang, L. Zhang, X. Zhang, and Y. Wang, "Challenges of 22 nm and beyond CMOS technology," *Sci. China Ser. F, Inf. Sci.*, vol. 52, no. 9, pp. 1491–1533, Sep. 2009, doi: 10.1007/s11432-009-0167-9.

[63] J.-N. Wu, Y.-M. Chang, Z.-Y. Shen, and H.-C. Chen, "Investigation on CMOS on-chip inductors using various patterned ground/floating shield techniques," in *Proc. Int. Conf. Electron. Commun., Internet Things Big Data (ICEIB)*, Dec. 2021, pp. 113–116, doi: 10.1109/ICEIB53692.2021.9686404.

[64] E. Ashenafi and M. H. Chowdhury, "Noise voltage analysis of spiral inductor for on-chip buck converter design," in *Proc. IEEE Int. Symp. Circuits Syst. (ISCAS)*, May 2017, pp. 1–4, doi: 10.1109/ISCAS.2017.8050820.

[65] J. Aguilera, J. D. No, A. Garcia-Alonso, F. Oehler, H. Hein, and J. Sauerer, "A guide for on-chip inductor design in a conventional CMOS process for RF applications," *Appl. Microw. Wireless*, vol. 13, no. 10, pp. 56–65, 2001.

[66] J. Craninckx and M. S. J. Steyaert, "A 1.8-GHz low-phase-noise CMOS VCO using optimized hollow spiral inductors," *IEEE J. Solid-State Circuits*, vol. 32, no. 5, pp. 736–744, May 1997.

[67] W. X. Lian, H. Ramiah, G. Chong, K. K. P. Churchill, N. S. Lai, Y. Chen, M. Pui-In, and R. P. Martins, "A −20-dBm sensitivity RF energy-harvesting rectifier front end using a transformer IMN," *IEEE Trans. Very Large Scale Integr. (VLSI) Syst.*, vol. 30, no. 11, pp. 1–5, Nov. 2022, doi: 10.1109/TVLSI.2022.3207158.

[68] Y.-C. Hsu, C.-Y. Ting, L.-S. Hsu, J.-Y. Lin, and C. C.-P. Chen, "A transient enhancement DC–DC buck converter with dual operating modes control technique," *IEEE Trans. Circuits Syst. II, Exp. Briefs*, vol. 66, no. 8, pp. 1376–1380, Aug. 2019, doi: 10.1109/TCSII.2018.2883889.

[69] T. Hu, M. Huang, Y. Lu, and R. P. Martins, "A 4 A 12-to-1 flying capacitor cross-connected DC–DC converter with inserted D>0.5 control achieving >2× transient inductor current slew rate and 0.73 theoretical minimum output undershoot of DSD," in *IEEE Int. Solid-State Circuits Conf. (ISSCC) Dig. Tech. Papers*, Feb. 2022, pp. 1–3, doi: 10.1109/ISSCC42614.2022.9731669.

[70] J. S. Rentmeister and J. T. Stauth, "A 92.4% efficient, 5.5V:0.4–1.2V, FCML converter with modified ripple injection control for fast transient response and capacitor balancing," in *Proc. IEEE Custom Integr. Circuits Conf. (CICC)*, Mar. 2020, pp. 1–4, doi: 10.1109/CICC48029.2020.9075902.

[71] Z. Xia and J. Stauth, "A two-stage cascaded hybrid switched-capacitor DC–DC converter with 96.9% peak efficiency tolerating 0.6V/μs input slew rate during startup," in *IEEE Int. Solid-State Circuits Conf. (ISSCC) Dig. Tech. Papers*, Feb. 2021, pp. 256–258, doi: 10.1109/ISSCC42613.2021.9365763.

[72] Z. Zhou, N. Tang, B. Nguyen, W. Hong, P. P. Pande, and D. Heo, "A wide output voltage range single-input-multi-output hybrid DC–DC converter achieving 87.5% peak efficiency with a fast response time and low cross regulation for DVFS applications," in *Proc. IEEE Custom Integr. Circuits Conf. (CICC)*, Mar. 2020, pp. 1–4, doi: 10.1109/CICC48029.2020.9075892.

[73] L. Cheng and W.-H. Ki, "A 30 MHz hybrid buck converter with 36 mV droop and 125 ns 1% settling time for a 1.25 A/2 ns load transient," in *IEEE Int. Solid-State Circuits Conf. (ISSCC) Dig. Tech. Papers*, Feb. 2017, pp. 188–189, doi: 10.1109/ISSCC.2017.7870324.

[74] F. Mao, Y. Lu, E. Bonizzoni, F. Boera, M. Huang, F. Maloberti, and R. P. Martins, "A hybrid single-inductor bipolar-output DC–DC converter with floating negative output for AMOLED displays," *IEEE J. Solid-State Circuits*, vol. 56, no. 9, pp. 2760–2769, Sep. 2021, doi: 10.1109/JSSC.2021.3062092.

[75] J. Yuan, Z. Liu, F. Wu, and L. Cheng, "A 12 V/24 V-to-1 V DSD power converter with 56 mV droop and 0.9μS 1% settling time for a 3 A/20 ns load transient," in *IEEE Int. Solid-State Circuits Conf. (ISSCC) Dig. Tech. Papers*, Feb. 2022, pp. 1–3, doi: 10.1109/ISSCC42614.2022.9731701.

[76] J. Jiang, X. Liu, W.-H. Ki, P. K. T. Mok, and Y. Lu, "A multiphase switched-capacitor converter for fully integrated AMLED microdisplay system," *IEEE Trans. Power Electron.*, vol. 35, no. 6, pp. 6001–6011, Jun. 2020, doi: 10.1109/TPEL.2019.2951799.

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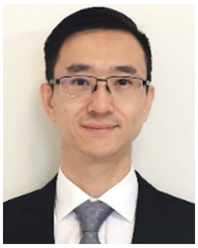

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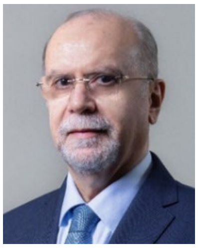

RUI P. MARTINS (Fellow, IEEE) was born in April 1957. He received the bachelor's, master's, and Ph.D. degrees from the Department of Electrical Engineering and Computers, Instituto Superior Técnico (IST), University of Lisbon, Portugal, in 1980, 1985, and 1992, respectively.

He has been with DECE/IST, University of Lisbon, since October 1980. Since October 1992, has been on leave from the University of Lisbon and the Department of Electrical and Computer Engineering, Faculty of Science and Technology (FST), University of Macau (UM), Macau, China, where he has been a Chair-Professor, since August 2013. At FST, he was the Dean, from 1994 to 1997, and has been UM's Vice-Rector, since September 1997. From September 2008 to August 2018, he was the Vice-Rector (Research), and from September 2018 to August 2023, he was the Vice-Rector (Global Affairs). He received the Habilitation for a Full Professor of electrical engineering and computers with the Department of Electrical Engineering and Computers, IST, University of Lisbon, in 2001. He was also the Co-Founder of Chipidea Microelectronics (Macao) [later Synopsys-Macao, and now Akrostar, where the CEO was his Ph.D. student, with double-degree FST-UM/IST-UTL], in 2001 and 2002. In 2003, he created the Analog and Mixed-Signal VLSI Research Laboratory, UM, elevated in January 2011, to the State Key Laboratory (SKLAB) of China (the first in Engineering in Macao), being its Founding Director. He was the Chair of UMTEC (UM company), from January 2009 to March 2019, supporting the incubation and creation, in 2018, of Digifluidic, the first UM Spin-Off, whose CEO is a SKLAB Ph.D. graduate. Within the scope of his teaching and research activities, he has taught 21 bachelor's and master's courses and, in UM, has supervised (or co-supervised) 47 theses: Ph.D. (26) and master's (21). He has authored or coauthored a total of 896 publications: nine books and 12 book chapters, 50 patents, USA (39), China (eight), 745 papers, in scientific journals (331) and in conference proceedings (414), and other 80 academic works (H-index=46/citations=10,000+, Google Scholar).

Prof. Martins has been a member of the Advisory Board of the *Journal of Semiconductors* of the Chinese Institute of Electronics (CIE), Institute of Semiconductors, Chinese Academy of Sciences, since January 2021, and a fellow of the Asia-Pacific Artificial Intelligent Association, since October 2021. He was also a member of the IEEE CASS Fellow Evaluation Committee (a member, in 2013, 2014, and 2019, the Chair, in 2018, and the Vice-Chair, in 2021 and 2022), the IEEE Nominating Committee of Division I Director (CASS/EDS/SSCS), in 2014; and the IEEE CASS Nominations Committee Member (2016–2017). He was the Founding Chair of the IEEE Macau Section (2003–2005) and the IEEE Macau Joint-Chapter on Circuits and Systems (CAS)/Communications (COM) (2005–2008) [2009 World Chapter of the Year of IEEE CAS Society (CASS)], the General Chair of the IEEE Asia-Pacific Conference on CAS—APCCAS 2008, the Vice-President (VP) Region 10 (Asia, Australia, and Pacific) (2009–2011), and VP-World Regional Activities and Membership of IEEE CASS (2012–2013), an Associate Editor of IEEE Transactions on Circuits and Systems—II: Express Briefs (2010–2013), nominated as a Best Associate Editor (2012–2013). In addition, he was the General Chair of ACM/IEEE Asia South Pacific Design Automation Conference—ASP-DAC 2016, receiving the IEEE Council on Electronic Design Automation (CEDA) Outstanding Service Award, in 2016, and also the General Chair of the IEEE Asian Solid-State Circuits Conference—A-SSCC 2019. He was the Vice President (2005–2014), the President (2014–2017), and the Vice-President (2021–2024) of the Association of Portuguese Speaking Universities (AULP), in September 2021, was a nominated Honorary Member of AULP (an honor only bestowed on five people in the world). He also received three Macao Government decorations: the Medal of Professional Merit (Portuguese-1999), the Honorary Title of Value (Chinese-2001), and the Medal of Merit in Education (Chinese-2021). On July 2010, he was elected, unanimously, to the Lisbon Academy of Sciences, as a Corresponding (2010–2022) and Effective Member (2022), being the only Portuguese Academician working and living in Asia.