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APPLIED RESEARCH

Novel Universal Power Electronic Interface for Integration of PV Modules and Battery Energy Storages in Residential DC Microgrids

VADIM SIDOROV[1], (Graduate Student Member, IEEE), ANDRII CHUB[1], (Senior Member, IEEE), DMITRI VINNIKOV[1], (Fellow, IEEE), AND ANDRE LINDVEST[2]

[1]Department of Electrical Power Engineering and Mechatronics, Tallinn University of Technology, 19086 Tallinn, Estonia
[2]Ubik Solutions OÜ, 14114 Tallinn, Estonia

Corresponding author: Vadim Sidorov (vadim.sidorov@taltech.ee)

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ABSTRACT This paper introduces the novel concept of a highly versatile smart power electronic interface for fast deployment of residential dc microgrids. The proposed approach has bidirectional power flow control capabilities, wide operating voltage range, and high efficiency resulting from the topology morphing control utilization. This enables universal compatibility with the majority of the commercial 60- and 72-cell photovoltaic modules, as well as the efficient charge/discharge control of the 24 V and 48 V battery energy storages using the same hardware platform. The proposed concept features fully autonomous operation where switching between the photovoltaic and battery interfacing modes is automatically done using the input source identification algorithm. Moreover, the proposed universal interface converter employs droop control and solid-state protection, making it fully compatible with the emerging standards and requirements for power electronic systems used in dc microgrid environments. A 350 W prototype was developed and tested in the residential 350 V dc microgrid with droop control to validate the proposed concept experimentally.

INDEX TERMS Microgrids, DC–DC converters, battery chargers, photovoltaic systems, universal converter.

I. INTRODUCTION

The European Commission has set the Energy Directive for at least a 55% reduction in greenhouse gas emissions and increasing renewable energy sources by 40% in buildings by 2030 [1]. Residential and commercial buildings contribute close to 40% of the total energy consumption in the European Union and U.S. [2]. One of the solutions for achieving these targets is to install photovoltaic (PV) and energy storage systems in residential buildings [3], [4], [5].

However, PV alone cannot cut carbon footprint of the building stock significantly. It should be accompanied by system-level energy efficiency optimization. Dc power distribution is the next technology step that can push the limits of possible efficiency optimization. Dc distribution minimizes losses in the residential power system and maximizes its utilization, improving the overall power supply reliability [6].

Dc houses could provide up to 15% higher efficiency in residential buildings and close to 20% in commercial buildings compared to those with ac distribution [7], [8]. Currently, a lack of standards and associated equipment impede the wider deployment of residential dc microgrids [9], while some countries, like the Netherlands, showed strong efforts in standardization [10].

New types of power electronic converters need to be developed to facilitate the deployment of residential dc microgrids. Modularity could enable new plug-and-play interface converters to be easily scalable for the needs of every customer, ensuring their low cost, simple system design, and fast deployment, as was shown for different power electronics applications [11], [12], [13], [14], [15], [16], [17], [18]. In residential applications, modular converters were shown

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for battery energy storage [12], [17], small wind turbines [14], and PV module-level power electronics [15].

Recent research proposes complementing modularity with application flexibility by extending the input-voltage regulation range [19]. As a result, the same stock-keeping units can be reused for deploying dc microgrids based on different technologies, like silicon (Si) and thin-film PV modules [27]. Extending the universal applicability concept from a single application type to several is logical. Matching PV modules with standardized battery packs in low-voltage dc microgrids (like 24 V or 48 V) is common. This inspired the proposed idea of the universal power electronic interface (UPEI) that can be universally used to integrate Si PV modules or low-voltage batteries.

The proposed concept of the UPEI is novel and provides unique features compared to the solutions on the market and in the literature. Previously presented isolated dc-dc converters have been highly specialized according to a type of input source. However, they feature virtually similar voltage ranges: dc-dc converters for single PV modules mostly operate within input voltage from 15 to 50 V [20], [21], [22], and battery converters operate from 20 to 60 V [23], [24], [25]. Recently, only one universal converter was present in the literature, capable of operating with a PV module and a battery [26]. However, the presented converter operates in the input range of 40…80 V and the output voltage between 60 V and 120 V, which does not allow connecting market-leading PV modules and batteries to the dc microgrid with the voltage bus of 350V. Furthermore, the maximum efficiency of the converter is less than 94% due to high voltage stress on the switches.

Generally, the UPEI follows the trend for universalization is evident in research and industry, especially in the recent decade. This trend could be observed in the following fields:

- universal solar converters with wide input voltage range for capability with different types of PV modules such as 60- or 72-cell Si-based, or CdTe- and CIGS-based thin-film types [27], [28], [29];
- universal electric vehicle chargers for different standards of battery packs (320, 360, 400, 450, 600, and 800 V) [30];
- rail-grade converters with wide input voltage range from 14 to 160 V and different output voltages such as 5, 12, 24, and 48 V needed to fit a wide variety of battery types used in the railway industry as defined by EN50155 standard [31], [32], [33];
- universal converters for USB Power Delivery 3.1 with different output voltages such as 5, 9, 12, 20, 28, 36, and 48 V [35].

The universality of power electronics reduces the soft cost of deployment in final systems, like those related to staff training, shipping and supply chain management, warranty claims, after-sale support, etc. For example, in residential solar systems, the soft costs correspond to 65% of the total system cost [34]. UPEI allows for simpler deployment of different PV modules or batteries in dc microgrids using a single stock-keeping unit. It is instrumental in the current state of the residential dc microgrid industry when a wide range of PV and battery products is emerging on the market. There are no solutions for the fast deployment of dc microgrids like UPEI. Hence, it is essential to validate UPEI performance in the target applications.

This paper presents an entirely novel concept of a highly versatile bidirectional power electronic interface for the fast deployment of residential dc microgrids. The proposed approach is characterized by enhanced voltage control capabilities based on the application of topology morphing control. This paper discusses the realization and experimental validation of the proposed UPEI concept. Section II focuses on the realization of the UPEI. Section III and Section IV describe the operation of the UPEI in the PV and battery interfacing modes, respectively, with selected design guidelines and experimental verifications. Further, Section V presents the input source identification algorithm allowing for the implementation of plug&play functionality. Finally, the conclusions of the paper are drawn in Section VI.

II. IMPLEMENTATION OF THE UPEI

The proposed UPEI was inspired by the bidirectional isolated hexa-mode dc-dc converter (IHMC), recently proposed by the authors in [36]. This section explains design requirements and provides a brief description of the topology and its modulation techniques used to implement the novel UPEI concept.

A. UPEI TECHNOLOGY

The converter consists of the MOSFET-based low- and high-voltage hybrid switching cells connected by a high-frequency transformer (Fig. 1). The UPEI provides buck-boost voltage regulation along with bidirectional operation capability, which significantly extends its voltage regulation range in both directions of power flow. The converter is controlled using the topology morphing control (TMC) principle [36], where the topology of both hybrid switching cells can be reconfigured on-the-fly from a full-bridge to a half-bridge and back. This allows the converter dc gain to be changed in the wide range in both directions of power flow. The capacitors C_2 and C_3 are primarily intended for blocking the dc bias when a hybrid switching cell is configured to a half-bridge. These capacitors form a series resonant tank with the leakage inductance (L_{lk}) of the transformer TX. The resonant tank is designed with a quality factor below 1 to operate under the discontinuous resonant current mode. The mathematical analysis of the IHMC was described in detail in [36].

The application of TMC is one of the distinguishing features of the proposed bidirectional UPEI. The TMC is realized on the fly by turning on one switch and turning off the other one in one leg, as shown in Fig. 2. By utilizing the TMC, the UPEI can operate with three topological configurations in both directions of power flow: full-bridge inverter (FBI) – the full-bridge rectifier (FBR), the half-bridge inverter (HBI) – FBR, and FBI – the

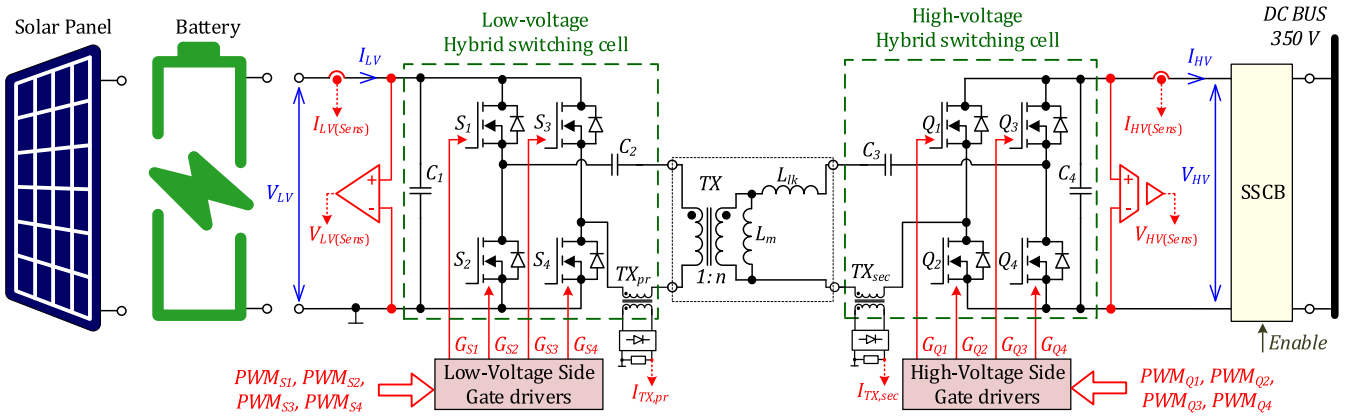

FIGURE 1. Power circuit diagram of the proposed UPEI.

half-bridge rectifier (HBR). Hence, the hybrid switching cells allow for applying six different control modulations in each power flow direction. The combination of topology configurations, operating modes, and corresponding ranges of the normalized dc gain are demonstrated in Fig. 2a.

There are two transition regions between the buck mode of one configuration and the boost mode of another one. Points of transitions are selected empirically or by estimating the converter efficiency. To avoid high current stresses during transitions, the algorithm for soft transitions and recharging series capacitors C_2 and C_3 was proposed in [40]. The main idea of the soft-transition algorithm is linearly increasing or decreasing the duty cycle of transistors in a leg. This results in the transistor being phased out from modulated to static state or vice versa to keep the input voltage and current levels at the same values.

There is no need for a special control algorithm to transition between buck and boost modes within one topology configuration, e.g., between the FBI-FBR buck and boost modes. This results from the modulations for the buck and modes providing the same switching sequence at these points. The series capacitors C_2 and C_3 neutralize any dc bias current in the transformer.

B. DESIGN AND SPECIFICATIONS OF THE PROTOTYPE

The bidirectional UPEI was designed to operate in the safe operating area (SOA) within the low voltage (LV) from 10 V to 60 V, the high voltage (HV) from 320 V to 380 V, the maximum power of 350 W, and the maximum current at the low-voltage side of ±12 A in both power directions. The SOA covers operation ranges of typical market-leading 60- and 72-cell Si PV modules and typical 24 V/48 V batteries. The bidirectional UPIE was designed for operation in droop-controlled 350 V dc microgrids deployed in the Netherlands according to the national standard [10]. Selected components and cooling conditions limit the maximum current and the maximum power of the converter.

Selecting the isolation transformer turns ratio is critical in designing a universal converter. A voltage of an input source can vary in a wide range. In addition, the global maximum power point (GMPP) of a PV module could move to a lower voltage under partial shading. Fig. 3 shows the most probable voltage operating ranges of typical 60- and 72-cells PV modules for different numbers of shaded substrings and two types of LiFePO4 batteries (24 V and 48 V) as the most used types in residential systems. In Fig. 3, boxes show the most probable operating range in residential applications, while the whiskers depict theoretically possible operating voltage. For example, typical 60-cell Si PV modules are arranged in three substrings with three bypass diodes. Without partial shading conditions, its global maximum power point would typically fall between 31 and 33 V, but it could be out of this range in very cold or hot climates.

However, if one substring is severely shaded, the global maximum power point could fall in the typical range of 20 V to 22 V. In some cases, when only one substring is not shaded, the global maximum power point could be near 10 V. Similar behavior could be observed for 72-cell Si PV modules. Moreover, batteries also have a specific operating voltage range that depends on the depth of discharge, which could be 80% to optimize the battery lifetime. All target applications could be fit in the input voltage range from 10 V to 60 V.

Thanks to the topology morphing control, the IHMC features three efficiency peaks at the normalized dc voltage gain equal to 0.5, 1, and 2. With an increase or decrease in the input voltage, efficiency would decrease because the converter operates with buck or boost control modulations, respectively. The efficiency decrease is mainly associated with the increasing RMS and switching currents in the converter. Bold green vertical lines in Fig. 3 show theoretical maximum efficiency voltages, and green gradient fields demonstrate the decreasing efficiency. This placement of maximum efficiency points considers the most probable ranges of the operating voltage and integer steps in the converter dc voltage gain.

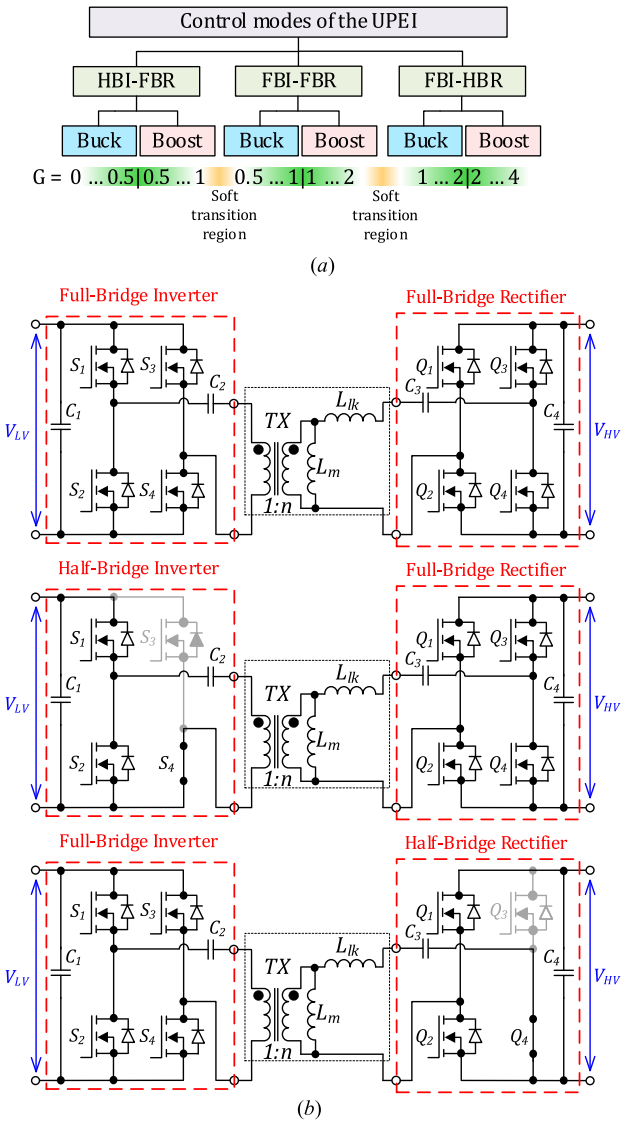

FIGURE 2. Topological configurations, operating modes, normalized voltage gains, and regions of soft transitions of the proposed UPEI (a); equivalent circuits of topology configurations (b).

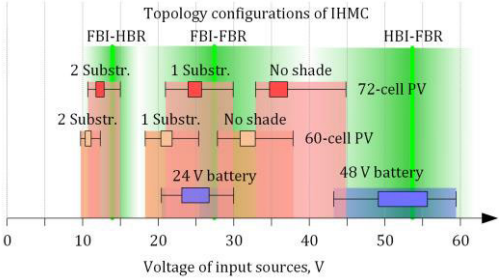

FIGURE 3. Operating voltage range of selected PV module and battery types and resulting target operating range for the UPEI.

The normalized dc voltage gain of the IHMC for the forward power flow can be defined as

$$G = \frac{V_{HV}}{V_{LV} \cdot n}, \tag{1}$$

and for the backward power flow, the voltage gain equals

$$G = \frac{V_{LV} \cdot n}{V_{HV}}. \tag{2}$$

To ensure high efficiency of the convert operating with a variable input source, the turn ratio of the transformer has been selected $n = 12.7$. This turns ratio provides high efficiency at the most probable input voltage values. A switching frequency f_{SW} of 100 kHz is selected as a compromise between component size and efficiency.

As described in [36], the forward buck FBI-HBI mode is the most critical mode for selecting resonant inductance. Previous analysis [37] shows that the inductance of the resonant tank L_{lk} should be high enough to achieve the lowest conduction and switching losses in the converter. On the other hand, the maximum value of the leakage inductance is limited by the Q-factor of the resonant tank, which should be below one for providing the discontinuous resonant current.

The maximum value can be defined in the buck FBI-HBR mode as

$$L_r < \frac{V_{out} \cdot f_S}{I_{out} \cdot \omega_r^2}. \tag{3}$$

By using Eq. (3), the loss-optimized leakage inductance equals 100 μH for operation in the required voltage and power ranges at $f_{SW} = 100$ kHz.

The magnetizing inductance L_m provides zero-voltage switching of low- and high-voltage side transistors in the forward and reverse modes, respectively, by recharging the output capacitances of switches. Therefore, the maximum value of the magnetizing inductance for the forward direction can be defined as

$$L_{m(\max)} \leq \frac{T_{D(LV)} \cdot n}{16 \cdot f_S \cdot C_{oss(LV)}}, \tag{4}$$

where $C_{oss(LV)}$ is the parasitic output capacitance of a low-voltage switch, $T_{D(LV)}$ is the dead-time of the low-voltage side switches.

In the backward power direction, the maximum value of the magnetizing inductance can be calculated as

$$L_{m(\max)} = \frac{T_{D(HV)}}{16 \cdot f_S \cdot C_{oss(HV)}}, \tag{5}$$

where $C_{oss(HV)}$ is the parasitic output capacitance of the high-voltage side switches, $T_{D(HV)}$ is the dead time of high-voltage side switches.

FDMS86180 MOSFETs with $C_{oss(LV)} = 2663$ pF from On Semiconductor were selected as the low-voltage switches. For the high-voltage side, C3M0120100K MOSFETs with $C_{oss(HV)} = 48$ pF from Wolfspeed were chosen. The dead times of $T_{D(LV)} = 100$ ns and $T_{D(LV)} = 150$ ns are selected for low- and high-voltage switches, respectively, resulting in the magnetizing inductance Lm = 2 mH selected.

The flux density achieves the maximum value in the forward buck FBI-FBR at the duty cycle of 0.5. The EE64/21 ferrite planar core from 3C95 material is selected for the transformer. Considering the feasible copper cross-section

area and core losses, the maximum flux density of 90 mT was achieved, and the turns number of the low- and

high-voltage windings equals 2 and 26, respectively. The windings were designed by using a custom 3D-printed split bobbin, which eliminates an external resonant inductor.

Another critical component of the topology is the series resonant capacitors C_2 and C_3. Due to a high current circulating through the low-voltage side, ceramic capacitors were used for realizing C_2. High-voltage film capacitors are selected for C_3 and used for adjusting resonant frequency due to low capacitance variations. The capacitance of the low-voltage ceramic capacitors C_2 should be much more than $C_3(C_2 \gg C_3)$ to avoid deviation of the resonant frequency. The value of the capacitor C_3 can be calculated as

$$C_3 \approx \frac{1}{L_{lk}\omega_r^2}. \tag{6}$$

From the calculation, the C_3 equals 25 nF and should carry the maximum voltage of 380 V. For the low-voltage side, the capacitor of 52 μH was selected, considering the maximum voltage stress of 60 V.

As was analyzed in [38], voltage ripple at any frequency influences the efficiency of PV power harvesting. For providing the maximum power reduction of 0.1%, the voltage ripple should be less than 1% of the nominal voltage at a maximum power point (MPP). At the same time, modern batteries can operate with any current or voltage ripples [39]. Therefore, the LV filter capacitor C_1 should be calculated considering PV applications. According to the requirement, the C_1 was selected at 150 μF with a maximum voltage stress of 60 V.

There is no requirement for voltage ripple in the dc microgrid due to a lack of standardization. However, it was considered to limit the voltage ripple of the HV side by 5% of the V_{HV} =350 V at the maximum power. To provide this, the capacitor C_4 of 5 μF was calculated. In practice, dc microgrid would have a substantially higher capacitance to avoid any voltage oscillations.

By using equations for the normalized voltage gains presented in [36] and Eq. (1), the curves of the low voltage as fictions of the duty cycles are plotted in Fig. 4 for two values of the operating powers $P_1 < P_2$ at $V_{HV} = 350$ V. The voltage ranges between the boost HBI-FBR and the buck FBI-FBR modes; the boost FBI-FBR and the buck FBI-HBR modes are transition regions. Points of transitions between these modes are selected based on the experimental or estimated efficiency curves.

A developed UPEI prototype embeds the power circuit, auxiliary power supply, gate drivers, sensors, protection circuitry, and microcontroller unit in a single four-layer PCB (Fig. 5). The components and parameters are listed in Table 1. The prototype was designed to operate within the maximum current of ±12 A and the maximum power of 350 W, forming a safety operation limit. It should be noted that according to the strict lifetime requirements for the PV microconverters, the developed prototype employs no electrolytic capacitors. The UPEI features natural convection cooling via PCB with

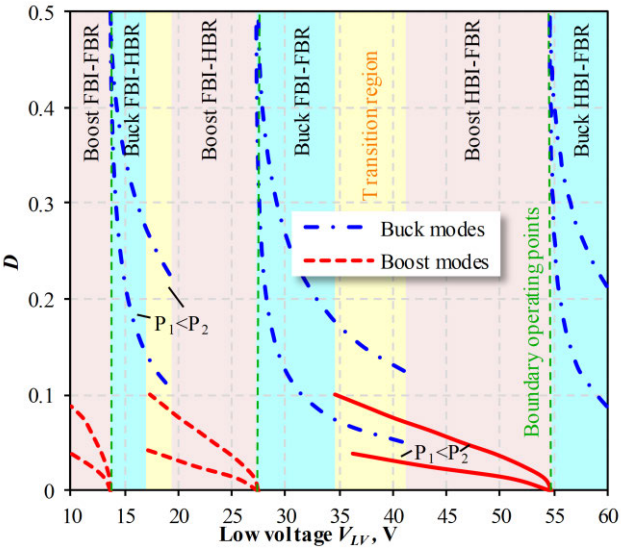

FIGURE 4. Low voltage as a function of the duty cycle.

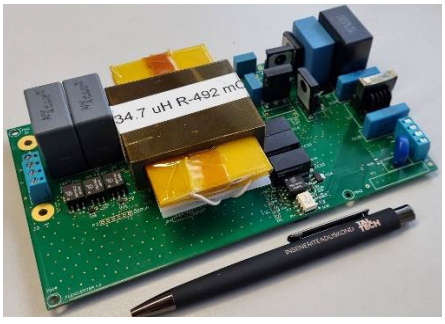

FIGURE 5. Developed 350 W prototype of the UPEI.

specially optimized thermal pads and vias used to move the heat from the parts into the core layers, thus eliminating the hotspots.

The control system of the UPEI (Fig. 6) was realized on the ST STM32G474 microcontroller unit (MCU). The control system has common ground with the low-voltage side of the converter. It allows for a low-cost non-isolated resistive divider for voltage sensing and a shunt for current sensing. The high-voltage side sensors use isolated operation amplifiers connected to the integrated 12-bit analog-to-digital converter pins of the MCU. The state machine has been used in the high-level part of the control architecture. The state machine is switched between eleven states depending on the control algorithms described in Sections III, IV, and V.

The middle level of the control architecture incorporates the following functions: Protection, Filters, Timer for PV rescanning, Synchronous rectifier, and Calculation of compare values. The last block calculates and sets required compare values for each high-resolution timer (HRTIM), implementing the control modulation for the needed direction of power flow. The synchronous rectifier block enables or disables control of rectifier switches depending on power, control

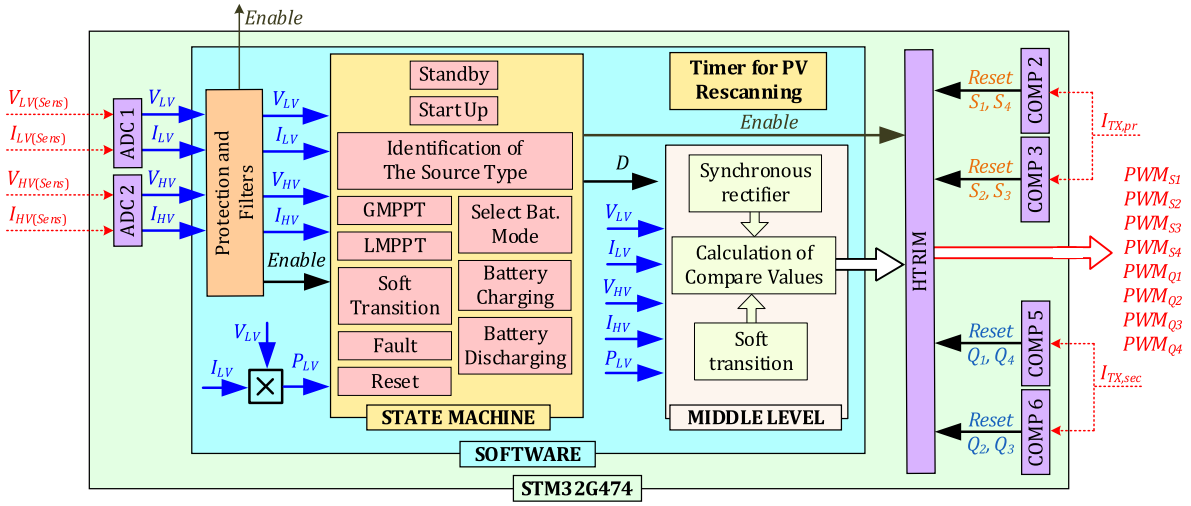

FIGURE 6. Control system of the UPEI.

TABLE 1. General specifications of the UPEI.

Operating Parameters	
V_{LV}	10…60 V
I_{LV}	±12 A
V_{HV}	320…380 V
I_{HV}	±1.1 A
f_{SW}	100 kHz
P	20…350 W
Power Components	
S_1…S_4	On Semiconductor FDMS86180
Q_1…Q_4	Wolfspeed C3M0120100K
TX	EE64/21 planar core, n = 12.8, L_{LK} = 100 µH, L_m = 2 mH
C_1	24 pcs. C1210C225K1R + 2 pcs. R60ER54705040K
C_2	24 pcs. C1210C225K1R
C_3	1pc. B32641B0153J + 1 pc. MC1206F106Z160CT
C_4	1 pc. ECWFG1B475J + 1 pc. B32653A0474J000
Driving and Measurements	
S_1…S_4 drivers	Silicon Labs SI8233BB-D-IS1R
Q_1…Q_4 drivers	Texas Instr. UCC21521ADW
Aux. power	Texas Instr. LM5010MH/NOPB
V_{LV} sensor	Resistive divider 1:20
I_{LV} sensor	Shunt 0.003Ω with OP Microchip MCP6L02T-E/SN
V_{HV} sensor	Texas Instr. AMC1200
I_{HV} sensor	Shunt 0.01Ω with Texas Instr. AMC1200

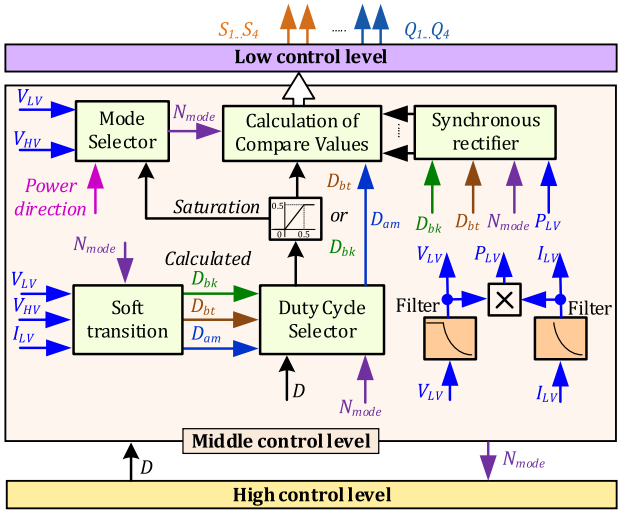

FIGURE 7. Block diagram of the middle-level control system.

modulation, and control mode. The timer for PV rescanning restarts global maximum power point tracking (GMPPT) every 30 minutes if the UPEI operates with a PV module. The software control algorithms execute only when the measured values are within the safety limits.

The SSCB provides a soft plug-in to the dc microgrid by charging the high-voltage capacitor C_4. On the low level, synchronous rectification has been implemented using current transformers and MCU internal comparators (COMPs) to improve the converter efficiency in each control mode [36]. These comparators are connected to the HRTIMs and can be selected as reset sources for output signals, providing a simple and effective solution. At low power, the control system disables the synchronous rectifier and switches from the hybrid phase shifted modulation (PSM) with synchronous rectification to the conventional PSM since the comparators cannot correctly detect the falling resonant current. A look-up table of minimum power has been generated for each control mode to define synchronous rectification limits.

To sum up described algorithms, the block diagram of the middle-level control system is presented in Fig. 7. The input control signal for the middle-level control system is a duty cycle D, which can be the duty cycles of buck modulations D_{bk} or the duty cycles of boost modulations D_{bt}. The high-level control system sets the duty cycle in the closed-loop control system. Depending on the dc voltage gain of the converter and the required power direction, the mode selector automatically chooses a control mode.

Besides, the mode selector changes a control mode when the duty cycle achieves saturation.

At the same time, when the system achieves one of the thresholds for the soft transition, the control system switches to the soft transition algorithm, and duty cycle selector applies calculated duty cycles D_{bk}, D_{bt}, and D_{am} for calculation of compare values.

Due to a lack of standardization, there are still no requirements for the control bandwidth of voltage or current regulation in dc microgrids. However, due to high capacitance, the dc microgrids feature a high voltage inertia. Therefore, fast regulation is unnecessary, and current or voltage regulators can be tuned for a low crossover frequency. The conventional PI regulator is a suitable and simple solution for controlling the voltage of a PV module as well as the current of a battery.

The parameters of the regulator should be tuned or calculated for each control mode and each type of energy source. During switching between control modes, the mode selector in the middle-level control system changes the parameters of regulators according to the control modes.

The SmartCtr tool in PSIM software is used to tune the regulator parameters. The criteria for the regulator in any control mode are a phase margin of 60 degrees and a crossover frequency of 300 Hz. These criteria provide aperiodic voltage or current step response.

C. EFFICIENCY MAPPING

To evaluate the performance of the designed UPEI in wide voltage and power range, efficiency has been measured by the precision power analyzer Yokogawa WT1800, approximated by thin-plate splines, and plotted in Fig. 8. The power of the converter is limited in the range from 20 W to 350 W, the maximum current at the low-voltage side is 12 A. The experimental analysis shows that the UPEI demonstrates efficiency above 90%, with a peak of 98.1% in both power directions. As described above, thanks to the TMC, the converter has three pronounced efficiency peaks at $V_{LV} \approx 14$, 27, 56 V when the converter operates between buck and boost mode with the lowest power losses. At low power, the synchronous rectifier does not operate, which results in efficiency reduction.

III. PV INTERFACING MODE

This section presents the control algorithm and experimental evaluation of UPEI in the PV interfacing mode.

A. MAXIMUM POER POINT TRACKING

Thanks to the ultrawide voltage gain regulation capability, the developed UPEI performs global maximum power point tracking (GMPPT) in all possible operating scenarios, including opaque shading of substrings. Among different global tracking approaches, the voltage sweep GMPPT was applied as a simple, effective, and robust algorithm that can operate with different types of PV modules [42].

The voltage sweep GMPPT is based on scanning a power-voltage curve of a PV module by decreasing the reference voltage $V_{LV(ref)}$ from the open-circuit voltage (OCV) to the minimum operation voltage V_{MIN} of the converter with

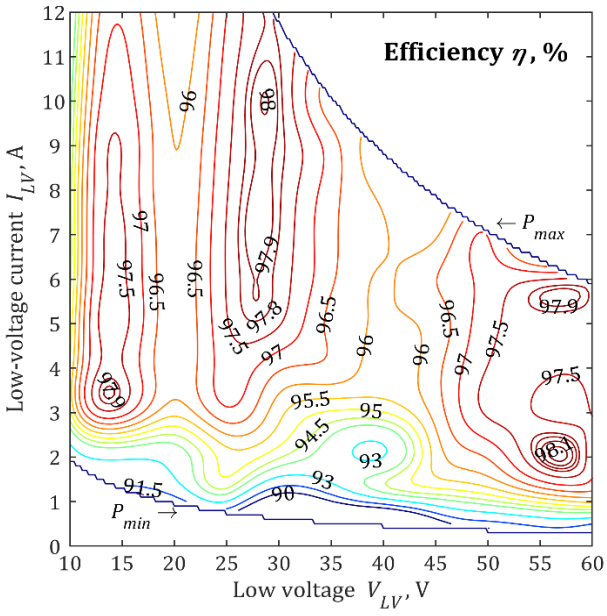

FIGURE 8. Efficiency map of the UPEI.

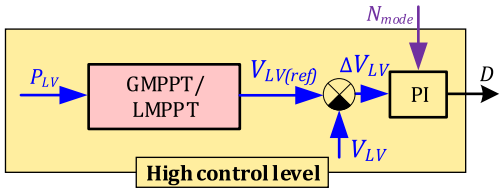

FIGURE 9. Block diagram of the high-level control system in the PV mode.

a voltage step V_{step}. After reaching the minimum operation voltage V_{MIN}, the GMMPT algorithm analyzes stored MPP data and finds the GMPP. Then the algorithm transits to the GMPP by setting the $V_{LV(ref)}$ equal to the voltage of the GMPP. After that, the control system switches to the local MPPT (LMPPT) based on the P&O algorithm.

The closed-loop control system for the GMPPT and LMPPT algorithms has been realized based on PI-regulator for controlling the PV voltage, as shown in Fig. 9. Moreover, the GMPPT and LMPPT operate only when the high voltage is in the operating range. In the PV mode, the UPEI operates as unidirectional convert and the control modulations corresponding to the reverse power flow are disabled.

B. MAXIMUM POER POINT TRACKING

To verify the UPEI performance in the PV mode, Longi LR4-60HBD-350M [48] and LR4-72HBD-425M [49] PV modules have been selected. The Solar Array Simulator (SAS) Keysight E4360A was used to emulate these PV modules. For emulating the dc microgrid iTECH IT6006C-800-25 Bi-directional Power Supply was utilized. The used measurement equipment includes an oscilloscope Tektronix DPO7254, differential voltage probes Tektronix P5205A,

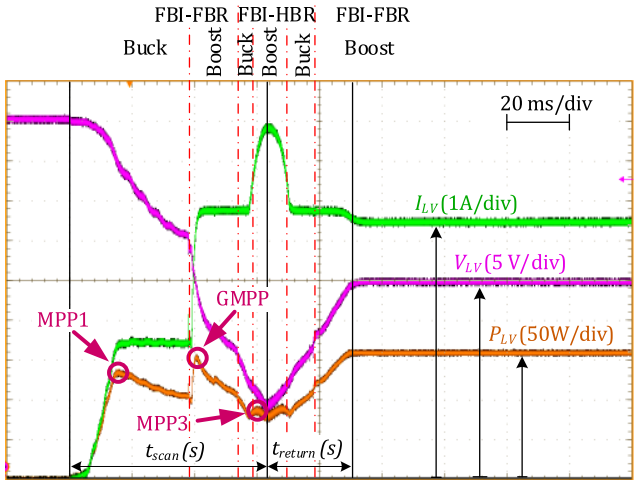

FIGURE 10. Tracking performance of the voltage sweep GMPPT algorithm with the LR4-72HBD-425M PV module operating under partial shading (irradiance of the substrings: 800 W/m^2, 600 W/m^2 and 300 W/m^2).

current probes Tektronix TCP0030A and PEM ultra-mini CWT015 Rogowski coil probe, and power analyzer Yokogawa WT1800.

The experimental result in Fig. 10 shows the performance of the voltage-sweep GMPPT algorithm with LR4-72HBD-425M PV module under a partial shading condition. The preset voltage ramp changes the reference voltage between the OCV and the minimum operating voltage. During the scanning, the middle-level control system switches through all the control modulations from the buck FBI-FBR to the boost FBI-HBR.

The soft transition algorithm allows the control system to recharge series capacitors and change topology configurations smoothly while keeping the voltage and current at the low-voltage side at the same value during the transitions. There are small oscillations in the voltage after transitions, but they do not influence GMPPT scanning since the control system is waiting for the low voltage stabilization before it continues the scanning. This experiment also verifies the continuous operation of the UPEI in the wide voltage range. After achieving the minimum voltage, the control system returns to the GMPP and switches to the LMPPT algorithm. The scanning time t_{scan} equals 62 ms, and the return time t_{return}took 23 ms, resulting in a total scanning time of 85 ms.

C. DAILY ENERGY YIELD TESTS

To verify the UPEI operation with a PV module under unfavorable conditions, a daily mission profile of solar irradiance and a module temperature under partial shading from a neighboring building were synthesized based on measurements (Fig. 11). One of the substrings in a PV module is shaded during the morning and evening hours.

Fig. 12 shows experimental results of UPEI operation with the LR72-425M PV module, under the partial shading conditions. Fig. 12 contains four parts from top to bottom:

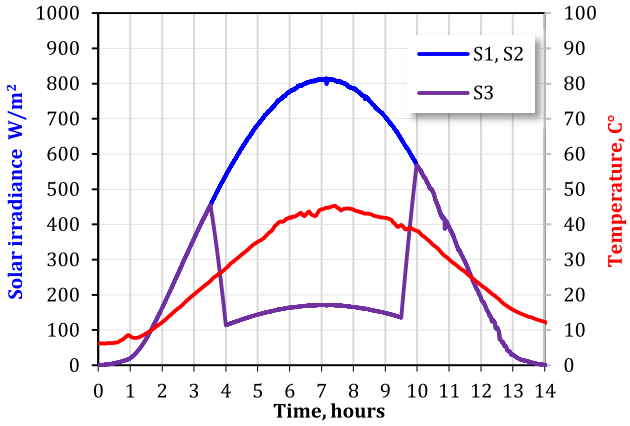

FIGURE 11. Daily profiles of solar irradiance of three PV module substrings under partial shading from a neighboring building and a cell temperature.

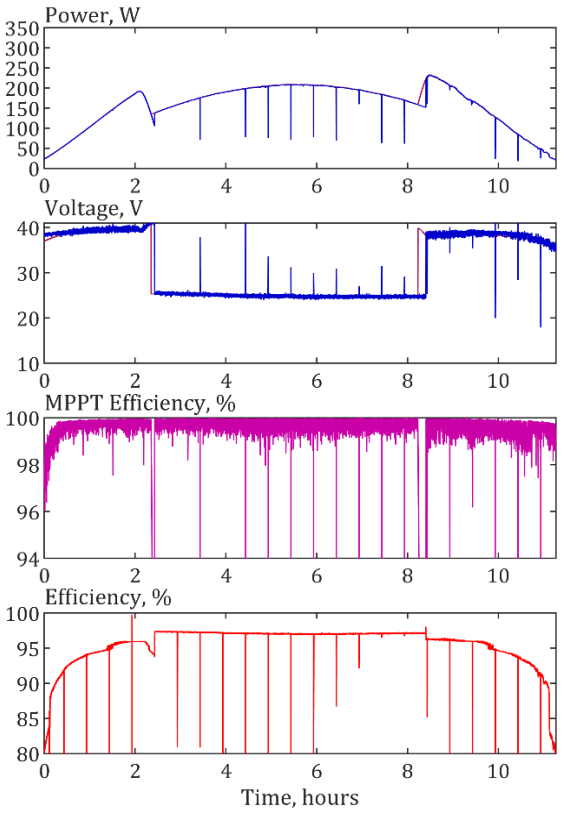

FIGURE 12. UPEI operation with LR72-425M PV module under synthesized partial shading from a neighboring building.

1) The red curve is the maximum available power from a PV module in the GMPP; the blue curve is the power drawn by the UPEI.
2) The red curve is the voltage of GMPPT, the blue curve is the instantaneous voltage of the PV module.
3) The magenta curve is the MPPT efficiency.
4) The red curve is the efficiency of the UPEI.

The UPEI tracks the GMPP with average MPPT efficiency of about 99.5 %. It could be recognized that the control

TABLE 2. UPEI operation with two PV module types under different shading conditions.

Energy and Efficiency	Profile and Type of PV module			
	NOCT		Build shade	
	60 cells	*72 cells*	*60 cells*	*72 cells*
E_{GMPP}, Wh	1355	1648	1478	1801
E_{PV}, Wh	1351	1644	1465	1788
E_{DC}, Wh	1312	1577	1403	1719
E_{PV}/E_{GMPP}, %	99.7	99.8	99.1	99.3
E_{DC}/E_{PV}, %	97.1	95.9	95.7	96.1
E_{DC}/E_{GMPP}, %	96.8	95.7	94.9	95.5

system rescans P-V curves of a PV module every 30 minutes to find the global MPP, as it was mentioned before. There are slight deviations between the maximum available power and the extracted power when the converter is stuck at the previous MPP until the next rescanning. The data were logged with a time step of 200 ms, which is less than the scanning time. In this connection, rescanning is not completely visible in the figures. At low powers, the converter efficiency has a step at the beginning and the end of the tests. It is mainly associated with enabling or disabling the synchronous rectifier by the control system.

The UPEI has been tested with SAS emulating LR60-350M and LR72-425M PV modules under partial shading and without it when the PV modules reach Nominal Operating Cell Temperature (NOCT) conditions dung the peak energy production hours. The second corresponds to the mission profile of solar irradiance of the third substring S_3 being the same as S_1 in Fig. 11.

To summarize the daily tests, the energy yield was calculated and listed in Table 2. It includes three energy values: available PV energy in the GMPP E_{GMPP}, the energy harvested by the UPEI E_{PV}, and the energy delivered EDC to the dc microgrid. In addition, MPPT efficiency E_{PV}/E_{GMPP}, the converter efficiency E_{DC}/E_{PV}, and the overall efficiency E_{DC}/E_{GMPP} are calculated. The tests show that the daily MPPT efficiency E_{PV}/E_{GMPP} is around 99.5%. The efficiency of the UPEI E_{DC}/E_{PV} during daily tests is around 96%. Considering these two efficiencies, the overall system efficiency is around 95.5 %.

IV. BATTERY INTERFACING MODE

This section presents the control algorithm and experimental evaluation of UPEI in the battery interfacing mode. It demonstrates how the droop control should be integrated at the high control level.

A. IMPLEMENTATION OF DROOP CONTROL

In the case of operation with a battery, the control system operates with the droop control algorithm when the battery

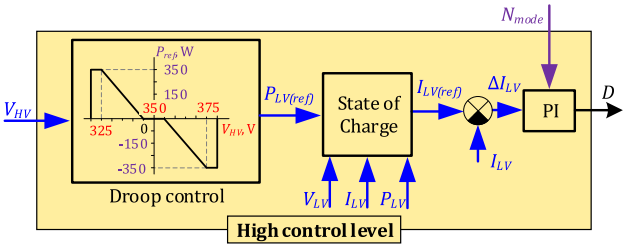

FIGURE 13. Block diagram of the high-level control system in the battery mode.

state of charge is within the allowed limits. The droop control allows for natural power sharing between parallel power sources and stabilizes the operation of the dc microgrid without any communication between converters [44].

The idea of the droop control for the battery mode is based on the derivation of the power reference value that linearly depends on the dc-bus voltage deviation from the nominal value outside the dead band of $V_{DB} = 10$ V around the nominal voltage $V_{HV(nom)} = 350$ V (Fig. 13). Based on the dc microgrid voltage (V_{HV}), the control system regulates the reference power of the converter and the power flow direction. When $V_{HV} > V_{HV(nom)}+V_{DB}/2$, the control system operates in the battery charging mode. In the case of $V_{HV} < V_{HV(nom)}$ - $V_{DB}/2$, the control system switches to the battery discharging mode. According to the Dutch national practical guidelines NPR 9090 [10], the high voltage is limited in the range of 320 V to 380 V. In the case of PV mode, the UPEI operates with the maximum available power within the permitted range of dc-microgrid voltages between 325 V and 375 V.

The block diagram of the high-level control system under the battery mode is shown in Fig. 13. The droop control block sets the reference power. The state of charge estimation block (SOC) protects the battery from under- or over-charging.

The state of charge estimation and control algorithm implements conventional constant voltage/constant current charging [45]. In the discharge mode, the control system operates with a constant current until the battery is fully discharged. To extend the battery lifetime, the control system limits the SOC of the battery in the range of 5% to 95%.

B. OPERATION WITH DROOP CONTROL

The experimental waveforms in Fig. 14 verify the operation of the UPEI with the selected Power Brick+ 48V 25A LiFePO4 battery at a SOC of 50% under droop control at both power flows. Two iTECH IT6006C-800-25 Bidirectional Power Supplies were emulating the dc microgrid and a battery. The bidirectional power supplies have an arbitrary generator function allowing for programming dc bus voltage and software for battery emulation with realistic SOC behavior. The closed-loop control in the battery mode linearly regulates and stabilizes the battery current depending on the dc microgrid voltage.

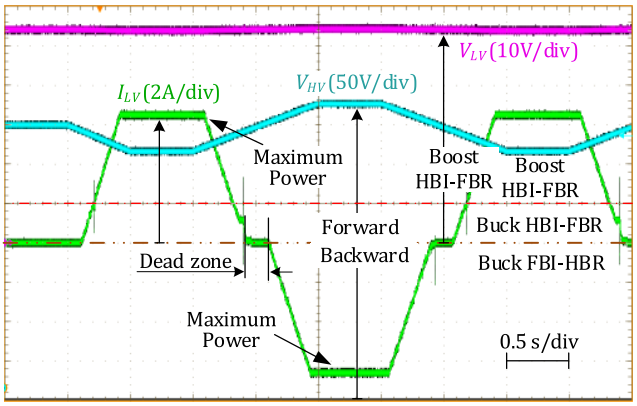

FIGURE 14. Operation of the UPEI with 48 V LiFePO4 battery with droop control.

The maximum current is limited to 6.8 A at the maximum operation power of 350 W with the battery 48 V.

At the nominal voltage of 350 V, the control system switched between the forward buck HBI-FBR and the backward buck FBI-HBR control modulations without current distortions.

C. DAILY TESTS OF UPEI WITH 24 V AND 48 V BATTERIES

To verify the UPEI operation in the battery mode, a daily profile of dc microgrid voltage was synthesized based on a daily load profile of a house and a daily profile of PV generation, as shown in Fig. 15. The power consumption profile has two recognizable maximums of 3.4 kW and 3.3 kW at 7 a.m. and 6 p.m., respectively, during breakfast and dinner hours.

To reproduce the dc microgrid operation under the droop control, the synthesized microgrid voltage is linearly proportional to the difference between consumption and generated power (the third plot in Fig. 15). Also, the dc microgrid voltage is limited in the range of 320 V to 380 V. During the night, the PV power equals zero, which results in the dc microgrid voltage below the nominal value of 350 V. With increasing generated power, this voltage increases in the morning. When the PV power falls to zero, the dc microgrid voltage drops below the nominal value.

Using the synthesized profile of dc-microgrid voltage, UPEI has been tested for 24 hours with two battery types: Power Brick+ 24V 32A LiFePO4 [47] and Power Brick+ 48V 25A LiFePO4. The test with the latter is shown in Fig. 15. The bottom four parts of the figure include the voltage mission profile of the dc microgrid (red curve), the corresponding battery current (blue curve), SOC of the battery (green curve), and the UPEI efficiency (magenta curve). Depending on the instantaneous dc microgrid voltage, the UPEI operates in the charging or discharging mode, as described in Section IV.

From midnight till morning, the UPEI transfers energy from the battery energy storage to the dc microgrid. When the dc microgrid voltage increases up to 355 V, the UPEI switches to charging batteries with PV energy. The maximum battery

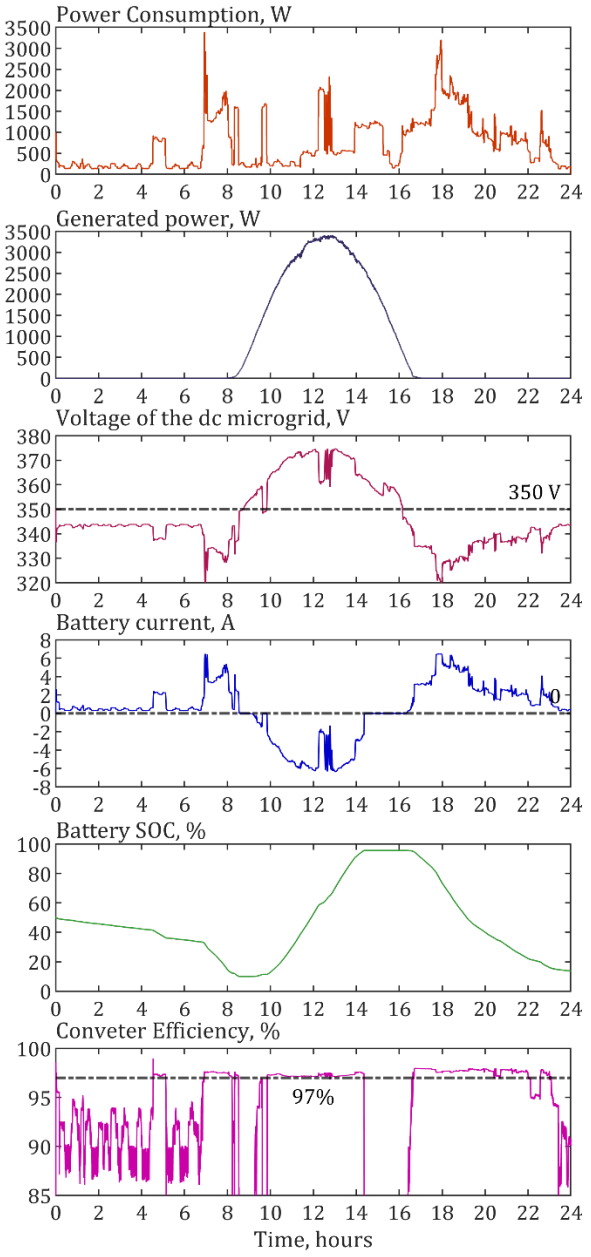

FIGURE 15. UPEI operation with Power Brick+ 48V 25A LiFePO4 battery for 24 hours.

SOC is limited by 95%. In the battery mode, the efficiency of UPEI is around 97%. However, the efficiency drops at low power when the synchronous rectifier cannot operate.

Table 3 lists calculated charged energy into batteries and transferred energy from batteries to the dc-microgrid. The full-charging efficiency (from 5% to 95% of SOC) $E_{BAT(ch)}/E_{DC(ch)}$ of the UPEI equals 96.3 % and 97.6% in the cases of 24 V battery and 48 V battery, respectively. In the discharging mode, the converter full-discharge efficiency (from 95% to 5% of SOC) $E_{DC(disch)}/E_{BAT(disch)}$ equals 97.3% and 97.5%. The round trip efficiency $E_{DC(disch)}/E_{DC(ch)}$ demonstrates how much of stored energy was returned to the

TABLE 3. UPEI 24H operation with two LFP battery types.

Operation mode	Energy and Eff.	Batteries	
		24V 32Ah	48V 25Ah
Charging (from 5% to 95%)	$E_{DC(ch)}$, Wh	-840.8	-1179.4
	$E_{BAT(ch)}$, Wh	-809.4	-1151.4
	$E_{BAT(ch)}/E_{DC(ch)}$, %	96.3	97.6
Discharging (from 95% to 5%)	$E_{BAT(disch)}$, Wh	757.4	1070.8
	$E_{DC(disch)}$, Wh	737.2	1044.0
	$E_{DC(disch)}/E_{BAT(disch)}$, %	97.3	97.5
Round trip	$E_{DC(disch)}/E_{DC(ch)}$, %	87.7	88.5

dc-microgrid and includes converter efficiencies in both modes and the losses in the battery. As Table 3 shows, the roundtrip efficiency equals 87.7% and 88.5% for 24 V and 48 V batteries, respectively.

V. SOURCE IDENTIFICATION ALGORITHM

This section introduces the algorithm of the input source type identification and provides its experimental verification.

A. ALGORITHM DESCRIPTION

As was described in the introduction, the UPEI can operate as a front-end PV microconverter or a front-end battery converter. After connecting an energy source, the converter should identify a type of connected source. The input source identification algorithm was previously proposed for the 2-mode version of the given converter [41]. This section shows how to integrate it into the UPEI and verifies its performance.

The main idea of the algorithm for the input source identification is based on scanning the I-V characteristic of a connected input source and calculating the differential conductance $\Delta I/\Delta V$. This approach allows for avoiding influences from the drift of source parameters, for example, due to aging or temperature changes. Therefore, it can be applied to different types of input sources.

The algorithm can identify input sources such as different PV modules and battery types. The main difference in I-V characteristics of these types of sources is the differential conductance $\Delta I/\Delta V$. In the case of a PV module, the differential conductance is not linear:

1) $\Delta I/\Delta V \ll 0$ from the OCV to the MPP;
2) $\Delta I/\Delta V < 0$ at the MPP;
3) $\Delta I/\Delta V \approx 0$ after the MPP.

In the case of a battery, the $\Delta I/\Delta V$ is virtually constant for one condition of the state of charge, and its absolute value is much higher than that of any PV module.

The flowchart of the identification algorithm is illustrated in Fig. 16, where ΔD is the incrementing step of the duty cycle, $I_{LV(max)}$ is the maximum current on the low-voltage side, which the UPEI can carry continuously. The identification process starts with an OCV of a connected input source.

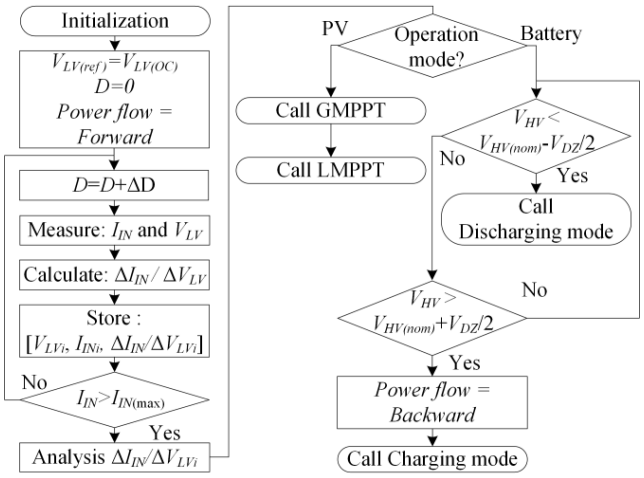

FIGURE 16. Flowchart of the identification algorithm.

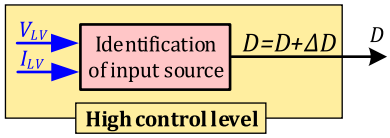

FIGURE 17. Block diagram of the high-level control system under the identification algorithm.

During identification, the control system increments the duty cycle to increase the low-voltage side current and decrease the voltage V_{LV}. After every duty cycle step, the control system calculates the input source differential conductance $\Delta I/\Delta V$.

This process continues until the current achieves the maximum $I_{LV(max)}$ value or an MPP. In the first case, the control system switches to the battery charging/discharging mode depending on the dc microgrid voltage. In the case of a connected PV module, the control system switches to the LMPPT/GMPPT algorithms. The algorithm also identifies a type of connected PV module (60-cells or 72-cells) or a battery (24 V or 48 V). Fig. 17 shows the implementation of the high-level control system. The algorithm block feds the duty cycle to the middle-level control system, which selects a control modulation automatically. The algorithm uses measured and filtered low-voltage side voltage and current for differential conductance calculations.

B. EXPERIMENTAL VERIFICATION OF THE INPUT SOURCE IDENTIFICATION

The experimental verifications of the identification algorithm with the LR4-72HBD-425M PV module and the Power Brick+ 48 V 25 A battery are shown in Figs. 10 and 18, respectively.

In the case of the PV module, the algorithm increased the duty cycle until the first MPP was found. Then, the high-level control system switched to the GMPPT algorithm and scanned the P-V curve of the PV module. After achieving the minimum voltage, the control system returned to the GMPP

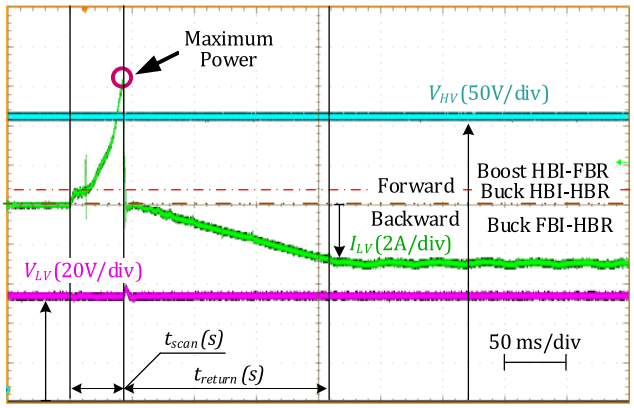

FIGURE 18. Identification of the battery and tracking performance of the discharging mode at $V_{HV} = 330$ V.

and switched to the LMPPT algorithm. The total time of PV scanning required is 85 ms.

The experimental results also verified the performance of the identification algorithm with the battery at the grid voltage V_{HV} of 330 V (Fig. 18). The control system

gradually increased the battery current I_{LV} until the maximum power was achieved. Depending on the dc microgrid voltage, the control system switches to the charging or discharging mode and sets the reference power. After identification, the control system decreases the battery current to zero as fast as possible and then switches to the backward buck HBI-FBR control mode to charge the battery, as shown in Fig18. The SOC block limits the slope of the reference current for correctly estimating the SOC of the battery. The scanning time took 48 ms, and the return time equals 154 ms.

VI. CONCLUSION

This paper demonstrates and provides experimental validation of the novel universal power electronic bidirectional interface for integration of PV modules and battery energy storages in residential dc microgrids. The analysis of application requirements shows that the proposed UPEI should have an input voltage range of 10 V to 60 V, bidirectional power flow capability, and be capable of operating with 350 ± 30 V residential droop-controlled dc microgrids. A technology demonstrator has been developed to validate the proposed concept and show its operation with various PV modules and battery energy storage types in residential dc microgrids.

Using the same hardware platform for different PV modules and storage batteries allows for simpler system design and faster deployment of dc microgrids. The UPEI concept is enabled by applying the topology morphing control in multimode dc-dc converters. The proposed UPEI operates in the wide input voltage range, which covers the voltage ranges of the most popular PV modules and storage batteries on the market. The wide input voltage range and the developed control algorithms allow the UPEI to recognize a connected energy source automatically and switch to a respective mode during 200 ms.

Daily tests with 60- and 72-cell PV modules under normal and partial shading conditions verified the high performance of the UPEI in both sunny and partially shaded conditions. The overall daily efficiency, including the MPPT and the converter efficiencies, is in the range of 94.9 – 96.8 %, depending on the operating conditions. The UPEI executes the GMPPT scanning in less than 100 ms.

The same prototype was used for the integration of battery energy storages. Its daily efficiency with 24 V and 48 V LiFePO4 batteries equals 96.3% and 97.6%, respectively, in the charging mode, and 97.3% and 97.5% in the discharging mode.

These results justify the high performance of the novel UPEI concept. It can be used to integrate either PV modules or batteries in residential dc microgrids thanks to its bidirectional power flow and input source identification capabilities. Applicability of this concept is limited to low-voltage PV modules and batteries operating at voltages below 60 V, which does not cover some residential thin-film PV modules and high-voltage battery energy storages. Nonetheless, the UPEI operates with the most commercially available residential PV modules and batteries. Further work will focus on efficiency optimization at a light load, economic viability analysis, and performance verification of the multiple UPEIs operating in one dc microgrid.

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VADIM SIDOROV (Graduate Student Member, IEEE) was born in Kazakhstan, in 1995. He received the B.Sc. and M.Sc. degrees in power electronics from Novosibirsk State Technical University, Novosibirsk, Russia, in 2017 and 2019, respectively. He is currently pursuing the Ph.D. degree with the Power Electronics Group, Tallinn University of Technology, Tallinn, Estonia. He has coauthored more than 20 articles and one book chapter on power electronics and applications. His research interests include power electronics systems, DC–DC converters, series resonant converters, DC–AC inverters, and electric drive systems.

ANDRII CHUB (Senior Member, IEEE) received the B.Sc. and M.Sc. degrees in electronic systems from Chernihiv State Technological University, Ukraine, in 2008 and 2009, respectively, and the Ph.D. degree in electrical engineering from the Tallinn University of Technology, Tallinn, Estonia, in 2016. He was a Visiting Research Fellow with Kiel University, in 2017, and a Postdoctoral Researcher with Federico Santa Maria Technical University, from 2018 to 2019. He is currently a Senior Researcher with the Power Electronics Group, Department of Electrical Power Engineering and Mechatronics, Tallinn University of Technology. He has coauthored more than 100 articles and a book chapter on power electronics and applications and holds several patents and utility models. His research interests include advanced DC–DC converter topologies, renewable energy conversion systems, energy-efficient buildings, reliability, and fault-tolerance of power electronic converters. He has received numerous best paper awards at IEEE conferences and the IEEE Industrial Electronics Society Best Conference Paper Award, in 2018. He is an Associate Editor of the IEEE JOURNAL OF EMERGING AND SELECTED TOPICS IN INDUSTRIAL ELECTRONICS.

DMITRI VINNIKOV (Fellow, IEEE) received the Dipl. (Eng.), M.Sc., and Dr.Sc.techn. degrees in electrical engineering from the Tallinn University of Technology, Tallinn, Estonia, in 1999, 2001, and 2005, respectively. He is currently the Head of the Power Electronics Group, Department of Electrical Power Engineering and Mechatronics, Tallinn University of Technology. He is also the Head of Research and Development and the Co-Founder of Ubik Solutions LLC—Estonian start-up company dedicated to innovative and smart power electronics for renewable energy systems. Moreover, he is one of the founders and leading researchers of ZEBE—Estonian Centre of Excellence for zero energy and resource efficient smart buildings and districts. He has authored or coauthored two books, five monographs and one book chapter, and more than 400 published articles on power converter design and development, and is the holder of numerous patents and utility models in this field. His research interests include the applied design of power electronic converters and control systems, renewable energy conversion systems (photovoltaic and wind), impedance-source power converters, and the implementation of wide bandgap power semiconductors. He is the Chair of the IEEE Estonia Section.

ANDRE LINDVEST received the M.Sc. degree in power engineering and the M.B.A. degree from the Tallinn University of Technology, Tallinn, Estonia.

He has 13 years experience in energy industry (mainly renewable energy) and five years in financials and startups. He is currently the CEO of Ubik Solutions and the Board Member of Sunly Startup, Tallinn. Previously, he was also running Estonian private investment company marble invest focused on renewable energy related technologies, products, and services. Prior to that, he was the Project Manager of Nelja Energia AS, which was a leading renewable energy developer and producer in Baltics and Eesti Energia AS, which is Estonian national energy company, developing several pioneer wind farms in Estonia, and worked in the dispatch center of Estonian transmission systems.