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RESEARCH ARTICLE

Quadruple Boost Switched Capacitor-Based Inverter for Standalone Applications

SRIMANNARAYANA KOVVALI[1], NAKKA JAYARAM[1], SATYA VENKATA KISHORE PULAVARTHI[2], (Student Member, IEEE), YANNAM RAVI SHANKAR[3], JAMI RAJESH[1], AND V. GOURI PRASANT[1]

[1]Department of Electrical Engineering, National Institute of Technology Andhra Pradesh, Tadepalligudem 534101, India
[2]Department of Electrical and Electronics Engineering, Sri Vasavi Engineering College, Tadepalligudem 534101, India
[3]School of Electrical and Computer Engineering, Dire Dawa University, Dire Dawa 1362, Ethiopia

Corresponding author: Yannam Ravi Shankar (yannam.ravi@ddu.edu.et)

ABSTRACT Conventional energy sources will not be sufficient to meet future electrical demands, and also pollute the environment. Therefore, to meet their electrical energy needs, and maintain clean and green environmental conditions, people are focusing more on renewable energy sources. Small-scale PV solar standalone AC loads or grid integration applications need high voltage at a desired level, transformer/inductor less operation, high gain DC-DC front-end converters, and DC-AC converters. To achieve all the above objectives, this paper proposes a step-up quadruple boost nine-level inverter, it works on switched capacitor technique with a reduced count of components for the application of renewable energy systems. The proposed topology balances the capacitor voltages with the control scheme itself without using any sensors. A level-shifted pulse-width modulation (LPWM) technique can be used in the control strategy of the proposed topology. This paper covers the operational modes of the proposed topology, voltage stress calculations, capacitors calculations, and losses calculations at various stages and compared with recent literature, that reveals this topology is more advantageous in terms of less total standing voltage, switch count, cost factor, better efficiency and the number of gate driver circuits. The theoretical performance can be validated through MATLAB/Simulink-based simulation and their results are validated through prototype experimentation. Further, the experimental results contain modulation index variations, frequency modulation, switching frequency variations, input voltage variations, and load variations. Finally, the max efficiency of 96.5% is achieved for the experimental prototype of the proposed topology.

INDEX TERMS Switched capacitor (SC) based inverter, high gain inverter topologies, solar PV, self-voltage balance and level shifted pulse width modulation (LSPWM).

I. INTRODUCTION

The demand for electrical energy can increase rapidly throughout the world from day to day. Electrical energy is majorly generated by the combustion of fossil fuels like coal, petroleum, natural gas, and nuclear materials. Those materials can expose harmful gases to the environment, which leads to an environmental imbalance that can exist throughout the world. The solution to meet the demand for increasing electrical energy, with environmentally friendly renewable energy sources is gaining more popularity. Renewable energy generating stations are far away from the load centers. Therefore, the transmission and distribution losses are increased to deliver the electrical energy from generating stations to load centers. To overcome this problem, rooftop distributed solar PV systems are introduced in current years. The available power and voltage ratings for small-scale solar PV rooftop systems are 0.5kw-5kw and 60-100v [1], [2], [3]. To supply the AC power at distributed voltage levels, the available R.M.S voltages are 230V for a single phase and 415V for a three-phase system. Solar rooftop PV cells can generate power in D.C nature at lower voltage levels. The lower voltage levels of DC can be stepped-up by high-gain DC-DC converters and DC-AC conversion will be needed to meet the

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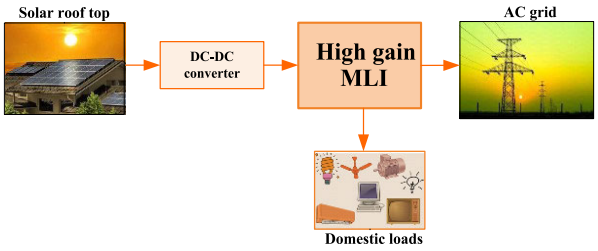

FIGURE 1. Interconnection of domestic loads with high gain MLI.

AC grid voltage levels [4]. The most prevalent approach of the above power conversion of solar PV rooftop to distributed AC voltage is MLI, this is popular due to the benefits of lower voltage stress across the switches, higher quality of THD at output voltage levels, modularity of the structure high and lesser electromagnetic interference. The traditional MLIs are diode-clamped MLI (DCMLI), flying capacitor MLI (FMLI), and cascaded H- bridge MLI (CHB). Both diodes clamped and flying capacitor MLIs suffer from capacitor unbalancing problems and output voltage levels may be collapsed due to the series connection of the switches [7], [8]. Cascaded H-bridge MLI is needed as an isolated DC voltage source, this may operate in either a symmetrical or asymmetrical manner [9], [10]. There have been many modifications done in recent years to reduce the count of no of switches, capacitor voltage balancing problems, and reduce the requirement of isolated DC sources and the control strategy of the MLI [5], [11]. Therefore, MLI structures in the current scenario are broadly differentiated in two ways, single dc source switched capacitor (SC) based boost type topologies and multiple dc sources non-boosting capability. Among all the categories of MLI switched capacitor-based boost-type topologies are more popular [12]. In switched capacitor-based topologies containing several switches or diodes, capacitors are connected in either series/parallel technique for generating output voltage levels [13]. Several advantages of the switched capacitor (SC) based MLI are most suitable for renewable energy, and solar PV rooftop applications. In this paper [14], a novel boost-switched capacitor inverter with a Marx structure was introduced. The operating principle of the Marx structure inverter is switched capacitor technique. The no of output voltage levels is increased by adding the Marx structure units to the H bridge. In this paper [15], a cascaded MLI was structured with front-end and back-end units, with 2 isolated dc voltage sources. The frontend unit is switched capacitor and the backend is the H bridge unit. If the no of levels is increased by using a combination of both the units with isolated dc voltage sources in a cascaded manner. In this paper [16], A Hybrid switched capacitor MLI was introduced with a single dc voltage source, one capacitor, and two complementary switches connected in a series/parallel nature. More no of voltage levels are achieved by connecting the basic configuration circuits in a series manner. In this paper [17], the SC technique was used to propose a generalized voltage boost MLI. switches, diodes, and capacitors are connected in series/parallel to the input voltage to generate the desired output voltage levels. In this paper [18], the SC technique can be used to design the quasi-resonant MLI. An inductor is inserted in the resonance circuit to generate the desired output voltage levels. In this paper [19], repeated SC units are cross-connected at the end of 2 T-type circuits. Every cross-connected unit has 6 switches and 2 capacitors, output levels are dependent on no cross-connected SC units. In this paper [20], a single dc source cascaded H bridge MLI developed with the isolated dc voltage sources can be replaced by capacitors. The capacitors, switches, and diodes are interacted with the input dc voltage source by switched capacitor technique to get output voltage levels. In this paper [21], a hybrid nine-level inverter with a series/parallel conversion (H9ISPC) inverter is introduced. It can boost up the voltage levels and also maintain the constant voltage by using a passive voltage balancing of the capacitors. In this paper [22], active neutral point clamped (ANPC) generalized inverter topology was introduced with a gain1. For a nine-level inverter having 12 switches with unity gain. To achieve more no of voltage levels by adding additional switches and capacitors. In this paper [23], a generalized 5-level inverter based on switched capacitor technique has four switches and single capacitor modules. To connect those modules then extend the levels of the output voltage levels. In this paper [24], a triple gain of a hybrid T-type nine-level inverter was proposed. A 5-level T-type network and four capacitors are used to boost the voltage levels. In this paper [25], a generalized CGSC-TL topology was proposed. The topology contains a series/parallel and capacitors set up modules, a series inductor to the voltage source, and an input capacitor in parallel with both source and modules. The no of capacitor modules added in series to previous modules gets the output voltage levels. In this paper, [26] the article CGT-9L boost inverter was introduced. The boost converter can be modified as the MLI with the series/parallel combinations of switches, diodes, and capacitors. This topology can design common ground that can provide in between the input dc source and output AC. In this paper [27], the output levels are formed by the two units one is generating unit, another one H-bridge unit. Generating unit contains switches, diodes, and capacitors. In [28], a nine-level switched capacitor is proposed with unipolar Bi-directional and Bipolar unidirectional switches with two capacitors. In [29], a seven-level switched capacitor topology is proposed with a gain of three only. To get compatible grid voltages with the low voltage PV panels, it requires more gain than three. For all the above topologies can be implemented based on switched capacitor technique. It does not require any sensor unit to detect and balance the voltage across the capacitors. All capacitors have self-balancing voltage ability itself. In this paper, a new topology is introduced with less no of components as compared with recent competitive topologies. This topology is mainly

suitable for lower to medium voltages with a single-source application using small-scale solar PV. Interconnection of the solar PV, DC-DC converter, AC grid, and domestic loads with proposed high gain MLI as shown in Fig.1. The proposed topology has the following dominant features

- single DC source is used to get 9 levels with quadruple voltage gain.
- Less number of components (10 switches and 2 capacitors)
- Self-balancing of the capacitors with the control scheme.
- For charging the capacitor, only 01 switch is enough. So, conduction losses are reduced
- Four out of 10 switches have only one transition in a cycle. So, switching losses are minimised.
- Voltage stress is minimum on switches.
- Cost factor of overall converter is minimum.

The rest of the manuscript is arranged as follows. The operation and operating modes of the proposed topology are presented in section II. Section III covers switching stress and TSV calculations of the switches and diodes. Section IV describes a brief note on control schemes using the LS-PWM technique and capacitor calculations. Loss calculation for determination of the efficiency of the proposed topology is discussed in section V. Comparative analysis of the proposed topology with other recent literature is presented in section VI. In section VII, Experimental results analysis is done. Simulation result analysis of the proposed topology can be done in section VIII. Finally, the conclusion of work is presented in section IX.

II. PROPOSED TOPOLOGY

The proposed quadruple boost nine-level topology is shown in Fig.2. It has one DC voltage source, two capacitors (C_1,C_2), and ten switches (IGBT/MOSFET), of which three are Bi-directional switches (S_1, S_2, S_6) and seven are unidirectional switches (S_3, S_4, S_5, S_7, S_8, S_9, S_{10}).

To prohibit a short circuit between the DC voltage source and the capacitors, the switches S_7, S_8, and S_9, S_{10} work in conjunction with one another. The two capacitors (C_1, C_2) are charged and discharged parallel and in series to DC voltage source to produce the desired voltage levels. The capacitors C_1, as well as C2, are charged and discharged to $+1V_{dc}$ and $+2V_{dc}$ respectively. Hence, the voltages across the capacitors are self-balanced. The output voltage levels across the load are $\pm4V_{dc}$, $\pm3V_{dc}$, $\pm2V_{dc}$, and $\pm1V_{dc}$. The charging and discharging of the capacitors are done by the parallel/series technique. With these balanced capacitors and the proper switching pattern, the aforementioned voltage levels are accomplished with a single DC voltage source. The charging, discharging, and floating conditions of the capacitors are indicated as ↑, ↓ and –. Six switches are continuously switched ON along with the discharged capacitor to generate all the voltage levels, with the notable exception of the zero-voltage level. Either the two switches of the upper arm or lower arm are switched ON to attain the zero-voltage level.

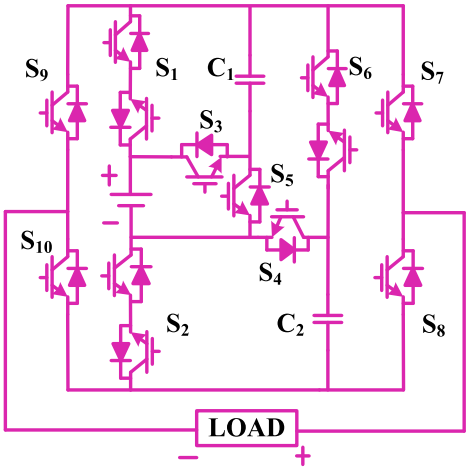

FIGURE 2. Proposed 9-level quadrable boost inverter.

The single switch is enough to charge capacitors. Therefore, the proposed topology can reduce switching losses.

A. OPERATING MODES OF THE PROPOSED TOPOLOGY

1) ZERO VOLTGE LEVELS

In the proposed topology, there are two ways to achieve the zero-voltage level, either by turning ON the upper arm switches (S_7, S_9) or by lower arm switches (S_8, S_{10}). Fig.3(a) shows the generation of zero voltage level using the upper arm switches.

2) POSITIVE VOLTGE LEVELS

$+1V_{dc}$ voltage level: Switches S_1, S_7, S_{10}, and S_2 are turned ON to bring the DC voltage source and the load is in series. In addition, switch S_5 turns ON to charge the capacitor C_1 is $+1V_{dc}$. Capacitor C_2 is being left in the floating condition (–), it doesn't charge or discharge. To transmit $+1V_{dc}$ towards the load as shown in Fig.3(b).

$+2V_{dc}$ voltage level: Switches S_3, S_7, S_{10}, and S_2 are turned ON to bring the DC Voltage source, capacitor C_1, and load in series. In addition, switch S_3 turns ON to discharge the capacitor C_1 is $+1V_{dc}$. switch S_6 is turned ON to charge the capacitor C_2 is $+2V_{dc}$. To transmit $+2V_{dc}$ towards the load as shown in Fig.3(c).

$+3V_{dc}$ voltage level: Switches S_1, S_7, S_{10}, and S_4 are turned ON to bring the DC voltage source, capacitor C_2, and load in series. In addition, switch S_4 is turned ON to discharge the capacitor C_2 is $+2V_{dc}$. Capacitor C_1 is being left in the floating condition (–), it doesn't charge or discharge. To transmit $+3V_{dc}$ towards the load as shown in Fig.3(d).

$+4V_{dc}$voltage level: Switches S_3, S_7, S_{10}, and S_4 are turned ON to bring the DC voltage source, capacitor C_1, capacitor C_2, and load in series. In addition, switch S_3 turns ON to discharge the capacitor C_1 is $+1V_{dc}$. switch S_4 turns ON to discharge the capacitor C_2 is $+2V_{dc}$. In this, both capacitors release their stored energy. To transmit $+4V_{dc}$ towards the load as shown in Fig.3(e).

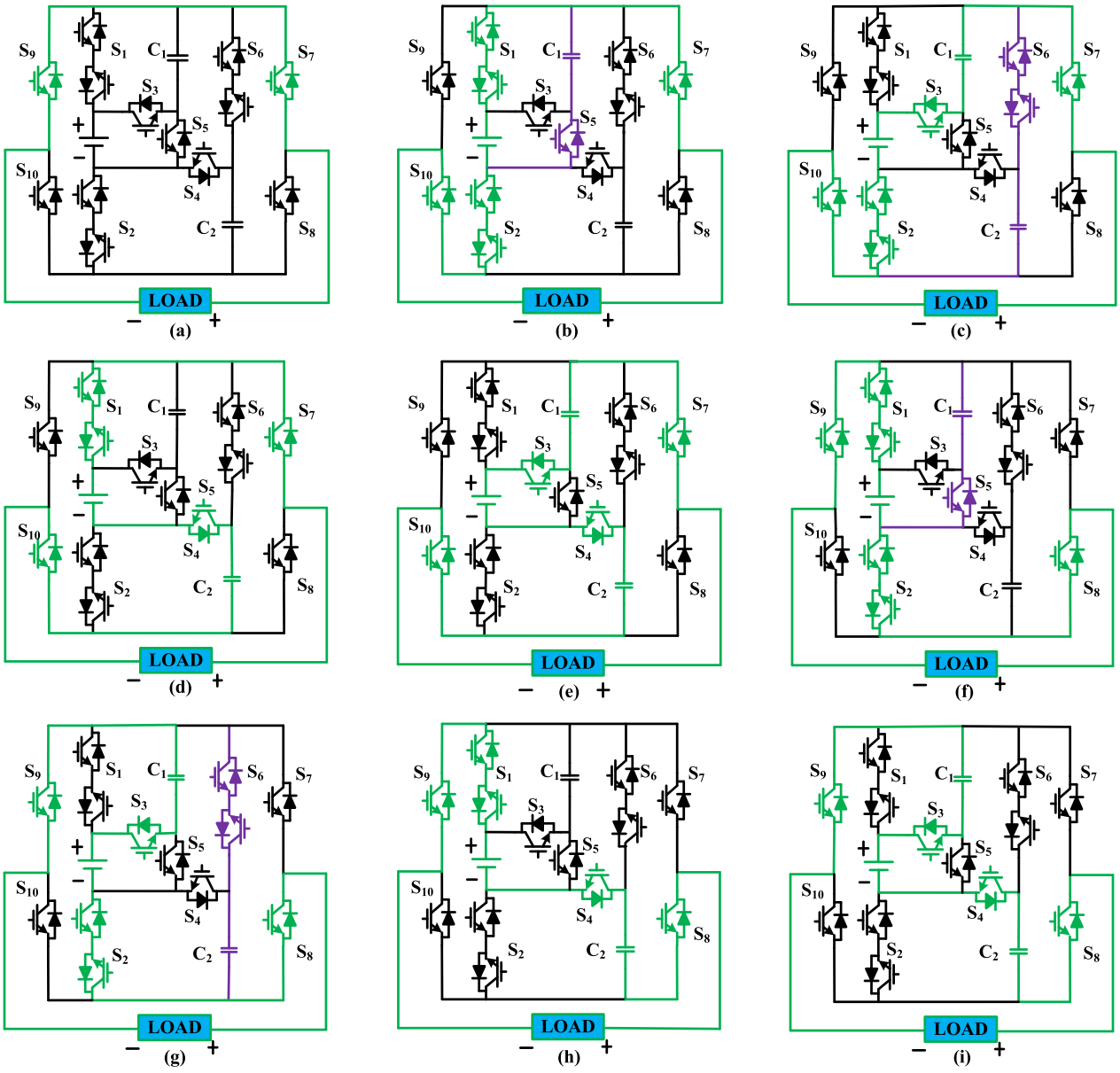

FIGURE 3. Operating modes of the proposed topology fig(a). Zero Voltage level, fig(b). $+1V_{dc}$ voltage level, fig(c). $+2V_{dc}$ voltage level, fig(d). $+3V_{dc}$ voltage level, fig(e). $+4V_{dc}$ voltage level, fig(f). $-1V_{dc}$ voltage level, fig(g). $-2V_{dc}$ voltage level, fig(h). $-3V_{dc}$ voltage level, fig(i). $-4V_{dc}$ voltage level.

3) NEGATIVE VOLTGE LEVELS

$-1V_{dc}$ voltage level: Switches S_1, S_9, S_8, and S_2 are turned ON to bring the DC voltage source and the load is in series. In addition, switch S_5 turns ON to charge the capacitor C_1 is $+1V_{dc}$. Capacitor C_2 is being left in the floating condition (–), it doesn't charge or discharge. To transmit $-1V_{dc}$ towards the load as shown in Fig.3(f).

$-2V_{dc}$ voltage level: Switches S_3, S_9, S_8, and S_2 are turned ON to bring the DC Voltage source, capacitor C_1, and load in series. In addition, switch S_3 turns ON to discharge the capacitor C_1 is $+1V_{dc}$. switch S_6 turns ON to charge the capacitor C_2 is $+2V_{dc}$. To transmit $-2V_{dc}$ towards the load as shown in Fig.3(g).

$-3V_{dc}$ voltage level: Switches S_1, S_9, S_8, and S_4 are turned ON to bring the DC voltage source, capacitor C_2, and load in series. In addition, switch S_4 is turned ON to discharge the capacitor C_2 is $+2V_{dc}$. Capacitor C_1 is being left in the floating condition (–), it doesn't charge or discharge. To transmit $+3V_{dc}$ towards the load as shown in Fig.3(h).

$-4V_{dc}$ voltage level: Switches S_3, S_9, S_8, and S_4 are turned ON to bring the DC voltage source, capacitor C_1, capacitor C_2, and load in series.

In addition, switch S_3 turns ON to discharge the capacitor C_1 is $+1V_{dc}$. switch S_4 turns ON to discharge the capacitor C_2 is $+2V_{dc}$. In this, both capacitors release their

TABLE 1. Switching states and their effect in switched capacitors.

V_O	S_1	S_2	S_3	S_4	S_5	S_6	S_7	S_8	S_9	S_{10}	C_1	C_2
$+4V_{dc}$	0	0	1	1	0	0	1	0	0	1	↓	↓
$+3V_{dc}$	1	0	0	1	1	0	1	0	0	1	–	↓
$+2V_{dc}$	0	1	1	0	0	1	1	0	0	1	↓	↑
$+V_{dc}$	1	1	0	0	1	0	1	0	0	1	↑	–
0	0	0	0	0	0	0	1	0	1	0	–	–
$-V_{dc}$	1	1	0	0	1	0	0	1	1	0	↑	–
$-2V_{dc}$	0	1	1	0	0	1	0	1	1	0	↓	↑
$-3V_{dc}$	1	0	0	1	1	0	0	1	1	0	–	↓
$-4V_{dc}$	0	0	1	1	0	0	0	1	1	0	↓	↓

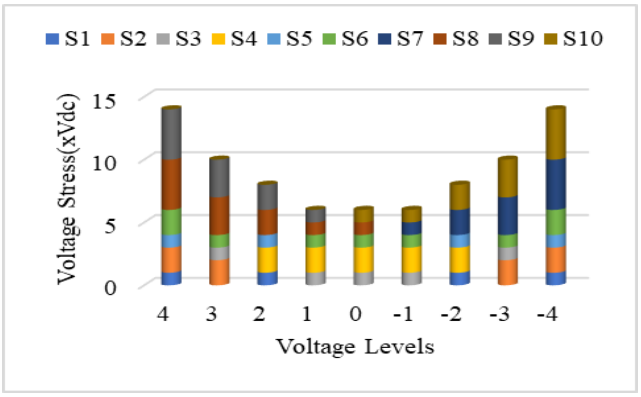

FIGURE 4. Voltage stresses on switches at a different voltage levels.

stored energy. To transmit $-4V_{dc}$ towards the load as shown in Fig.3(i).

III. SWITCHING STRESS AND TSV CALCULATIONS

In this topology, switches S_7, S_8, and S_9, and S_{10} operate in complement mode, with a peak inverse voltage (PIV) of 4Vdc. The suffix even number switches S_2, S_4, and S_6 having peak inverse voltage 2Vdc. The suffix odd number switches S_1, S_3, and S_5 have peak inverse voltage 1Vdc. TSV of the proposed inverter is less because more switches have lesser peak inverse voltage (PIV). The mathematical expression for TSV calculation is represented in Eq (1). TSV of the proposed topology is 6.25, then each switch's peak inverse voltages at various output voltage levels are plotted in a bar chart with different colors as shown in Fig 4. TSV of the proposed inverter is

$$(T.S.V)_{(p.u)} = \frac{\sum V_{(peak\_sw)} + \sum V_{(peak\_D)}}{V_{o_{(peak)}}} \qquad (1)$$

IV. MADULATION TECHNICS AND CAPACITOR CALCULATIONS

A. MODULATION SIGNAL

To generate switching pulses, a level-shifted pulse width modulation (LSPWM) technique is implemented. The no of carrier signals required in LSPWM technique = number

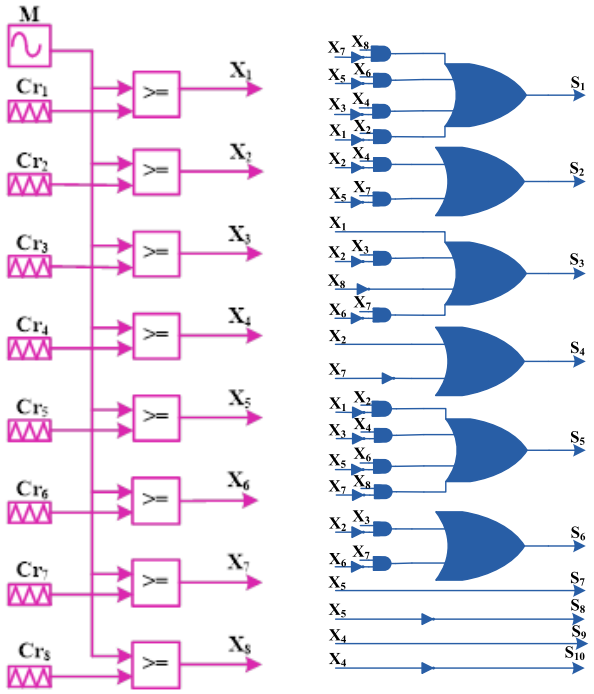

FIGURE 5. Logic pattern for switching pulses.

of output voltage levels–1. In these, the LSPWM technique uses one sinusoidal modulating signal ($M = V_m \sin(2\pi f_m t)$) and eight triangular carrier signals ($Cr_1 - Cr_8$) as depicted in Fig.5. When the modulating signal is compared with carrier signals to generate 8 pluses ($X_1 - X_8$). In case of the positive cycle, X_1 stands for comparing the modulating signal with carrier signal one (M, Cr_1), X_2 stands for comparing the modulating signal with carrier signal two (M, Cr_2), and so on. In case of negative cycles, X_8 stands for comparing the modulating signal with carrier signal eight (M, Cr_8), X_7 stands for comparing the modulating signal with carrier signal seven (M, Cr_7), and so on. The switching table as represented in Table.1. is used to create the logic pattern, for proper switching pulses to the switches.

B. AMPLITUDE MODULATION (M_a)

The carrier signal amplitude has been maintained constant but the modulated signal amplitude can be varied from 0–4. To obtain the different amplitude modulation index values Ma = 0.4, Ma = 0.7, Ma = 0.9.

C. FREQUENCY MODULATION (M_a)

The modulating signal frequency has been kept constant, carrier signal frequency can be varied 125Hz, 150Hz, and 200Hz.To obtain the frequency modulation at load frequency 50Hz. The harmonics shift up in order as the carrier signal frequency increases, but because switching transition losses (ON/OFF) also increases, the carrier frequency is restricted at 5 KHz.

D. CAPACITOR CALCULATIONS

It is necessary to estimate the capacitance values for producing, desired output voltage levels with tolerable voltage ripple. The amount of energy either can be charging or discharging of the capacitor can produce the output voltage levels.

The maximum discharging intervals, as depicted in Fig.6 are taken to account while computing the capacitance value. To calculate the amount of charge. In this topology, capacitor C_1 can discharge at output voltage levels $\pm 2V_{dc}$, $\pm 4V_{dc}$, and C_2 can discharge at output voltage levels of $\pm 3V_{dc}$, $\pm 4V_{dc}$. The switching transitions of each voltage level instants (as shown in Fig.6) t_a, t_b, t_c, t_a^*, t_b^*, t_c^* are formulated as

$$t_a = \frac{sin^{-1}\left(\frac{1}{4}\right)}{\omega_m} \tag{2}$$

$$t_b = \frac{sin^{-1}\left(\frac{2}{4}\right)}{\omega_m} \tag{3}$$

$$t_c = \frac{sin^{-1}\left(\frac{3}{4}\right)}{\omega_m} \tag{4}$$

$$t_{a^*} = \frac{\pi - sin^{-1}\left(\frac{3}{4}\right)}{\omega_m} \tag{5}$$

$$t_{b^*} = \frac{\pi - sin^{-1}\left(\frac{2}{4}\right)}{\omega_m} \tag{6}$$

$$t_{c^*} = \frac{\pi - sin^{-1}\left(\frac{1}{4}\right)}{\omega_m} \tag{7}$$

A maximum amount of discharging can take place during resistive load conditions at voltage level $\pm 4V_{dc}$. More voltage drops falls in the time interval of $(t_x - t_y)$. while calculating the capacitance values considering large discharging time intervals of each capacitor. The charge /discharge cycles can happen n times in the interval of $(t_x - t_y)$. Discharging time intervals of capacitor C_1 are $(t_{x1} - t_{x2})$. Similarly, discharging time intervals of capacitor C_2 is $(t_{y1} - t_{y2})$. Each capacitor's amount of discharging charge is their respective time intervals

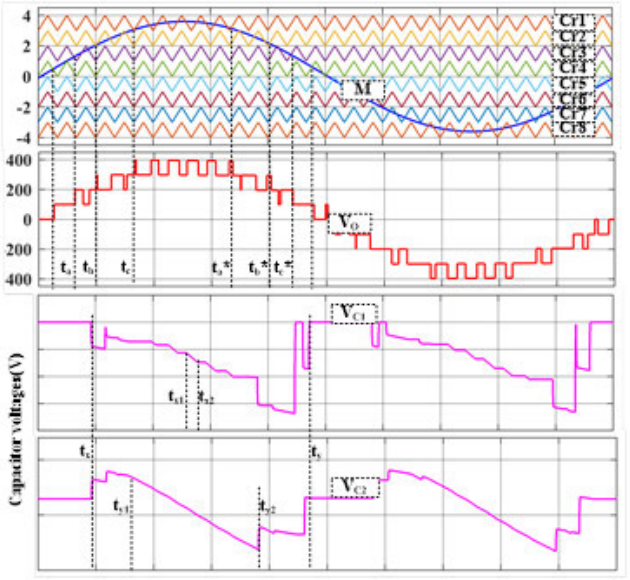

FIGURE 6. Level-shifted pulse width modulation scheme and Capacitor voltages concerning output voltage.

as represented in Eq. (8) & (9).

$$\Delta Q_k^{C_1} = \int_{t_{x1}}^{t_{x2}} I_O.sin\,(\omega_m t).dt \tag{8}$$

$$\Delta Q_k^{C_2} = \int_{t_{y1}}^{t_{y2}} I_O.sin\,(\omega_m t).dt \tag{9}$$

where $\Delta Q_k^C 1$ and $\Delta Q_k^C 2$ are the discharging amount of charge k^{th} (k = 1,2,3.....n) cycle of the capacitors C_1& C_2, I_o is the magnitude output current, and $\omega_m = 2\pi f_m$.

The total amount of charge for each capacitor can be expressed as in Eq. (10) & (11).

$$Q^{C_1}{}_{total} = \sum_0^n Q_z^{C_1} = \sum_0^n \left[\int_{t_{x1}}^{x2} I_O.\sin\,(\omega_m t).dt\right] \tag{10}$$

$$Q^{C_2}{}_{total} = \sum_0^n Q_z^{C_2} = \sum_0^n \left[\int_{t_{y1}}^{t_{y2}} I_O.\sin\,(\omega_m t).dt\right] \tag{11}$$

Assume, at worst conditions there is no charge is observed by the capacitors, with permissible voltage ripple, the min capacitances can be calculated in Eq. (12) & (13).

$$C_{1min} = \frac{Q^{C_1}{}_{total}}{V^{C_1}{}_{ripple}} \tag{12}$$

$$C_{2min} = \frac{Q^{C_2}{}_{total}}{V^{C_2}{}_{ripple}} \tag{13}$$

V. POWER LOSS CALCULATIONS

The total power losses of the proposed converter may be categorized as follows,

A. switching power losses.
B. conduction power losses.
C. capacitor voltage ripple (charging) losses.

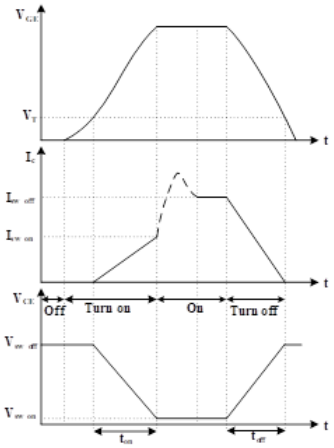

FIGURE 7. Turn ON and Turn OFF characteristics of the semi-conductor switches.

A. SWITCHING POWER LOSSES

Switching losses can occur due to turning on/turning off the switches (as shown in figure.7) (IGBTs), rapidly throughout a cycle. These losses differ depending on variables such as blocking voltage (V_{BO}), collector current (I_c), Gate-Emitter voltage (V_{GE}), Gate resistance (R_{GE}), and Junction temperature (T_j).

1) TURN ON CONDITION

when the switch is turned ON, V_{GE} is more than the threshold voltage, I_c starts rising, and Collector-Emitter voltage (V_{CE}) starts falling. The time(t_{on}) can take place to settle V_{CE} reaches V_{sw_on}. In this time (t_{on}) the V_{CE}, and I_c are the finite values that cause switching turn-on losses, as represented in Eq. (14).

2) TURN OFF CONDITION

The time (t_{off}), V_{CE} and I_c are also the finite values which cause switching turn OFF losses, as represented Eq. (15).

$$\begin{aligned} P_{sw\_loss,j(ON)} &= f_{cr}\int_0^{t_{on}} V_{sw\_off}, i(t) * i(t)dt \\ &= f_{cr}\int_0^{t_{on}} -\left(\frac{\left(V_{sw\_off}\right), i}{t_{on}}\left(t - t_{on}\right)\right) \\ &\quad * \left(\frac{\left(I_{sw\_on}\right), i}{t_{on}}(t)\right)dt \\ &= \frac{1}{6} f_{cr} * V_{sw\_off}, i * I_{sw\_on}, i * t_{on} \end{aligned} \tag{14}$$

$$\begin{aligned} P_{sw\_loss,j(OFF)} &= f_{cr}\int_0^{t_{off}} \left(V_{sw\_off}\right), i(t) * i(t)dt \\ &= f_{cr}\int_0^{t_{off}} \left(\frac{\left(V_{sw\_off}\right), i}{t_{off}}(t)\right) \\ &\quad * \left(-\frac{\left(I_{sw\_off}\right), i}{t_{off}}\left(t - t_{off}\right)\right)dt \\ &= \frac{1}{6} f_{cr} * V_{sw\_off}, i * I'_{sw\_on}, i * t_{off} \end{aligned} \tag{15}$$

The total switching losses during turn ON, turn OFF and all other variable conditions as represented in Eq. (16).

$$\begin{aligned} P_{sw\_loss,j(ON/OFF)} &= P_{sw\_loss,j(ON)} \\ &\quad + P_{sw\_loss,j(OFF)}.\text{adj}\ (T_j).\ \text{adj}\ (V_{GE}) \\ &\quad .\ \text{adj}\ (V_{bo}).\ \text{adj}\ (I_c). \end{aligned} \tag{16}$$

where, $P_{sw\_loss,j(ON)}$, $P_{sw\_loss,j(OFF)}$ are the turn ON & turn OFF switching losses for j^{th} switch available on IGBT data sheet, adj (T_j) adj (V_{GE}) adj (V_{bo}) adj (I_c) are adjustable parameters concerning their operating conditions.

The number of times each switch and diode turn ON/OFF for one cycle reference waveform can be calculated as in Eq.(17).

$$N_{sw\_on} = N_{sw\_off} = \frac{f_{cr}}{f_m} \tag{17}$$

where f_{cr} is carrier signal frequency (Hz), f_m is modulating signal frequency (Hz), N_{sw} is no of switches.

Therefore, the total switching losses are

$$\begin{aligned} \left(P_{Total\ sw\_losses}\right) = \sum_{j=1}^{N_{sw}} \Bigg(\Bigg(\sum_{k=1}^{N_{sw\_on}(j)} P_{sw\_loss(ON)}\,(jk) \Bigg) \\ + \Bigg(\sum_{k=1}^{N_{sw\_off}(j)} P_{sw\_loss(OFF)} \Bigg) \Bigg) \end{aligned} \tag{18}$$

B. CONDUCTION LOSSES

Due to their ON state resistance and voltage across the switches and diodes will experience losses in the conduction state. Eq. (19) & (20) are the general expression of switches and diode conduction losses.

$$P_{sw\_con\ loss} = V_{sw\_on} * I_{sw\_avg} + R_{sw\_on} * I^2_{sw\_rms} \tag{19}$$

$$P_{D\_con\ loss} = V_{D\_on} * I_{D\_avg} + R_{D\_on} * I^2_{D\_rms} \tag{20}$$

where $P_{swconloss}$ is switching conduction losses, $P_{D\_conloss}$ is Diode conduction losses, V_{sw_con} is switch across ON state voltage, V_{D_con} is a diode across ON state voltage, R_{sw_on} is switch ON state resistance, R_{D_on} is diode ON state resistance, I_{sw_rms}, I_{D_rms}, I_{sw_avg}, I_{D_avg} are Root mean square and average currents of the switches and diodes. For different voltage levels, the switching and diode conduction losses are changed, so each voltage level's conduction losses are calculated in Eq. (21).

$$\begin{aligned} P_{con\_loss(V_O=+1V_{dc})} &= 7\left(V_{sw\_on} * I_{sw\_avg} + R_{sw\_on} * I^2_{sw\_rms}\right) \\ &\quad + 2\left(V_{D\_on} * I_{D\_avg} + R_{D\_on} * I^2_{D\_rms}\right) \\ P_{con\_loss(V_O=+2V_{dc})} &= 7\left(V_{sw\_on} * I_{sw\_avg} + R_{sw\_on} * I^2_{sw\_rms}\right) \\ &\quad + 1\left(V_{D\_on} * I_{D\_avg} + R_{D\_on} * I^2_{D\_rms}\right) \\ P_{con\_loss(V_O=+3V_{dc})} &= 5\left(V_{sw\_on} * I_{sw\_avg} + R_{sw\_on} * I^2_{sw\_rms}\right) \\ &\quad + 1\left(V_{D\_on} * I_{D\_avg} + R_{D\_on} * I^2_{D\_rms}\right) \end{aligned}$$

TABLE 2. Comparison of the proposed topology with other 9_level topologies.

Topology	N_S	N_{SW}	$N_{Drivers}$	N_D	V_C		N_C	G	MBV ($*V_{dc}$)	$T.S.V_{(p.u)}$	N_{Total}	C.F	No of voltage levels	Reported efficiency
					$1\ V_{dc}$	$2V_{dc}$								
2012[14]	1	13	13	0	3	0	3	4	4	6.25	16	36.25	9	85.9%
2013[15]	1	12	12	2	2	0	2	4	4	6.25	16	35.25	9	83%
2014[16]	1	8	8	6	3	0	3	4	4	8	17	34	9	91.5%
2014[17]	1	10	10	3	3	0	3	4	4	6.25	16	33.25	9	91.6%
2017[18]	1	10	10	4	3	0	3	4	4	7.5	18	34.25	9	93.5%
2018[19]	1	17	17	0	4	0	4	1	4	7.25	21	46.25	9	NA
2019[20]	1	18	18	5	4	0	4	4	4	7	27	53	9	92.5%
2019[21]	1	12	11	0	3	0	3	4	4	6.5	15	33.25	9	90%
2020[22]	1	12	12	0	4	0	4	1	1	12	16	41	9	96%@
2020[23]	1	16	16	0	3	0	3	4	4	7	19	43	9	NA
2021[24]	1	12	11	2	4	0	4	3	3	7.5	18	37.5	9	94.5%
2021[25]	1	14	14	0	5	0	5	4	4	7.5	19	41.5	9	98.3%
2022[26]	1	9	9	2	5	0	5	4	2	10	16	36	9	94%
2022[27]	1	12	12	1	1	0	2	4	4	7.5	14	35.5	9	87-95.5%
2022[28]	1	10	10	0	1	1	2	4	4	6.25	12	29.25	9	97%
2022[29]	1	11	10	0	2	0	2	3	4	5.53	13	29.53	7	98.77%
Proposed	1	10	10	0	1	1	2	4	4	6.25	12	29.25	9	96.5%

N_S =no of sources, N_{SW} = no of switches, $N_{Drivers}$ =no of gate driver circuits, V_C g=voltage across the capacitor, N_C=no of capacitors, G =gain, MBV=max blocking voltage, TSV=total standing voltage, N_{Total}=total no of components, C.F =cost factor.

$$
\begin{aligned}
P_{con\_loss(V_O=+4V_{dc})} &= 4\left(V_{sw\_on} * I_{sw\_avg} + R_{sw\_on} * I^2_{sw\_rms}\right)\\
P_{con\_loss(V_O=-1V_{dc})} &= 7\left(V_{sw\_on} * I_{sw\_avg} + R_{sw\_on} * I^2_{sw\_rms}\right)\\
&\quad + 2\left(V_{D\_on} * I_{D\_avg} + R_{D\_on} * I^2_{D\_rms}\right)\\
P_{con\_loss(V_O=-2V_{dc})} &= 7\left(V_{sw\_on} * I_{sw\_avg} + R_{sw\_on} * I^2_{sw\_rms}\right)\\
&\quad + 1\left(V_{D\_on} * I_{D\_avg} + R_{D\_on} * I^2_{D\_rms}\right)\\
P_{con\_loss(V_O=-3V_{dc})} &= 5\left(V_{sw\_on} * I_{sw\_avg} + R_{sw\_on} * I^2_{sw\_rms}\right)\\
&\quad + 1\left(V_{D\_on} * I_{D\_avg} + R_{D\_on} * I^2_{D\_rms}\right)\\
P_{con\_loss(V_O=-4V_{dc})} &= 4\left(V_{sw\_on} * I_{sw\_avg} + R_{sw\_on} * I^2_{sw\_rms}\right)
\end{aligned}
\tag{21}
$$

The total conduction losses are calculated by adding all the voltage levels of conduction losses are represented in Eq. (22).

$$
\begin{aligned}
\left(P_{Total\_con\ loss}\right) &= P_{con\_loss(V_O=+1V_{dc})} + P_{con\_loss(V_O=+2V_{dc})}\\
&\quad + P_{con\_loss(V_O=+3V_{dc})} + P_{con\_loss(V_O=+4V_{dc})}\\
&\quad + P_{con\_loss(V_O=-1V_{dc})} + P_{con\_loss(V_O=-2V_{dc})}\\
&\quad + P_{con\_loss(V_O=-3V_{dc})} + P_{con\_loss(V_O=-4V_{dc})}
\end{aligned}
\tag{22}
$$

C. CAPACITOR RIPPLE VOLTAGE CALCULATIONS

The differences between source voltage and capacitor voltage cause power losses. when there are in parallel those losses are calculated as in Eq.(23).

$$
P_{c\_loss} = \frac{1}{2}\sum_{k=1}^{n} C.\Delta V^2{}_k.f_{ref}. \tag{23}
$$

where n is no of capacitor charging states, ΔV_k is voltage charging ripples in capacitors.

Therefore, the total power losses can be calculated by adding all the power losses available at each stage and can be represented in Eq. (24).

Total power losses,

$$
\begin{aligned}
(P_{total\_losses}) &= (P_{totalsw\_loss}) + (P_{total\_conloss})\\
&\quad + (P_{c\_losses})
\end{aligned}
\tag{24}
$$

TABLE 3. Components used in experimental prototype.

Parameter	Value
Input voltage supply	20-30V
Power switches	IRP460
Power diodes	MUR860
Capacitors	2200µf/450V
Controller	Dspace cp1104
Switching frequency	1kHz,2.5 kHz
output frequency	50 Hz
Resistive loads	100Ω-300 Ω
Inductive loads	25mH-300mH
DSO	DSOX1204A,200MHz ,2GSa/s

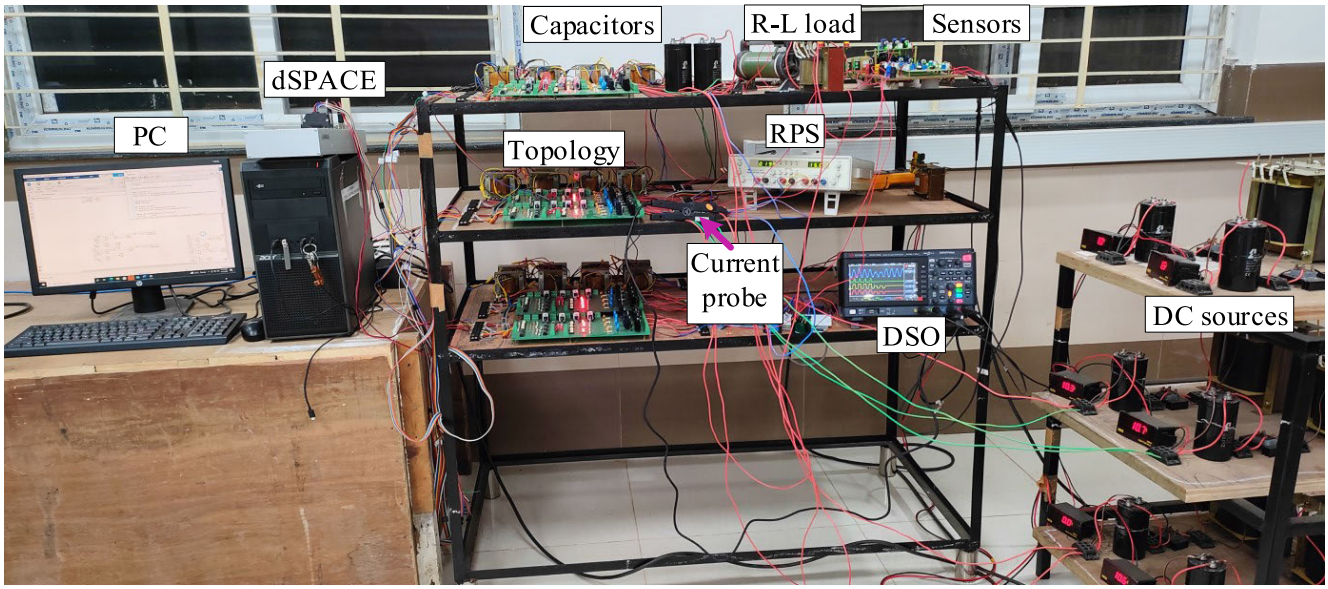

FIGURE 8. Experimental prototype set up in the laboratory.

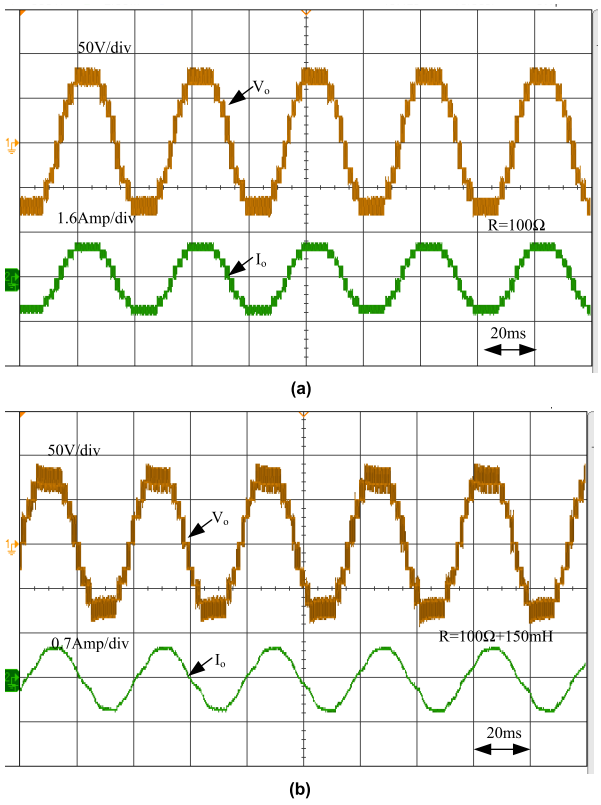

FIGURE 9. Output voltage and load current (a) for the. R = 100Ω, (b) for the RL = 100Ω + 150 mH.

The overall efficiency of the proposed topology can be calculated with the help of all the above power losses equations,

$$\text{Output power } (P_{out}) = (P_{In}) - (P_{total\_losses}) \quad (25)$$

$$\text{Efficiency } (\eta) = (P_{output})/(P_{input}) * 100 \quad (26)$$

$$\eta = \frac{V_{dc} * I_{dc} - P_{Total\ sw\_losses} - P_{Total\_con\ loss} - P_{c\_loss}}{V_{dc} * I_{dc}} * 100 \quad (27)$$

where η is MLI efficiency, V_{dc}& I_{dc} are input DC voltage and current respectively, ($P_{total\ sw\_loss}$) and ($P_{total\_con\ loss}$) are total switching and conduction losses respectively of all switches and (P_{c_losses}) are capacitors voltage ripple (charging) losses.

VI. COMPARISON ANALYSIS WITH RECENT TOPOLOGY

Table.2, shows a comparison of various recent competitive topologies with proposed one, based on no the sources, no of switches, no of gate driver's circuits, no of capacitors, MBV (in terms of V_{dc}, total no of components, cost factor (C.F) and efficiency. The mathematical expression for the cost factor is $(CF) = N_{SW} + N_D + N_{Drivers} + N_C + N_S + \delta$T.S.V where δ is the weight factor. When $\delta < 1$, switching components weightage is more. when $\delta > 1$, T.S.V weightage is more. If $\delta = 1$ the weightage of both switching components and T.S.V are equal. so $\delta = 1$ is taken into account to calculate the cost factor proposed topology. In [14], the topology having the number of switch count and T.S.V value is the same as the proposed one. But an extra capacitor is used across the dc voltage source. The total components cost factor is more. In [15], it has less switch count, but the capacitor count and T.S.V value are the same. But an extra 2 diodes are used that can increase the total no of components count as well as cost factor. An additional dc voltage source is also used to generate a 9-level output voltage. In [16], topology having several switch counts is less but an extra 6 diodes and one

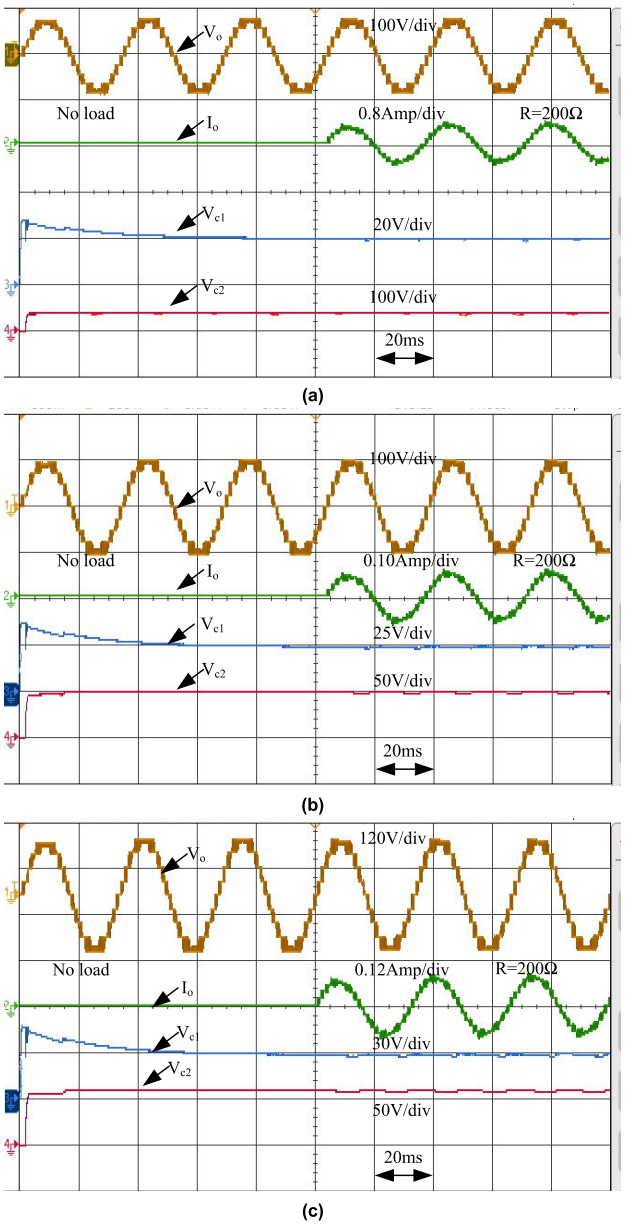

FIGURE 10. Output voltage, load current and capacitor voltage at no load to R = 200Ω load (a) for Vin=20V, (b) for Vin=25V, (c) for Vin = 30V.

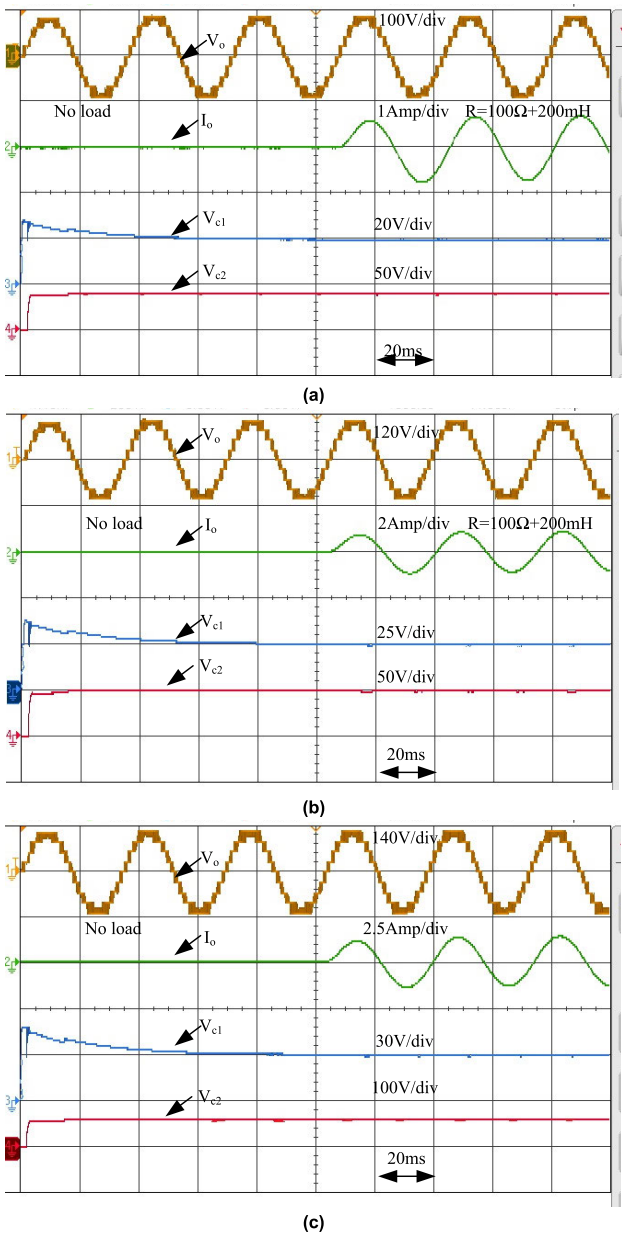

FIGURE 11. Output voltage, load current and capacitor voltage at no load to RL=100Ω+200mH load (a) for Vin=20V, (b) for Vin=25V, (c) for Vin=30V.

more capacitor are used. The value of T.S.V is very high, which may reduce the life span of the switches. In [17], topology 10 switches,3 diodes, and 3 capacitors are used. Even though the T.S.V value is the same as the proposed one, the total number of components and cost factor is more. In [18], a quasi-resonant converter has an inductor in the resonance circuit. It has a count of 10 switches, 4 diodes, and 4 capacitors. The T.S.V and cost factor value of this topology is high. The total power losses are more, efficiency is less. In [19], topology has an extra 4 switches and 2 capacitors as compared to proposed one, the total circuit design cost is high. T.S.V also has more and also efficiency is less. In [20], topology the total no of component count and T.S.V value is more, and the efficiency is less as compared to proposed one. In [21], topology the no of switch count is less, but an extra capacitor is used. T.S.V value and cost factor value are more and efficiency is less. In [22], topology T.S.V is very high; this causes failure of the switches due to high stresses. Gain of the circuit unity only. In [23], the topology of switches and capacitors is more, and then also the total number of components and T.S.V are more. In [24], topology the no of switches is less but, an extra 2 capacitors and diodes are used, so the total components and also T.S.V is more. Gain and Efficiency are less. In [25], topology components count switches, capacitors, a total count of components, and T.SV more. More T.S.V. creates stress on the switches and

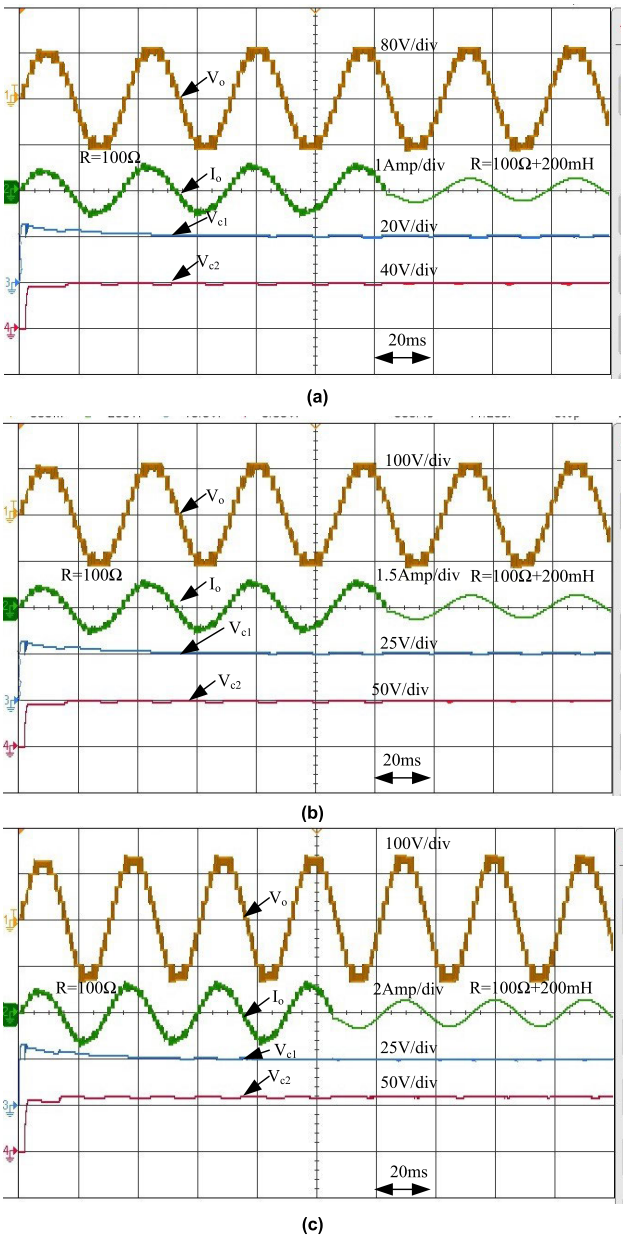

FIGURE 12. Output voltage, load current and capacitor voltage at R=100Ω load to RL=100Ω + 200mH load (a) for Vin=20V, (b) for Vin=25V, (c) for Vin=30V.

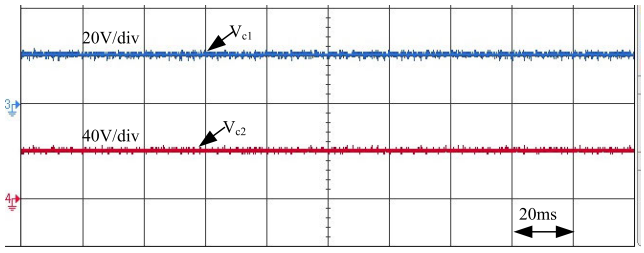

FIGURE 13. Balanced capacitor C_1 and C_2 voltages.

leads to damage. In [26], the topology switch count is less but, an extra 2 diodes and 3 capacitors are used. The T.S.V is very high, and stress on switches causes more losses.

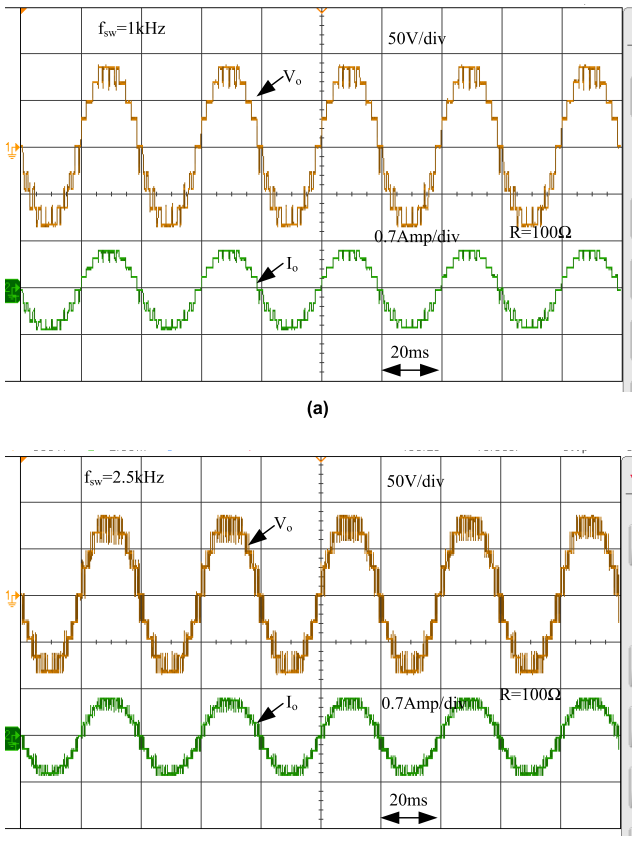

FIGURE 14. Output voltage and load current at different switching frequency (a) for switching frequency f_{sw} = 1kHz (b) for switching frequency f_{sw} = 2.5kHz.

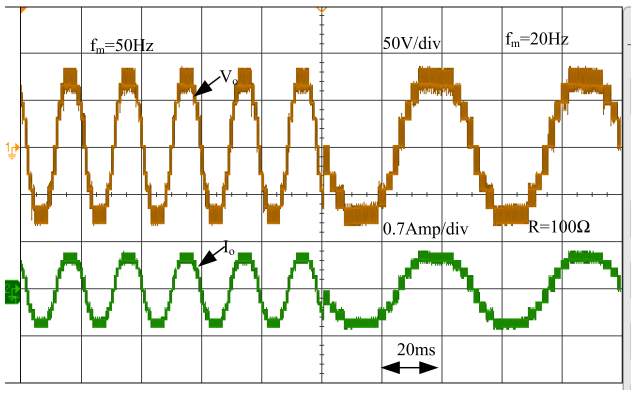

FIGURE 15. Output voltage and load current at frequency modulation f_m = 50Hz to f_m = 20Hz.

The cost factor value is high. In [27], topology efficiency is almost the same as the proposed one and the total no of component values is less. T.S.V value is high, causing stress on the switches. In the topology proposed in [28], T.S.V value and switch count are the same as that of proposed topology. However, the proposed topology can withstand a wide range of loading conditions. In [29], the T.S.V value is lower than the proposed topology, however, it can produce only 7 levels

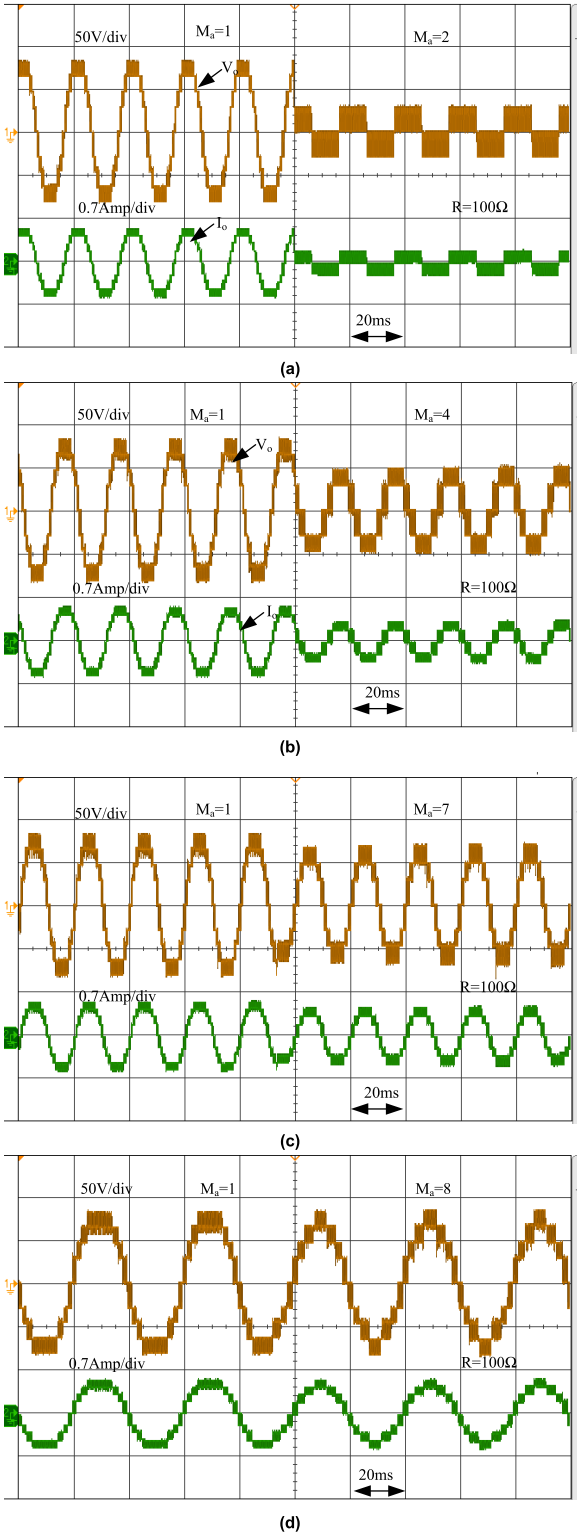

FIGURE 16. Output voltage and load current at different modulation index (a) for the $M_a = 0.2$, (b) for the $M_a = 0.4$ (c) for the $M_a = 0.4$ and (d) for the $M_a = 0.8$.

of output voltage. Proposed topology is improved to produce nine levels with a gain of four and better total harmonic distortion (THD).

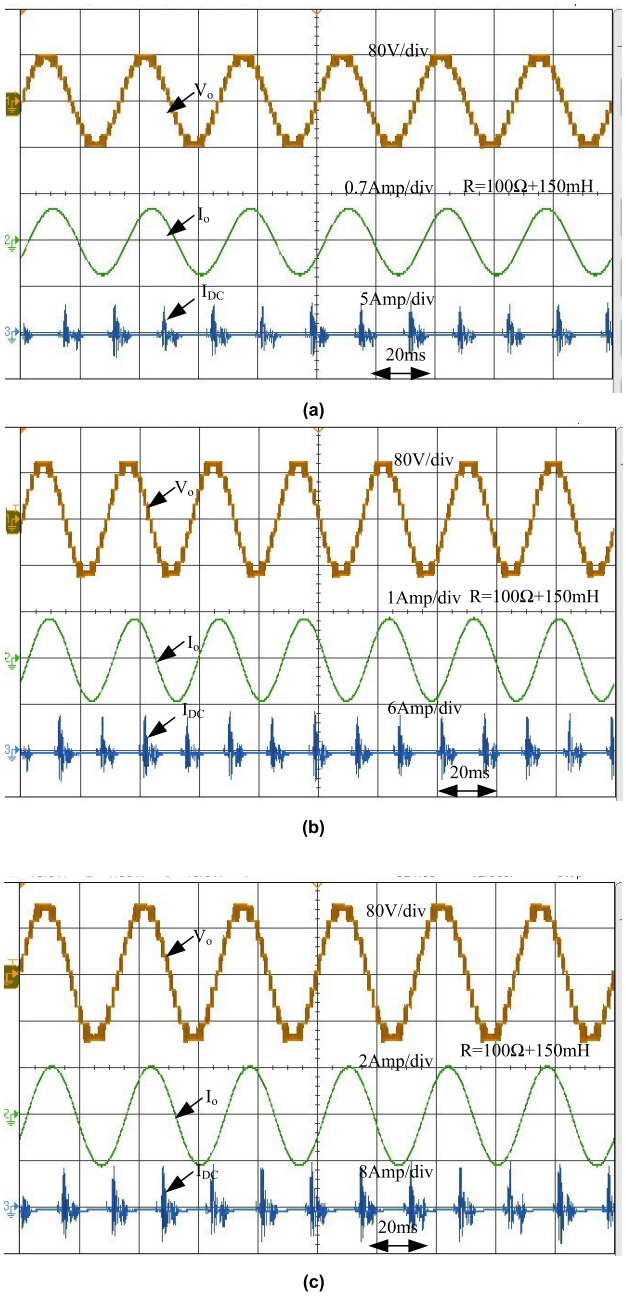

FIGURE 17. Output voltage, load current and input current at load RL=100Ω+ 150mH load (a) for Vin=20V, (b) for Vin=25V, (c) for Vin=30V.

VII. EXPERIMENTAL ANALYSIS

The experimental results of proposed topology can be analyzed through a prototype set-up for various input voltage values as shown in Fig 8. The rating of various components used in prototype arrangement is tabulated in table.3. Dspace cp1104 controller can be used to implement the LSPWM scheme for the switching gate signals. For Vin = 20V, the output voltage and load current at load R = 100Ω and RL = 100Ω+150mH as shown in Fig.9(a) and Fig.9(b) respectively. It is observed that the current can be in phase for R load and lag behind the output voltage for RL load.

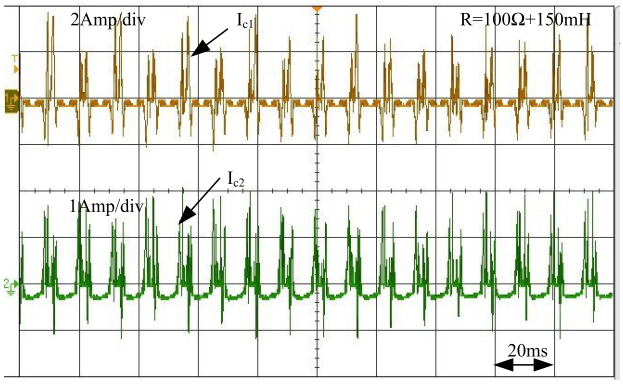

FIGURE 18. Capacitor C_1 and C_2 current at RL = 100Ω + 150 mH.

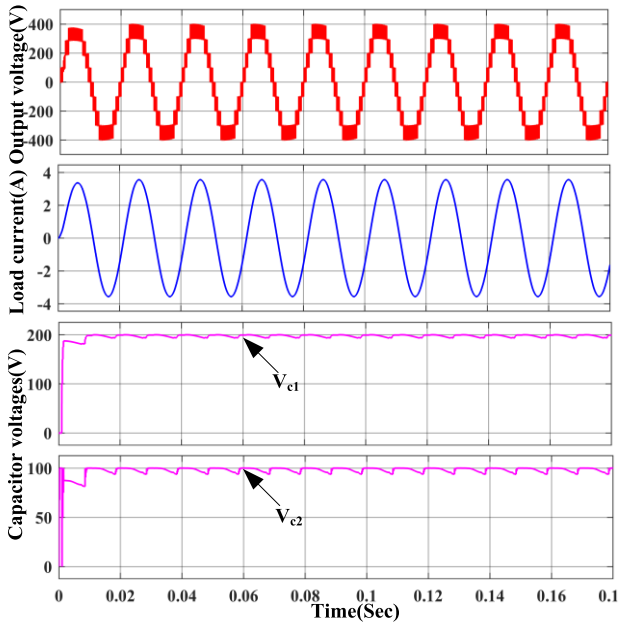

FIGURE 19. Output voltage, current and capacitor voltages at100Ω + 150mH.

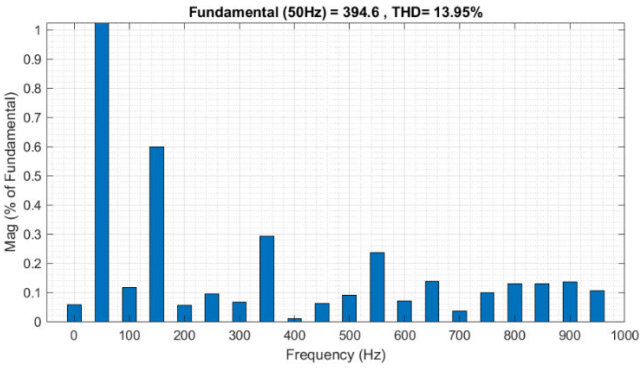

FIGURE 20. THD of the load voltage at100Ω + 150mH.

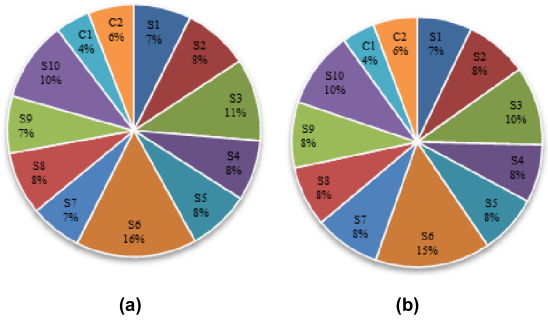

FIGURE 21. Percentage of total losses (a) for the RL = 100Ω, (b) for the RL = 100Ω + 150 mH.

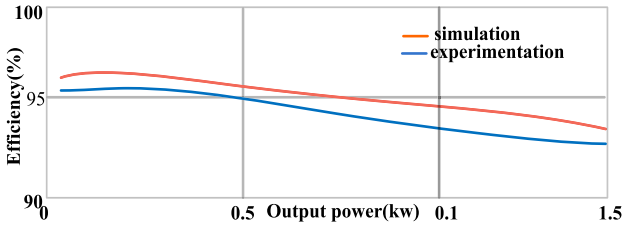

FIGURE 22. Efficiency at load variation of 0-1.5kw.

Output voltage, load current, and capacitor voltages at no load to R = 200Ω load are shown in Fig. 10(a),10 (b), and 10(c) respectively, for the input voltage values Vin = 20 V, Vin = 25 V, and Vin = 30 V. Similarly, the output voltage, load current, and capacitor voltages are shown in Fig. 11(a), 11(b), and 11(c) from no load to RL = 100Ω+200 mH load. In these cases, output voltage and capacitor voltage are maintained at their respective values, but the current magnitude is varied. When the load variation transients R = 100Ω to RL = 100+200mH for voltages Vin = 20V, Vin = 25V, and Vin = 30V, as shown in Fig. 12(a), 12(b), and 12(c). Here, the current nature can be shifted from phase to lag with the output voltage. Balanced capacitor voltages of C_1 and C2 are V_{dc} and $2V_{dc}$ are shown in Fig.13. Output voltage and load current at load RL = 100Ω+150mH with switching frequency f_{sw} = 1kHz as shown in Fig.14(a). At the same load condition with switching frequency f_{sw} = 2.5kHz as shown in Fig.15(b). The switching transients either high or low due to switching frequencies can impact the output voltage at each level. When the modulating frequencies can be changed f_m = 50Hz to f_m = 20Hz as shown in Fig 15. It can be observed that the proposed topology can bear any frequency range of operations. When the modulation index can change Ma = 1 to Ma = 0.2 the output voltage level can change from nine to three as shown in Fig 16(a).Here modulating signals can compare with the only two carrier signals Cr_4 and Cr_5. When the modulation index can change Ma = 1 to Ma = 0.4 the output voltage levels as shown in Fig 16(b).Here modulating signals can compare with only four carrier signals Cr_3, Cr_4, Cr_5, and Cr_6. When the modulation index can change from Ma = 1 to Ma = 0.7, the output voltage level can change from nine to seven as shown in Fig 16(c).

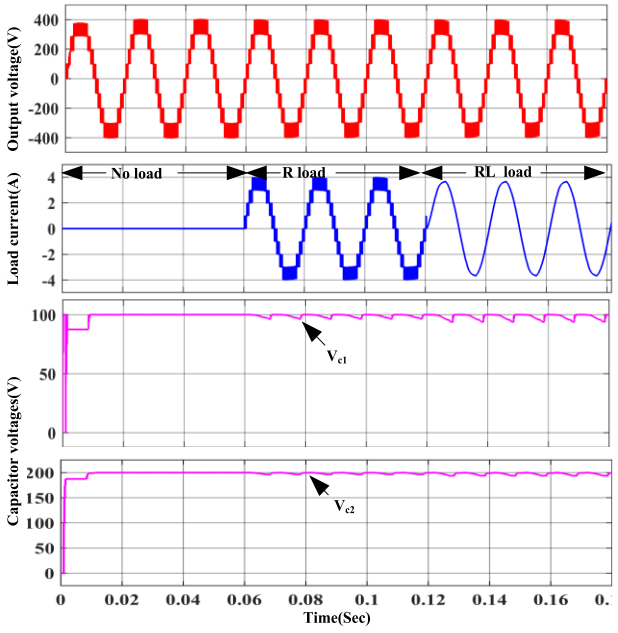

FIGURE 23. Output voltage, current and capacitor voltages for no load,100Ω and 100Ω + 150mH.

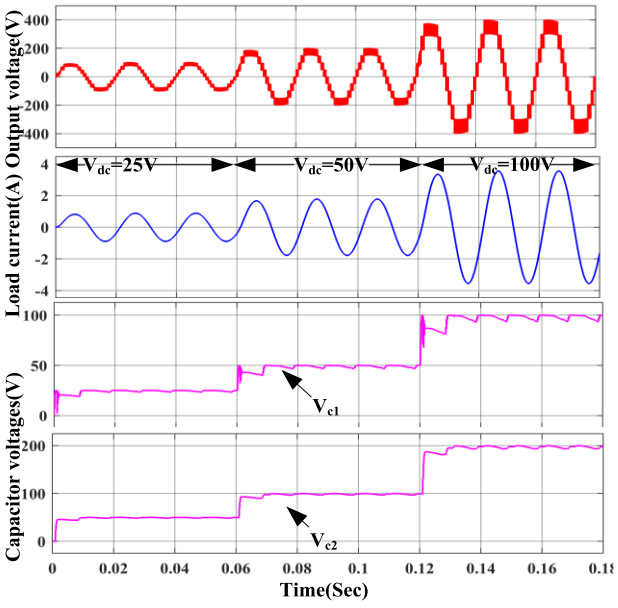

FIGURE 24. Output voltage, current and capacitor voltages for input voltage changes V_{dc} = 25V, V_{dc} = 50V and V_{dc} = 100V.

Here modulating signals can compare with all the carrier signals except Cr_1 and Cr_8. When the modulation index can change Ma = 1 to Ma = 0.8 the output voltage levels ($+4V_{dc}$ &$-4V_{dc}$) cannot change as shown in Fig 16(d). But their width can be reduced due to comparison of modulating signal (M) and carrier signal Cr_1 is reduced. Output voltage, load current and input current at load RL = 100Ω+ 150mH are shown in Fig. 17 (a), 17 (b), and 17 (c), respectively, for

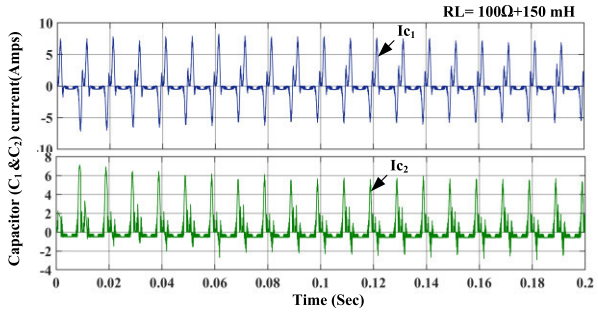

FIGURE 25. Capacitor C_1 and C_2 current at RL = 100Ω + 150 mH.

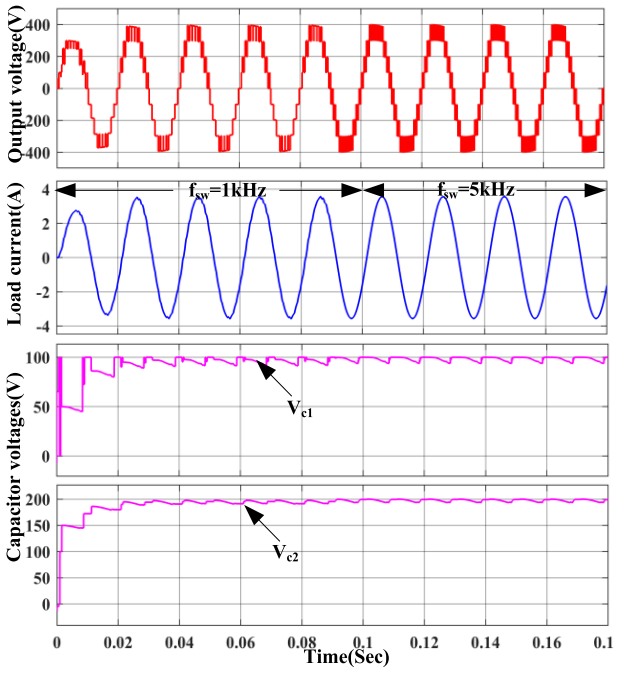

FIGURE 26. Output voltage, current and capacitor voltages for switching frequency f_{sw} = 1kHz and f_{sw} = 5kHz.

the input voltage values Vin = 20 V, Vin = 25 V, and Vin = 30 V. Capacitor currents in the experimentation at a load of RL=100Ω+ 150mH is shown in Fig. 18.

VIII. MATLAB/SIMULATION RESULTS AND ANALYSIS

The performance of the proposed topology can be validated through MATLAB/Simulink results with various parameters of the components at different load conditions. Here the components parameters are taken as the input dc voltage = 100V, capacitors $C_1 = 2200\mu$f, $C_2 = 2200\mu$f. At the load condition of RL = 100Ω+150mH with modulation index (M = 1), the output voltage, load current and capacitor voltages are shown in Fig 19. The proposed topology can boost the input voltage 100V - 400V output voltage and balance the capacitor voltages at C_1 = 100V and C_2 = 200V. Voltage THD and fundamental components of the output voltage waveform as shown in Fig. 20.

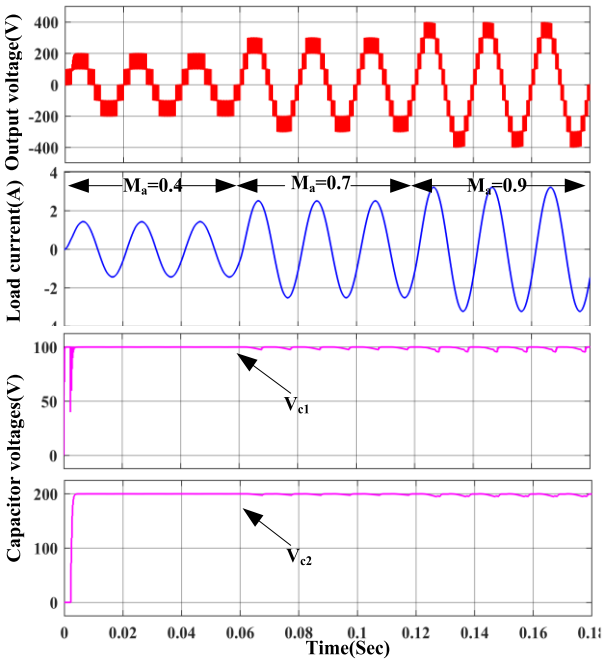

FIGURE 27. Output voltage, current and capacitor voltages for modulation index $M_a = 0.4$, $M_a = 0.7$ and $M_a = 0.9$.

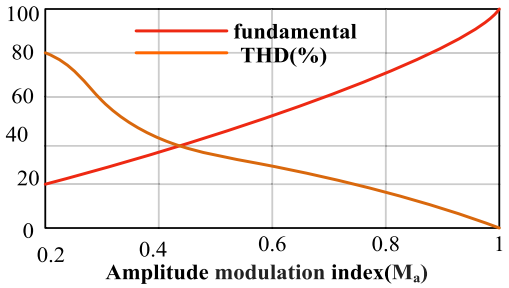

FIGURE 28. Fundamental component and THD (%) for $M_a = 0.4 - 1$.

For calculation of total losses like switching losses, capacitor ripple voltage losses, and conduction losses, the topology is modeled in PLECS software. The percentage of the total losses of switches, capacitors, and diodes at a load of 100Ω and 100Ω+150mHis shown in Fig 21(a). and Fig 21(b). The efficiency of the proposed topology can be plotted at load conditions of 0 to 1.5kw as shown in Fig 22. When no load to various load conditions such as in-phase (R = 100Ω) and lagging (RL = 100Ω+100mH) loads are analyzed, the output voltage, output current, and capacitor voltages are shown in Fig 23. In this condition the output voltage is maintained at all above-mentioned loading conditions, the current magnitude can vary from zero, in-phase and lagging with output voltage and the capacitor voltages may dip with the permissible limits of the IEEE standards. When input dc voltage can be varied $V_{dc} = 25V$, $V_{dc} = 50V$ and $V_{dc} = 100V$.At this condition, the output voltage is maintained nine levels, but the magnitude of both output voltage and current magnitudes are changed. Capacitors voltages are balanced at Vc_1 = 25V,50V,100V

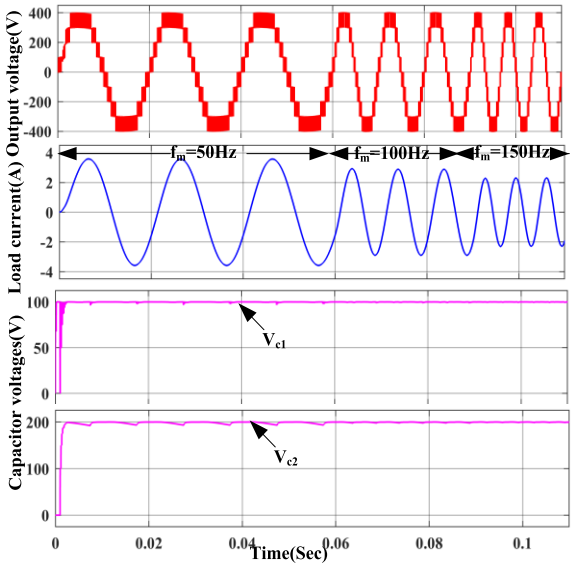

FIGURE 29. Output voltage, current and capacitor voltages for frequency modulation $f_m = 50Hz$, $f_m = 100Hz$ and $f_m = 150Hz$.

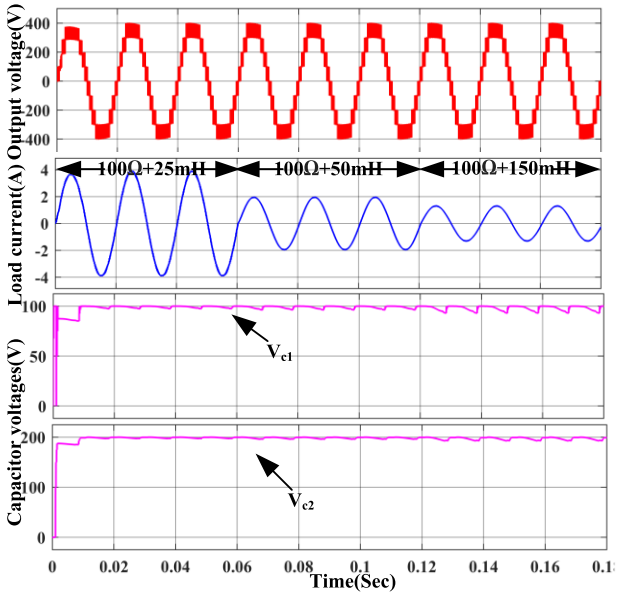

FIGURE 30. Output voltage, current and capacitor voltages at RL = 100Ω+ 25mH, RL = 100Ω + 50 mH and RL = 100Ω + 150 mH.

and Vc_2 = 50V,100V,200V. all those corresponding output waveforms are shown in Fig 24.Capacitor currents for the topology at 100Ω + 150 mH load, as shown in Fig 25. Switched capacitor MLIs draw an impulse current from a DC source to charge the capacitor at its initial condition. The impulse charging current can be reduced by using a small value of inductor.output voltage, output current, and capacitor voltage results are shown in Fig. 26. When the switching frequency (carrier frequency) varies from f_{SW} = 1kHz to f_{SW} = 5kHz. In this, at higher switching frequency conditions out voltage levels are generated with higher switching

transients of the switches, which may cause more switching losses.

It can also be observed when higher switching frequency harmonics are shifted, these can help us reduce the filter size. When the magnitude modulation index can be changed to $M_a = 0.4$, $M_a = 0.7$ and $M_a = 0.9$ then output voltage, load current and capacitor voltages are shown in Fig 27. Here, the output voltage and load current magnitude can change due to corresponding M_a values of the modulating signals compared with carrier signals. When the M_a values are increased then the corresponding fundamental component increase and THD (%) value decreased as shown in Fig 28. When modulating signal frequency has changed from 50Hz to 150Hz and the corresponding load voltage, current and capacitor voltages are shown in Fig 29. The load impedance can increase due to increasing the supply frequency. If load impedance increases, the load current can decrease and vice versa. When variable lagging loading conditions 100Ω+25mH, 100Ω+25mH, and 100Ω+150mH output voltage, load current, and capacitor voltages as shown in Fig 30. Load current is a lagging nature while increasing the load and magnitude also reduced.

IX. CONCLUSION

In this article, a single DC Source new step up nine level inverter was reported with a reduced count of components for solar PV stand alone system. The proposed topology with quadruple voltage gain capability operates with the parallel/series-charging/discharging technique of the capacitor. An LSPWM technique was used for balancing the capacitor voltages to achieve the desired output voltage and also to get lower stress on the components. Furthermore, the experimental setup of the proposed topology can be tested at different load conditions, input voltage variations, amplitude modulation variations, switching frequency variations, and frequency modulation variations. The THD of the output voltage and voltage ripples of the capacitors are within the limits. Moreover, a comparative analysis reveals that the proposed topology has simple structure, lower switch count, quadruple boosting capability, higher efficiency, less cost factor and less $T.S.V_{(p.u)}$. The effectiveness of the proposed topology validates through MATLAB/Simulations and prototype experimental results. Therefore, the proposed topology provides an innovative solution to renewable solar PV applications, where DC-AC power conversion is needed with a quadruple gain of voltages, low switching stress for lesser no of switch count using a single dc source. The future focus of this work will be to interconnect the proposed converter with small-scale rooftop PV systems.

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SRIMANNARAYANA KOVVALI received the B.Tech. degree from Andhra University, Visakhapatnam, India, in 2018. He is currently pursuing the M.Tech. degree in power electronics and drives with the National Institute of Technology Andhra Pradesh, Tadepalligudem, India. He was a Lecturer with NZVD Polytechnic College, India, for two years. His research interests include multilevel inverter topologies, electric vehicles, dc–dc converters, and grid integration of renewable energy systems.

NAKKA JAYARAM received the B.Tech. degree in electrical and electronics engineering from Jawaharlal Nehru Technological University, Hyderabad, India, in 2007, the M.Tech. degree from the Vellore Institute of Technology, Vellore, India, in 2009, and the Ph.D. degree in electrical engineering from the Indian Institute of Technology, Roorkee, India, in 2014. Currently, he is with the Department of Electrical Engineering, National Institute of Technology Andhra Pradesh, India. He has published articles in many international and national journals and conferences. His research interests include multilevel inverters, high-power converters, and renewable energy systems. He is a reviewer of many international journals.

SATYA VENKATA KISHORE PULAVARTHI (Student Member, IEEE) received the B.E. degree in electrical and electronics engineering from Andhra University, India, in 2009, and the M.Tech. degree in power electronics from the National Institute of Technology, Calicut, India, in 2011, and the Ph.D. degree from the National Institute of Technology Andhra Pradesh, India. He was an Assistant Professor with the Vignan's Institute of Information Technology, India, for five years, and Dire Dawa University, Ethiopia, for three years. He is currently an Assistant Professor with Vasavi Engineering College, Tadepalligudem, India. His research interests include multilevel inverters, high power factor converters, grid integration of renewable energy systems, and power electronics.

YANNAM RAVI SHANKAR was born in July 1986. He received the B.Tech. degree in electrical and electronics engineering from the Prakasam Engineering College, JNTU Hyderabad, Andhra Pradesh, India, in 2008, and the M.Tech. degree in power and industrial drives from JNTU Kakinada, India, in 2011. He was an Assistant Professor with SSN Engineering College, Ongole, Andhra Pradesh, India, for two years. He is currently an Assistant Professor with Dire Dawa University, Dire Dawa, Ethiopia. His research interests include power electronics, power systems, advanced control systems, and electrical machines.

JAMI RAJESH received the B.Tech. degree in electrical and electronics engineering from Jawaharlal Nehru Technological University, Hyderabad, India, in 2007, the M.E. degree from the Andhra University College of Engineering, Visakhapatnam, in 2012, and the Ph.D. degree from the National Institute of Technology (NIT) Andhra Pradesh, India, in 2022. His research interests include multilevel inverters, high-power factor converters, and power electronics.

V. GOURI PRASANT received the B.Tech. degree from Pondicherry University, Pondicherry, India, in 2018. He is currently pursuing the M.Tech. degree in power electronics and drives with the National Institute of Technology Andhra Pradesh, Tadepalligudem, India. His research interests include multilevel inverter topologies, electric vehicles, pulse width modulation techniques, grid integration of renewable energy systems, and motor drives and control.