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RESEARCH ARTICLE

An Improved Protection Circuit Design for Fast Detection of Short-Circuit in IPM

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ABSTRACT Short-circuit protection plays a vital role in ensuring the overall reliability of intelligent power module (IPM), where the shorter the duration of a short-circuit fault, the smaller its impact on the module. The conventional V_{CE} desaturation detection circuit suffers from a blanking time problem. This paper aims to solve this problem by improving the IPM short-circuit fast detection and protection circuit with integrated shunts in order to achieve ultra-fast detection and protection of the IPM short-circuit faults. At the same time, the number of shunts is decreased from three to two, which reduces the impact on the power density of the device. First, the types of IPM short-circuit faults and the experimental principle of a short-circuit are introduced in this paper. Second, the overcurrent fault protection of the improved circuit with the shunts integrated at different positions in the IPM power unit is analyzed and verified using the PSPICE simulations. Third, a method for selecting the component parameters of a compensation link of the improved circuit is proposed, and the functions for the remaining parts in the circuit are introduced. Last, it is verified through experiments that the improved circuit can quickly detect various short-circuit faults, and initiate the corresponding shutting down of the insulated gate bipolar transistor (IGBT) after 490 ns. Compared with the conventional V_{CE} desaturation detection method, the detection time of the proposed method and the associated short-circuit loss for modules under different short-circuit faults are significantly reduced.

INDEX TERMS Insulated gate bipolar transistor (IGBT), intelligent power module (IPM), short-circuit detection and protection, shunts.

I. INTRODUCTION

With the rapid development of insulated gate bipolar transistors (IGBTs) and the related drive protection technology, use of an intelligent power module (IPM) consisting of an IGBT power unit, drive protection part and heat sink is also becoming popular. Compared with the conventional IGBT devices, the IGBT IPMs do not require bulky supporting drive protection circuits, improve the integration inside the module, and are simpler to install. These features reduce the user's difficulty and shorten the development time for the whole system, along with significant improvements in performance and reliability [1]. As the IPMs are used in critical applications, such as household appliances, inverter control, switching power supplies, wind power generation, photovoltaic power generation and electric vehicles, it is highly crucial to study the fast detection and protection of IPM short-circuit faults [2].

The research on IGBT short-circuit protection technology indicates that the tunnel magnetoresistance (TMR) based on the Wheatstone bridge can be utilized to measure the collector-emitter current I_C of the IGBT [3]. This method is applicable to the IPM, and only needs to increase the TMR outside the IGBT for the measurement of I_C. Nevertheless, experiments were carried out on only one type of short-circuit in the reported work, where the protection action time was 1.23 μs, which clearly indicated that the method was desirable but had a few limitations.

In another work [4], a gate voltage detection protection circuit was proposed that could simultaneously detect various short-circuit faults. The reported method was capable of detecting two types of short-circuit faults in 0.6 μs and 0.5 μs, respectively, without changing the internal structure of the module. However, the design of the detection circuit

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was complex that increased its volume, which was not conducive to the integrated applications in IPMs. Another commonly used method is the di_C/dt detection method, which relies on detecting the rate of change of the collector current. Although this method can rapidly detect different short-circuit faults, it cannot be integrated in IPMs due to the non-existence of Kelvin emitters in IPMs [5], [6], [7].

The authors in [8] designed a detection protection circuit without blanking time based on internally integrated shunts inside the IPM. This method only required setting of the threshold voltage corresponding to the current I_C of the detection circuit in order to achieve fast detection of different short-circuit faults. Accordingly, in this paper, an improved fast detection protection circuit is designed based on the method reported in [8].

The rest of this paper is organized as follows: Section II introduces the principle of short-circuit experiments and analyzes the short-circuit waveform. This is followed by an analysis of the principle and problems of the conventional V_{CE} desaturation detection circuit currently used for IPMs. Furthermore, the principle and application of the shunts detection method are also introduced in this section. In Section III, the short-circuit fault detection of the integrated shunts at different positions inside the IPM power unit is analyzed and simulated. Correspondingly, an improved protection circuit is proposed for fast detection of short-circuits based on the internally integrated shunts. In Section IV, a double-pulse test platform is built to verify the effect of the compensation link of the detection circuit. Similarly, a short-circuit test platform is developed to test the detection time of the short-circuit current, the delay time of the protection circuit action, and the fault duration of the overall circuit under different short-circuit faults. Last, the short-circuit fault detection time, protection action time and short-circuit loss obtained in this work are compared with those obtained using the conventional V_{CE} desaturation protection method to verify the reliability and superiority of the proposed design.

II. IPM SHORT-CIRCUIT TYPES AND THE CONVENTIONAL PROTECTION METHOD

A. IPM SHORT-CIRCUIT TYPES

The short-circuits in IPM can be divided into two types [9], [10], [11] according to the related size of inductance in the short-circuit loop. The first type is a phase to phase short or relative to ground short with a large inductance usually at the μH level [12], [13]. For such faults, the device under test (DUT) is shorted during the conduction, and this type of short-circuit is known as a fault under load (FUL) [14], [15]. The second type of short-circuit corresponds to the straight-through short-circuit in bridge arm with a small inductance, usually around 100 nH [16]. In this case, the straight-through short-circuit occurs in a bridge arm before the DUT is turned on, and is known as a hard switching fault (HSF).

The FUL occurs when the IGBT is in the on-state. Its core features are a long short-circuit loop path, a large inductive reactance, and a relatively slow rise in the short-circuit current. The collector current begins to rise after the short-circuit occurs, where the rate of this rise is determined by the short-circuit impedance and the DC bus voltage. Once the current rises to a level determined by the IGBT transconductance and the gate voltage V_{GE}, the IGBT begins to exit the saturation region. Furthermore, the collector voltage V_{CE} begins to rise. Simultaneously, V_{GE} begins to rise due to the displacement current generated by the Miller capacitance. This rise causes the collector current to increase that eventually manifests as a large collector current overshoot, leading to the IGBT failure. The above analysis shows that in the absence of a shutdown signal, the IGBT exits the saturation region and the V_{CE} rises above the safety threshold, which can be used as the characteristic signal of FUL. The relationship between the collector voltage V_{CE} and collector current I_C also follows the output characteristic curve of IGBT, and the safety threshold voltage can be set according to the ability of IGBT to withstand the short-circuit current.

The HSF occurs when the IGBT is in the off state. The collector current will rise sharply if the IGBT is turned on in this short-circuit state. The current level is determined by the characteristics of the gate driver and the IGBT transconductance. The core features of HSF are: 1) small short-circuit path, 2) low inductance, and 3) rapid increase of short-circuit current. Compared with the FUL, the hard short-circuit fault state requires a faster detection method in order to timely limit the short-circuit current. In this fault state, the collector-emitter voltage drops rapidly and then rises to the DC bus voltage level again. Its change trend no longer follows the process of exiting the saturation region, therefore, the collector voltage used to detect soft short-circuits does not necessarily meet the conditions of hard short fault detection.

In practical applications, FUL is the most difficult fault to deal with. The schematic diagram of FUL test is shown in Fig. 1(a). The bus voltage increases to the required voltage in this experiment. The lower IGBT serves as the DUT and an air-core inductor L_1 serves as the short-circuit inductor. The FUL will occur when a single pulse signal of 10 μs is applied to the lower IGBT.

The schematic diagram of the HSF test is shown in Fig. 1(b). The bus voltage is increased to the required voltage in the experiment. The lower IGBT serves as the DUT, while the upper IGBT is shorted by a thick short copper bar. When a single pulse signal of duration 10 μs is applied to the lower IGBT, the upper and lower bridge arms are directly connected to create the HSF.

The relevant FUL and HSF simulation waveforms are shown in Figs. 2 and 3, respectively.

The normal switching process of an IGBT is similar to that of a MOSFET device. The only exception is the presence of residual carriers in the turn-off process that exhibit the tail current phenomenon. This phenomenon gets more severe as the bus voltage decreases. The authors in [17] described normal turn-on and turn-off waveforms for an IGBT. In the following, the FUL waveform is presented first.

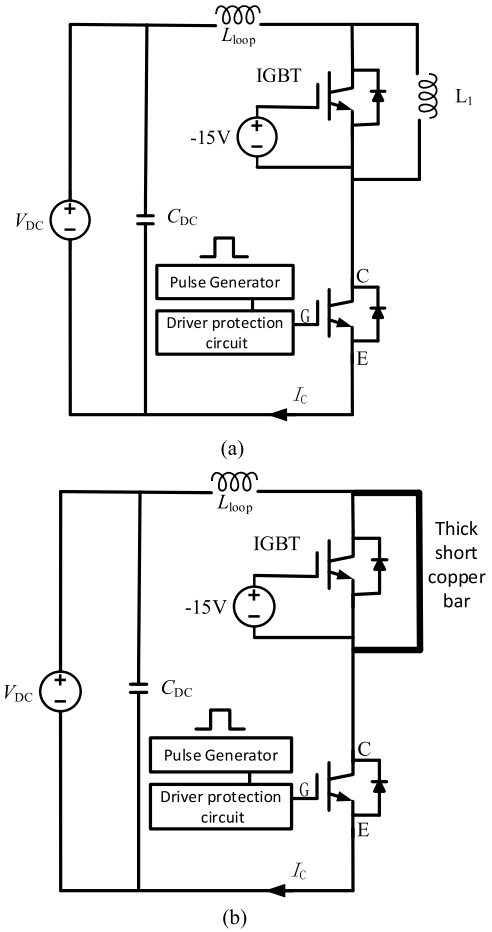

FIGURE 1. Schematic diagrams of test experiments. (a) FUL test circuit diagram. (b) HSF test circuit diagram.

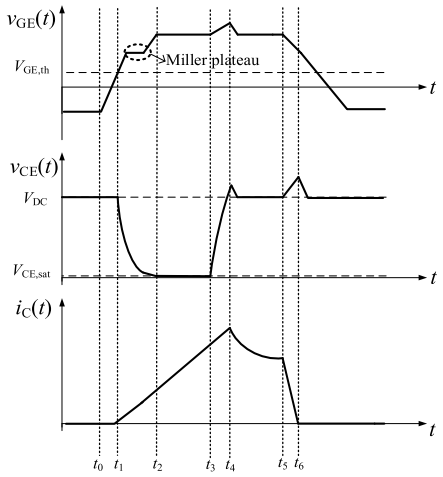

FIGURE 2. Waveform under FUL.

1) t_0-t_1 stage: Gate current I_G charges the parasitic input capacitance C_{GE} and C_{GC}, and V_{GE} increases exponentially with the time constant of R_G ($C_{GE} + C_{GC}$). In this region, V_{CE} remains at V_{DC} because the collector current I_C does not flow through the IGBT. Changes in the Miller capacitance C_{GC} and gate capacitance C_{GE} will affect the switching characteristics of the IGBT [18]. An increase in C_{GE} will increase I_G, which will slow down dic/dt without affecting dv_{CE}/dt. Furthermore, it will suppress the reverse recovery current peak and bus overvoltage during turn-on and turn-off, respectively. Similarly, the use of additional C_{GC} can slow down dv_{CE}/dt without affecting dic/dt; but an increase in C_{GE} and C_{GC} will increase the power consumption of the driving circuit. It should be noted that when dv_{CE}/dt is adjusted by using an additional C_{GC}, it must be ensured that its withstanding voltage value is considerably higher than the IGBT bus voltage.

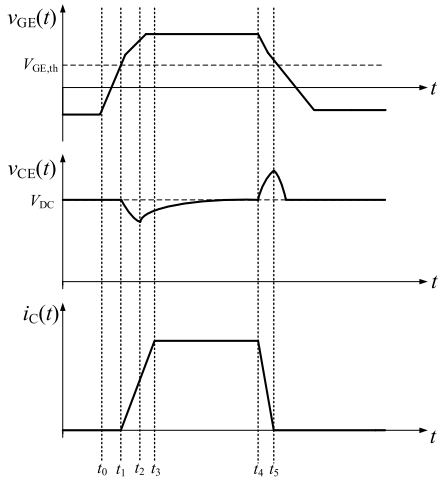

FIGURE 3. Waveform under HSF.

2) t_1-t_2 stage: At the moment t_1, the gate voltage V_{GE} reaches the device conduction threshold voltage $V_{GE,th}$. In addition, the P-region below the oxide layer of the device forms an anti-pattern conductive channel, creating a pathway for the movement of electrons. At this stage, due to the large nductance in the short-circuit, I_C increases with a positive slope dic/dt and V_{CE} begins to fall rapidly below the bus voltage. At the moment t_2, V_{CE} decreases to the saturation conduction voltage $V_{CE,sat}$, and the device enters the saturation region. As the gate current starts to charge the Miller capacitor C_{GC}, the Miller plateau appears at this stage of V_{GE}.
3) t_2-t_3 stage: During this phase, the device operates in the saturation region where the gate voltage is stable, and I_C increases linearly. The device is always in this stage when it is in the normal conduction state, and the current will increase linearly according to the size of the load inductance. However, the current will only increase to near the rated current value due to the presence of the load. Therefore, the loss is small when the device works in a saturated conduction state.
4) t_3-t_4 stage: At the moment t_3, I_C generally increases to about four times the rated current, and V_{CE} starts exiting the saturation zone and rises rapidly to the peak value. Meanwhile, the displacement current i_{GC} appears at the gate of IGBT under the influence of Miller capacitor C_{GC} and dV_{CE}/dt, resulting in a

voltage spike in V_{GE}. The rise in gate voltage will cause an I_C overshoot, where the IGBT is very likely to exhibit the Prime effect and failure phenomenon. The i_{GC} can be expressed by (1) as follows:

$$i_{GC} = C_{GC}\frac{dv_{CE}}{dt} \tag{1}$$

5) t_4-t_5 stage: The current I_C stops increasing and there is no longer any voltage on the short-circuit inductor L. The IGBT enters the short-circuit mode from the saturation mode. The value of V_{CE} drops to the supply voltage V_{DC}, and I_C starts to reduce to a static stable value.
6) t_5-t_6 stage: At the moment t_5, the device starts to shut down, V_{GE} starts decreasing, and the conductive channel is completely clamped off. Moreover, I_C starts to decrease significantly due to the combined effect of the high rate of change of current and the stray inductance of the short-circuit. Here, V_{CE} exhibits a spike in the shutdown voltage, and subsequently decreases continuously to a value close to V_{DC}. Accordingly, at the moment t_6, I_C drops to zero and the device is shut down completely.

Furthermore, the analysis of HSF test waveform shown in Fig. 3 is similar to that in Fig. 2, except that the short-circuit inductance for HSF is very small. Thus, the device does not exhibit any saturation conduction, and V_{CE} only decreases slightly and then stabilizes back around the V_{DC} value. The variation in V_{CE} is not significant, and the V_{GE} spike and I_C overshoot do not appear as in the FUL case. Therefore, the device generates more hazards in the FUL case than in the HSF case [19], [20].

B. CONVENTIONAL SHORT-CIRCUIT PROTECTION METHOD FOR IPM

The V_{CE} desaturation detection method corresponds to the conventional short-circuit protection method in IPM. This method exploits the fact that the device exits the saturation region in the FUL state, where the voltage V_{CE} starts increasing to V_{DC} from the on-state saturation voltage drop of $V_{CE,sat}$. The working principle behind this method is that the short-circuit current rises sharply after a short-circuit fault occurs, and the junction temperature of the IGBT also rises accordingly. As the impedance of the IGBT has a positive temperature coefficient, it will exit from the fully conductive state at this time and enter the active area to complete the exit saturation process. When the short-circuit is detected, the driver evaluates the desaturation process of the IGBT based on the collector voltage, thereby detecting the short-circuit fault.

The V_{CE} desaturation detection circuit principle is presented in Fig. 4. After the driver chip IC receives the lead signal from the pulse generator, the switch V_{Ta} is turned off and the current source I_b starts to charge the capacitor C_b. At this stage, the comparator does not detect the collector emitter voltage V_{CE} of the device. This period is known as

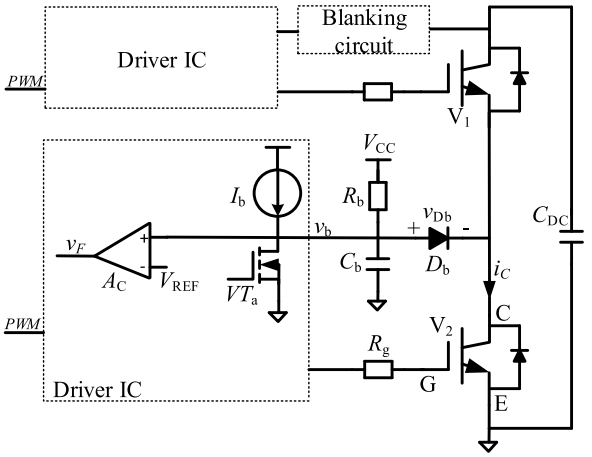

FIGURE 4. Conventional V_{CE} desaturation detection.

the blanking time of the detection circuit. The typical value of V_{REF} is 7-9 V, which can be obtained using the mathematical expression given in (2), where V_{CC} is the drive supply voltage and v_{Db} is the diode D_b forward conduction voltage drop. The blanking time t_b for the conventional V_{CE} desaturation detection is determined by the blanking capacitor C_b, the resistor R_b, the driving voltage V_{CC}, the current source I_b, and the reference voltage V_{REF}. Moreover, it can be mathematically expressed by (3).

$$\left(V_{CE,sat} + V_{Db}\right) < V_{REF} < V_{CC} \tag{2}$$

$$t_b \approx \frac{V_{REF} \cdot R_b C_b}{V_{CC} + I_b R_b} \tag{3}$$

The existence of the blanking time of detection circuit is caused by the normal saturation conduction, which occurs during both the normal conduction and the FUL state of the device. Likewise, the corresponding blanking time is set to avoid the mis-operation of the protection circuit during normal operation of the device. A margin is usually left based on this time that is generally set to a few μs. For the IGBTs with a high blocking voltage (starting from 3.3 kV), the time required prior to the saturation conduction is longer, thus indicating a larger corresponding blanking period. The presence of blanking time in conventional V_{CE} desaturation detection causes the device to suffer from longer short-circuit shocks in the HSF and FUL states, thereby inducing higher short-circuit losses in the device. The authors in [21] proposed a V_{CE} desaturation detection circuit to solve this short-circuit loss problem caused by the blanking time. This circuit could adaptively adjust the detection blanking time according to the period length of the device saturation conduction, thus significantly reducing the time of the protection action in the FUL state. However, the design of such detection circuit is complex, large and costly, and hence it is difficult to integrate it in the IPM.

The desaturation detection circuit also has certain limitations. The currently used mainstream high-power IGBT devices can generally withstand a maximum short-circuit current of 10 μs. Thus, a short-circuit fault should be detected

and shut down within 10 μs at most. However, the response time of the V_{CE} desaturation detection method is almost equal to the maximum withstand time of the IGBT, and there is a risk of damage. Furthermore, a short-circuit fault in the IGBT is not necessarily accompanied by a desaturation process within 10 μs. Therefore, relying solely on the desaturation circuit is not sufficient to detect all short-circuit fault states within 10 μs, which is not conducive to fault detection and protection.

To address the aforementioned issues, an improved fast short-circuit protection method is proposed in this paper, which fundamentally relies on the internally integrated shunts detection method. The shunts detection method involves a low parasitic inductance in series with the load current circuit of the IGBT. The load current passing through the resistor generates a corresponding voltage drop. Therefore, it is necessary to design the relevant voltage detection protection circuit to protect the IGBT from a short-circuit. A limitation of the shunts detection method is the introduction of additional losses in the circuit. On the other hand, the advantages linked to this method are simple circuit design, fast protection response, near-zero blanking time, and complete protection against the HSF, FUL and overcurrent fault conditions.

The shunts detection method can be divided into two categories, i.e., the internal integrated shunts detection method and the external shunts detection method. The latter method corresponds to adding resistance outside the discrete device and designing additional detection and protection circuits. As the voltage and current levels of the discrete devices are relatively small, this method requires a relatively simple detection and protection circuits design, where the effect of increased external resistive losses on the internal device can be ignored. On the other hand, the internal integrated shunts detection method requires lower values of shunt resistance and parasitic inductance to reduce the impact of the integrated shunts on the turn-on/turn-off waveforms and power density of the device. The advantages of this method are its utility in large-scale integration applications, and its suitability for medium/high voltage and high current power modules.

This paper improves the fast detection protection circuit designed in [8], which proposes to integrate three shunts inside the IGBT based on the internally integrated shunts of the IPM. The circuit could quickly detect both HSF and FUL, and achieve better detection speed and short-circuit loss compared to conventional detection circuit. However, following the detection of a short-circuit fault, there is a delay period of around 1 μs before the protection circuit starts operating, which causes additional short-circuit losses to the device. Hence, the reported circuit should be improved. In order to verify the effectiveness of the internal integrated shunts detection method for detecting the HSF, FUL and load overcurrent faults under actual operating conditions of the IPM, we present a theoretical analysis and PSPICE simulation in the following that validates the overcurrent detection of the shunts at different locations.

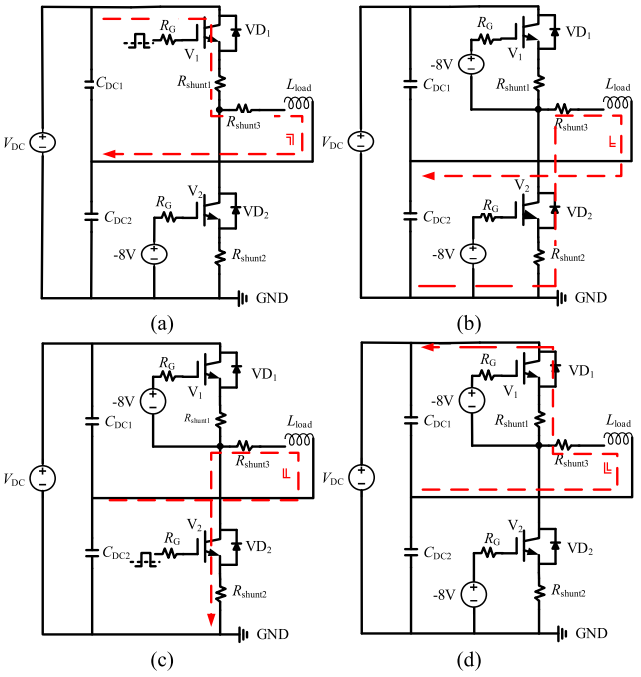

FIGURE 5. Half-bridge inverter circuit principle: (a) V_1 turned on, V_2 turned off; (b) V_1 turned off, VD_2 turned on; (c) V_2 turned on, V_1 turned off; (d) V_2 turned off, VD_1 turned on.

III. CIRCUIT DESIGN AND SIMULATION

A. ANALYSIS AND SIMULATION VERIFICATION

The IPMs can be divided into H-type (one internal IGBT), D-type (two internal IGBTs, half bridge), C-type (six internal IGBTs, three-phase bridge) and R-type (seven internal IGBTs), depending on the number of IGBT modules packaged in them. Out of these types, the analysis of the module packaged as an IGBT half-bridge is particularly important, and forms the basis for the C-type and R-type IPMs. Therefore, this paper starts with the simulation analysis of short-circuit fault detection in the inverter circuit of the IGBT half-bridge module for different shunt positions. Fig. 5 demonstrates the actual operation principle of the half-bridge inverter circuit. To complete the simulation of fault detection for the shunts at different positions of the half-bridge module, the shunts R_{shunt1}, R_{shunt2} and R_{shunt3} are added to the corresponding positions of the half-bridge module in Fig. 5. There are four operating states in the actual operation of the half-bridge circuit:

1) The upper bridge arm V_1 is turned on and the lower bridge arm V_2 is turned off, as shown in Fig. 5(a). The capacitor C_{DC1} supplies the inductive load through circuit 1.
2) The upper bridge arm V_1 is off, as shown in Fig. 5(b). The current cannot change its direction immediately due to presence of the inductor. Therefore, VD_2 conducts to renew the current through circuit 2 until the current drops to zero.
3) The lower bridge arm V_2 is turned on, as shown in Fig. 5(c). The capacitor C_{DC2} supplies the inductive load through circuit 3.

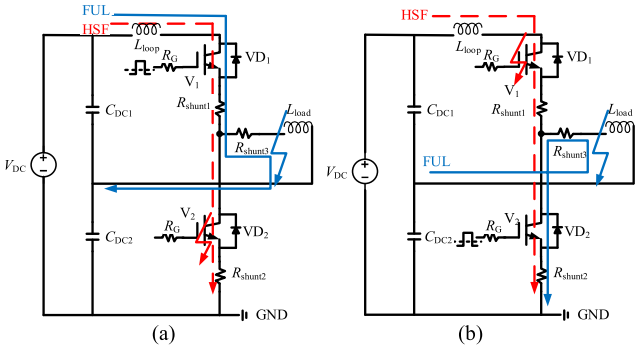

FIGURE 6. Half-bridge inverter circuit short-circuit fault: (a) V_1 under HSF and FUL; (b) V_2 under HSF and FUL.

4) The lower bridge arm V_2 is turned off, as shown in Fig. 5(d). As the direction of the current flowing through an inductor cannot change abruptly, VD_1 conducts and continues the flow of current through loop 4 until the current drops to zero.

In the half-bridge inverter circuit, the upper and lower bridge arms are straight that correspond to the HSF state, and the shorted load corresponds to the FUL state. Fig. 6 shows the failure principle.

Next, the short-circuit fault principle of the half-bridge inverter circuit presented in Fig. 6 is analyzed. The analysis shows that for the HSF state of V_1, V_2 is already on before V_1 is on, and the short-circuit current will flow through R_{shunt1} and R_{shunt2}. Furthermore, in the FUL state of V_1, the load is short-circuited when V_1 is on, and the short-circuit current will flow through R_{shunt1} and R_{shunt3}. Moreover, the HSF and FUL states of V_2 are identical. The short-circuit current in HSF state flows through R_{shunt1} and R_{shunt2}, while the short-circuit current in FUL state flows through R_{shunt2} and R_{shunt3}. Furthermore, the detection of load overcurrent is consistent with the FUL state.

The HSF states, FUL states and the load overcurrent are simulated using PSPICE for verifying the actual operation of IGBT half-bridge module in an inverter circuit. Fig. 7 shows the waveforms of HSF, FUL and load overcurrent simulations for upper bridge arm V_1 and lower bridge arm V_2 of IGBT, respectively.

Parasitic inductance in the loop is set to 50 nH for the HSF state simulation, and the parasitic inductance is set to 1 μH for the FUL state simulation. The normal inductive load L_{load} is set to 20 μH, the resistance R_{shunt} of the shunts is set to 0.34 mΩ, the bus voltage V_{DC} is set to 600 V, and the bus capacitances C_{DC1} and C_{DC2} are both set to 1000 μH. The simulation results show that R_{shunt1}, R_{shunt2} and R_{shunt3} detect the upper and lower bridge arm faults of the half-bridge circuit, as illustrated in Table 1.

The results shown in Fig. 7 demonstrate that both R_{shunt1} and R_{shunt2} can detect the HSF if it occurs in V_1 or V_2 during the actual operation of an IGBT half-bridge module. Similarly, both R_{shunt1} and R_{shunt3} can detect the FUL or

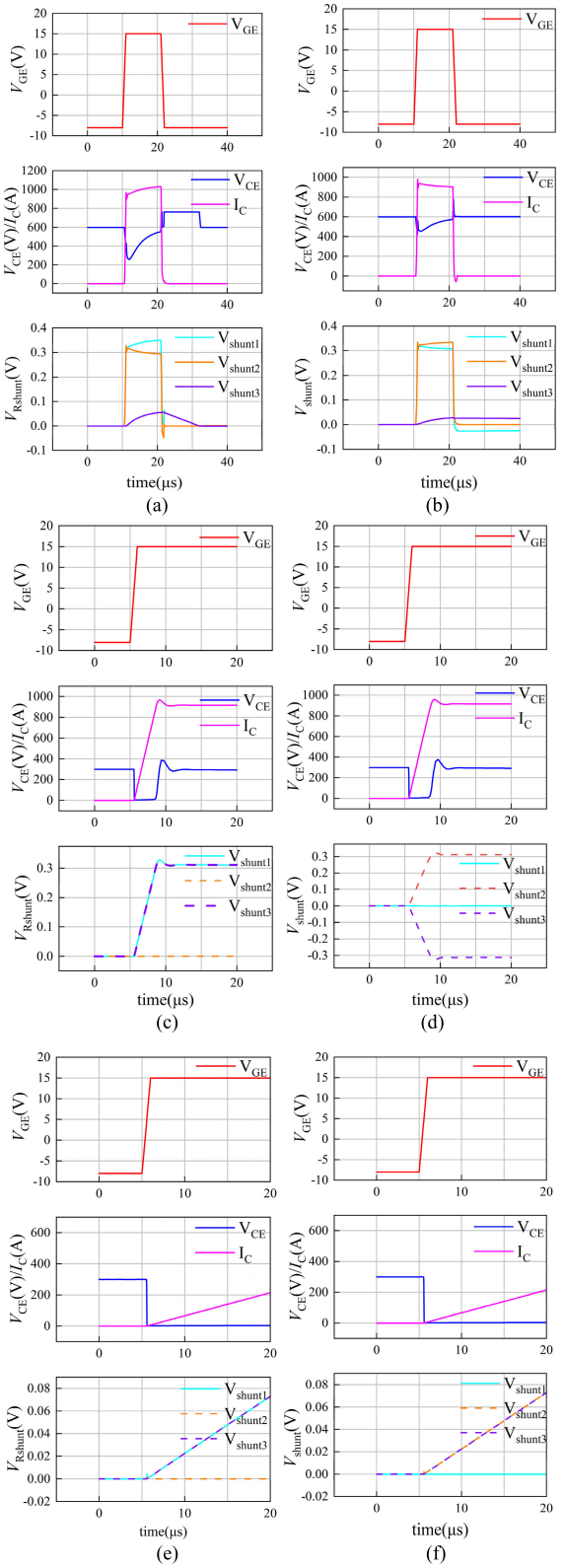

FIGURE 7. Simulation of IGBT's upper and lower bridge arms short-circuit fault and load overcurrent: (a) HSF waveform of upper bridge arm V_1; (b) HSF waveform of lower bridge arm V_2; (c) FUL waveform of upper bridge arm V_1; (d) FUL waveform of lower bridge arm V_2; (e) Load overcurrent waveform of upper bridge arm V_1; (f) Load overcurrent waveform of lower bridge arm V_2.

TABLE 1. Detection with shunts for different overcurrent faults.

State	R_{shunt1}	R_{shunt2}	R_{shunt3}
HSF state (V_1)	√	√	×
HSF state (V_2)	√	√	×
FUL state (V_1)	√	×	√
FUL state (V_2)	×	√	√
Load overcurrent (V_1)	√	×	√
Load overcurrent (V_2)	×	√	√

load overcurrent if it occurs in V_1. Lastly, both R_{shunt2} and R_{shunt3} can detect the FUL or load overcurrent if it occurs in V_2. The obtained simulation results are consistent with the analysis provided in Fig. 6, which validates the reliability of the analysis. In summary, it can be observed that only two shunts are required to be integrated as R_{shunt1} and R_{shunt2} in order to detect all the faults in the actual operation of an IGBT half-bridge module. Compared with the integration of three shunts inside the module as proposed in [8], the corresponding impact on the power density of the device can be potentially reduced by decreasing the number of internally integrated shunts.

B. DETECTION AND PROTECTION CIRCUIT DESIGN

A shunt cannot be a purely resistive element and a parasitic inductance exists in it. Therefore, the shunt element is equivalent to a resistor R_s and an inductor L_σ connected in series. Fundamentally, the current passing through a shunt produces a voltage drop across it, which can be mathematically expressed as follows:

$$U_{\text{shunt}} = R_s i_C + L_\sigma \frac{di_C}{dt} \tag{4}$$

It can be gathered from (4) that owing to the presence of the parasitic inductance, the voltage will oscillate and spike when the IGBT is turned on or turned off. Subsequently, the voltage can be compensated through an RC compensation network. The selection criteria for R_{comp} and C_{comp} in a compensation network are given in (5). If the product of R_{comp} and C_{comp} satisfies (5), there is no distortion between the measured and actual voltages. However, if the product is greater than the left side of (5), an overcompensation phenomenon will occur, and vice versa, which will result in an under-compensation [8].

$$\frac{L_\sigma}{R_s} = R_{comp} \cdot C_{comp} \tag{5}$$

In the PSPICE simulation circuit, the values of R_s and L_σ for R_{shunt} are set as 0.34 mΩ and 0.2 nH, respectively. The value of R_{comp} for the compensation circuit is set to 1 kΩ, while the current flowing through the shunt is set to a maximum 200 A square wave current signal. Using (5), C_{comp} of the compensation network is calculated as 600 pF. Two additional values for C_{comp} are also selected, i.e., 1 nF and 300 pF, in order to comparatively analyze the effects of C_{comp}. The compensation circuit principle and the simulated waveforms are shown in Figs. 8 and 9, respectively.

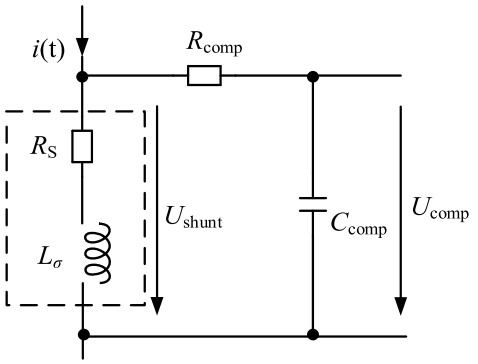

FIGURE 8. Compensation circuit principle.

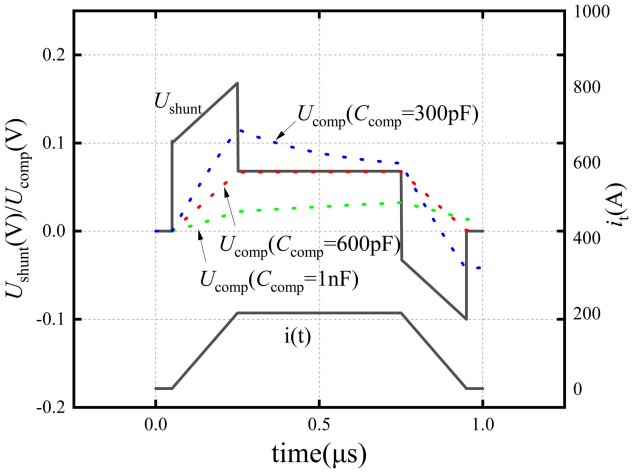

FIGURE 9. Compensation circuit simulation results.

Fig. 9 shows that 1) when C_{comp} is 300 pF, the circuit is in the under-compensation state; 2) when C_{comp} is 1 nF, the circuit is in the over-compensation state; 3) when C_{comp} is 600 pF, there is no distortion between the measured and actual signals. It can be concluded that the key to accurately selecting the parameters R_{comp} and C_{comp} in a compensation circuit is to determine the parasitic inductance of the shunt L_σ. Generally, the parasitic inductance of a shunt is around a few nH. If its specific value is known, it can be directly substituted in (5) to extract the parameters of the compensation circuit.

Nevertheless, it is necessary to calculate the parameters of the shunt if they are not clear or if multiple shunts are used in parallel. In this work, the parasitic inductance of the shunt is estimated using (6) based on the influence of shunt's parasitic inductance on the U_{shunt} waveform. The aforementioned equation estimates the parasitic inductance by utilizing the rate of change of current in a rise or fall process, and the amount of overshoot and fall in U_{shunt} caused by the superposition of parasitic inductance. The corresponding equation can be expressed as

$$\Delta U_{\text{shunt}} = L_\sigma \frac{di}{dt} \tag{6}$$

where ΔU_{shunt} is the change in voltage across R_{shunt} during the rise or fall of current (V), L_σ is the parasitic inductance of

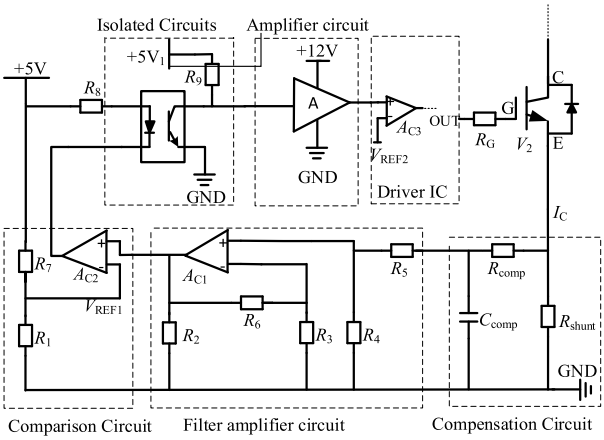

FIGURE 10. Improved IPM short-circuit fast detection and protection circuit.

R_{shunt} (μH), and di/dt is the rate of change of current flowing through R_{shunt} (A/μs).

In simulations, the voltage overshoot ΔU_{shunt} during the current rise is 200 mV, where the current rises from 0 A to 200 A in 200 ns at a current change rate of 1 A/ns. Using (6), L_σ is calculated to be 0.2 nH, which is the same as the inductive parameter of the shunt. Note that the simulated waveform is an ideal waveform, and the size of the parasitic inductance for the actual waveform can only be estimated using (6) in order to narrow down the parameter range for the compensation circuit.

In order to ensure the availability of the output signal U_{comp} (mV level) from the compensation circuit so that short-circuit fault protection can be achieved, an improved circuit for the fast detection and protection of short-circuit current is designed in this work. This circuit is elaborated in Fig. 10.

The collector current I_C produces a corresponding voltage drop when it flows through the shunt R_{shunt}. Initially, the measured voltage signal is compensated by the RC compensation circuit, where it is at mV level after compensation. Hence, the amplification factor of amplifier A_{C1} must be adjusted according to the device data sheet. Next, the amplified voltage is compared with V_{REF1} setting using a high-speed comparator A_{C2}. Furthermore, the high- and low-level signals from the comparator output are isolated, amplified and sent to the driver chip IC. The threshold voltage V_{REF1} is determined by the maximum value of the permitted collector current $I_{\text{C,max}}$. When the amplified voltage is larger than the threshold voltage V_{REF1}, the high-level output signal of A_{C2} is isolated and amplified to 12 V, which is larger than the set threshold voltage V_{REF2} (9 V) of the comparator A_{C3} integrated inside the driver chip 1ED020I12FA2.

Here, the driver changes the output to a value of -8 V in order to turn off the switching devices, and the output state is locked to avoid the re-conduction of switching devices and reduce any short-circuit loss. Alternatively, if the amplified voltage is lower than the threshold voltage V_{REF1}, the output of the comparator A_{C2} is a low-level signal. This signal remains at a low level (less than V_{REF2}) after isolation and

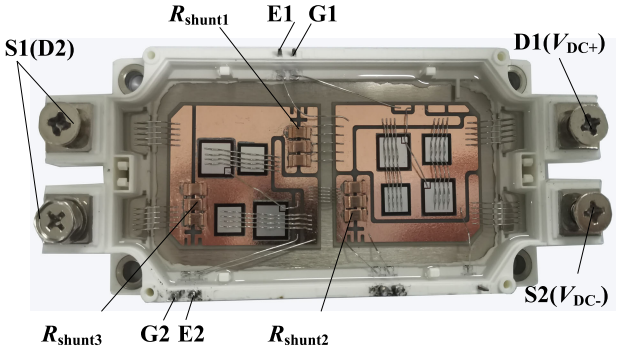

FIGURE 11. IPM power unit with internally integrated shunts.

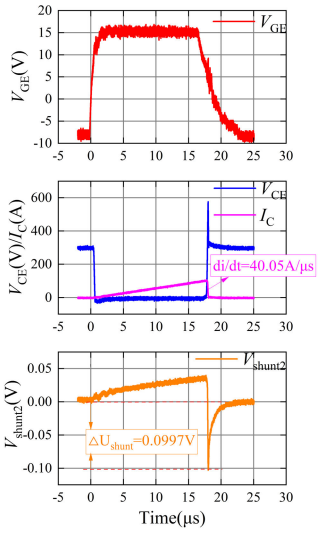

FIGURE 12. Waveform under single-pulse test.

amplification, and hence the driver circuit works normally. It can be concluded by analyzing the circuit that the improved protection circuit for the fast detection of short-circuit faults can be tailored for IPMs of different power levels by a simple adjustment of the parameters of the compensation circuit, amplification of A_{C1}, and adjusted threshold voltage V_{REF1} of A_{C2}.

IV. EXPERIMENTAL VERIFICATION

A. DOUBLE PULSE TEST

An IPM power unit with a voltage level of 1200 V and a rated current of 100 A is prototyped based on an internally integrated shunt. The location of the integrated shunt of the IPM power unit used in [8] is shown in Fig. 11.

In order to verify the effect of compensation circuit on the fast short-circuit detection circuit, a double-pulse test platform is built to conduct single-pulse and double-pulse experiments on the IPM power unit with two internally integrated shunts. To ensure high performance of the detection circuit, the parameters of each part of the proposed circuit are adjusted according to the waveform shown in Fig. 12. The test is performed for the lower bridge arm V_2, where the bus voltage is set to 300 V, and the inductance of the inductor parallel to the upper IGBT is equal to 200 μH. The shunt

TABLE 2. Parameters of the shunts.

Parameters	Value
Resistance value /mΩ	1
Resistance value accuracy /%	1
Power /W	3
Self-inductance /nH	<10
Rated current /A	78
Spike current /A	390
Temperature drift /(10^{-6}·K-1)	<50
Temperature drift error /%	0.5

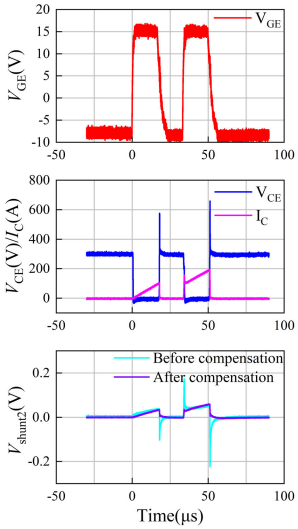

FIGURE 13. Waveform under double-pulse test.

voltage is chosen to test the voltage across R_{shunt2}. Moreover, the internally integrated shunt is composed of three resistors connected in parallel, where the resistance value of each resistor is 1 mΩ. The resistor parameters are shown in Table 2. The shunt resistance after parallel connection is calibrated to 0.34 mΩ using a method proposed in [8].

The authors in [22] and [23] described the principle of the double-pulse test: the shunt resistance is very low, and the voltage across it can represent the value of I_C flowing through it, where the voltage waveform of R_{shunt2} must be the same as the waveform of current I_C through the resistor. According to this principle, the rate of change of the current I_C and the corresponding voltage drop of the shunt ΔU_{shunt} are calculated using the single-pulse experimental test waveform shown in Fig. 12.

Next, the required values are substituted in (6) to calculate the equivalent parasitic inductance of the shunt R_{shunt2} as 2.4 nH. Additionally, R_{comp} of the compensation circuit is set to 1 kΩ and thus, the value of C_{comp} is estimated as 7 nF. Fig. 13 shows the output waveform of the double pulse experimental test and the waveform of the shunt before and after compensation. The current I_C reaches a value of 100 A at the end of the first pulse. The shunt resistance is 0.34 mΩ, while the voltage across the shunt R_{shunt2} at this time is 34 mV, which clearly indicates that there is no distortion in the voltage signal and the relevant requirements are satisfied. Note that in order to avoid any distortion of the output waveform of the compensation circuit after the estimation of C_{comp} based on (6), a fine-tuning of the capacitance value is required in the actual circuit.

B. SHORT-CIRCUIT TEST

The short-circuit loss of the module is irreversible, which reduces its reliability. Thus, it is necessary to devise a fast short-circuit protection method to improve its service life and reliability. A short-circuit fault in the IPM causes a large current flow in the circuit. Accordingly, a current threshold is set in the detection circuit. The device is turned off when the current exceeds this threshold. The threshold can be adjusted without affecting the shunt and the normal operation of the IPM. In this paper, the most commonly used V_{CE} desaturation circuit is utilized for the comparison experiments. The large blanking time of V_{CE} desaturation circuit (4 μs) in the HSF is due to the simultaneous identification of both HSF and FUL short-circuit faults. If the blanking time is set as too short, a Class II short-circuit will not be identified. As the device will conduct normally when a Class II short-circuit occurs, it will only enter the short-circuit mode if the current through it increases to a certain value.

In order to test the effectiveness of the improved short-circuit protection circuit, the designed circuit is used to conduct short-circuit experiments on the IPM power unit prototype. When the collector current reaches 200 A (two times the rated current), the shunt voltage after compensation is 68 mV. Subsequently, after 20 times amplification by A_{C1}, it is equal to 1.36 V. Therefore, the threshold voltage V_{REF1} of the comparator A_{C2} can be set to 1.4 V. Moreover, the bus voltage V_{DC} is set to 600 V in the short-circuit experiments. The experimental waveforms of the HSF state under the two considered short-circuit protection methods are shown in Fig. 14. Furthermore, after the FUL state occurs, the IGBT first saturates and conducts, and subsequently desaturates when the collector current rises to about four to six times the rated current. The FUL experimental waveforms for the two short-circuit protection methods are shown in Fig. 15.

The short-circuit protection characteristics of the improved method are compared with the commonly used V_{CE} desaturation detection method through results illustrated in Figs. 14 and 15. Table 3 provides the comparison results.

The detection time is defined as the time when the current rises to the set threshold current. It corresponds to the time period $t_1 \sim t_2$ in Figs. 14 and 15. The comparison reveals that the proposed method can quickly detect the short-circuit faults within the detection times of about 400 ns and 1.27 μs for the HSF and FUL states of the device, respectively. In addition, the delay in the action of the protection circuit is only 490 ns once the HSF and FUL states are detected. Meanwhile, the short-circuit fault losses of the device in the HSF and FUL states are 0.173 J and 0.067 J, respectively, with the proposed protection method. These losses are 80.8% and

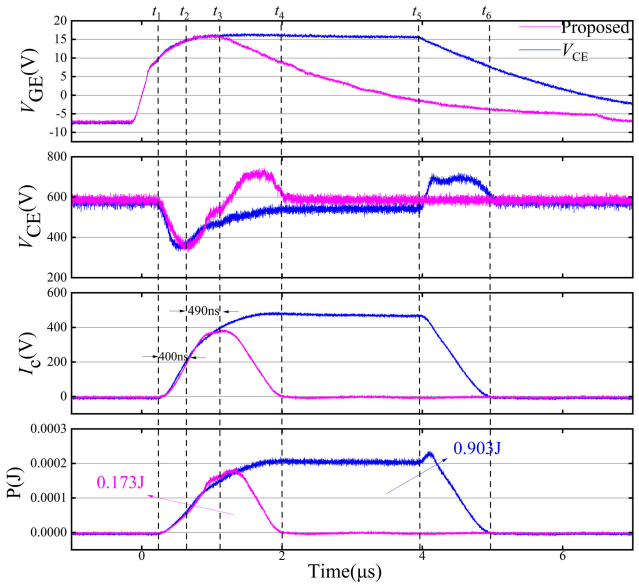

FIGURE 14. Waveforms of HSF test.

TABLE 3. Comparison of short-circuit detection methods.

Characteristics	V_{CE} detection	Proposed method
Drive resistance (turn on, turn off)	2 Ω, 12 Ω	2 Ω, 12 Ω
Time to detect HSF state	4 μs	400 ns (t_1~t_2)
Time to detect FUL state	4 μs	1.27 μs (t_1~t_2)
Delay time of protection action	Around 200 ns	490 ns (t_2~t_3)
Short-circuit loss under HSF	0.903 J	0.173 J
Short-circuit loss under FUL	0.259 J	0.067 J
Method of I_C measurement	Indirectly	Directly
Availability of detection blanking time?	4 μs	No
Whether to change the module structure?	No	Yes

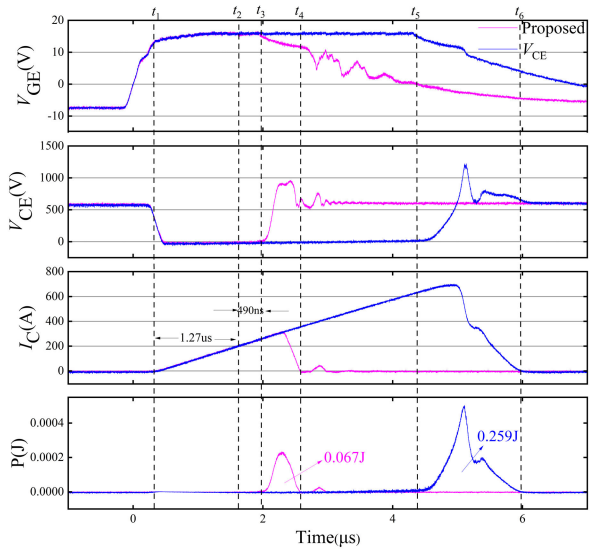

FIGURE 15. Waveforms of FUL test.

74.1% lower than the corresponding short-circuit loss of the V_{CE} desaturation detection method, respectively. Essentially, it can be concluded that the proposed method can significantly reduce the detection time for short-circuit fault and short-circuit loss of IPM.

V. CONCLUSION

The short-circuit protection circuit of IPM significantly impacts its safe and stable operation. In this paper, we analyzed the problem of blanking time of conventional V_{CE} desaturation detection circuit commonly integrated in the IPM. We improved the fast detection protection circuit based on three integrated shunts inside the IPM, as proposed in [8]. First, the influence of integrated shunts on the detection of short-circuit faults and the load overcurrent was verified through theoretical analysis and PSPICE simulations. These shunts were located at different positions inside the IPM power cell. It was demonstrated that all overcurrent faults could be practically detected by integrating only two shunts inside the IPM. This reduction in the number of internally integrated shunts reduced the impact on the power density of the device. Second, an improved short-circuit fast detection protection circuit was proposed based on the internally integrated shunts, and a 1200 V/100 A IPM power unit was prototyped. Last, the effect of compensation link on the proposed protection circuit was verified via double-pulse experiments. In addition, the protective action of the improved circuit and the conventional V_{CE} desaturation circuit in the HSF and FUL states of the device were compared using a short-circuit testbed. These experiments revealed that the improved circuit significantly reduced the detection time, protection action time and short-circuit loss for the HSF and FUL states of the device. Compared with the work in [8], the protection action time was shortened from μs to ns level once the current reached the set threshold current. Such promising results indicated that the improved short-circuit fast detection protection circuit proposed in this work could significantly reduce the short-circuit withstanding time of the IGBTs, and provide a more effective method for the fast detection and protection of short-circuit faults in IPMs.

REFERENCES

[1] N. Iwamuro and T. Laska, "IGBT history, state-of-the-art, and future prospects," *IEEE Trans. Electron Devices*, vol. 64, no. 3, pp. 741–752, Mar. 2017, doi: 10.1109/TED.2017.2654599.

[2] M. Otsuki, M. Watanabe, and A. Nishiura, "Trends and opportunities in intelligent power modules (IPM)," in *Proc. IEEE 27th Int. Symp. Power Semiconductor Devices IC's (ISPSD)*, Hong Kong, May 2015, pp. 317–320.

[3] S. Shao, N. Yu, X. Xu, J. Bai, X. Wu, and J. Zhang, "Tunnel magnetoresistance-based short-circuit and over-current protection for IGBT module," *IEEE Trans. Power Electron.*, vol. 35, no. 10, pp. 10930–10944, Oct. 2020, doi: 10.1109/TPEL.2020.2980680.

[4] X. Li, D. Xu, H. Zhu, X. Cheng, Y. Yu, and W. T. Ng, "Indirect IGBT over-current detection technique via gate voltage monitoring and analysis," *IEEE Trans. Power Electron.*, vol. 34, no. 4, pp. 3615–3622, Apr. 2019, doi: 10.1109/TPEL.2018.2856777.

[5] Z. Wang, X. Shi, L. M. Tolbert, F. Wang, and B. J. Blalock, "A DI/DT feedback-based active gate driver for smart switching and fast overcurrent protection of IGBT modules," *IEEE Trans. Power Electron.*, vol. 29, no. 7, pp. 3720–3732, Jul. 2014, doi: 10.1109/TPEL.2013.2278794.

[6] F. Huang and F. Flett, "IGBT fault protection based on di/dt feedback control," in *Proc. IEEE Power Electron. Specialists Conf.*, Orlando, FL, USA, Jun. 2007, pp. 1478–1484.

[7] J. X. Chen and A. Shorten, "An automatic IGBT collector current sensing technique via the gate node," in *Proc. Int. Exhib. Conf. Power Electron., Intell. Motion, Renew. Energy Energy Manag.*, Nuremberg, Germany, 2016, pp. 1–8.
[8] Z. Meng, Y. Yang, Y. Gao, S. Ai, Z. Fang, Y. Wen, and L. Wu, "A novel IC measurement without blanking time for short-circuit protection of high-power IPM," *IEEE Access*, vol. 8, pp. 64475–64485, 2020, doi: 10.1109/ACCESS.2020.2984542.
[9] X. Huang, X. Li, F. Wang, Y. Liu, and H. Sun, "Short circuit detection and driving control with no blanking time for high voltage high power insulated gate bipolar transistors," *IET Power Electron.*, vol. 14, no. 6, pp. 1138–1148, May 2021, doi: 10.1049/pel2.12097.
[10] M. H. Mohamed Sathik, P. Sundararajan, F. Sasongko, J. Pou, and V. Vaiyapuri, "Short circuit detection and fault current limiting method for IGBTs," *IEEE Trans. Device Mater. Rel.*, vol. 20, no. 4, pp. 686–693, Dec. 2020, doi: 10.1109/TDMR.2020.3018717.
[11] Y. Shi, R. Xie, L. Wang, Y. Shi, and H. Li, "Switching characterization and short-circuit protection of 1200 V SiC MOSFET T-type module in PV inverter application," *IEEE Trans. Ind. Electron.*, vol. 64, no. 11, pp. 9135–9143, Nov. 2017, doi: 10.1109/TIE.2017.2682800.
[12] M. A. Rodriguez-Blanco, A. Claudio-Sánchez, D. Theilliol, L. G. Vela-Valdés, P. Sibaja-Terán, L. Hernández-González, and J. Aguayo-Alquicira, "A failure-detection strategy for IGBT based on gate-voltage behavior applied to a motor drive system," *IEEE Trans. Ind. Electron.*, vol. 58, no. 5, pp. 1625–1633, May 2011, doi: 10.1109/TIE.2010.2098355.
[13] M. Oinoneni, M. Laitineni, and J. Kyyra, "Current measurement and short-circuit protection of an IGBT based on module parasitics," in *Proc. 16th Eur. Conf. Power Electron. Appl.*, Lappeenranta, Finland, 2014, pp. 1–9.
[14] R. S. Chokhawala, J. Catt, and L. Kiraly, "A discussion on IGBT short-circuit behavior and fault protection schemes," *IEEE Trans. Ind. Appl.*, vol. 31, no. 2, pp. 256–263, Mar. 1995, doi: 10.1109/28.370271.
[15] R. Pagano, Y. Chen, K. Smedley, S. Musumeci, and A. Raciti, "Short circuit analysis and protection of power module IGBTs," in *Proc. IEEE APEC*, Austin, TX, USA, Mar. 2005, pp. 777–783.
[16] Y. Chen, W. Li, F. Iannuzzo, H. Luo, X. He, and F. Blaabjerg, "Investigation and classification of short-circuit failure modes based on three-dimensional safe operating area for high-power IGBT modules," *IEEE Trans. Power Electron.*, vol. 33, no. 2, pp. 1075–1086, Feb. 2018, doi: 10.1109/TPEL.2017.2682114.
[17] B.-G. Park, J.-B. Lee, and D.-S. Hyun, "A novel short-circuit detecting scheme using turn-on switching characteristic of IGBT," in *Proc. IEEE Ind. Appl. Soc. Annu. Meeting*, Edmonton, AB, Canada, Oct. 2008, pp. 1–5.
[18] Y. Yang, Y. Wen, and G. Y. Li, "Review on high-power IGBT module and drive circuit," *High Voltage Eng.*, vol. 44, no. 10, pp. 3207–3220, 2018, doi: 10.13336/j.1003-6520.
[19] K. Yuasa, S. Nakamichi, and I. Omura, "Ultra high speed short circuit protection for IGBT with gate charge sensing," in *Proc. 22nd Int. Symp. Power Semicond. Devices (ISPSD)*, Hiroshima, Japan, 2010, pp. 37–40.
[20] P. J. Grbovic, "An IGBT gate driver for feed-forward control of turn-on losses and reverse recovery current," *IEEE Trans. Power Electron.*, vol. 23, no. 2, pp. 643–652, Feb. 2008, doi: 10.1109/TPEL.2007.915621.
[21] M. Chen, D. Xu, X. Zhang, N. Zhu, J. Wu, and K. Rajashekara, "An improved IGBT short-circuit protection method with self-adaptive blanking circuit based on VCE measurement," *IEEE Trans. Power Electron.*, vol. 33, no. 7, pp. 6126–6136, Jul. 2018, doi: 10.1109/TPEL.2017.2747587.
[22] Z. Wang, X. Shi, L. M. Tolbert, B. J. Blalock, and M. Chinthavali, "A fast overcurrent protection scheme for IGBT modules through dynamic fault current evaluation," in *Proc. 28th Annu. IEEE Appl. Power Electron. Conf. Exposit. (APEC)*, Long Beach, CA, USA, Mar. 2013, pp. 577–583.
[23] J.-B. Lee and D.-S. Hyun, "Gate voltage pattern analyze for short-circuit protection in IGBT inverters," in *Proc. IEEE Power Electron. Specialists Conf.*, Orlando, FL, USA, Jun. 2007, pp. 1913–1917.

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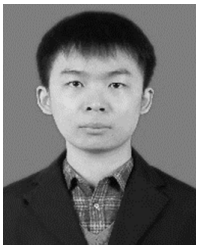

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