IEEE Access
Multidisciplinary ⋮ Rapid Review ⋮ Open Access Journal

Received 17 February 2023, accepted 15 March 2023, date of publication 20 March 2023, date of current version 23 March 2023.

Digital Object Identifier 10.1109/ACCESS.2023.3259323

RESEARCH ARTICLE

An Adaptive Hybrid Control of Reduced Switch Multilevel Grid Connected Inverter for Weak Grid Applications

TILA MUHAMMAD[1], ADNAN UMAR KHAN[1], YOUSRA ABID[1], MUHAMMAD HILAL KHAN[2], NASIM ULLAH[3], VOJTECH BLAZEK[4], LUKAS PROKOP[4], AND STANISLAV MISÁK[4]

[1]Department of Electrical and Computer Engineering, International Islamic University Islamabad, Islamabad 44000, Pakistan
[2]Department of Electrical Engineering, City University of Science and Information Technology, Peshawar 25000, Pakistan
[3]Department of Electrical Engineering, College of Engineering, Taif University, Taif 11099, Saudi Arabia
[4]ENET Centre, VSB—Technical University of Ostrava, 708 00 Ostrava, Czech Republic

Corresponding authors: Nasim Ullah (nasimullah@tu.edu.sa) and Tila Muhammad (eng.tila@gmail.com)

This work was supported by the following projects: TN02000025 National Centre for Energy II and CK04000060 Development of analytical tools for effective transition to electromobility. This work was also supported in part by the Taif University Researchers Supporting Project (TURSP-2020/144), Taif University, Taif, Saudi Arabia.

ABSTRACT Grid-connected inverters have a very significant role in the integration of renewable energy resources with utility grids. However, in recent studies, it is revealed that grid-connected inverters are vulnerable to instability when the nature of the grid changes from strong to weak, which produces uncertainty and performance degradation. An increase in grid impedance decreases stability margins, tremendously increases total harmonic distortion after a certain limit, and amplifies the voltage harmonics in the grid. A cascaded reduced switch symmetrical multilevel inverter along with an adaptive hybrid control technique is proposed for injecting power generated from distributed energy resources efficiently and stably to the utility grid. This research contributes twofold: a multilevel inverter topology and the other is its control method. The multilevel inverter reduces total harmonic distortion and size of the filter while increasing power handling capability. The control unit of the proposed system further consists of two parts: one is the synchronous frame current controller, and the other is stationary frame adaptive harmonic compensators. The grid current controller which is working in a synchronous reference frame ensures regulated current injection to the grid. It is not favorable to implement a harmonic compensator in a synchronous reference frame due to computation complexities. Therefore, the stationary reference frame controllers are used for harmonic compensations. But the resultant harmonic compensators have narrow bandwidth. Thus, these are not robust against variation in grid frequency. In this research, this problem is resolved by adding the adaptive features within the harmonic compensators, which shift its passing band according to the frequency of the grid while remaining with the same bandwidth. The proposed design of the hybrid frame controller is validated by considering a nine-level inverter connected with a weak grid.

INDEX TERMS Adaptive harmonic compensators, grid-connected inverters, harmonic compensators, multilevel inverters, phase disposition level shift carrier pulse width modulation, reduced switch multilevel inverters, total harmonic distortion, weak grid.

I. INTRODUCTION

Grid connected inverters(GCIs) play an important role in enabling the use of renewable energy resources. It is used to connect Distributed Generators(DGs) with the existing grid or within a microgrid. Most of the renewable energy resources are intermittent in nature [1], [2]. Thus, the energy produced is affected by environmental conditions like weather, temperature, sunlight, speed of the wind and humidity can affect its output. Therefore, storage devices

The associate editor coordinating the review of this manuscript and approving it for publication was Snehal Gawande.

are required to make electricity available when there is less power generation than demand or the power generation is not possible [1]. The commonly used device for electrical energy storage is a battery, which has fixed cycles of charge-discharge. After these cycles, the performance of the batteries degrades and needs replacement. This problem is common in the system where photovoltaic generation occurs because sunlight is available only in the daytime. Thus, the energy has to be stored in order to provide uninterrupted power to the users at night e.g. in the case of thermal power plants connected to the grid reserve fossil fuels during the daytime when energy enters from solar panels, and at night the thermal power plant runs by using the fuels that were reserved in the daytime. The theme looks like the energy is stored in the grid indirectly during the daytime and used at night. Due to higher utilization, batteries need replacement which increases the maintenance cost of photovoltaic systems. The cost-effective solution for this problem is to supply the excessive energy to the grid and extract it again when needed, by doing this the requirements of storage devices like batteries can be minimized. The core component used for this purpose to transfer energy from distributed sources to the grid is called GCIs. Thus, the GCIs play an important role in the integration of distributed power sources.

The GCIs are not much different from isolated inverters in circuit parameters, the main difference lies in their control and protection unit. Due to the increase in the utilization of renewable energy resources, the GCI is one of the hot areas of research. Currently, the research is focused on the efficiency and stability of inverters which is a challenging task. The grid itself to which GCIs are connected can be classified at a certain locality as strong or weak. The strength of a grid can be defined in two ways, grid impedance and short circuit ratio (SCR). The SCR is the ratio of the short circuit power at the point of common coupling (PCC) and the rated power of the inverter. When the SCR is below 10, the grid is weak. In the case when the SCR is above 20, the grid is strong [3], [4], [5]. Moreover, the grid impedance of a strong grid is considered zero while a weak grid has some considerable impedance. Some contemporary techniques have considered and tested for grid impedance up to 9mH [6] while in reference the inverter is tested up to 15mH [7].

The integration of GCIs with a weak grid becomes more challenging. The grid impedance of a weak grid varies due to parameters like distribution lines, line frequency transformer, distance from generation units, and short circuit ratio [3], [4], [5]. The inverter controller is designed by considering a dynamic model with the assumption that grid impedance does not vary but in practice, the impedance of weak grid varies [6], [8]. This variation can change the stability margins of the GCI which make the system at risk to become unstable. The research in this paper is focused on: GCI topology improvements, determining the stability of the connected GCI, and robust control techniques.

In [9], the GCI is formulated in the form of a closed-loop system which is used for the evaluation of stability. Moreover, it is found that the ratio of grid impedance and inverter output impedance must satisfy the Nyquist criteria of stability. In [10] further detail of impedance-based stability is discussed.

The development of GCI occurs either in form of improvements in topology or in its controller. Both parts of GCI are of equal significance. Therefore, this research contributes to both domains by improving the power handling capability, stability, and THD of the entire system. The control unit of the GCI plays a vital role in the stability of the system. It usually performs three main functions: synchronization, current regulation, and harmonic compensation. The synchronization unit extracts the phase of the grid voltage and forwards it to the current controller. The extracted phase is further used in Direct-Quadrature-Zero (DQZ) transformation and reference generation. The current controller regulates the current and generates the current that is in phase with the grid voltage which results in active power transfer.

The controller must be designed to inject pure sine wave currents even in the presence of grid harmonics but in most cases, the inverter controller can not minimize those harmonic and the inverter injects current polluted with low-order harmonics into the grid. Therefore, harmonic compensators are used in addition to the current controller to reduce these harmonics' content in the grid current.

In the weak grid, any increase in impedance boosts the voltage harmonics. These harmonics propagate through the phase lock loop (PLL) circuit and reach the control unit. Where it adds up to the grid current and increases the total harmonic distortion. In [7], PLL based on a second-order generalized integrator (SOGI) filter is used which helps to minimize the harmonic contents in the phase generated by PLL. Moreover, the controller used in PLL is Proportional Integral (PI) which is a synchronous frame controller and requires orthogonal signals for DQZ transformation. The SOGI filters also help in the generation of the required orthogonal signals.

The PI controller is one of the suitable and commonly used current controllers for PWM due to its robustness and ease of implementation but the grid current is an AC signal which can not be controlled with the PI controller directly. Therefore, first, the current signal is converted to a synchronous frame using DQZ transformation and then a PI controller can be used. DQZ transformation converts the AC signal into DC form and after the processing by the PI controller, the controlled signal converts to AC form with the help of inverse DQZ transformation [11]. Additional feedback of capacitor current is also used to work as active damping and avoid resonance created by a capacitor of LCL filter [12].

Although PI control reduces the total harmonic distortion due to switching and dead time the low-order harmonics are still present. Therefore, additional PI controllers or Proportional Resonance (PR) are used as harmonic compensators. Each technique has its own pros and cons. The PI controllers are not appropriate for harmonic compensation because for a single harmonic two PI controllers in addition

to the complexity of DQZ transformation are required [13]. Therefore, PI controllers are not recommended for this purpose. PR controllers are suitable compensators but they have narrow bandwidth. Therefore, even a small variation in grid frequency can affect their performance [14]. This problem of frequency variation can be fixed with the help of increasing the damping factor and using adaptive harmonic compensators [15].

The GCI is intrinsically a slow response system that produces many complications. The response time of the GCI can be improved with the help of voltage feedforward. In recent studies, voltage feedforward is considered an integrated part of GCI. Moreover, grid voltage feedforward minimizes the burden on the current controller and reduces the effect of sag and spike in grid voltage [16]. There are different techniques used for voltage feedforwards like proportional voltage feedforward, fundamental voltage feedforward, adaptive voltage feedforward [6] and full voltage feed-forward [17], [18] are some of the commonly used techniques. Although the voltage feedforward plays an important role in GCI but it reduces the stability margins of the inverter. Therefore, different techniques are proposed to overcome this limitation. The full voltage feedforward, proportional voltage feedforward, selective harmonic voltage feedforward, and fundamental voltage feedforward are the commonly used techniques for this purpose [18], [19]. In [20], it is found that fundamental voltage feedforward has more stability margin as compared to others. Therefore, fundamental voltage feedforward is used here.

An inverter is the core part of a GCI and it is critical to select an appropriate inverter topology. Therefore, the inverters can be classified on the basis of different parameters to find the appropriate topology. On the basis of, power rating there are low, medium, and high power inverters like fly back, push-pull, and half-bridge inverters are used as low-cost and low-power inverters. The H-bridge inverters are used as medium power inverters and multilevel inverters are suitable to use in medium to high power applications.

In a comparison of the H-bridge and multilevel inverters, the H-bridge inverters have the advantage of the minimum number of power electronic switches, but it requires filter components with higher values which compromises the advantage of the minimum number of power electronic switches. The increase in the values of filter components increases the cost, size, weight, and losses. Moreover, the minimum number of switches increases stress on the switches, thus it requires switches with a higher rating. Therefore, considering these constraints the smaller number of switches does not look promising [21], [22].

Instead of a full bridge inverter, the multilevel inverter produces a sine wave in stair form. Where each stair is encoded with pulse width modulation(PWM). Hence, the voltages across the switches producing PWM vary by a smaller value as compared to the zero and peak values in the case of the full bridge inverter. Due to this, the stress on power switches reduces and the transient response improves.

There are many multilevel inverter topologies available in literature but clamped diodes, flying capacitors and cascaded multilevel inverters are the classical topologies [23], [24]. The other topologies are derived forms of these inverters. Each of these topologies has its own advantages and disadvantages. On the basis of better output waveform resolution, symmetry in the circuit, simple PWM, and reduced total harmonic distortion, the cascaded multilevel inverter is a good choice for GCI. Moreover, its structure is more suitable for photovoltaic-based power plants, therefore the cascaded multilevel inverter is considered suitable for the way forward for this research.

The cascaded symmetrical multilevel inverter integrates multiple isolated sources to generate different levels in the output waveform. The requirement of isolated sources limits its usage. But in the case of PV panels as a source of energy, each panel or string of panels can be used as an isolated source which makes it useful. Another limitation of MLI is the requirement of many power switches. To minimize this limitation, many variants have been proposed to reduce the number of switches. Similarly, this research is focused on one such variant which uses a reduced number of switches.

In [25] the author has proposed a reduced switch topology with an additional feature of equal voltage source sharing. This is further extended in this research, by proposing an adaptive hybrid frame controller to make it promising for weak grid-connected applications.

The contributions of this research are:

1) Designed and controlled reduced switched cascaded multilevel inverter for grid-connected applications having the feature to utilize sources equally.
2) A hybrid Adaptive controller is implemented which is working in both, synchronous and stationary frames of references simultaneously for performance improvement.
3) The adaptive harmonic compensators are designed to minimize the effect of grid frequency and grid impedance variations on its performance and improve the robustness of the system.

Moreover, this paper is arranged such as Section II is related to reduced switch cascaded MLI, Section III consists of mathematical modeling, Section IV explains the proposed hybrid control, Section V discusses impedance-based stability, Section VI presents results and analysis, and Section VII consists of conclusion.

Renewable energy resources can be connected to the AC grid in four possible configurations as given in Figure 1. The merits and demerits of each configuration are summarized in Table 1. Table 1 shows that a multilevel inverter is a suitable solution. Because the DC sources can be used individually if required and they can be combined by using the multilevel inverter to connect them with the grid effectively.

II. REDUCED SWITCH CASCADED MLI

The reduced switch cascaded multilevel inverter as shown in Figure 2 consists of two stages: stage 1 is a level synthesizing cell, while stage 2 consists of an H-bridge. The

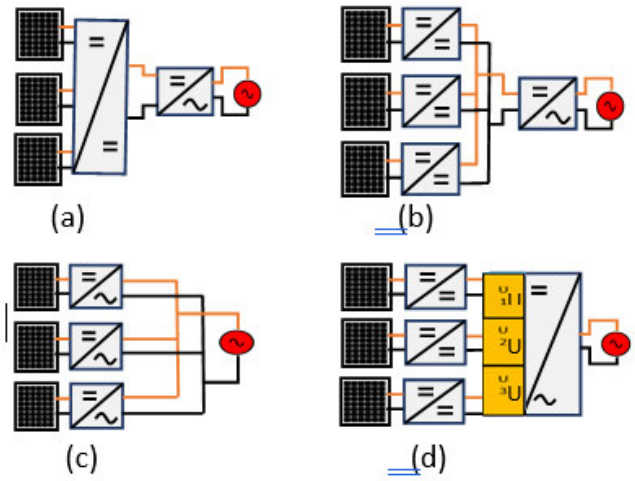

FIGURE 1. The architecture of GCI.

TABLE 1. The architecture of GCI.

Figure	Disadvantages	Advantages
Fig.1a	Distributed system has centralized solution	Easy control
Fig.1b	Distributed sources can be used individually.	Integration of DC-DC converters need a DC microgrid.
Fig.1c	Distributed system has distributed solution.	Parallel and nearer connection of GCI create stability issues
Fig.1d	Distributed system has distributed solution	Multiple DC-DC converters can be connected with a single inverter.

level synthesizing cells are used for generating levels and the H-Bridge is used for polarity inversion. Each synthesizing cell can generate two levels a positive and a negative level. Moreover, a single synthesizing cell consists of a discrete diode and a power electronic transistor packed with an anti-parallel diode. The required number of switches N_{sw}, diodes N_d and isolated DC sources N_{DC} can be calculated from (1), (2) and (3) respectively by using desired level of the inverter N_L.

$$N_{sw} = \frac{N_L - 1}{2} + 4. \tag{1}$$

$$N_d = \frac{N_L - 1}{2}. \tag{2}$$

$$N_{DC} = \frac{N_L - 1}{2}. \tag{3}$$

To demonstrate the working principle of the proposed design we have considered an arbitrary nine-level inverter as a case study shown in Figure 3. The number of control switches (power transistors) required in the nine-level inverter are eight and the discrete diodes are computed from (1) and (2). We have considered 4 dc sources V_{dc1}, V_{dc2}, V_{dc3} and V_{dc4} of equal magnitude. Four switches are required in stage 1, namely S_1, S_2, S_3 and S_4 along with four diodes D_1, D_2, D_3 and D_4, respectively while 4 switches in stage 2 denoted by A_1, A_2, A_3 and A_4 coupled with their respective anti-parallel diodes.

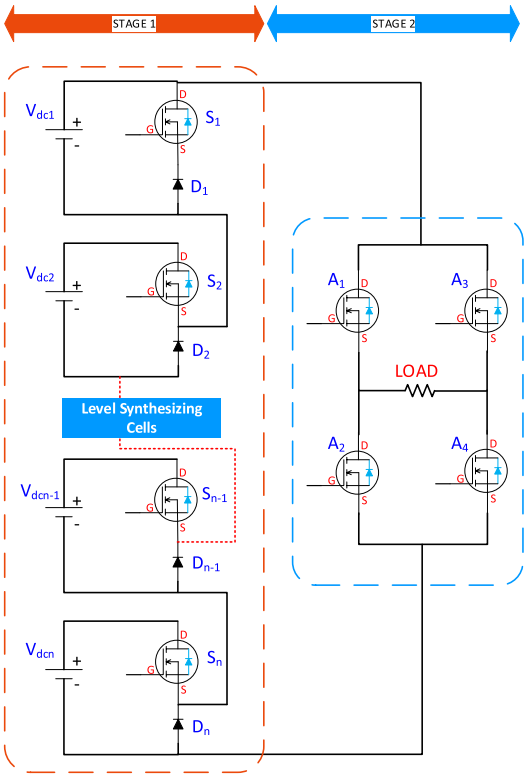

FIGURE 2. Reduced Switch Cascaded N-Level Inverter.

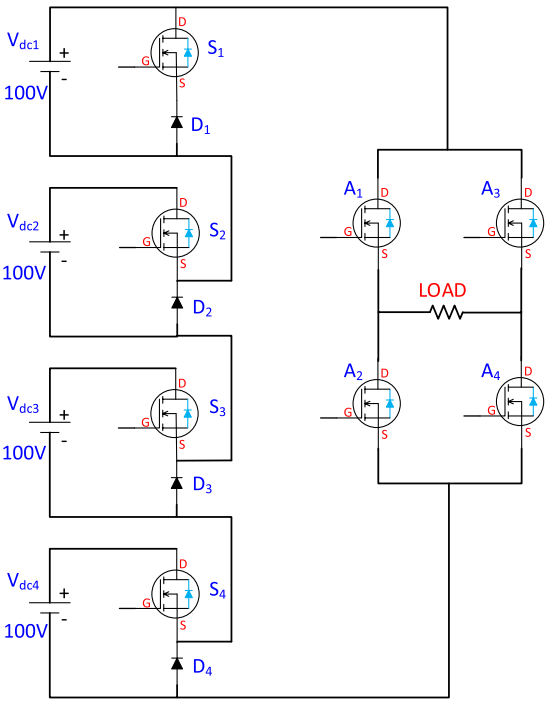

FIGURE 3. Reduced Switch Cascaded 9-Level Inverter.

A. PHASE DISPOSITION PWM AND EQUAL SOURCE SHARING

PWM plays an important role in the control of any power electronic converter. The most common of these are available in [26]. Here, the phase disposition Pulse Width

TABLE 2. The specification of level shifted carriers used in PDPWM.

Parameter	Value	Parameter	Value
Triangular1 lower peak	0V	Triangular1 upper peak	0.25V
Triangular2 lower peak	0.25V	Triangular2 Upper peak	0.5V
Triangular3 lower peak	0.5V	Triangular3 upper peak	0.75V
Triangular4 lower peak	0.75V	Triangular4 Upper peak	1V

Modulation(PDPWM) technique is used which consists of level-shifted carriers with the same amplitude and phase [27]. The carriers of the PDPWM is described here by C_i which has a frequency ω_c (the ω_c is 1kHz in this section II-A for ease of demonstration while in the remaining sections, the ω_c is 10kHz). The carriers can be defined as

$$C_i = E((-1)^{f(i)} y_c(w_c, \varphi) + i - \frac{N}{2}). \tag{4}$$

where, E is amplitude of a single triangular carrier, N is the number of levels, i=1, 2, . . . , N-1 and y_c is a normalized symmetrical triangular carrier defined as

$$y_c(w_c, \varphi) = (-1)^{[\alpha]}((\alpha mod 2) - 1) + \frac{1}{2}. \tag{5}$$

where,

$$\propto = \frac{w_c t + \varphi}{\pi}. \tag{6}$$

The phase angle of y_c is represented by φ and mod represents the modulus function. The y_c is a periodic function having the time period $T_c = 2\pi/\omega_c$. For the PDPWM technique $f(i) = 0$. On the basis of these assumptions and specifications the four carriers which are used here are summarised in Table2.

Figure 4 shows the classical PDPWM technique of multilevel inverter and the switching signals generated on the basis of classical PDPWM for the transistors of level enhancement cells. In Figure 5, the proposed modulation technique is presented along with pseudocode which makes the utilization of sources on an equal basis. It is shown in Figure 5b that in the positive half cycle, the utilization of source 1 to source 4 is decreasing while in the negative half cycle, the utilization of source 4 to source 1 is decreasing. The switching signals for the corresponding switches of level enhancement cells are given in Figure 5b.

To minimize the energy losses in the transistor switches PWM signal is applied to any one transistor in the track of the ON transistors at the same time and the remaining transistors of the same path will just be kept ON. Similarly, zero is applied to the rest of the transistors to keep them OFF at the meanwhile. This pattern of switching technique is explained with the help of Table 3.

On the basis of the modulation technique given in Figure 4 the generated output of the inverter is given in Figure 6a.

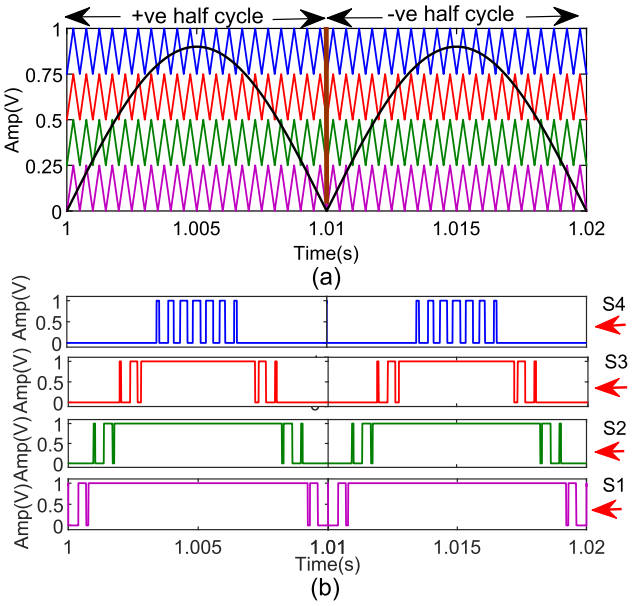

FIGURE 4. The PDPWM for 9-Level GCI (a) Multi carriers and reference signal (b) Gate signal generated by conventional PDPWM.

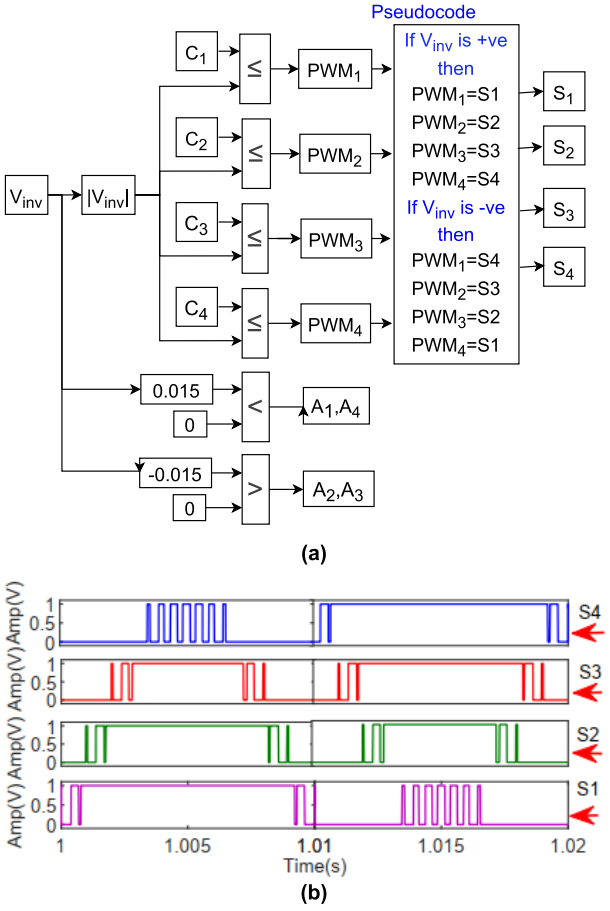

FIGURE 5. The PDPWM for 9-Level GCI for equal sources sharing (a) Modulation based on proposed pseudocode (b) gate signals generated for equal source sharing.

Similarly, the switching patterns for S_1 to S_4 are generated on the basis of the modulation technique given in Figure 5

TABLE 3. Gate signals for of switches used in nine level inverter.

Output Voltage	S_1	S_2	S_3	S_4	A_1, A_4	A_2, A_3
0	0	0	0	0	0	0
+(V_{dc1})	PWM	0	0	0	1	0
+(Vdc1+ V_{dc2})	1	PWM	0	0	1	0
+(Vdc1+ Vdc2+ V_{dc3})	1	1	PWM	0	1	0
+(Vdc1+ Vdc2+ Vdc3 +V_{dc4})	1	1	1	PWM	1	0
+ (Vdc1+ Vdc2+ V_{dc3})	1	1	PWM	0	1	0
+ (Vdc1+ V_{dc2})	1	PWM	0	0	1	0
+ (V_{dc1})	PWM	0	0	0	1	0
0	0	0	0	0	0	0
- (V_{dc4})	0	0	0	PWM	0	1
-(V_{dc3}+Vdc4)	0	0	PWM	1	0	1
-(V_{dc2}+ Vdc3+ Vdc4)	0	PWM	1	1	0	1
-(V_{dc1}+ Vdc2+ Vdc3 +Vdc4)	PWM	1	1	1	0	1
-(V_{dc2}+ Vdc3 +Vdc4)	0	PWM	1	1	0	1
-(V_{dc3}+ Vdc4)	0	0	PWM	1	0	1
-(V_{dc4})	0	0	0	PWM	0	1
0	0	0	0	0	0	0

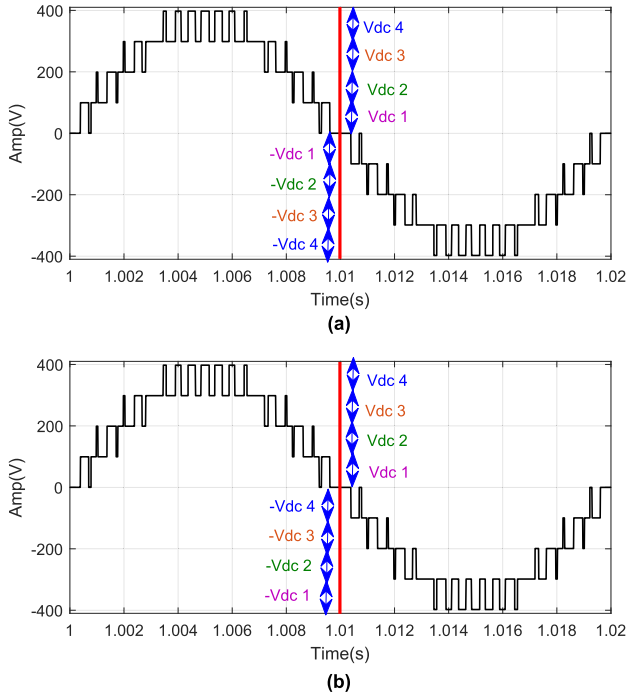

FIGURE 6. Output wave form of 9 level inverter (a) Conventional (b) Equal voltage source sharing.

and the resulting output of the 9-level inverter is given in Figure 6b.

III. SYSTEM MODELING

The proposed model of the system is shown as a block diagram in Figure 7. Here the single-phase grid is considered as mostly residential consumers are connected with a single phase. The model can be extended to a 3-phase inverter with minor modifications. The blocks of the proposed GCI system model consist of i) Multilevel inverter, ii) inductor-capacitor-inductor (LCL) filter, iii) Control unit which further consists of a current regulator and harmonic compensator, iv) Pulse width modulator, v) A weak grid (represented by Thevinen circuit of an impedance along with a voltage source) at the

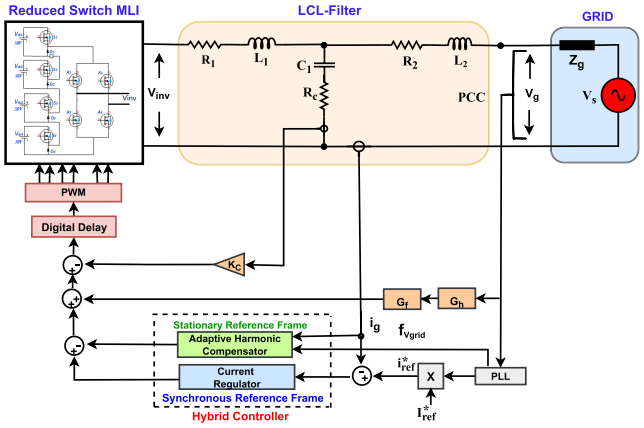

FIGURE 7. Multilevel(9-Level) weak GCI model.

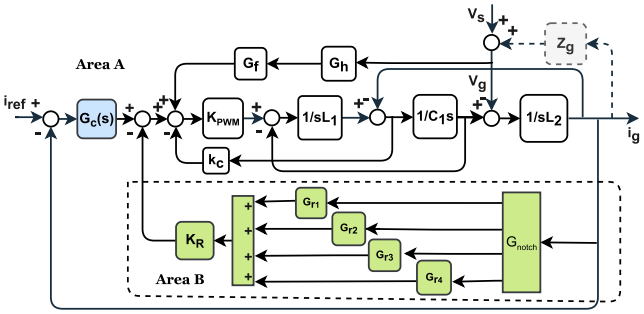

FIGURE 8. The proposed average switch control model of GCI.

point of common coupling, vi) A PLL used for the phase detection of grid voltage to generate reference current and frequency for the adaptive harmonic compensators and vii) an extra loop is used for active damping.

IV. PROPOSED HYBRID CONTROL

The average switch control model of the proposed inverter is given in Figure 8. Based on the functionality of the systems blocks can be divided into two parts as:

Area A consists of grid, inverter, LCL filter, modulator, active damping loop, voltage feedforward loop and feedback current controller designed in a synchronous frame of reference.

Area B represents the adaptive harmonic compensator working in the stationary reference frame and adaptive notch filter.

The important parts of the average model are elaborated in the below subsections.

A. SYNCHRONIZATION

The inverters output current i_g must be synchronized with grids voltage V_g for injecting active power within the grid. Here, PLL is used to estimate the phase and frequency of grid voltage V_g.

The PLL used here uses a synchronous frame controller, which needs direct-quadrature-zero (DQZ) transformation of AC signal but DQZ transformation of single phase system cannot be implemented directly like in the three-phase system. In a single-phase system orthogonal signals

TABLE 4. Symbols, description and values of system parameters.

Symbols	Description	Values
P	Rated Power	5kW
V_{DC}	DC voltage sources	100V each
	V_{DC_1}, V_{DC_2}, V_{DC_3} and V_{DC_4}	
V_s	Grid Source Voltage (RMS)	220V
f_g	Grid frequency	50Hz
	Grid frequency	49Hz<f_g<51Hz
L_1	Inverter side inductor	0.75mH
L_2	Grid side inductor	0.45mH
C_f	Fiter Capicitor	6.01uF
k_c	Active damping constant	10.6/400
$Z_{g(s)}$	Grid impedance	0–15 mH
k_o	SOGI filter damping factor	0.5
k_{or}	Compensator damping factor	0.001
k_{on}	Notch filter damping factor	7
K_r	Compensator gain	250
K_p	Proportional gain	50
K_i	Integral time constant	741
f_n	Low pass filter natural frequency	150 Hz
T_L	Low pass filter time constant	3.18 × 103
Kp_{pll}	Proportional gain PLL	10
Ti_{pll}	Integral time constant PLL	20 × 10
G_f	Proportional voltage feed forward	1
K_{pwm}	Modulation index	0.7
k_c	Gain of active damping loop	$10.6/\lvert K_{pwm}\rvert$

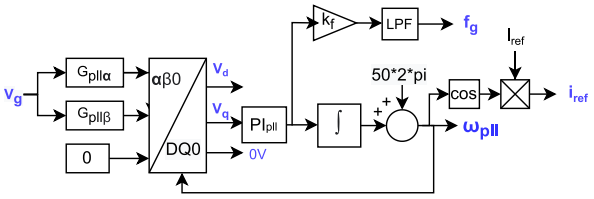

FIGURE 9. PLL block diagram for extraction of phase and frequency of V_g along with SOGI-based orthogonal signal generator.

are required for DQZ transformation which are generated by SOGI-based orthogonal signal generation method. The transfer function of SOGI filters used here are given in (7) and (8). The G_{pll_α} given in (7) remove high order harmonics and noise from V_g and allow V_α at the output and G_{pll_β} given in (8) removes high order harmonic as well as produces a delay of 90^o in V_g to make it orthogonal to V_α. The orthogonal signals generated are converted from stationary reference frame to synchronous reference frame by using DQZ transformation which produces V_d and V_q as given in Figure 9. Now, by using PLL technique f_g, i_{ref} and ω_{pll} can be extracted.

$$G_{pll_\alpha} = \frac{k_{pll}\omega_{pll}s}{s^2 + k_{pll}w_{pll}s + (\omega_{pll})^2}. \tag{7}$$

$$G_{pll_\beta} = \frac{k_{pll}\omega_{pll}^2}{s^2 + k_{pll}w_{pll}s + (\omega_{pll})^2}. \tag{8}$$

There are other advanced techniques that can be used to improve the synchronization of the GCI with grid voltage, some of the latest are [28], [29], [30], and [31]. The focus of this research is on designing an adaptive harmonic compensator for multilevel GCIs therefore an existing PLL technique is implemented in [7] is used in this research to evaluate the performance of the proposed technique.

B. CURRENT REGULATOR

The current regulator is used to control injected power into the grid. The controller used here is the PI controller, and its transfer function is given in (9). The injected current within the grid is AC, if the PI controller is implemented to control the AC waveform it has reduced bandwidth and can become unstable. This issue can be overcome by converting the AC signal from a stationary reference frame to its corresponding synchronous frame as discussed in subsection IV-A. Where, the AC signal is converted into its corresponding DC, for this purpose, a DQZ transformation is used here. The orthogonal signal generators are again required like in subsection IV-A to convert a single phase current signal to two orthogonal signals but the same technique orthogonal signal generation is not appropriate here because the removal of harmonic from the input signal is not desired here. Therefore, the grid current i_g is considered as i_α as given in (10) and the other signal i_β is produced by passing the grid current i_g through two low pass filters with a phase lag of 45° per filter as given in (11). Then, with the help of Park transformation, the orthogonal signals are converted into their corresponding DC form I_d and I_q which is given (12). The I_d and I_q and are subtracted from their respective reference signals and the error signals are generated. Both of the error signals of the D-axis and Q-axis are passed through PI controller which is expressed in (13) and (14) respectively. The inverse Park transform is used to convert the controlled signals to their respective orthogonal signals in (17). This whole process of current control is described in a simplified form in Figure 10.

$$G_c(s) = K_p + \frac{K_i}{s}. \tag{9}$$

$$i_\alpha(s) = i_g(s). \tag{10}$$

$$i_\beta(s) = (i_g(s))\frac{1}{1+Ts}. \tag{11}$$

$$\begin{bmatrix} I_d \\ I_q \end{bmatrix} = \begin{bmatrix} coswt & sinwt \\ -sinwt & coswt \end{bmatrix} \begin{bmatrix} i_\alpha \\ i_\beta \end{bmatrix}. \tag{12}$$

$$V_{cd}(s) = (I_d^* - I_d)G_c(s). \tag{13}$$

$$V_{cq}(s) = (I_q^* - I_q)G_c(s). \tag{14}$$

$$V_{inv\_d} = V_{cd}(s) - I_q(\omega_0(L_1 + L_2)) + V_{gd}. \tag{15}$$

$$V_{inv\_q} = V_{cq}(s) - I_d(\omega_0(L_1 + L_2)) + V_{gq}. \tag{16}$$

$$\begin{bmatrix} V_{inv\_\alpha} \\ V_{inv\_\beta} \end{bmatrix} = \begin{bmatrix} coswt & -sinwt \\ sinwt & coswt \end{bmatrix} \begin{bmatrix} V_{inv\_d} \\ V_{inv\_q} \end{bmatrix}. \tag{17}$$

The desired values of K_p and K_i are selected with the help of the MATLAB SISO tool, which is listed in Table 4.

C. ADAPTIVE HARMONIC COMPENSATORS

The harmonic compensators are used to minimize the harmonics contents in the current feeding into the grid. The reduction of harmonics in grid current enhances the performance and increases the stability of the GCIs. The grid impedance variation changes the harmonics content in the grid current. Therefore, harmonics compensators are helpful to provide robustness against the variation of grid impedance.

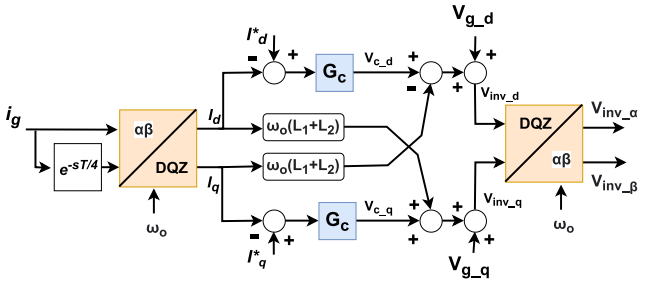

FIGURE 10. Block diagram of synchronous frame current regulator along with DQZ and inverse DQZ transformation.

The synchronous reference frame compensator uses two controllers for each harmonic. Hence, for four harmonics eight controllers are required but instead of synchronous only four stationary reference frame controllers are required. Therefore, the resonant controllers selected here for this purpose are stationary frame controllers. The controllers estimate the harmonic frequencies present within the grid and mitigate them. The realization of the controller in a digital domain is complex due to which its usage is limited. This limitation is overcome by adding a damping factor which not only makes it realizable but also increases its bandwidth. The advantage of the broad bandwidth is that controllers can estimate harmonics even if there exist small variations in fundamental and harmonic frequencies. The limitation of broader bandwidth is that contents of fundamental can also pass through the filters because the magnitude of the fundamental signal is very large as compared to the harmonics. To overcome this, and stop the fundamental signal contents from entering to the resonant filters a notch filter is used here. The notch filter has a very narrow bandwidth and is difficult to realize therefore a damping factor is also added to the notch filter to increase its bandwidth for realization. Both filters with relatively larger bandwidths perform well within very slight variations in frequencies of the grid. But in the case of little larger frequency variations, the performance of these filters significantly degrades and sometimes produces adverse effects.

The notch filter transfer function G_{no} is given in (18) and the transfer function of resonant filters G_{rn} is given in (19). Both of these filters are cascaded with gain K_R to form a fixed value harmonic compensator G_R which is given in (20). The first four odd harmonic compensators are shown in area B of Figure 8.

$$G_{no} = \frac{s^2 + 0s + \omega_o^2}{s^2 + k_{on}s + \omega_o^2}. \tag{18}$$

$$G_{rn} = \frac{k_{or}\omega_o s}{s^2 + k_{or}w_o s + (n\omega_o)^2}. \tag{19}$$

$$G_R = K_R G_{no} \sum_{i=3}^{n} G_{ri}. \tag{20}$$

where i is an odd integer starting from 3.

In this research, to fix this problem of limitation that fix frequency harmonic compensator can not properly work when there is a variation in grid frequency, the fixed valued notch and resonant filters are replaced with adaptive filters. Sometimes, a larger variation occurs in grid frequency due to rapid variations in load or generating stations. In such conditions, the performance of the fixed value compensator degrades or produces some adverse effects. In this research, this limitation is overcome by designing adaptive filters. Although the bandwidths of the adaptive filters to estimate harmonics are the same as that of fixed value filters, but the adaptive filters tune themselves to the frequencies of the harmonics. Therefore, it is found that the variation in the fundamental frequency has a minor effect on the performance of compensators.

The designed adaptive filters adapt themselves according to frequency estimated by PLL. The block diagrams of the adaptive compensators are given in Figure 11(a) and (b). The transfer functions of the filter are given in (21) and (22). These adaptive filters are cascaded with the gain K_R and work as adaptive harmonic compensators as given in (23).

$$G_{no_{ad}} = \frac{s^2 + \omega_{pll}^2}{s^2 + k_{on}s + \omega_{pll}^2}. \tag{21}$$

$$G_{rn_{ad}} = \frac{k_{or}\omega_o s}{s^2 + k_{or}w_o s + (n\omega_{pll})^2}. \tag{22}$$

$$G_{R_{ad}} = K_R G_{no_{ad}} \sum_{i=3}^{n} G_{ri_{ad}}. \tag{23}$$

where i is an odd integer starting from 3.

Figure 11(c) shows the frequency response of adaptive resonance compensators and notch filter against the grid frequencies of 49Hz, 50Hz or 51Hz labeled as blue, black and red respectively.

Thus, every adaptive harmonic compensator work according to the grid frequency and set the cutoff values of its filter such that low-order odd harmonics lies in the bandwidth of its corresponding compensator. This phenomenon is explained with the help of Figure 11 which shows that the performance of the harmonic compensator depends on the grid frequency that is if the grid frequency is 51Hz then the frequency of the 9^{th} odd harmonic is 459Hz. Thus, in the case of fixed values harmonic compensators the resonance filter will not pass the harmonic but in the case of adaptive, it will pass through the filter as the response of Figure 11 shows the result. There in the case of frequency variation fixed valued harmonic compensator devalues its performance, and a larger variation can make it unstable. The harmonic compensator takes frequency as the input from PLL continuously.

The adaptive notch filter is playing an important role to minimize the content of grid frequency in the output signal of the adaptive resonant filters. The notch filter blocks the grid frequency to enter into the resonant filter as shown in Figure 11(a). The results of Figure 12 show the notch filter has a significant role to improve the result.

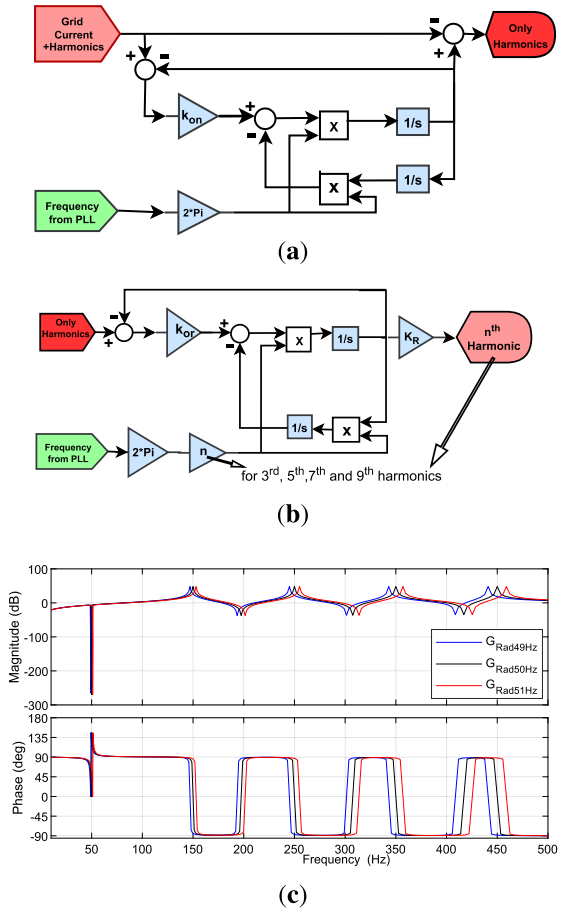

FIGURE 11. Adaptive resonance harmonic compensator (a) Adaptive notch filter (b) Adaptive resonance filter (c) Frequency response of adaptive harmonic compensator for 49Hz, 50Hz and 51Hz.

D. PARAMETERS SELECTION OF CURRENT CONTROLLER AND HARMONIC COMPENSATOR

To find the appropriate parameters of the current controller and harmonic compensator for the desired stability margin (gain margin −3 to −5 dB and phase margin 30° to 60°), the open loop gain (24), as shown at the bottom of the page, is derived from the proposed system given in Figure 8 by using block reduction method. The values of parameters are extracted with the help of Bode Plot and MATLAB SISO Tool and listed in Table 4.

The Bode plots of the open loop gain is given in Figure 13 by using the parameters given in Table 4. The responses are for three different values of grid impedance 5mH, 10mH, and 15mH. The results show that the minimum phase margin and gain margin are $3dB$ and 50° respectively. The G_h in (24) is given in (25):

$$G_h = \frac{k\omega_o s}{s^2 + k\omega_o s + \omega_o^2}. \tag{25}$$

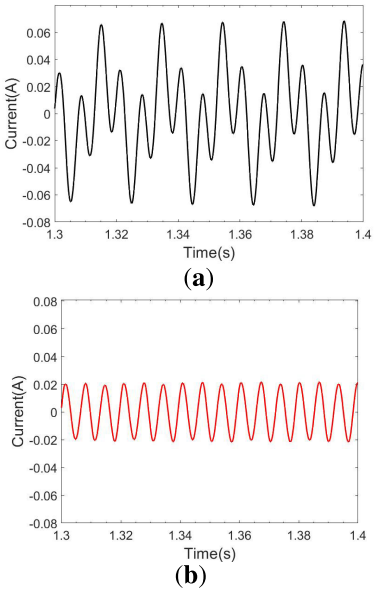

FIGURE 12. Impact of adaptive notch filter (a) 3^{rd} harmonic without notch filter (b) 3^{rd} harmonic with notch filter.

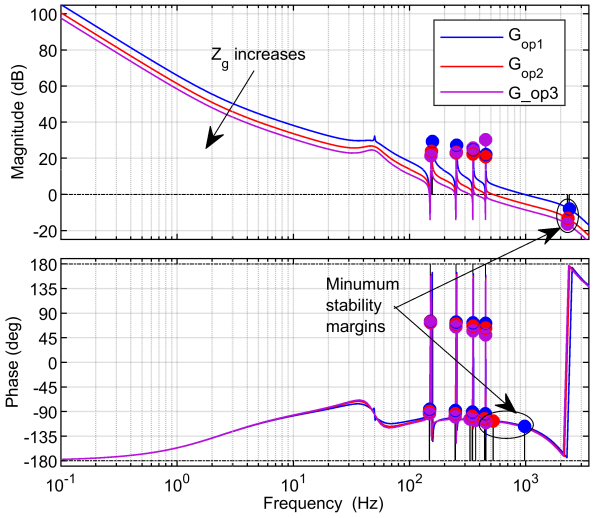

FIGURE 13. The open loop gain of the proposed system.

V. IMPEDANCE-BASED STABILITY

The stability of the whole system is tested with the help of the impedance-based stability method. The proposed system given in Figure 7 is divided into two equivalent subsystems the inverter side is represented in Norton form and the grid along with grid impedance is represented in Thevenin form as given in Figure 14.

The network of Figure 14 can be solved with the help of the superposition theorem to find the grid current given in

$$G_{i_{ref}}^{i_g} = \frac{G_c k_{pwm}}{s^3 L_1 L_2 C_1 + s^2 L_1 Z_g C_1 + s^2 L_2 C_1 k_c k_{pwm} + s Z_g C_1 k_c k_{pwm} + s L_1 + s L_2 + Z_g - Z_g G_f G_h k_{pwm} + k_{pwm} K r G_{PR}} \tag{24}$$

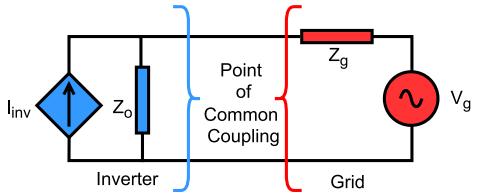

FIGURE 14. GCI presented in Norton form connected with grid presented in Thevinen form.

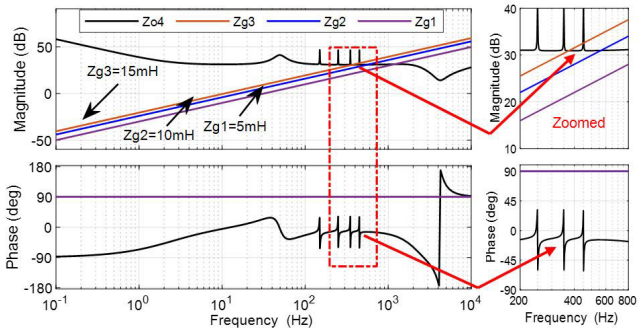

FIGURE 15. Impedance based stability analysis using Bode Plot.

(26) and further simplified in (27).

$$i_g = \frac{I_{inv}(s)Z_o(s)}{Z_o(s)+Z_g(s)} - \frac{V_s(s)}{Z_o(s)+Z_g(s)} \tag{26}$$

$$i_g = \left[I_{inv}(s) - \frac{V_s(s)}{Z_o(s)}\right] \frac{1}{1+Z_g(s)/Z_o(s)}. \tag{27}$$

Using the method of stability testing from [9], the impedance ratio Z_g/Z_o from (27) can be used for impedance-based stability test.

Here, the system is evaluated by considering Z_g=5mH, 10mH, and 15mH. The grid impedance is derived from Figure 8 by ignoring the doted part of the grid impedance. Furthermore, the relation between V_g and i_g is found by ignoring reference current i_{ref}. Thus, the derived output admittance is represented by Y_o and impedance represented by Z_o are given in (28) and (29), as shown at the bottom of the next page, respectively.

The stability can be checked through the Bode plot or with the help of the Nyquist Stability Theorem by checking the encirclement of the point (−1,0). The Bode plot of the grid impedance ratio is given in Figure 15. From Figure 15 it can be seen that the system is stable where the inverter output impedance is greater than the grid impedance. In another place, where the grid impedance is greater than the inverter output impedance the roles can be checked from [9]. The pole-zero plot of the impedance ratio shows that all poles lie in left half plane. The plot shows that the system remains stable for all three grid impedances.

To further confirm the stability, the Nyquist plot of impedance ratio is plotted in Figure 16) which shows the stability of inverter against three different impedances 5mH, 10mH, and 15mH respectively. The Nyquist stability criteria state that a system is stable if there is no encirclement of point (−1,0) or the counterclockwise encirclements of point (−1,0) are equal or greater than the clockwise encirclement, Vice versa the system is unstable if counterclockwise encirclement is less than the clockwise encirclement of point (−1,0). Thus, the Nyquist stability conditions are satisfied and the proposed system is a stable system. The Nyquist plots of Figure 16 show that for all three graphs, none of the loops encircle the point (−1,0) clockwise. Therefore, it is concluded that the closed system is stable.

VI. RESULTS AND ANALYSIS

Simulation of the proposed system is performed within MATLAB Simulink environment. The study of a GCI is conducted by considering the peak current rating of the system as 50A and the peak voltage of the grid as 310V. The available grid is defined as a voltage source in series with an impedance. Hence, it represents the weak grid. The real part of the impedance is ignored because it does not contribute to the instability of the system. Therefore, the impedance consider here is an inductance only, which is represented in mili Henry (mH). The system is tested for three different values of grid impedance 5mH, 10mH, and 15mH.

The inverter uses a total of 4 DC voltage sources and 8 control switches with anti-parallel diodes with each switch. The inverter generates 9 levels of output and PWM is implemented with the help of the phase disposition level shift carrier method. The specification of the level shift carrier is given in Table 2 and equal the voltage source sharing switching technique is described in Table 3.

The harmonic distortion within voltage affects the harmonic distortion present within the current feeding to the grid. Therefore, low order first four odd harmonics are added in grid voltage. The grid voltage along with the profile of the harmonics in it is given in Figure 17. Here, the grid frequency is 50Hz and the first four odd harmonics are added with it having frequencies of 150, 250, 350, and 450Hz respectively. The grid frequency has a peak amplitude 310V and the harmonics 3^{rd}, 5^{th}, 7^{th} and 9^{th} have peak amplitude of 10V, 5V, 5V and 5V respectively. The grid frequency is varied between 49Hz to 51Hz to check the adaptivity of harmonic compensators. There are three different cases on the basis of which the results are discussed here:

A. CASE 1: TEST FOR GRID IMPEDANCE VARIATION

In this case, the proposed system is tested to show its robustness against grid impedance variation and its performance is evaluated based on THD. Here the proposed inverter is tested for three different values of grid impedance Zg=5mH, Zg=10mH, and Zg=15mH and results are given in Figure 18. The results reveal that the system is stable and the total harmonic distortion does not increase from the IEEE Standard set for the GCIs and the performance in form of reduced total harmonic distortion is better than the existing techniques.

Moreover, the results of the proposed technique are compared with the existing techniques found in [7], [32], and [33] as given in Table 5

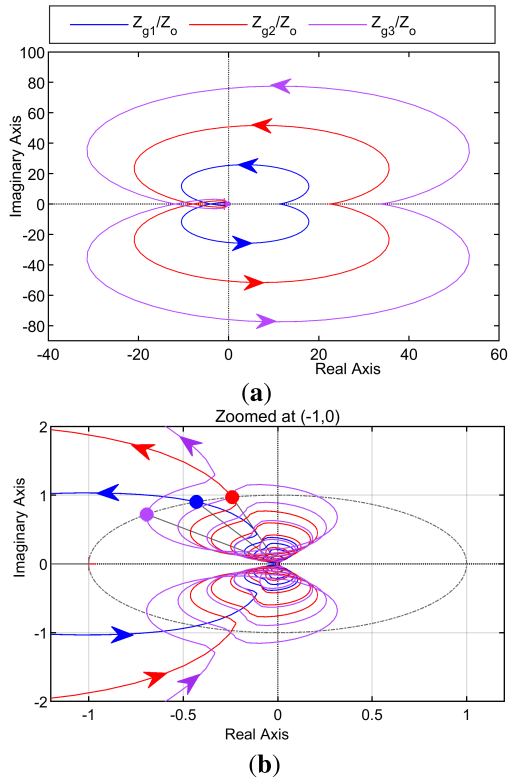

FIGURE 16. Impedance-based stability analysis using Nyquist plot (a) Nyquist plot of impedance ratio $Z_{g1}(s)/Z_o(s)$,$Z_{g2}(s)/Z_o(s)$ and $Z_{g3}(s)/Z_o(s)$. (b) Zoomed at $(-1,0)$.

TABLE 5. Comparison of the proposed technique on the bases of THD under grid impedance variation.

Technique	THD in %		
Grid impedance	Z_g =5mH	Z_g= 10mH	Z_g=15mH
Technique used in [7]	3.5%	3.2%	2.9%
Technique used in [32]	2.1%	2.9%	3.3%
Technique used in [33]	1.9%	2.4%	2.8%
Proposed Technique	0.27%	0.3%	1.07%

B. CASE 2: TEST FOR FREQUENCY VARIATION

The adaptive behavior of the proposed is tested in this case. A variation of 2% in the grid frequency is introduced to check its robustness against the frequency variation. First, the proposed system is tested for 51Hz, 50.5Hz and 50Hz to evaluate its performance when the grid frequency is greater than its rated value of 50Hz and the results are given in Figure 19(a). The extracted results of Figure 19(a) are compared with the other techniques mentioned [34] and [35]

TABLE 6. Comparison of the proposed technique on the basis of THD against grid frequency variation up to 2%.

Technique	THD in %				
Grid Frequency	49Hz	49.5Hz	50Hz	50.5Hz	51Hz
Technique used in [34]	3.08%	2.02%	1.49%	2.13%	3.16%
Technique used in [35]	2.8%	2.9%	2.9%	2.9%	3.0%
Proposed Technique	2.57%	1.63%	0.29%	1.91%	0.6%

TABLE 7. Comparison of the proposed technique for 1% of grid frequency variation at i_g 25A.

Technique	THD in %	
Grid frequency	49.5Hz	50.5Hz
Technique used in [37]	1.03%	0.95%
Technique used in [36]	0.66%	0.51%
Proposed Technique	0.64%	0.46%

in Table 6. The Comparison shows that the proposed system is working good and producing promising results as compared to the existing contemporary techniques.

The system is also tested for the case when there is a decrease in grid frequency from its rated values such as 49Hz, 49.5Hz, and 50Hz. Again the system is found stable and the adaptive harmonic compensators show promising results as given in Figure 19(b). For these values of grid frequency the system is compared with [34] and [35] in Table 6 which shows that the proposed system is performing better than other techniques.

At a lower rating when the grid current is 25A, the proposed system is tested and it is found that it has almost similar or better performance as compared to the 3-level inverter given in [36]. The result for the 25A grid injected current at 50.5Hz and 49.5Hz generated from the proposed system are given in Figure 20. The results are compared with [36] in Table 7.

C. CASE 3: TEST FOR POWER HANDLING

In this case, the proposed solution is tested to verify that it mitigates three limitations of 3-level inverters by 1) decreasing stress on switching transistors, 2) improving power handling capability 3) decreasing the rate of change of voltage (dV/dt).

The power handling capability of the inverter increases when there is a change from three levels to nine levels. In a multilevel inverter, the low-power switches are used in cascade to handle high voltage. Thus, the rating of

$$Y_o^{U_s-i_g} = \frac{G_f G_h Kpwm - C_1 L_1 s^2 - C_1 k_c k_{pwm} s - 1}{L_1 L_2 C_1 s^3 + L_2 C_1 k_c k_{pwm} s^2 + (L_1 + L_2)\, s + G_c k_{pwm} + K_r k_{pwm} G_{PR}} \tag{28}$$

$$Z_o^{i_g-U_s} = \frac{L_1 L_2 C_1 s^3 + L_2 C_1 k_c k_{pwm} s^2 + (L_1 + L_2)\, s + G_c k_{pwm} + K_r k_{pwm} G_{PR}}{G_f G_h Kpwm - C_1 L_1 s^2 - C_1 k_c k_{pwm} s - 1} \tag{29}$$

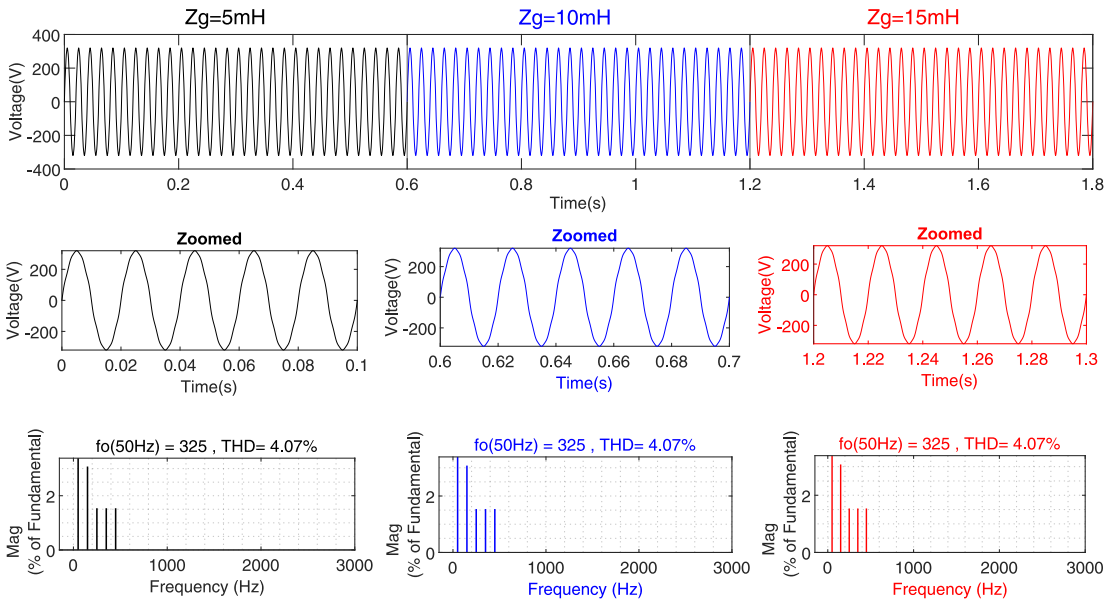

FIGURE 17. Grid source voltage polluted with 3^{rd}, 5^{th}, 7^{th}, and 9^{th} *harmonics.*

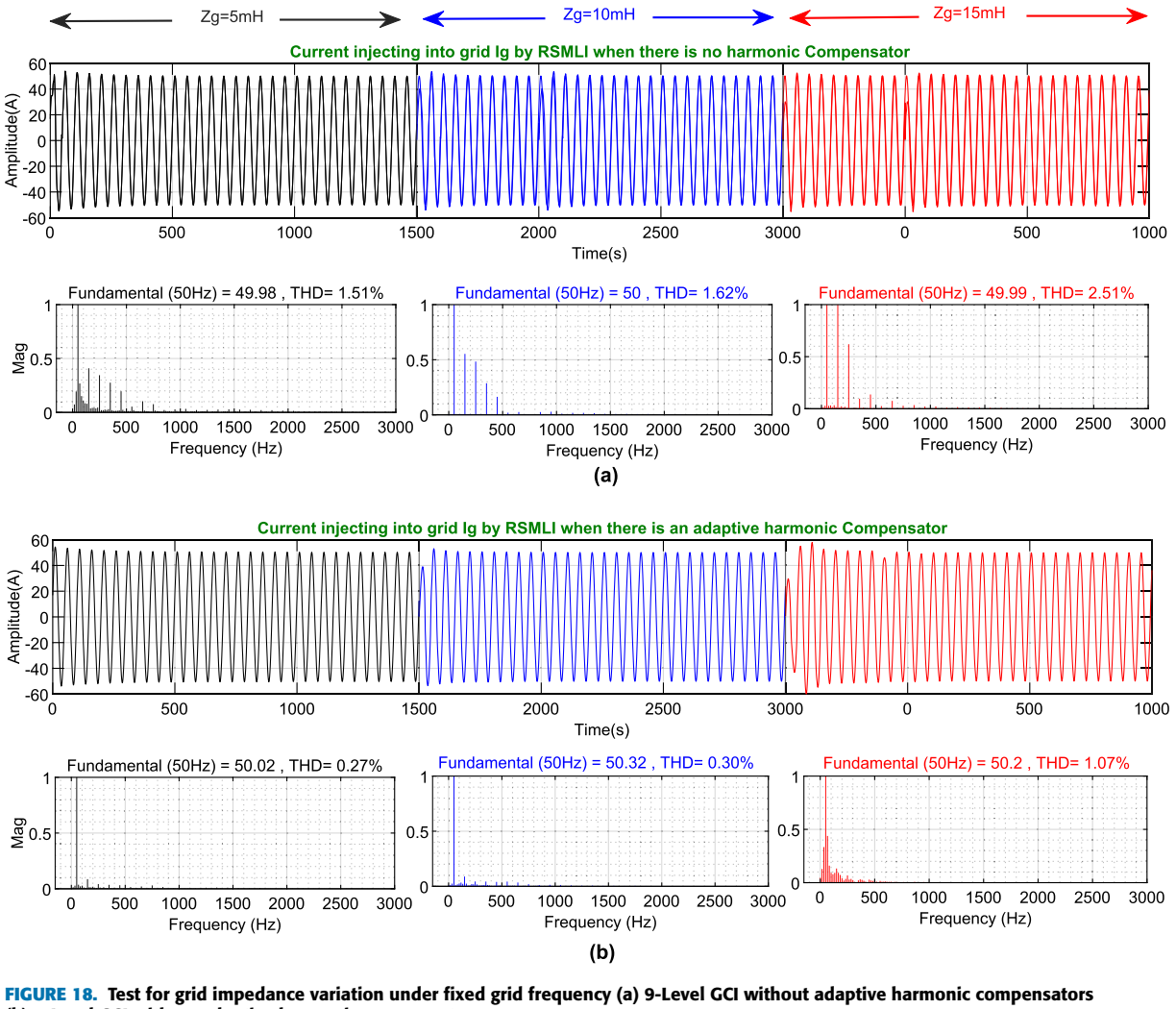

FIGURE 18. Test for grid impedance variation under fixed grid frequency (a) 9-Level GCI without adaptive harmonic compensators (b) 9-Level GCI with an adaptive harmonic compensators.

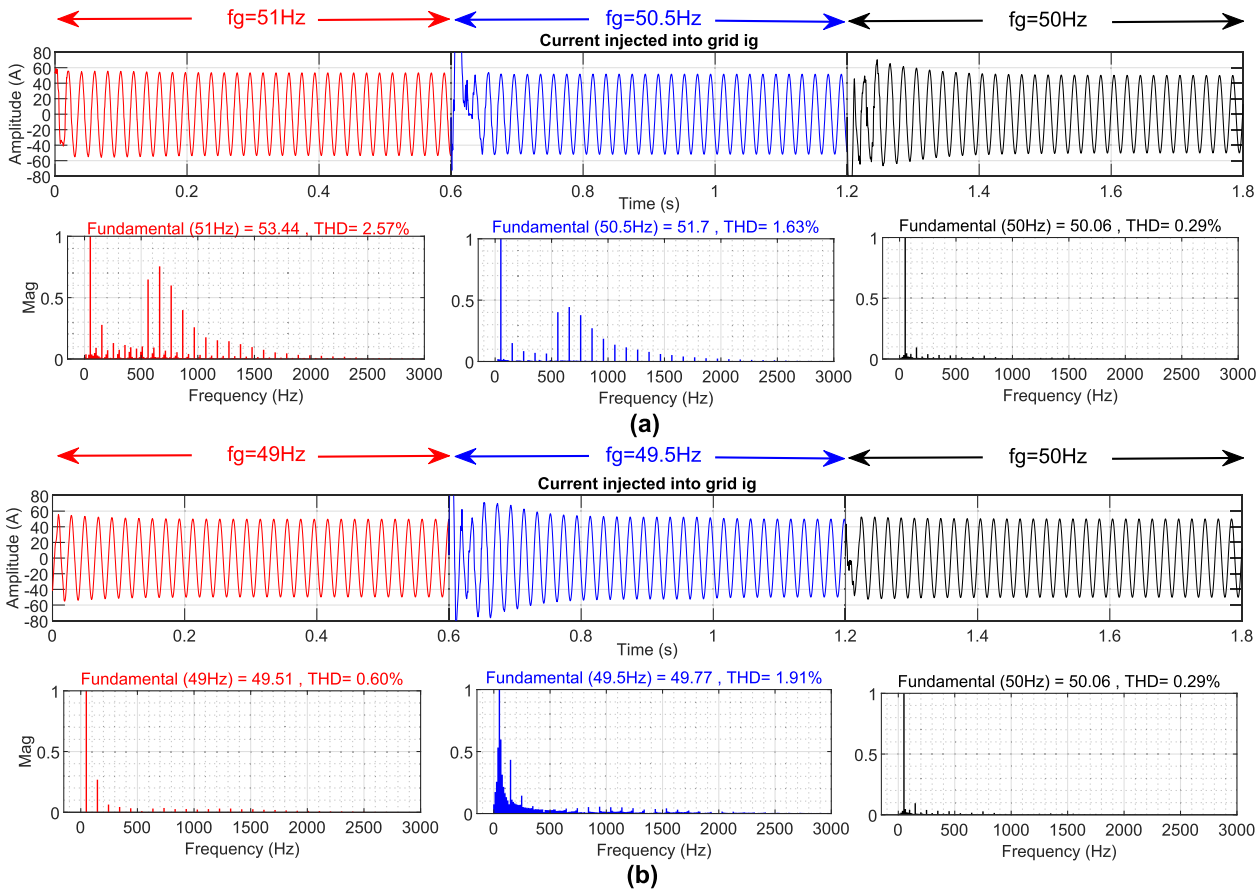

FIGURE 19. Test for 2% grid frequency variation (a) Results for 51Hz, 50.5Hz and 50Hz (b) Results for 49Hz, 49.5Hz and 50Hz.

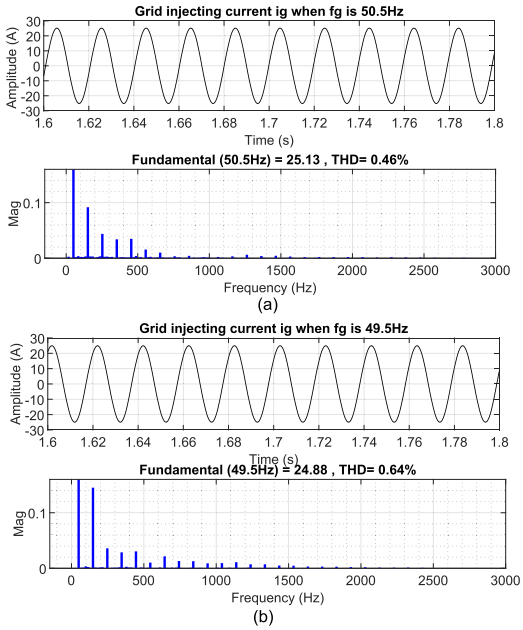

FIGURE 20. Test for 1% grid frequency variation keeping current i_g to 25A (a) Results for 50.5Hz (b) Results for 49.5Hz.

the switches decreases as the level increases. There is another important aspect of a multilevel inverter that is

TABLE 8. Comparison of the proposed multilevel GCI with 3-Level GCI.

Technique	THD in %				
Current i_g	30A	40A	50A	60A	70A
3-level GCI given in [36]	0.49% THD	0.38% THD	3.84% THD	unstable	unstable
Proposed 9-level GCI	0.38% THD	0.41% THD	0.60% THD	0.61% THD	3.28% THD

the output of a multilevel inverter can be filtered by using smaller components of the filter. Hence, the weight, volume and losses of LCL filter of the inverter decrease by using the multilevel inverter. The multilevel inverter output has smoother output voltages and current waveforms as compared to the 3 levels inverter. Therefore, a multilevel inverter shows much more stability than compared to 3-level inverters.

In the proposed case of nine level inverter, the output voltage jump or step is almost four times smaller than the jump in 3 levels inverter. Here, both 3-levels and 9-level inverters are tested by using the same switching frequency and filter components. The results are given in Figure 21 where Figure 21(a) shows results of 3-level inverter [36] and Figure Figure 21(b) results of the proposed 9-level inverter. The results show the three-level inverter becomes unstable when i_g>50A but the proposed MLI remains stable even after 70A. It is also shown in Fig.21 that even in the case when i_g

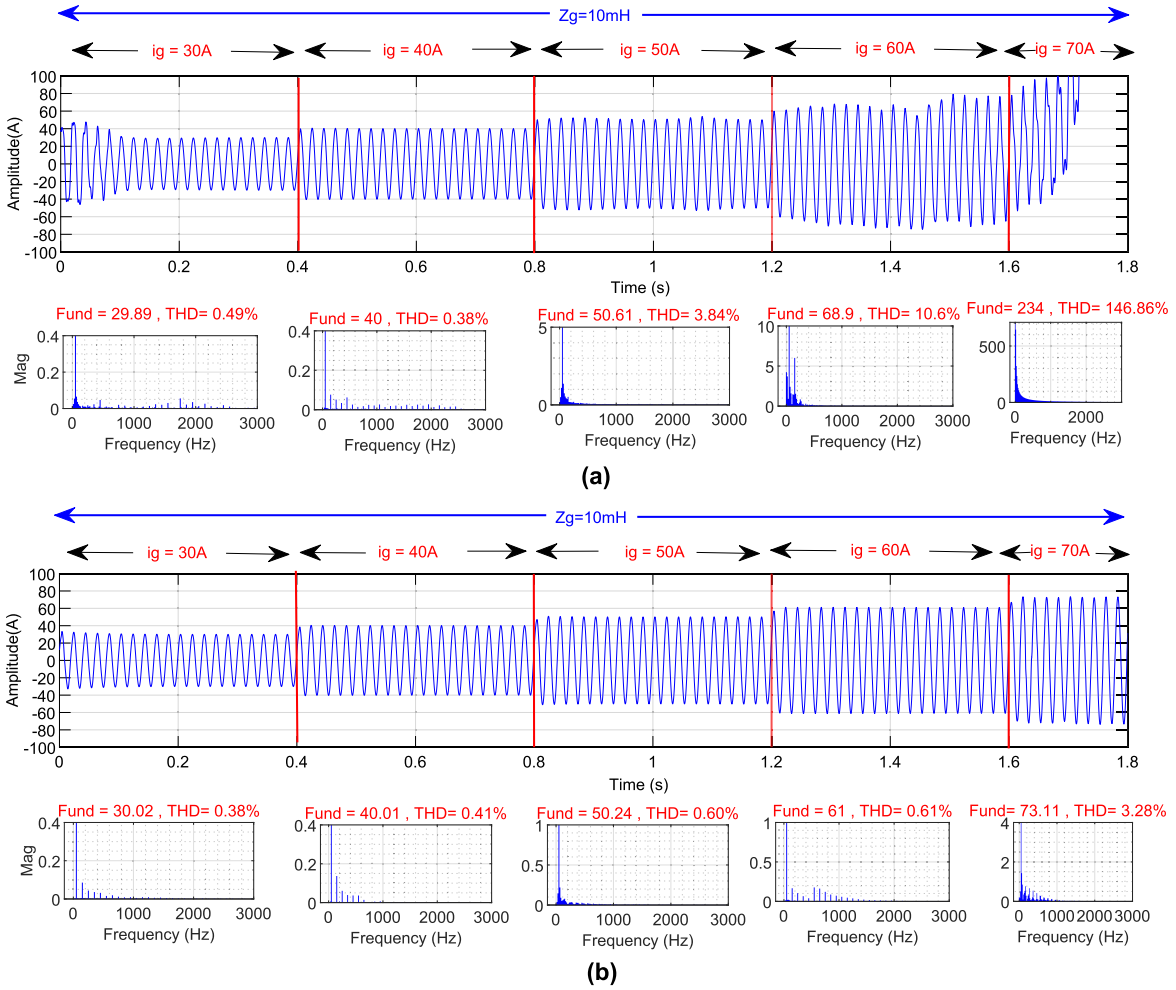

FIGURE 21. Power Handling capability testing (a) 3-Level Inverter (b) 9-level Inverter.

is 50A still the multilevel inverter has superior performance as compared to the 3-level inverter. From Figure 21 it is also concluded that the transient response of MLI is far better than a 3-level inverter and the settling time of MLI is much smaller than a 3-level inverter. On the basis of these conclusions, MLI has superior performance as compared to 3-level inverters in Table 8.

The comparison given in Table 8 shows that the proposed multilevel GCIs have superior performance and stability as compared to 3-level GCIs.

VII. CONCLUSION

A hybrid frame controller where the synchronous frame is used for the current regulator and the stationary framed controller is used for the adaptive harmonic compensator. A multilevel GCI with a hybrid framed controller is presented in this research paper. The multilevel inverter used is a cascaded symmetric multilevel inverter with reduced switches and an equal sharing of sources. The proposed MLI has low THD and increased power handling capability and increasing power handling capability. The PLL used for synchronization of grid voltage and inverter current is SOGI-based PLL which removes unwanted signals from the sensing voltage signal and helps to increase robustness. Moreover, the same PLL is used for estimation of frequencies of the first four odd harmonics which are used in adaptive harmonic compensators. The proposed control improved the performance of the inverter by decreasing the THD and increasing the robustness of the grid impedance and frequency variation. The proposed solution is also compared with relevant research published in recent years and it is found the proposed solution is better in terms of THD reduction.

REFERENCES

[1] A. J. Headley and D. A. Copp, "Energy storage sizing for grid compatibility of intermittent renewable resources: A California case study," *Energy*, vol. 198, May 2020, Art. no. 117310.

[2] E. Y. Pramono and S. Isnandar, "Criteria for integration of intermittent renewable energy to the Java Bali grid," in *Proc. Int. Conf. High Voltage Eng. Power Syst. (ICHVEPS)*, Oct. 2017, pp. 91–94.

[3] A. Etxegarai, P. Eguia, E. Torres, A. Iturregi, and V. Valverde, "Review of grid connection requirements for generation assets in weak power grids," *Renew. Sustain. Energy Rev.*, vol. 41, pp. 1501–1514, Jan. 2015.

[4] L. Huang, C. Wu, D. Zhou, and F. Blaabjerg, "Impact of grid strength and impedance characteristics on the maximum power transfer capability of grid-connected inverters," *Appl. Sci.*, vol. 11, no. 9, p. 4288, May 2021.

[5] *Integrating Inverter-Based Resources Into Low Short Circuit Strength Systems*, NERC, Atlanta, GA, USA, 2017.

[6] J. Xu, S. Xie, Q. Qian, and B. Zhang, "Adaptive feedforward algorithm without grid impedance estimation for inverters to suppress grid current instabilities and harmonics due to grid impedance and grid voltage distortion," *IEEE Trans. Ind. Electron.*, vol. 64, no. 9, pp. 7574–7586, Sep. 2017.

[7] J. Xu, Q. Qian, B. Zhang, and S. Xie, "Harmonics and stability analysis of single-phase grid-connected inverters in distributed power generation systems considering phase-locked loop impact," *IEEE Trans. Sustain. Energy*, vol. 10, no. 3, pp. 1470–1480, Jul. 2019.

[8] N. P. W. Strachan and D. Jovcic, "Stability of a variable-speed permanent magnet wind generator with weak AC grids," *IEEE Trans. Power Del.*, vol. 25, no. 4, pp. 2779–2788, Oct. 2010.

[9] J. Sun, "Impedance-based stability criterion for grid-connected inverters," *IEEE Trans. Power Electron.*, vol. 26, no. 11, pp. 3075–3078, Nov. 2011.

[10] Y. Liao and X. Wang, "Impedance-based stability analysis for interconnected converter systems with open-loop RHP poles," *IEEE Trans. Power Electron.*, vol. 35, no. 4, pp. 4388–4397, Apr. 2020.

[11] A. M. Mnider, D. J. Atkinson, M. Dahidah, and M. Armstrong, "A simplified DQ controller for single-phase grid-connected PV inverters," in *Proc. 7th Int. Renew. Energy Congr. (IREC)*, Mar. 2016, pp. 1–6.

[12] C. Bao, X. Ruan, X. Wang, W. Li, D. Pan, and K. Weng, "Step-by-step controller design for LCL-type grid-connected inverter with capacitor–current-feedback active-damping," *IEEE Trans. Power Electron.*, vol. 29, no. 3, pp. 1239–1253, Mar. 2014.

[13] R. A. Khan and W. Choi, "An improved harmonic compensation method for a single-phase grid connected inverter," *Trans. Korean Inst. Power Electron.*, vol. 24, no. 3, pp. 215–227, 2019.

[14] A. V. Timbus, M. Ciobotaru, R. Teodorescu, and F. Blaabjerg, "Adaptive resonant controller for grid-connected converters in distributed power genaration systems," in *Proc. 21st Annu. IEEE Appl. Power Electron. Conf. Expo.*, Apr. 2006, p. 6.

[15] S. Golestan, E. Ebrahimzadeh, J. M. Guerrero, and J. C. Vasquez, "An adaptive resonant regulator for single-phase grid-tied VSCs," *IEEE Trans. Power Electron.*, vol. 33, no. 3, pp. 1867–1873, Mar. 2017.

[16] J. Xu, Q. Qian, S. Xie, and B. Zhang, "Grid-voltage feedforward based control for grid-connected LCL-filtered inverter with high robustness and low grid current distortion in weak grid," in *Proc. IEEE Appl. Power Electron. Conf. Expo. (APEC)*, Mar. 2016, pp. 1919–1925.

[17] K. G. Khajeh, F. Farajizadeh, D. Solatialkaran, F. Zare, J. Yaghoobi, and N. Mithulananthan, "A full-feedforward technique to mitigate the grid distortion effect on parallel grid-tied inverters," *IEEE Trans. Power Electron.*, vol. 37, no. 7, pp. 8404–8419, Jul. 2022.

[18] X. Wang, K. Qin, X. Ruan, D. Pan, Y. He, and F. Liu, "A robust grid-voltage feedforward scheme to improve adaptability of grid-connected inverter to weak grid condition," *IEEE Trans. Power Electron.*, vol. 36, no. 2, pp. 2384–2395, Feb. 2021.

[19] X. Wang, X. Ruan, S. Liu, and C. K. Tse, "Full feedforward of grid voltage for grid-connected inverter with LCL filter to suppress current distortion due to grid voltage harmonics," *IEEE Trans. Power Electron.*, vol. 25, no. 12, pp. 3119–3127, Dec. 2010.

[20] Y. Hu, J. Xu, H. Qian, S. Bian, and S. Xie, "Robustness and harmonics suppression of grid-connected inverters with different grid voltage feedforward compensations in weak grid," in *Proc. IEEE 29th Int. Symp. Ind. Electron. (ISIE)*, Jun. 2020, pp. 779–784.

[21] T. Muhammad, A. U. Khan, H. Jan, M. Y. Usman, J. Javed, and A. Aslam, "Cascaded symmetric multilevel inverter with reduced number of controlled switches," *Int. J. Power Electron. Drive Syst. (IJPEDS)*, vol. 8, no. 2, p. 795, Jun. 2017.

[22] S. Choudhury, M. Bajaj, T. Dash, S. Kamel, and F. Jurado, "Multilevel inverter: A survey on classical and advanced topologies, control schemes, applications to power system and future prospects," *Energies*, vol. 14, no. 18, p. 5773, Sep. 2021.

[23] X. Zhang, T. Zhao, W. Mao, D. Tan, and L. Chang, "Multilevel inverters for grid-connected photovoltaic applications: Examining emerging trends," *IEEE Power Electron. Mag.*, vol. 5, no. 4, pp. 32–41, Dec. 2018.

[24] S. Kouro, M. Malinowski, K. Gopakumar, J. Pou, L. G. Franquelo, B. Wu, J. Rodriguez, M. A. Pérez, and J. I. Leon, "Recent advances and industrial applications of multilevel converters," *IEEE Trans. Ind. Electron.*, vol. 57, no. 8, pp. 2553–2580, Aug. 2010.

[25] D. Batool, Q. Malik, T. Muhammad, A. U. Khan, and J. Kim, "Comparative study on minimization of conduction and switching losses in cascaded multilevel inverter via reduced switches and equal voltage source-sharing," *Circuit World*, vol. 2022, pp. 1–21, Mar. 2022.

[26] N. Prabaharan and K. Palanisamy, "A comprehensive review on reduced switch multilevel inverter topologies, modulation techniques and applications," *Renew. Sustain. Energy Rev.*, vol. 76, pp. 1248–1282, Sep. 2017.

[27] R. Naderi and A. Rahmati, "Phase-shifted carrier PWM technique for general cascaded inverters," *IEEE Trans. Power Electron.*, vol. 23, no. 3, pp. 1257–1269, May 2008.

[28] K. Hasan, S. T. Meraj, M. M. Othman, M. S. H. Lipu, M. A. Hannan, and K. M. Muttaqi, "Savitzky–Golay filter-based PLL: Modeling and performance validation," *IEEE Trans. Instrum. Meas.*, vol. 71, pp. 1–6, 2022.

[29] W. Xu, C. Huang, and H. Jiang, "Analyses and enhancement of linear Kalman-filter-based phase-locked loop," *IEEE Trans. Instrum. Meas.*, vol. 70, pp. 1–10, 2021.

[30] S. Golestan, J. M. Guerrero, A. Vidal, A. G. Yepes, and J. Doval-Gandoy, "PLL with MAF-based prefiltering stage: Small-signal modeling and performance enhancement," *IEEE Trans. Power Electron.*, vol. 31, no. 6, pp. 4013–4019, Jun. 2016.

[31] Y. Hoon, M. A. M. Radzi, M. K. Hassan, and N. F. Mailah, "Operation of three-level inverter-based shunt active power filter under nonideal grid voltage conditions with dual fundamental component extraction," *IEEE Trans. Power Electron.*, vol. 33, no. 9, pp. 7558–7570, Sep. 2018.

[32] C. R. D. Osorio, G. G. Koch, H. Pinheiro, R. C. L. F. Oliveira, and V. F. Montagner, "Robust current control of grid-tied inverters affected by LCL filter soft-saturation," *IEEE Trans. Ind. Electron.*, vol. 67, no. 8, pp. 6550–6561, Aug. 2020.

[33] H. Safamehr, T. A. Najafabadi, and F. R. Salmasi, "Adaptive control of grid-connected inverters with nonlinear LC filters," *IEEE Trans. Power Electron.*, vol. 38, no. 2, pp. 1562–1570, Feb. 2023.

[34] Y. Yang, K. Zhou, H. Wang, F. Blaabjerg, D. Wang, and B. Zhang, "Frequency adaptive selective harmonic control for grid-connected inverters," *IEEE Trans. Power Electron.*, vol. 30, no. 7, pp. 3912–3924, Jul. 2015.

[35] J. Ye, L. Liu, J. Xu, and A. Shen, "Frequency adaptive proportional-repetitive control for grid-connected inverters," *IEEE Trans. Ind. Electron.*, vol. 68, no. 9, pp. 7965–7974, Sep. 2021.

[36] T. Muhammad, A. U. Khan, M. T. Chughtai, R. A. Khan, Y. Abid, M. Islam, and S. Khan, "An adaptive hybrid control of grid tied inverter for the reduction of total harmonic distortion and improvement of robustness against grid impedance variation," *Energies*, vol. 15, no. 13, p. 4724, Jun. 2022.

[37] Z. Pan, X. Wang, Q. Guan, Y. Chen, and L. Tian, "Adaptive current harmonics suppression strategy for grid-tie inverters," *ISA Trans.*, vol. 128, pp. 698–710, Sep. 2022.

TILA MUHAMMAD received the B.S. and M.S. degrees in electronic engineering from International Islamic University Islamabad, in 2010 and 2015, respectively, where he is currently pursuing the Ph.D. degree in electrical engineering. He is currently a Faculty Member with the Department of Electrical and Computer Engineering, International Islamic University Islamabad. He is working on power electronic converters, specifically on grid-connected inverters and power drives. He has experience of more than ten years of working on the design and development of power electronic converters. Recently, he started working on the development of smart electrical technology for agriculture.

ADNAN UMAR KHAN received the B.B. degree in electrical and electronic engineering from Eastern Mediterranean University, Cyprus, in 1994, the M.S. degree in communication systems from the University of Portsmouth, U.K., in 1995, and the Ph.D. degree from De Montfort University, U.K. He is currently an Assistant Professor with the Department of Electrical Engineering, International Islamic University Islamabad, Pakistan.

YOUSRA ABID received the B.S. degree in electronic engineering from International Islamic University Islamabad, in 2018, and the M.S. degree in electrical engineering from Air University, Islamabad, in 2021. She is currently pursuing the Ph.D. degree with the Centre for Advance Electronics and Photovoltaic Engineering on the Pakistan–U.K. mutual project for energy harvesting and storage at International Islamic University Islamabad. Her research interest includes power electronic converters.

MUHAMMAD HILAL KHAN received the B.Sc. degree in electrical engineering from the University of Engineering and Technology, Peshawar, in 2007, the M.Sc. degree in electrical engineering from the University of Engineering and Technology, Taxila, in 2012, and the Ph.D. degree in electrical engineering from the CECOS University of IT and Emerging Sciences, Peshawar, in 2021. His research interests include renewable energy, microgrid, smart grids, power electronic applications in power systems, and smart transformers.

NASIM ULLAH received the B.Sc. degree in electrical engineering from the University of Engineering and Technology, Peshawar, in 2004, and the Ph.D. degree in mechatronics engineering from Beihang University, Beijing, China, in 2013. He is currently a Professor with the Electrical Engineering Department, Taif University, Saudi Arabia. His research interests include renewable energy, microgrid, smart grids, power electronic applications in power systems, smart transformers, robotics, and flight control systems. He has completed several research projects funded by the Deanship of Scientific Research, Taif University, and the Ministry of Education, Saudi Arabia, as a Principal Investigator (PI). He has authored/coauthored more than 200 research articles in peer-review journals and contributed several book chapters.

VOJTECH BLAZEK was born in the Czech Republic, in 1991. He received the Ing. degree from the Department of Electrical Engineering, VSB—Technical University of Ostrava, in 2016, where he is currently pursuing the internal doctoral student degree. He is currently a Junior Researcher with the research Centre ENET—Energy Units for Utilization of Non-Traditional Energy Sources. His current work includes developing modern and green technologies in off-grid systems with vehicle-to-home technologies.

LUKAS PROKOP graduated (Ing.) in electrical power engineering from FEEC Brno. He was an Associate Professor with FEI TU Ostrava. He is currently engaged in renewable energy sources, modern technologies, and methods in electrical power engineering and electrical measurements. He is a research team member of Czech and international research projects. He serves as the Deputy Head for the ENET Research Centre.

STANISLAV MISÁK was born in the Czech Republic, in 1978. He received the Ing. and Ph.D. degrees from the Department of Electrical Engineering, VSB—Technical University of Ostrava, in 2003 and 2007, respectively. He is currently a Professor and the CEO of the Research Centre ENET and the Centre for Energy and Environmental Technologies. He holds a patent for a fault detector for medium-voltage power lines. His current work includes the implementation of smart grid technologies using prediction models and bio-inspired methods.