

RESEARCH ARTICLE

A Modified PI-Controller Based High Current Density DC–DC Converter for EV Charging Applications

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ABSTRACT Electric vehicles (EVs) are getting more popular in automobiles due to environmental factors. Since electric vehicles manage their power from the rechargeable battery, therefore, it's essential to have a reliable, efficient, and economical battery charger to provide stable required output for the specified EV's battery. In this paper, a DC-DC converter with a modified PI controller has been presented which helps to achieve the required output voltage and high current density with negligible overshoot for the specified lithium-ion battery system to minimize the charging time. Apart from minimizing the power loss of the active switches, the proposed system minimizes the junction temperature eventually improving the life cycle of the converter. The analysis of the proposed converter is performed both in ideal and non-ideal conditions. The power loss of the active switches and the junction temperature have also been analyzed. An effective and economical dc and ac side inductors have been designed and analyzed the performance of total power loss and temperature rise. The results show that the proposed converter can maintain a power factor around 90% and a total harmonic distortion around 0.46%, which is ideal for the high-density load current. The reliability of the dc-dc converter is also evaluated. A hardware prototype has also been implemented to confirm its viability for EV battery charging applications.

INDEX TERMS Buck, lithium-ion battery charger, electric vehicle battery charger, ac-dc converter, isolated ac-dc converter, power factor correction, MOSFET power loss estimation, MOSFET thermal analysis, modified PI controller, state-space representation of converter.

I. INTRODUCTION

In electric vehicles (EVs) the rechargeable battery is one of the important and sophisticated systems which deliver power to run the EVs. So, it is important to have an efficient, reliable, and economical battery charger for EVs. An AC-DC converter is needed to full fill the requirement [1], [2], [3], [4], [5].

An AC-DC converter can be isolated or non-isolated. In the non-isolated system, the diode and active switch do face more stress which conveys more power loss will take place. Consequently, the temperature will be higher, and since iso-

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lation is not present it might be an issue in terms of safety. Whereas in an isolated system the diode and active switch might face less stress since the voltage can be lowered to maintain the requirement which states that the power loss will be lower, and the temperature will be lower in the junction of these devices besides the safety factor will be higher since its isolated. Consequently, improve the reliability of the overall system [6].

To perform the AC-DC operation the conventional diode rectifier might be used which leads to more power loss consequently the power factor as well as THD degrades. To maintain the PFC topology might be used which is complicated and costly [7], [8], [9], [10], [11], [12], [13], [14], [15], [16], [17], [18]. To get rid of it a low-frequency

coupled inductor-based AC-DC converter has been used which is associated with a LCL filter and two diodes [19], [20], [21], [22]. Afterward, the voltage might need to be regulated according to the lithium-ion battery's condition. To fulfill this task, a closed-loop DC-DC converter can be used. The conventional closed-loop DC-DC converter dissipates high power loss in the active switches which might decay the life cycle of the overall system. The most power loss occurs in conventional closed-loop DC-DC converters due to conduction, switching, and leakage power losses [23]. Besides, the overshoot does present at the output voltage and current which might be ailing the lithium-ion battery [24].

To conquer a modified proportional integral (MPI) controller be bought from our previous work and again modified which helps to reduce not only the overshoot at the output voltage and current but also to reduce the conduction power loss, switching power loss, and leakage power loss [25], [26]. Besides, the current prosecution has also been improved. This implies total power loss will be reduced without sacrificing the switching frequency that helps to maintain the size of passive components.

With the active switch, the thermal management heatsink has been addressed which helps to maintain the junction temperature by increasing the surface area associated with ambient [27], [28].

This paper presents a reliable, efficient, and economical AC-DC converter for charging Electric Vehicles' lithium-ion battery. A detailed analysis of the converter as well as the power loss and junction temperature of the MOSFETs also be analyzed with three different conditions. At the end, the hardware prototype's consequence is also presented to validate the proposed prosecution.

II. PROPOSED SYSTEM

The proposed system is depicted in Figure 1. The single-phase ac source delivers power to the load. Adjacent to the ac source the LCL network has been assigned for filtering purposes. It also helps to manipulate the power factor and THD. The two diodes D5 and D6 help to manipulate the ac flow to the primary side of the coupled inductor. From the secondary side of the coupled inductor, the rippled dc has been obtained. The RC3, RC4, C3, and C4 help to reduce the dc ripples. Afterward, the four MOSFETs M1, M2, M3, and M4 help to manipulate the dc output voltage based on the consequence of the load. The other diodes D1, D2, D3, and D4 help to maintain the dc flow. Components like L1, L2, and C1 are responsible for storing and filtering purposes. The two fuses F1 and F2 are assigned for protection. Eventually, the Lithium-Ion battery (48V 100Ah) was used as a load.

III. AC-DC SYSTEM WITH LCL FILTER

Single phase ac does change the phase so this system will have two different modes and discussed hereunder.

IV. MODE ONE

At 0° - 180° supply voltage, this mode would take place and L3, L4, D5, and L5 are in conduction mode whereas D6 is in non-conduction mode consequently generating positive voltage at L7 and depicted in Figure 2(a).

V. MODE TWO

At 180° - 360° supply voltage, this mode would take place and L6, D6, L4, and L3 are in conduction mode whereas D5 is in non-conduction mode and again generating a positive voltage at L7 as depicted in Figure 2(b).

VI. DESIGN AND ANALYSIS OF LCL FILTER

The grid current can be estimated based on equation 1.

$$I_{\text{Grid}} = \frac{\sqrt{2} \times P_{\text{Load}}}{V_{\text{AC}}} \text{A} \quad (1)$$

The required inductance can be computed using equation 2.

$$L = \frac{x_L}{2 \times \pi \times f_{\text{AC}}} \text{H} \quad (2)$$

where, $x_L = \text{Inductor reactance} = 2\pi fL$

The L3 and L4 will be half of the inductance that has been calculated.

The ac side capacitance can be calculated as

$$C2 = \frac{1\% \times P_{\text{Load}}}{2 \times \pi \times f_{\text{AC}} \times V_{\text{AC}}^2} \text{F} \quad (3)$$

The resonant frequency can be computed as

$$F_r = \frac{1}{2 \times \pi \times \sqrt{\frac{L3 \times L4}{L3+L4} \times C2}} \text{Hz} \quad (4)$$

The damping resistance can be calculated as

$$R_d = \frac{1}{6 \times \pi \times F_r \times C2} \text{ohm} \quad (5)$$

where, $f_{\text{AC}} = \text{Grid frequency}$, $P_{\text{Load}} = \text{Filter load power}$.

The designed filter frequency response can be analyzed based on the transfer function and given herewith.

$$\text{SYS (s)} = \frac{R_d \times C2s + 1}{L3 \times L4 \times C2s^3 + (L3 + L4) \times R_d \times C2s^2 + (L3 + L4)s} \quad (6)$$

After manipulating the above equations, the bode plot has been computed and depicted in Figure 3. The Figure implicates the consequences of the designed filter frequency response and the stability. After adding the damping resistor, the overall response smooths and minimizes the spike that is associated with the system besides when the damping resistor was not concerned spikes do take place. Consequently, the designed filter exhibits more stability while the damping resistor is integrated.

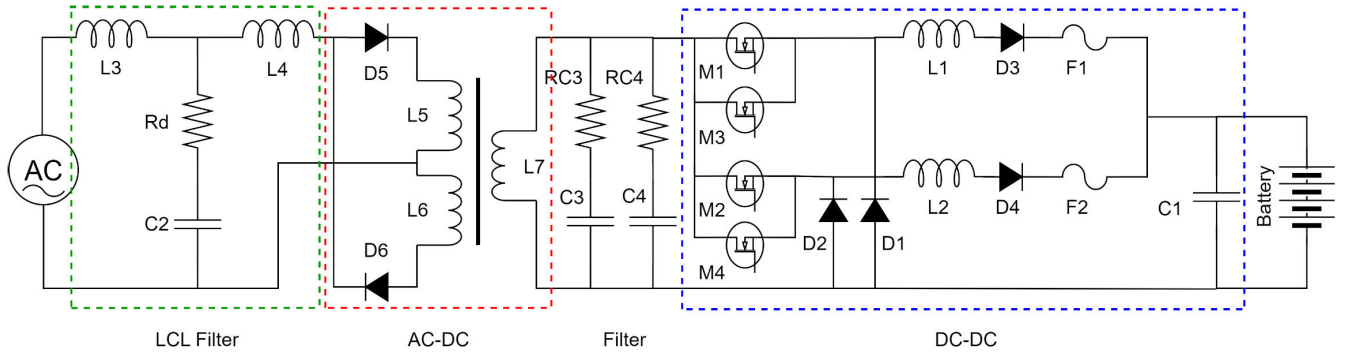


FIGURE 1. Proposed system.

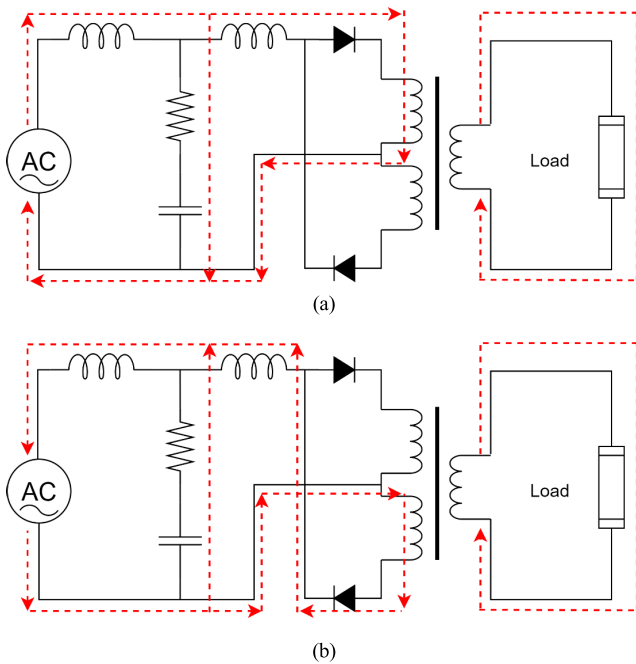


FIGURE 2. Working modes of the AC-DC converter with LCL filter (a) MODE ONE and (b) MODE TWO.

VII. STEADY STATE ANALYSIS OF THE PROPOSED DC-DC SYSTEM

A. IDEAL CONDITION

All the components are assumed to be ideal for this analysis. Besides the switching frequency and the duty cycle has considered being fixed. The system is being analyzed in open-loop continuous conduction mode. The proposed DC-DC converter has four modes and has been discussed herewith.

1) MODE ONE

The converter has analyzed at $0 < t < DT$ s period. At this moment MOSFETs one and two are in conduction mode whereas, MOSFETs three, four and diodes one and two are in non-conduction mode. The left side of inductors one and

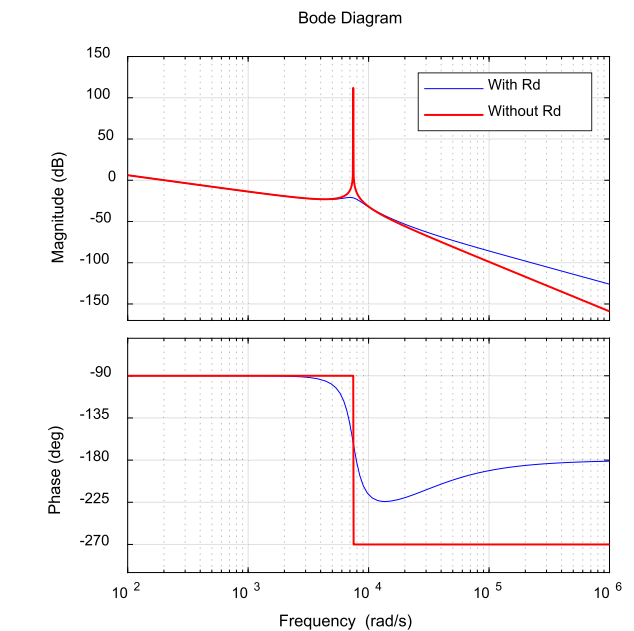


FIGURE 3. Bode plot of the designed LCL filter.

two are now connected to the input source as shown in Figure 4(a). The important equations of this mode have been given hereunder.

$$v_{L1} = V_g - V_o \tag{7}$$

$$v_{L2} = V_g - V_o \tag{8}$$

$$\frac{di_{L1}}{dt} = \frac{V_g - V_o}{L1} \tag{9}$$

$$\frac{di_{L2}}{dt} = \frac{V_g - V_o}{L2} \tag{10}$$

$$i_{C1} = I_{L12} - I_o \tag{11}$$

2) MODE TWO

The converter has now been analyzed at $DTs < t < Ts$ period. This time four MOSFETs are in non-conduction mode. Diodes one and two are now in conduction mode. The left side of inductors one and two have connected to the

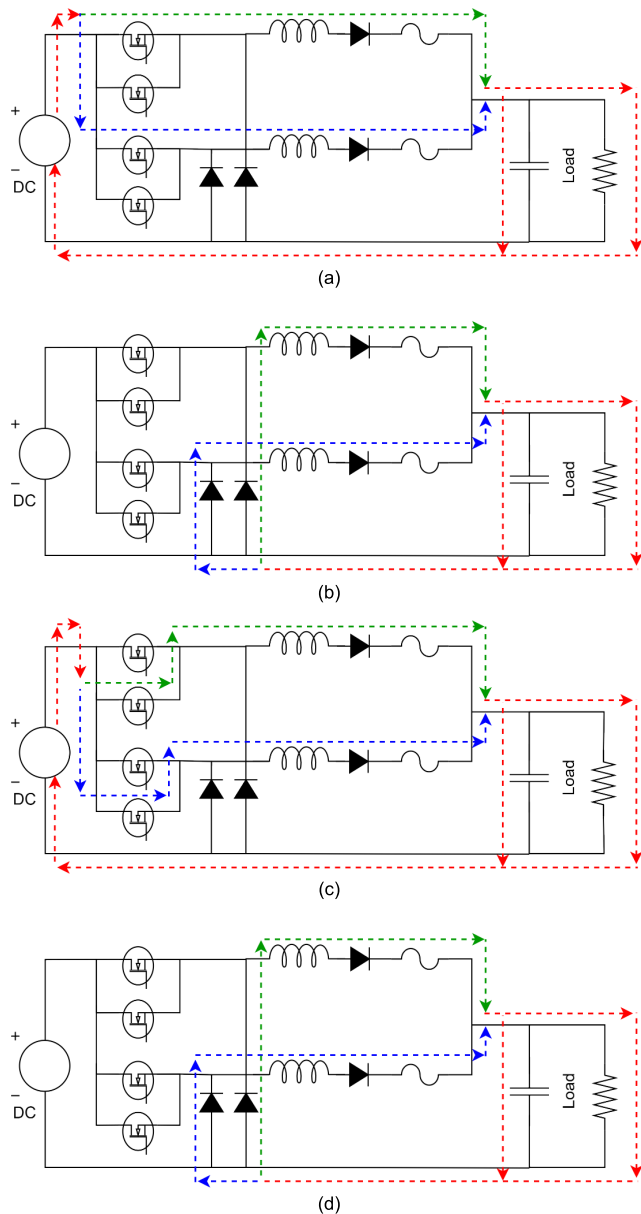


FIGURE 4. Working modes of the proposed DC-DC converter: (a) **MODE ONE** (b) **MODE TWO** (c) **MODE THREE** and (d) **MODE FOUR**.

ground and the circuit becomes Figure 4(b). The important equations in this mode are.

$$v_{L1} = -V_o \tag{12}$$

$$v_{L2} = -V_o \tag{13}$$

$$\frac{di_{L1}}{dt} = \frac{-V_o}{L1} \tag{14}$$

$$\frac{di_{L2}}{dt} = \frac{-V_o}{L2} \tag{15}$$

$$i_{C1} = I_{L12} - I_o \tag{16}$$

3) MODE THREE

The converter has now been analyzed at $T_s < t < 2DT_s$ period. This time MOSFETs three and four are in conduction mode whereas MOSFETs one and two and diodes one and

two are in non-conduction mode. The left side of inductors have again connected to the input voltage leading to the circuit of Figure 4(c). The important equations are.

$$v_{L1} = V_g - V_o \tag{17}$$

$$v_{L2} = V_g - V_o \tag{18}$$

$$\frac{di_{L1}}{dt} = \frac{V_g - V_o}{L1} \tag{19}$$

$$\frac{di_{L2}}{dt} = \frac{V_g - V_o}{L2} \tag{20}$$

$$i_{C1} = I_{L12} - I_o \tag{21}$$

4) MODE FOUR

The converter has now been analyzed at $2DT_s < t < 2T_s$ period. This time four MOSFETs again are in non-conduction mode whereas diodes one and two are in conduction mode. The left side of inductors have again connected to the ground and the circuit becomes Figure 4(d). The important equations are.

$$v_{L1} = -V_o \tag{22}$$

$$v_{L2} = -V_o \tag{23}$$

$$\frac{di_{L1}}{dt} = \frac{-V_o}{L1} \tag{24}$$

$$\frac{di_{L2}}{dt} = \frac{-V_o}{L2} \tag{25}$$

$$i_{C1} = I_{L12} - I_o \tag{26}$$

Based on equations 7 to 26, inductor’s voltage, current, and capacitor current waveforms have been plotted in Figure 5 in terms of the switching pattern of four MOSFETs.

The graphs imply that the inductor’s voltage and current waveforms complete their one complete cycle at every nT_s point consequently the inductors encounter twice the switching frequency than the MOSFETs. Eventually, this helps to reduce the inductors and capacitor size while the junior rating MOSFETs in terms of switching frequency and conduction capability can be utilized besides the power loss of MOSFETs would be reduced and discussed afterward. The dc conversion ratio for L1 and L2 at $0 < t < T_s$ would be.

$$L1 = G1 = D \tag{27}$$

$$L2 = G2 = D \tag{28}$$

Besides at $T_s < t < 2T_s$ the dc conversion ratio for L1 and L2 would be.

$$L1 = G1 = D \tag{29}$$

$$L2 = G2 = D \tag{30}$$

After manipulating equations 27 to 30 with various duty cycles the gain vs duty cycle graph has been depicted in Figure 6. The graph itself implies that the gain increases as the duty cycle increases.

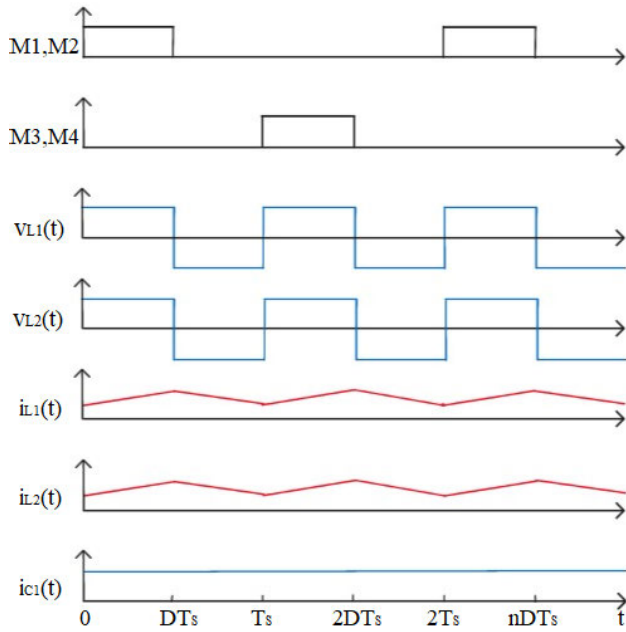


FIGURE 5. Proposed DC-DC converter waveforms: Switch or MOSFET one, two, three and four pulses (M1, M2, M3, M4), inductors voltage (v_{L1} and v_{L2}), inductors current (i_{L1} and i_{L2}) and capacitor current (i_{C1}).

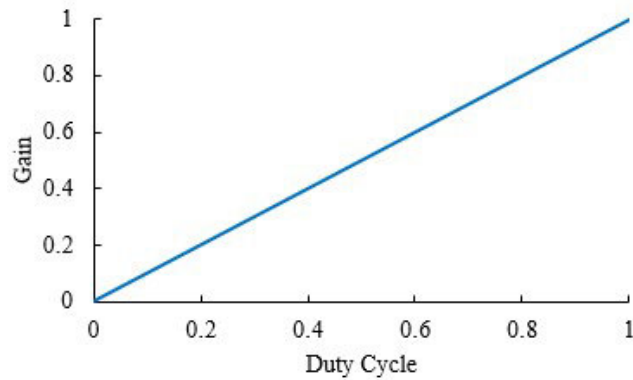


FIGURE 6. Ideal gain of the proposed DC-DC converter: G_1 at $0 < t < T_s$. G_2 at $0 < t < T_s$. G_1 at $T_s < t < 2T_s$. G_2 at $T_s < t < 2T_s$.

B. NON-IDEAL CONDITION

All the components are assumed to be non-ideal and the SUP60020E MOSFET has been selected for this analysis. The frequency and the duty cycle are assumed to be constant, and the system has been analyzed in continuous conduction mode. The proposed DC-DC system has four modes as explained in the previous section.

1) MODE ONE

The important equations of this mode are.

$$v_{L1} = V_g - V_{M1} - I_{RL1}R_{M1} - I_{RL1}R_{L1} - V_{D3} - I_{RL1}R_{D3} - I_{RL1}R_{F1} - V_o \quad (31)$$

$$v_{L2} = V_g - V_{M2} - I_{RL2}R_{M2} - I_{RL2}R_{L2} - V_{D4} - I_{RL2}R_{D4} - I_{RL2}R_{F2} - V_o \quad (32)$$

$$\frac{di_{L1}}{dt} = \frac{(V_g - V_{M1} - I_{RL1}R_{M1} - I_{RL1}R_{L1} - V_{D3} - I_{RL1}R_{D3} - I_{RL1}R_{F1} - V_o)}{L1} \quad (33)$$

$$\frac{di_{L2}}{dt} = \frac{(V_g - V_{M2} - I_{RL2}R_{M2} - I_{RL2}R_{L2} - V_{D4} - I_{RL2}R_{D4} - I_{RL2}R_{F2} - V_o)}{L2} \quad (34)$$

$$i_{C1} = I_{L12} - I_o \quad (35)$$

2) MODE TWO

The important equations of this mode are.

$$v_{L1} = -I_{RL1}R_{L1} - V_{D3} - I_{RL1}R_{D3} - I_{RL1}R_{F1} - V_o - I_{RL1}R_{D1} - V_{D1} \quad (36)$$

$$v_{L2} = -I_{RL2}R_{L2} - V_{D4} - I_{RL2}R_{D4} - I_{RL2}R_{F2} - V_o - I_{RL2}R_{D2} - V_{D2} \quad (37)$$

$$\frac{di_{L1}}{dt} = \frac{(-I_{RL1}R_{L1} - V_{D3} - I_{RL1}R_{D3} - I_{RL1}R_{F1} - V_o - I_{RL1}R_{D1} - V_{D1})}{L1} \quad (38)$$

$$\frac{di_{L2}}{dt} = \frac{(-I_{RL2}R_{L2} - V_{D4} - I_{RL2}R_{D4} - I_{RL2}R_{F2} - V_o - I_{RL2}R_{D2} - V_{D2})}{L2} \quad (39)$$

$$i_{C1} = I_{L12} - I_o \quad (40)$$

3) MODE THREE

The important equations of this mode are.

$$v_{L1} = V_g - V_{M3} - I_{RL1}R_{M3} - I_{RL1}R_{L1} - V_{D3} - I_{RL1}R_{D3} - I_{RL1}R_{F1} - V_o \quad (41)$$

$$v_{L2} = V_g - V_{M4} - I_{RL2}R_{M4} - I_{RL2}R_{L2} - V_{D4} - I_{RL2}R_{D4} - I_{RL2}R_{F2} - V_o \quad (42)$$

$$\frac{di_{L1}}{dt} = \frac{(V_g - V_{M3} - I_{RL1}R_{M3} - I_{RL1}R_{L1} - V_{D3} - I_{RL1}R_{D3} - I_{RL1}R_{F1} - V_o)}{L1} \quad (43)$$

$$\frac{di_{L2}}{dt} = \frac{(V_g - V_{M4} - I_{RL2}R_{M4} - I_{RL2}R_{L2} - V_{D4} - I_{RL2}R_{D4} - I_{RL2}R_{F2} - V_o)}{L2} \quad (44)$$

$$i_{C1} = I_{L12} - I_o \quad (45)$$

4) MODE FOUR

The important equations of this mode are.

$$v_{L1} = -I_{RL1}R_{L1} - V_{D3} - I_{RL1}R_{D3} - I_{RL1}R_{F1} - V_o - I_{RL1}R_{D1} - V_{D1} \quad (46)$$

$$v_{L2} = -I_{RL2}R_{L2} - V_{D4} - I_{RL2}R_{D4} - I_{RL2}R_{F2} - V_o - I_{RL2}R_{D2} - V_{D2} \quad (47)$$

$$\frac{di_{L1}}{dt} = \frac{(-I_{RL1}R_{L1} - V_{D3} - I_{RL1}R_{D3} - I_{RL1}R_{F1} - V_o - I_{RL1}R_{D1} - V_{D1})}{L1} \quad (48)$$

$$\frac{di_{L2}}{dt} = \frac{(-I_{RL2}R_{L2} - V_{D4} - I_{RL2}R_{D4} - I_{RL2}R_{F2} - V_o - I_{RL2}R_{D2} - V_{D2})}{L2} \quad (49)$$

$$i_{C1} = I_{L12} - I_o \quad (50)$$

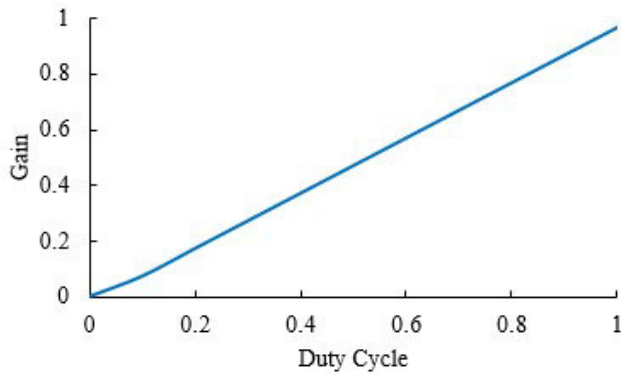


FIGURE 7. Non-Ideal gain of the proposed DC-DC converter: G1 at $0 < t < T_s$. G2 at $0 < t < T_s$. G1 at $T_s < t < 2T_s$. G2 at $T_s < t < 2T_s$.

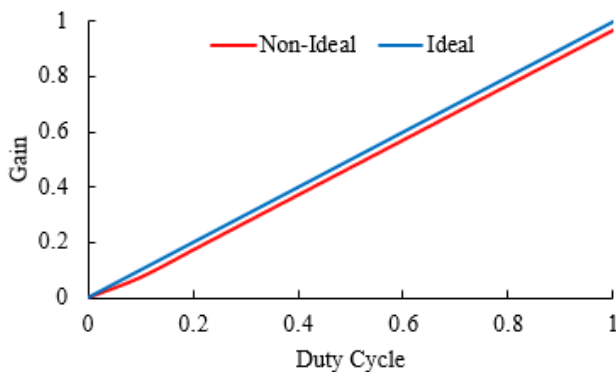


FIGURE 8. Ideal vs Non-Ideal gain comparison of the proposed DC-DC converter: G1 at $0 < t < T_s$. G2 at $0 < t < T_s$. G1 at $T_s < t < 2T_s$. G2 at $T_s < t < 2T_s$.

At $0 < t < T_s$ the dc conversion ratio for L1 and L2 would be

$$L1 = G1 = D \times \left(\frac{2 \times \left(1 - \frac{V_{M1}}{V_g} - \frac{V_{D3}}{DV_g} - \frac{D'V_{D1}}{DV_g} \right)}{\frac{DR_{M1} + R_{L1} + R_{D3} + R_{F1} + 2R + D'R_{D1}}{R}} \right) \quad (51)$$

$$L2 = G2 = D \times \left(\frac{2 \times \left(1 - \frac{V_{M2}}{V_g} - \frac{V_{D4}}{DV_g} - \frac{D'V_{D2}}{DV_g} \right)}{\frac{DR_{M2} + R_{L2} + R_{D4} + R_{F2} + 2R + D'R_{D2}}{R}} \right) \quad (52)$$

At $T_s < t < 2T_s$ the dc conversion ratio for L1 and L2 would be

$$L1 = G1 = D \times \left(\frac{2 \times \left(1 - \frac{V_{M3}}{V_g} - \frac{V_{D3}}{DV_g} - \frac{D'V_{D1}}{DV_g} \right)}{\frac{DR_{M3} + R_{L1} + R_{D3} + R_{F1} + 2R + D'R_{D1}}{R}} \right) \quad (53)$$

$$L2 = G2 = D \times \left(\frac{2 \times \left(1 - \frac{V_{M4}}{V_g} - \frac{V_{D4}}{DV_g} - \frac{D'V_{D2}}{DV_g} \right)}{\frac{DR_{M4} + R_{L2} + R_{D4} + R_{F2} + 2R + D'R_{D2}}{R}} \right) \quad (54)$$

After manipulating equations 51 to 54 with various duty cycles the gain vs duty cycle graph has been depicted in Figure 7.

The graph conveys the impact on the dc conversion ratio in terms of the non-idealities. Besides, the gain increases as the duty cycle increases.

A gain comparison has been done between ideal and non-ideal conditions and is depicted in Figure 8. The graph implies that the gain is lower in non-ideal conditions than in the ideal condition.

VIII. DESIGN OF PROPOSED CLOSED LOOP CONTROLLER

The modified proportional integral (MPI) with logic closed loop controller is depicted in Figure 9. The consequence of the modified PI controller has been shown in the previous work [25], [26]. The instantaneous desired output voltage is defined as.

$$V_{ref}(t) = nu(t) \quad (55)$$

This instantaneous desired output voltage is modified by the sample and process block which works in terms of equation 56.

$$V'_{ref}(t) = \frac{n}{m}r(t - 0) - \frac{n}{m}r(t - m) \quad (56)$$

where n and m are the desired battery output voltage and settling time. The modified desired output voltage is then compared with the actual output voltage and the resultant goes to the first PI block which is associated with the desired output current. The output of the first PI is then inverted and compared with the actual output current, and the resultant goes to the second PI block. The consequence of the second PI block goes to the PWM Modulator. The PI tuning for both the first and second blocks have been done by utilizing Zeigler-Nichols method. The PWM Generator block generates the required pulse at a given frequency based on the consequence of the second PI and the Sawtooth block. Afterward, the generated pulse goes to the logic block which controls the MOSFETs. For the first conduction period, MOSFETs one and two conduct while three and four do not conduct. And for the second conduction period, MOSFETs three and four conduct while one and two do not conduct. In the non-conduction period, all MOSFETs stay in non-conduction mode as explained in the previous section. A complete flow chart of the proposed prosecution of the closed loop system has been given in Figure 10.

IX. PROPOSED SYSTEM RESULTS ANALYSIS

The important parameters of the proposed system have been summarized in Table 1.

A comparison between the conventional PI and the proposed control system has been done and depicted in Figure 11. The graph implies that the proposed control system takes 96.98% less time to reach the steady state than the conventional PI after 1st PI controller in terms of the current control processing which makes the proposed control system computing faster. It is to be noted that the controller response shown in Figure 11 is the consequence of the 1st PI current prosecution. This is not the direct battery response. Besides

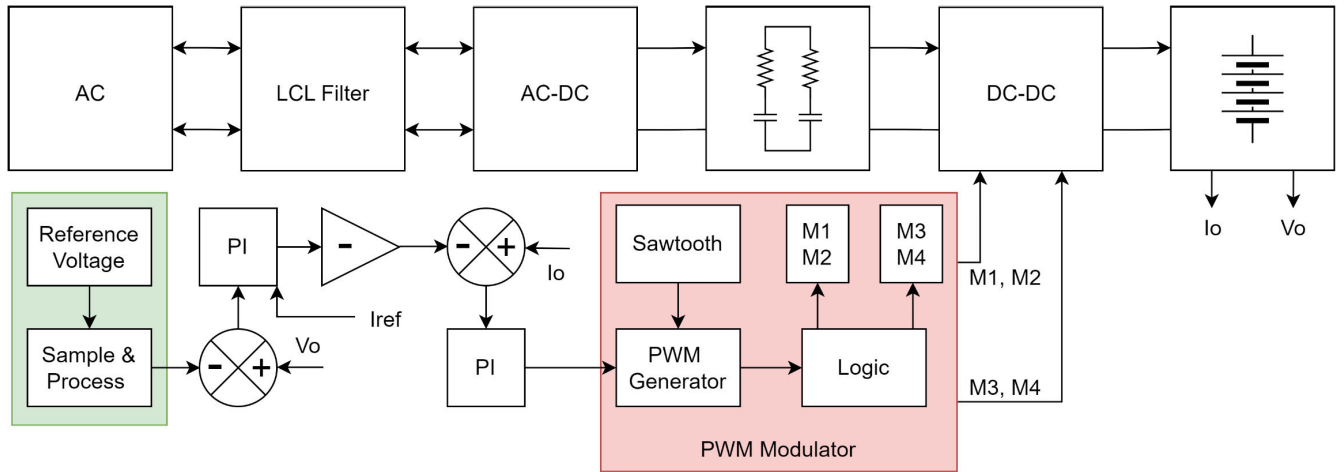


FIGURE 9. Block diagram of the closed loop proposed system.

TABLE 1. Parameters of the proposed system.

Parameters	Value
Source	Single phase AC (Grid)
Output voltage	54V
Output current	154A
Switching frequency	31kHz
DC inductor (L1, L2)	0.2mH
AC inductor (L3, L4)	2.47mH
Output capacitor (C1)	300uF
Input capacitor (C2)	14.5uF
Filter capacitor (C3, C4)	100uF

MATLAB’s lithium-ion battery model has been used for simulation.

The proposed system with the proposed prosecution has been created in MATLAB Simulink and shown in Figure 9 to charge the lithium-ion battery from a single-phase ac grid. The results have been obtained from the simulation and depicted in Figures 12 to 14. The results show that the proposed system with the proposed prosecution successfully maintained the constant required battery voltage and current with negligible overshoot while charging the lithium-ion battery. The charging current was achieved up to around 152.1A with settling time of 0.21 second. The battery voltage was maintained at around 53.3V, and the SOC increased from 60% to 60.04% within around 1 second which convey to charge to 100% the charger would require around 17 minutes which satisfies the two-level fast charging characteristics and shown in Figure 12. Besides, while charging, the grid voltage and current were almost in phase and the power factor was found to be more than 0.90, and the THD was found to be 0.46% as depicted in Figures 13 and 14 respectively.

X. POWER LOSS CALCULATION OF MOSFETS

To predict the converter’s reliability and effectiveness in terms of the proposed prosecution, the power loss of MOSFETs must be computed in non-ideal conditions. The control signal of each MOSFET and the consequence in terms of voltage and current of each MOSFET are shown in Figure 15. Where M1, M2, M3, and M4 are the control pulses and the M1p, M2p, M3p and M4p implicate the voltage and current phenomena indicated with blue and red consistently.

Figure 15. Shows that the response of MOSFETs in terms of control pulses is not instantaneous and results in power losses [29].

For MOSFETs 1 and 2 from t4 to t9 the MOSFETs are in non-conduction mode and some current is flowing and the voltage is attenuated in between t6 to t7 since the adjacent MOSFETs 3 and 4 conducts in that time and the leakage power loss is minimized and the process repeats.

For MOSFETs 3 and 4 from t5 to t8 the MOSFETs are in conduction mode and the remaining times are in non-conduction mode and the voltage generated across these two MOSFETs are attenuated at t2-t3 and t10-t11 since the MOSFETs 1 and 2 conducts and as a result the leakage power loss minimized. Figure 15 also implies that while the MOSFETs are operating the frequency and the duty cycle of each MOSFET are divided into half of the control signal which has been generated from the closed loop proposed control system consequently the conduction, switching and leakage power losses are minimized of each MOSFET.

The total power loss of each MOSFET can be computed from equation 57.

$$p_t = p_1 + p_2 + p_3 + p_4 + p_5 + p_6 \quad (57)$$

where

- p_t = Total power loss
- p_1 = Turn on delay time power loss
- p_2 = Rise time power loss
- p_3 = On time power loss

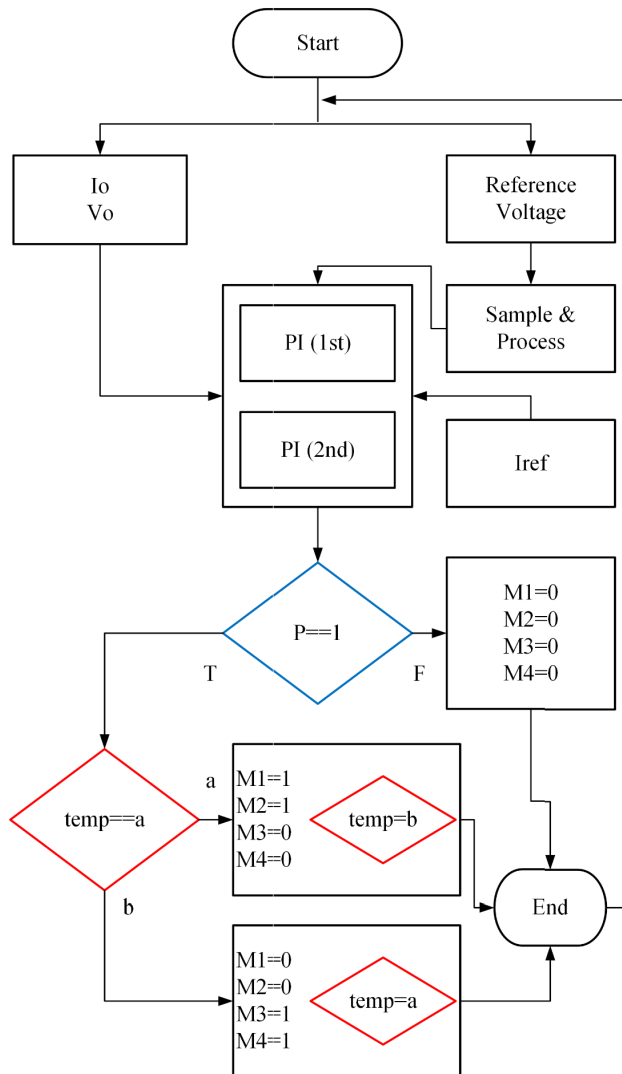


FIGURE 10. Flow chart of the proposed prosecution working principle of the closed loop proposed system.

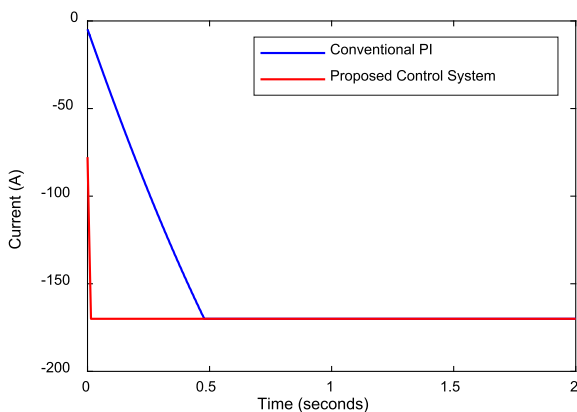


FIGURE 11. Simulated comparison between conventional PI and the proposed control system in terms of the current prosecution.

- p_4 = Turn off delay time power loss
- p_5 = Fall time power loss
- p_6 = Leakage power loss.

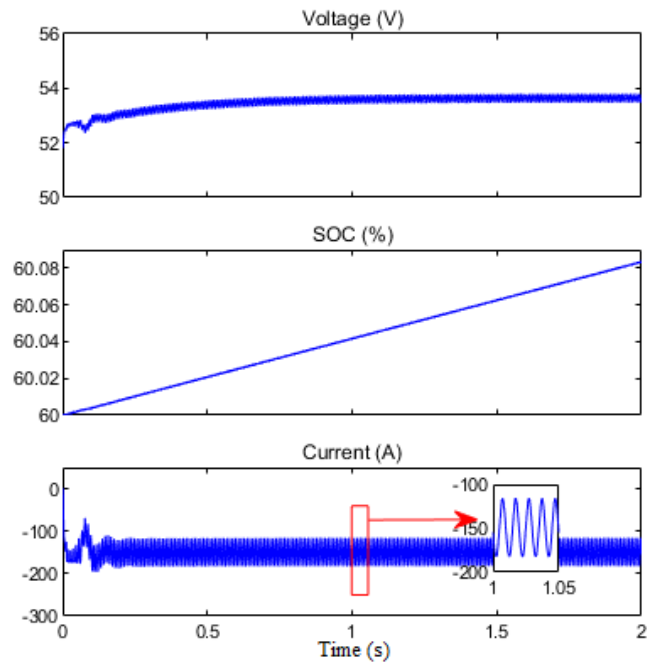


FIGURE 12. Simulated characteristics of battery voltage, soc and charging current under non-ideal condition of the proposed system with proposed prosecution.

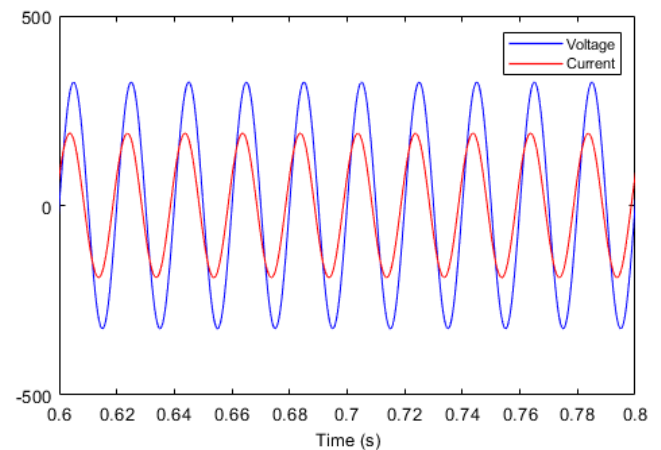


FIGURE 13. Simulated consequence of the grid voltage and current under non-ideal condition of the proposed system with proposed prosecution.

and can be computed using the following equations.

$$p_1 = V_D \times I_{DSS} \times t_{don} \times f_{sw} \quad (58)$$

$$p_2 = \frac{V_D \times I_D \times t_r \times f_{sw}}{6} \quad (59)$$

$$p_3 = I_D^2 \times R_{DSon} \times t_{on} \times f_{sw} \quad (60)$$

$$p_4 = I_D^2 \times R_{DSon} \times t_{doff} \times f_{sw} \quad (61)$$

$$p_5 = \frac{V_D \times I_D \times t_f \times f_{sw}}{6} \quad (62)$$

$$p_6 = V_D \times I_{DSS} \times t_{off} \times f_{sw} \quad (63)$$

After manipulating equations 57 to 63 with parameters from Table 1 in MATLAB simulation in the non-ideal condition

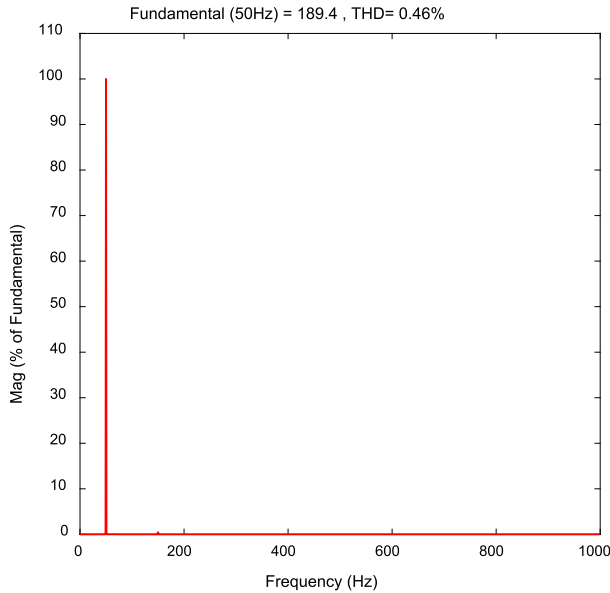


FIGURE 14. Simulated THD in terms of grid current under non-ideal condition of the proposed system with proposed prosecution.

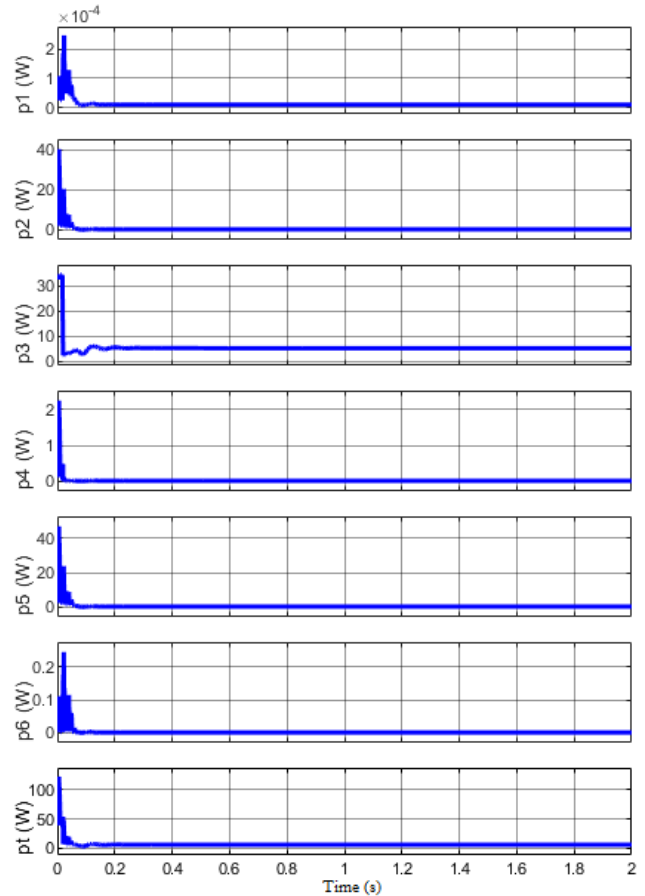


FIGURE 16. Simulated MOSFET one's power losses analysis of the proposed non-ideal converter in terms of proposed prosecution.

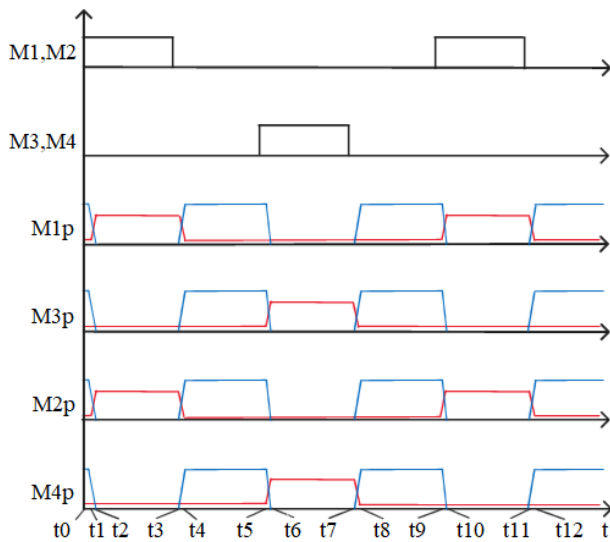


FIGURE 15. MOSFETs voltage and current waveforms of the proposed non-ideal DC-DC converter in terms of proposed prosecution.

the power losses of MOSFETs have been computed and depicted in Figures 16 to 19. These graphs imply that the MOSFETs dissipate spike power losses at the very beginning of the prosecution. The four MOSFETs' power loss patterns are almost identical. Each MOSFET generates a total power loss of 6.103W while charging the lithium-ion battery with 152.1A charging current.

A comparison between the proposed system and the reference has been done in terms of individual high-side MOSFET power losses and depicted in Figure 20 [30]. Instead of the MOSFET control logic, all the other parameters with the closed loop controller were identical in both cases.

The result shows that the proposed converter dissipates less power losses on each high-side MOSFET whereas the reference converter dissipates significant power losses on a high-side MOSFET. The total each high-side MOSFET power loss for the proposed system is about 6.103W whereas the reference high-side MOSFET dissipates almost about 37.13W while charging the lithium-ion battery with 152.1A which would increase the junction temperature of a MOSFET and decay the life cycle of the MOSFET as well as the overall system.

Figure 21 shows that instead of the leakage power loss all other power losses have been reduced. Since in the proposed converter each high-side MOSFET spends a longer time in non-conduction mode compared to the reference, that's why the leakage power loss is higher. However, the total power loss of the proposed converter in terms of each high-side MOSFET has been reduced to 83.6%.

XI. THERMAL ANALYSIS OF MOSFETS

Based on the thermal conduction method the MOSFETs junction temperature have been analyzed. The geometrical thermal connection between the junction of the MOSFET and

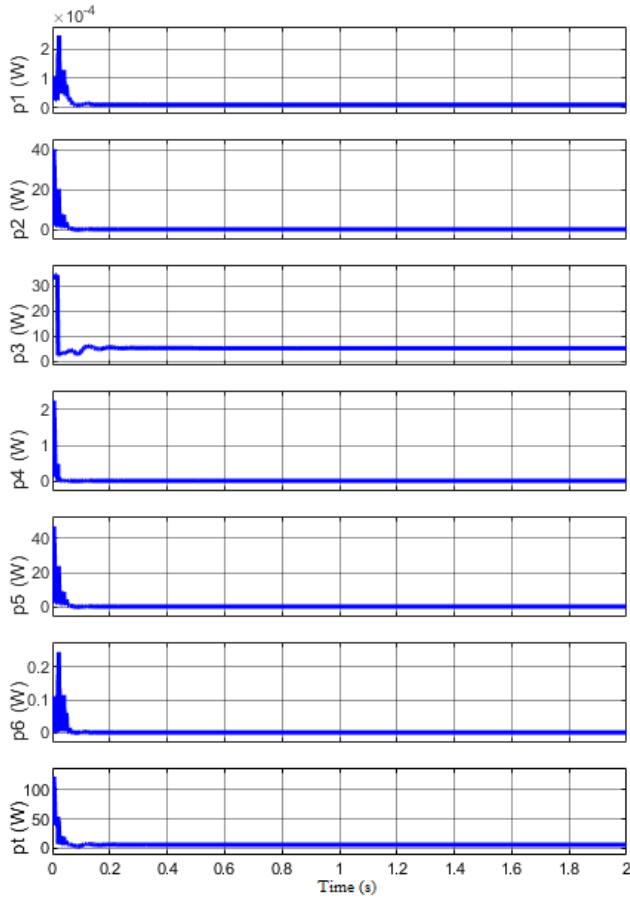


FIGURE 17. Simulated MOSFET two's power losses analysis of the proposed non-ideal converter in terms of proposed prosecution.

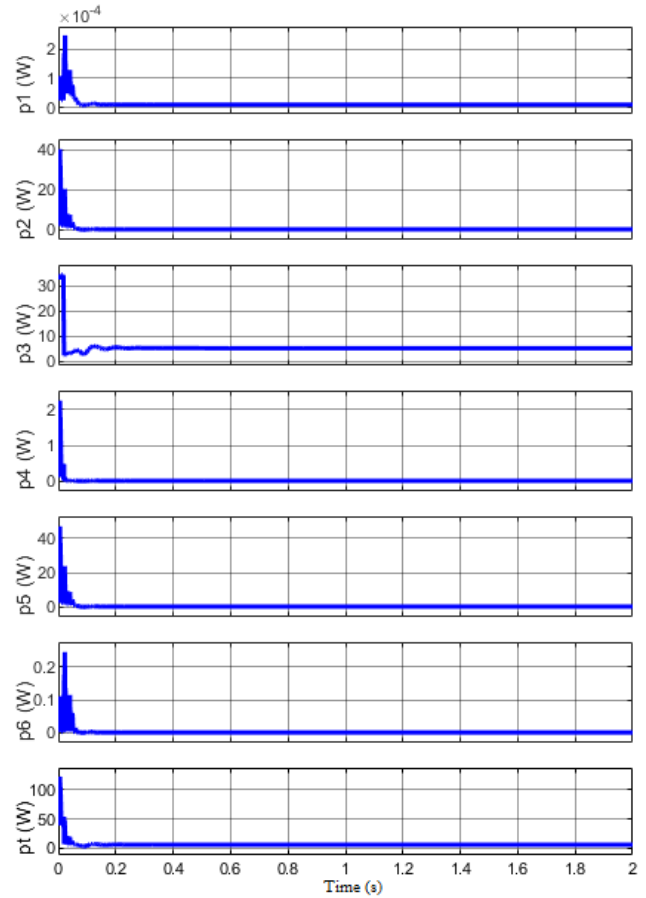


FIGURE 18. Simulated MOSFET three's power losses analysis of the proposed non-ideal converter in terms of proposed prosecution.

the heat sink has been expressed in equation 64.

$$T_j = P_t \times (R_{\theta_{ja}} + R_{\theta_{sa}} + R_{\theta_{cs}} + R_{\theta_{jc}}) + T_a \quad (64)$$

where

- T_j = MOSFET junction temperature
- P_t = MOSFET total power loss
- $R_{\theta_{ja}}$ = Junction to Air thermal conduction resistance
- $R_{\theta_{sa}}$ = Heat sink to Air thermal conduction resistance
- $R_{\theta_{cs}}$ = Case to Heat sink thermal conduction resistance
- $R_{\theta_{jc}}$ = Junction to Case thermal conduction resistance
- T_a = Ambient temperature.

Three different modes concerned with the MOSFETs junction temperature have been analyzed. MOSFET without an external heatsink and with natural cooling (t j1). MOSFET with an external heatsink and with natural cooling (t j2). MOSFET with an external heatsink and with forced cooling (t j3). For the external heatsink, the RA-T2X-64E has been chosen to perform the analysis. Besides in terms of forced cooling 500 (ft/min), airflow has been chosen at ambient temperature and assumed to be constant. Besides mica has been considered in between the external heatsink and MOSFET for better connection and isolation.

After manipulating equations 57 to 64 the MOSFETs junction temperature have been computed in three different modes by considering non-ideal conditions and depicted in Figures 22 to 25. These Figures imply that the temperature that has generated from the junction of each MOSFET is almost identical. Without an external heatsink and with natural cooling (tj1) each MOSFET generates around 271°C and a huge spike of around 1500°C takes place at the initial state. At the external heatsink and with natural cooling (tj2), each MOSFET generates around 60.055°C with an inrush temperature spike of around 250°C. After adding a cooling fan with an external heatsink (tj3), the temperature even dropped to around 33.61°C with an inrush temperature spike of 80°C. The consequence shows that at t j1 and t j2 phenomenon, there is an inrush temperature spike present which exceeds the limitation of the selected MOSFETs maximum junction temperature limit. The consequence time is low and will not degrade the MOSFET's performance immediately but keep doing it over time might degrade the reliability of the MOSFETs, so it's wise to use t j3, which inrush temperature spike is in the limitation of the selected MOSFETs maximum junction temperature limit besides this phenomenon would improve the reliability of the MOSFETs as well as the overall system.

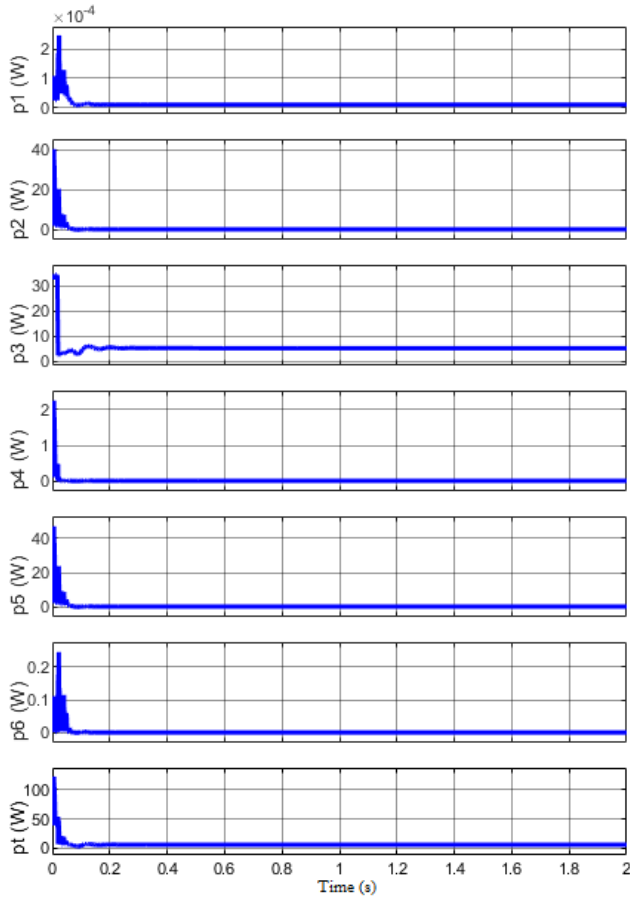


FIGURE 19. Simulated MOSFET four's power losses analysis of the proposed non-ideal converter in terms of proposed prosecution.

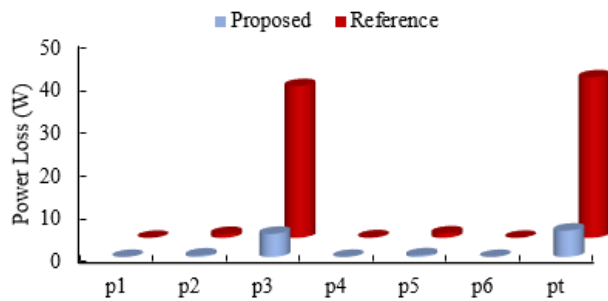


FIGURE 20. Comparison between the proposed converter (non-ideal) with proposed prosecution and the reference converter (non-ideal) in terms of individual high side MOSFET power losses.

XII. INDUCTOR DESIGN AND ANALYSIS

In every converter, the inductor plays an important role. The wrong manipulation of an inductor would increase the total power loss and temperature which may lead to saturation. Indeed, a parapet exists in size, efficiency, operating frequency, cost, and the material used in the core. In this section, economical and effective DC and AC side inductors will be designed using the Area Product approach [31].

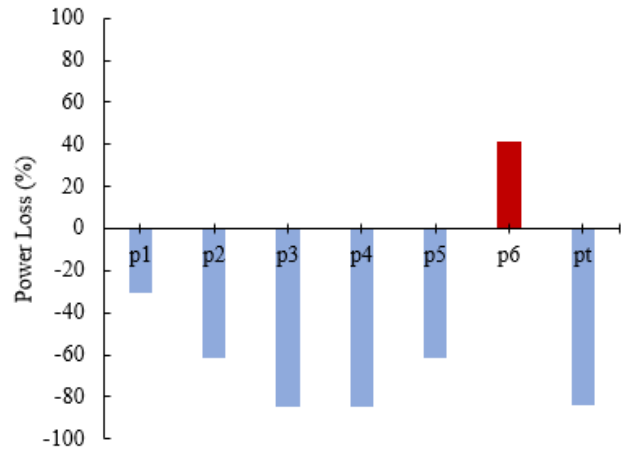


FIGURE 21. Performance improvement of the proposed converter (non-ideal) with proposed prosecution in terms of the reference converter (non-ideal) of individual high side MOSFET power losses.

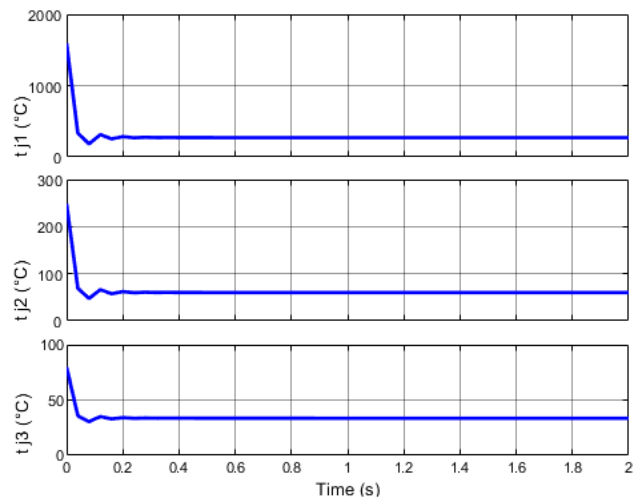


FIGURE 22. Simulated MOSFET one thermal analysis of the proposed non-ideal converter with proposed prosecution.

A. DC INDUCTOR DESIGN

All the data have been taken from simulation and Table 1 considering non-ideal conditions. Besides, two identical DC inductors have been in the proposed system.

The Area Product can be calculated, A_p

$$A_p = \frac{2(\text{Energy}) 10^4}{B_m J K_u} \left[\text{cm}^4 \right] \tag{65}$$

where, B_m = Operating flux density, J = Current density, K_u = Window utilization factor.

The closest A_p of available core must be selected.

Calculate the wire bare area, $A_{w(B)}$

$$A_{w(B)} = \frac{I_{rms}}{J} \left[\text{cm}^2 \right] \tag{66}$$

The closest $A_{w(B)}$ of available wire must be selected.

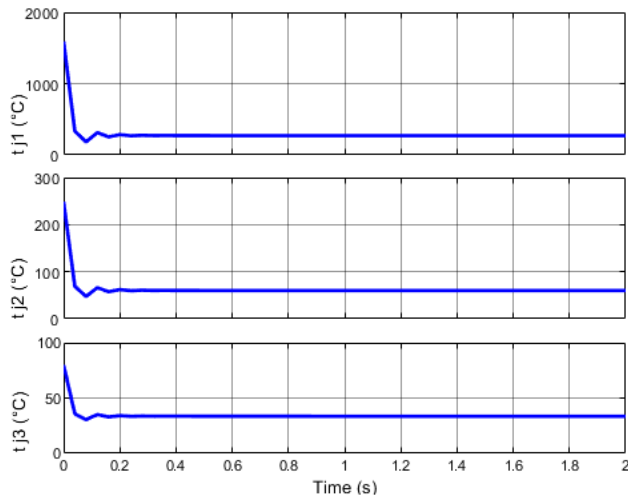


FIGURE 23. Simulated MOSFET two thermal analysis of the proposed non-ideal converter with proposed prosection.

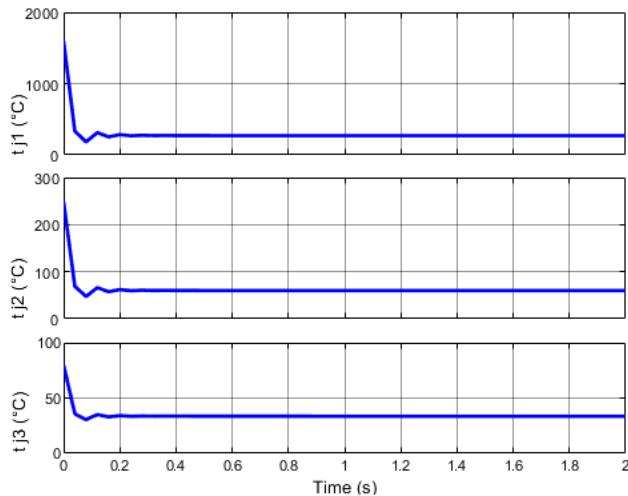


FIGURE 24. Simulated MOSFET three thermal analysis of the proposed non-ideal converter with proposed prosection.

Calculate the effective window area, $W_{a(eff)}$

$$W_{a(eff)} = W_a S_3 \text{ [cm}^2\text{]} \quad (67)$$

Calculate the number of turns using insulated wire area, N

$$N = \frac{W_{a(eff)} S_2}{A_{w(l)}} \text{ [turns]} \quad (68)$$

Calculate the required air gap, l_g

$$l_g = \frac{0.4\pi N^2 A_C 10^{-8}}{L} - \frac{MPL}{\mu_m} \text{ [cm]} \quad (69)$$

where, A_C = Iron area, L = Inductance, MPL = Magnetic path length, μ_m = Material.

Calculate the fringing flux factor, F

$$F = 1 + \frac{l_g}{\sqrt{A_C}} \ln \left(\frac{2G}{l_g} \right) \quad (70)$$

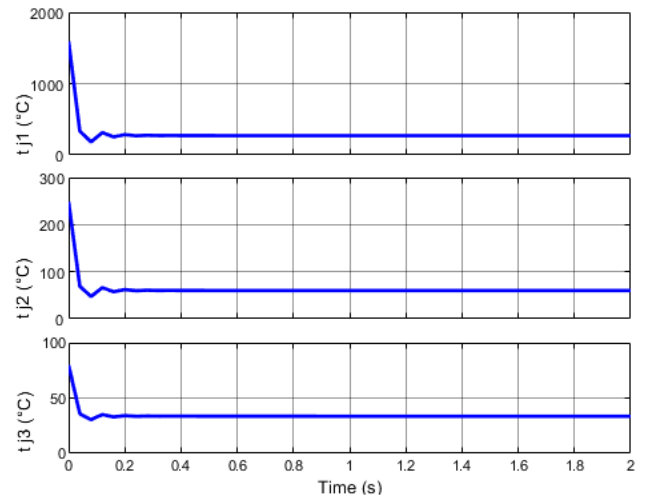


FIGURE 25. Simulated MOSFET four thermal analysis of the proposed non-ideal converter with proposed prosection.

where, G = Winding length.

Again, calculate the number of turns by utilizing the fringing flux factor, N_n

$$N_n = \sqrt{\frac{l_g L}{0.4\pi A_C F 10^{-8}}} \text{ [turns]} \quad (71)$$

Calculate the copper loss, P_{cu}

$$P_{cu} = I_{rms}^2 R_L \text{ [watts]} \quad (72)$$

where, R_L = Winding Resistance.

Calculate the AC flux density, B_{ac}

$$B_{ac} = \frac{0.4\pi N_n F \left(\frac{\Delta I}{2} \right) 10^{-4}}{l_g + \frac{MPL}{\mu_m}} \text{ [teslas]} \quad (73)$$

Calculate milliwatts per gram, mW/g

$$mW/g = k f^{mn} B_{ac}^n \quad (74)$$

where, k , m , and n are the coefficient of selected material and frequency.

Calculate the core loss, P_{fe}

$$P_{fe} = mW/g W_{tfe} 10^{-3} \text{ [watts]} \quad (75)$$

where, W_{tfe} = Core weight

Calculate the total loss, ΣP

$$\Sigma P = P_{cu} + P_{fe} \text{ [watts]} \quad (76)$$

Calculate the watt density per unit area,

$$\Psi = \frac{\Sigma P}{A_t} \left[\frac{\text{watts}}{\text{cm}^2} \right] \quad (77)$$

where, A_t = Surface area

Calculate the temperature rise, T_r

$$T_r = 450 \Psi^{0.826} \text{ [}^\circ\text{C]} \quad (78)$$

Calculate the peak flux density,

$$B_{pk} = \frac{0.4\pi N_n F (I_{Pk}) 10^{-4}}{l_g + \frac{MPL}{\mu_m}} \text{ [teslas]} \quad (79)$$

B. AC INDUCTOR DESIGN

The required data have been taken from the simulation and Table 1 by considering non-ideal conditions. The calculated two AC inductors will share the same core, just like one inductor with center tapped phenomena.

The Area Product can be calculated, A_P

$$A_P = \frac{VA10^4}{K_f K_u f B_{ac} J} \text{ [cm}^4\text{]} \quad (80)$$

where, VA = Apparent power, K_f = Waveform coefficient, f = Operating frequency, B_{ac} = Flux density.

The closest A_P of available core must be selected.

Calculate the number of turns is required, N

$$N = \frac{V_L 10^4}{K_f B_{ac} f A_c} \text{ [turns]} \quad (81)$$

where, V_L = Line voltage.

Calculate the flux density, B_{ac}

$$B_{ac} = \frac{V_L 10^4}{K_f N A_c f} \text{ [teslas]} \quad (82)$$

Calculate the inductor wire bare area,

$$A_{w(B)} = \frac{I_L}{J} \text{ [cm}^2\text{]} \quad (83)$$

The closest $A_{w(B)}$ of available wire must be selected.

Calculate the copper loss, P_{cu}

$$P_{cu} = I_L^2 R_L \text{ [watts]} \quad (84)$$

Calculate watts per kilograms, W/K

$$W/K = k f^{m} B_{ac}^n \quad (85)$$

Calculate the core loss, P_{fe}

$$P_{fe} = W/K W_{tfe} \text{ [watts]} \quad (86)$$

Calculate the total loss, ΣP

$$\Sigma P = P_{cu} + P_{fe} \text{ [watts]} \quad (87)$$

Calculate the temperature rise, T_r

$$T_r = 450 \Psi^{0.826} \text{ [}^\circ\text{C]} \quad (88)$$

C. RESULT ANALYSIS OF THE INDUCTORS

After manipulating the previous equations, the DC and AC inductors core and wire have been selected. For each DC inductor L1 and L2, three parallel U93-76-16 ferrite core with #AWG 2 wire have been selected with 28 turns. And for AC inductors, both inductors L3 and L4 share the same core and three parallel 240UI silicon core with #AWG 0000 wire have been selected with 34.5 turns each. To analyze the inductors all the required data have been taken from the simulation while supplying 152.1A load current and from the datasheets

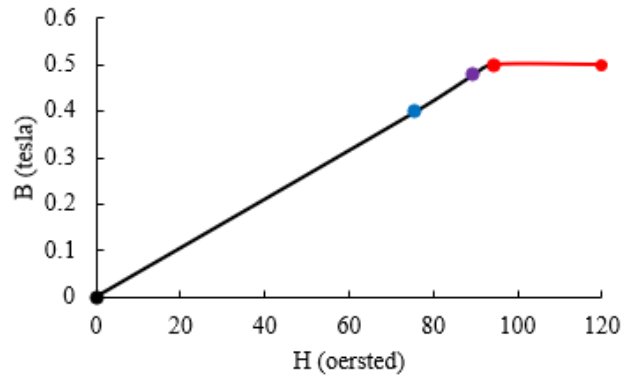


FIGURE 26. Designed each DC inductor L1 and L2 B-H consequence of the proposed system in non-ideal condition with proposed prosecution.

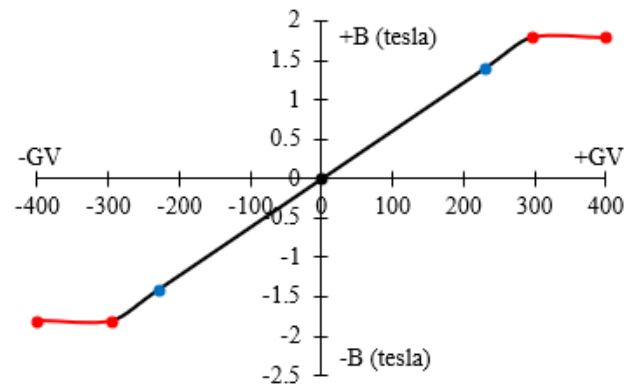


FIGURE 27. Designed associated AC inductors L3 and L4 B-GV consequence of the proposed system in non-ideal condition with proposed prosecution.

by considering non-ideal conditions. Afterward, the saturation, power loss, and temperature consequence of the designed inductors of the proposed system with proposed prosecution have been computed and depicted in Figures 26 to 29.

Figures 26 and 27 implicate the saturation consequence of the designed DC and AC inductors while supplying 152.1A charging current. In Figure 26, each high frequency designed DC inductor L1 and L2 exhibits a DC flux density of 0.39866 tesla at 75.54644 oersted marked with blue color, and the peak flux density is 0.478 tesla at 89.45572 oersted marked with purple color. Eventually, the peak flux density is underneath the saturation point of 0.5 tesla at 94.425 oersted marked with red color.

In Figure 27, designed associated AC inductors L3 and L4 exhibit an AC flux density of 1.41 tesla at a grid voltage of 230v marked with blue color which is underneath the saturation point of 1.8 tesla at a grid voltage of 295v marked with red color.

Figures 28 and 29 implicate the power loss and temperature rise consequence of the designed DC and AC inductors.

In Figure 28, each DC inductor L1 and L2 exhibit 3.1536W of core power loss (P_{fe}) and 24.56W of copper power loss

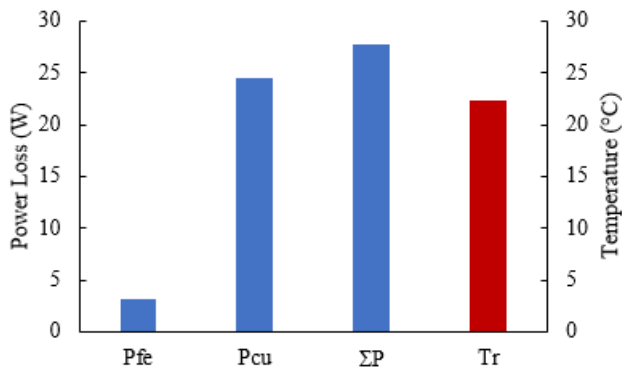


FIGURE 28. Designed each DC inductor L1 and L2 Power Loss and Temperature rise consequence of the proposed system in non-ideal condition with proposed prosecution.

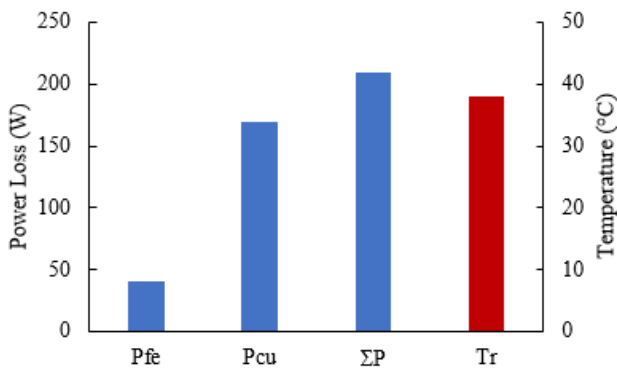


FIGURE 29. Designed associated AC inductors L3 and L4 Power Loss and Temperature rise consequence of the proposed system in non-ideal condition with proposed prosecution.

(P_{cu}) eventually a total power loss (ΣP) of 27.7136W. Consequently, the temperature (T_r) generated from each DC inductor is around 22.3872°C at natural cooling.

Figure 29, states that associated AC inductors L3 and L4 exhibit 40W of core power loss (P_{fe}) and 169W of copper power loss (P_{cu}), eventually a total power loss (ΣP) of 209W. Consequently, the temperature generated (T_r) from associated AC inductors are around 38°C at natural cooling.

III. RELIABILITY ANALYSIS OF THE PROPOSED DC-DC CONVERTER

In this section, the reliability of the proposed DC-DC converter with the proposed controller will be investigated. Afterward, the reliability comparison will be summarized between the proposed DC-DC converter and the reference DC-DC converter’s topology. All the specifications remain the same as explained in the previous sections.

From the previous sections, it was found that each MOSFET will generate around 33.61°C junction temperature when a cooling fan with an external heatsink are added and each DC inductor will generate around 22.3872°C temperature at natural cooling. Eventually, for the sake of the overall

system reliability analysis, a worst-case junction temperature of 105°C has been selected.

To analyze the failure rate, the constitution of the part stress method has been utilized. Afterward, the required data has been collected from the military handbook, MIL-HDBK-217F(N1/2) [32].

Each component failure rate is associated with several factors and noted hereunder.

$$\lambda_{pR} = \lambda_b \pi_T \pi_P \pi_Q \pi_S \pi_E \quad (89)$$

$$\lambda_{pL} = \lambda_b \pi_T \pi_Q \pi_E \quad (90)$$

$$\lambda_{pM} = \lambda_b \pi_T \pi_Q \pi_E \pi_A \pi_B \quad (91)$$

$$\lambda_{pMCU} = (C_1 \pi_T + C_2 \pi_E) \pi_Q \pi_L \quad (92)$$

$$\lambda_{pC} = \lambda_b \pi_T \pi_P \pi_Q \pi_S \pi_E \quad (93)$$

$$\lambda_{pD} = \lambda_b \pi_T \pi_Q \pi_S \pi_E \pi_C \quad (94)$$

$$\lambda_{pCS} = \lambda_b \pi_T \pi_P \pi_Q \pi_E \quad (95)$$

$$\lambda_{pF} = \lambda_b \pi_E \quad (96)$$

$$\pi_T = e^{-\frac{E_a}{k} \left(\frac{1}{T+273} - \frac{1}{298} \right)} \quad (97)$$

where

- λ_{pR} = Resistor Failure Rate
- λ_{pL} = Inductor Failure Rate
- λ_{pM} = MOSFET Failure Rate
- λ_{pMCU} = Microcontroller unit Failure Rate
- λ_{pC} = Capacitor Failure Rate
- λ_{pD} = Diode Failure Rate
- λ_{pCS} = Connector and Socket Failure Rate
- λ_{pF} = Fuse Failure Rate
- λ_b = Base Failure Rate
- π_T = Temperature Factor
- π_P = Active Pin Factor
- π_Q = Quality Factor
- π_S = Power Stress Factor
- π_E = Environment Factor
- π_A = Application Factor
- π_B = Acceleration voltage Factor
- C₁ = Die Complexity Failure Rate
- C₂ = Package Failure Rate
- π_L = Learning Factor
- π_C = Capacitance Factor
- t = time.

After manipulating all the equations, the component’s failure rate per 1000000 hours in terms of junction temperature has been analyzed and depicted in Figures 30 to 36.

From Figures 30-36, with the junction temperature increased the failure rate per 1000000 hours also increased.

Afterward, the overall reliability of the proposed DC-DC converter with the proposed prosecution can be analyzed using exponential distribution in terms of the electrical circuit geometry of the short (R_{sc}(t)) and open circuit (R_{oc}(t)) failure and interpreted hereunder.

$$R_{sc}(t) = \left(1 - \left(\left(1 - \left(e^{-\lambda_{psc}Mt} \times e^{-\lambda_{psc}Mt} \times e^{-\lambda_{psc}Dt} \times e^{-\lambda_{psc}Dt} \right) \times e^{-\lambda_{psc}Dt} \times e^{-\lambda_{psc}Lt} \times e^{-\lambda_{psc}Dt} \times e^{-\lambda_{psc}Ft} \right) \right) \right)$$

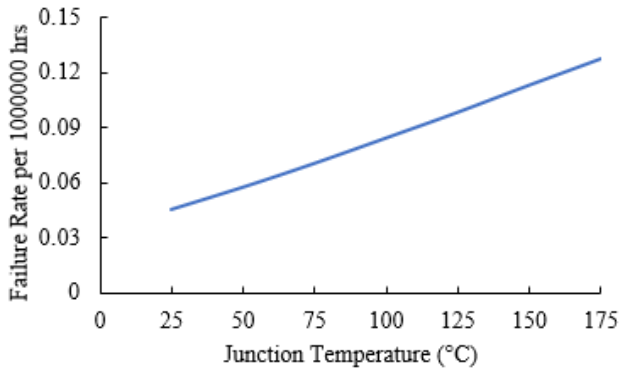


FIGURE 30. Resistor failure rate in terms of junction temperature of the proposed DC-DC converter (non-ideal) with proposed prosecution.

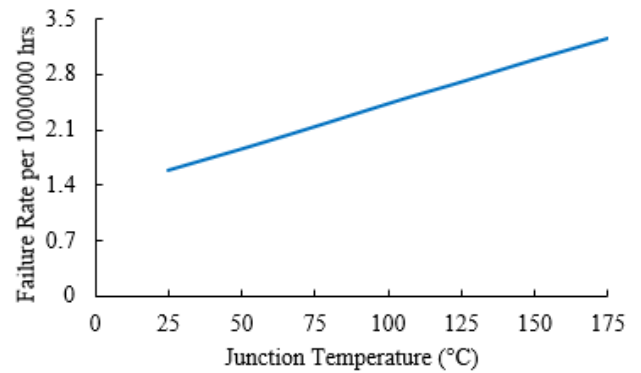


FIGURE 33. MCU failure rate in terms of junction temperature of the proposed DC-DC converter (non-ideal) with proposed prosecution.

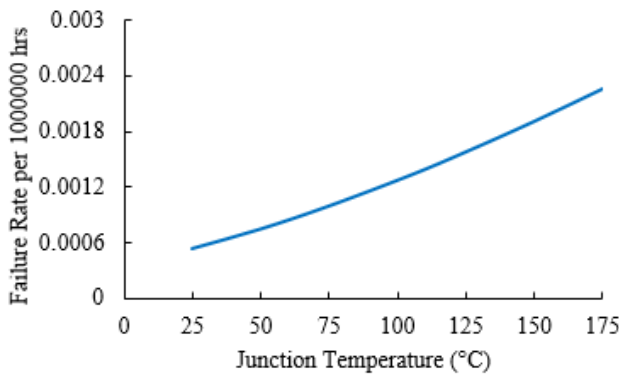


FIGURE 31. Inductor failure rate in terms of junction temperature of the proposed DC-DC converter (non-ideal) with proposed prosecution.

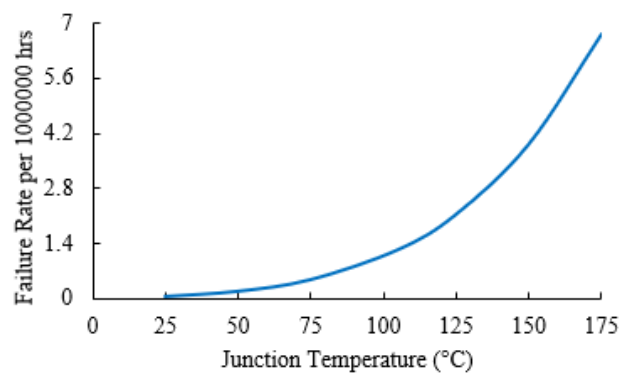


FIGURE 34. Capacitor failure rate in terms of junction temperature of the proposed DC-DC converter (non-ideal) with proposed prosecution.

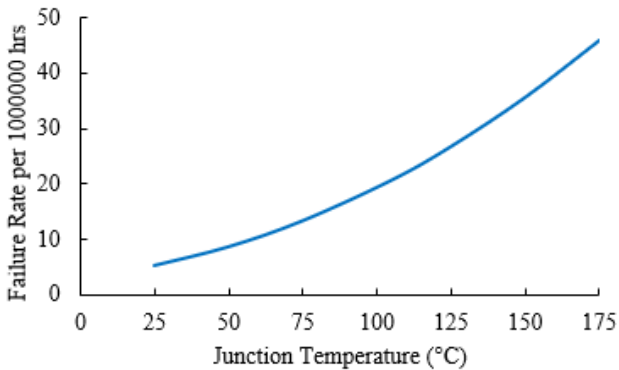


FIGURE 32. MOSFET failure rate in terms of junction temperature of the proposed DC-DC converter (non-ideal) with proposed prosecution.

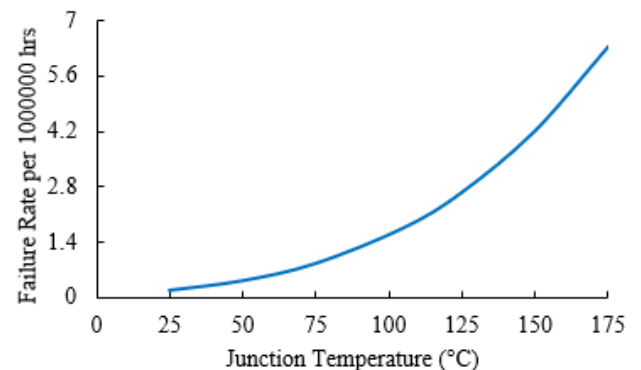


FIGURE 35. Diode failure rate in terms of junction temperature of the proposed DC-DC converter (non-ideal) with proposed prosecution.

$$\begin{aligned}
 & \times \left(1 - \left(e^{-\lambda_{psc}Mt} \times e^{-\lambda_{psc}Mt} \times e^{-\lambda_{psc}Dt} \right. \right. \\
 & \times e^{-\lambda_{psc}Dt} \\
 & \times e^{-\lambda_{psc}Dt} \times e^{-\lambda_{psc}Lt} \times e^{-\lambda_{psc}Dt} \\
 & \times e^{-\lambda_{psc}Ft} \left. \left. \left. \left. \right) \right) \right) \times e^{-\lambda_{psc}Ct} \\
 & \times e^{-\lambda_{psc}MCUt} \tag{98}
 \end{aligned}$$

$$R_{oc}(t) = \left(1 - \left(\left(1 - \left(1 - \left(1 - e^{-\lambda_{poc}Mt} \right) \times \left(1 - e^{-\lambda_{poc}Mt} \right) \right) \right) \right) \right)$$

$$\begin{aligned}
 & \times e^{-\lambda_{poc}Dt} \times e^{-\lambda_{poc}Lt} \times e^{-\lambda_{poc}Dt} \times e^{-\lambda_{poc}Ft} \left. \right) \\
 & \times \left(1 - \left(\left(1 - \left(1 - e^{-\lambda_{poc}Mt} \right) \times \left(1 - e^{-\lambda_{poc}Mt} \right) \right) \right) \right) \\
 & \times e^{-\lambda_{poc}Dt} \times e^{-\lambda_{poc}Lt} \\
 & \times e^{-\lambda_{poc}Dt} \times e^{-\lambda_{poc}Ft} \left. \left. \left. \left. \right) \right) \right) \times e^{-\lambda_{poc}MCUt} \tag{99}
 \end{aligned}$$

After manipulating the above equations, the overall proposed DC-DC system reliability has been computed and

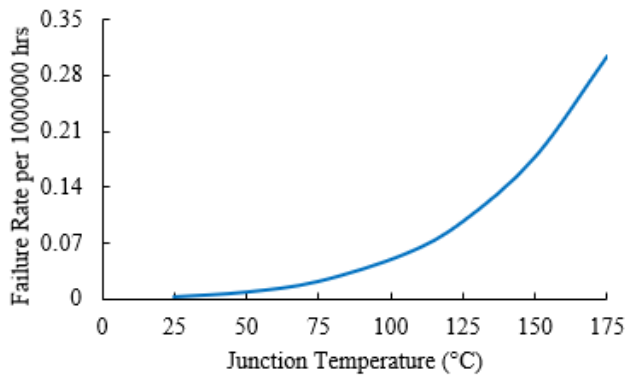


FIGURE 36. Connector and Socket failure rate in terms of junction temperature of the proposed DC-DC converter (non-ideal) with proposed prosecution.

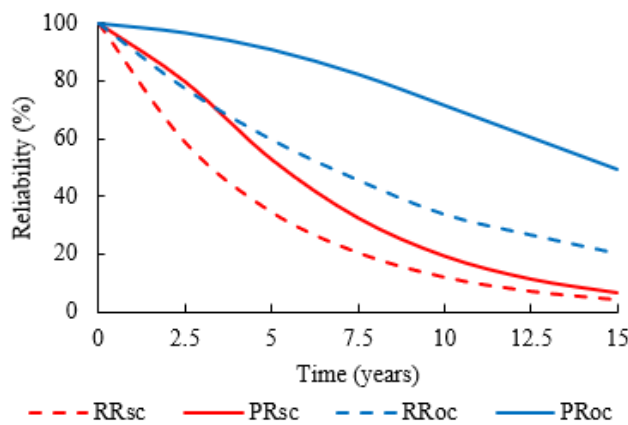


FIGURE 37. Reliability comparison between the proposed with proposed prosecution and the reference DC-DC converter in terms of short and open circuit failure.

depicted in Figure 37 with the comparison of the reference [30].

For the proposed system the overall system reliability in terms of short (PR_{sc}) and open (PR_{oc}) circuit failure are marked with red solid and blue solid lines whereas the reference system’s overall reliability in terms of short (RR_{sc}) and open (RR_{oc}) circuit failure are marked with red dashed and blue dashed lines.

From the plot, it is clear that the proposed DC-DC converter with the proposed prosecution has higher reliability than the reference DC-DC converter topology in terms of both short and open circuit failure. Eventually, the proposed DC-DC converter will perform much higher reliability than the computed reliability. Because in operation mode the component’s junction temperature was lower than the worst-case temperature discussed in the previous sections.

XIV. STATE-SPACE ANALYSIS OF PROPOSED DC-DC SYSTEM

After manipulating section V, the state-space model of the proposed DC-DC converter with proposed prosecution in the

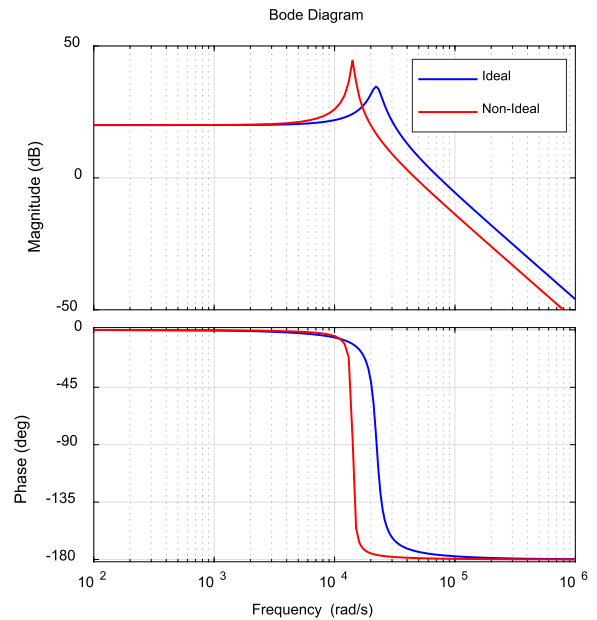


FIGURE 38. Bode Plot of the proposed with proposed prosecution open loop dc-dc converter (Ideal and Non-Ideal) at $0 < t < T_s$.

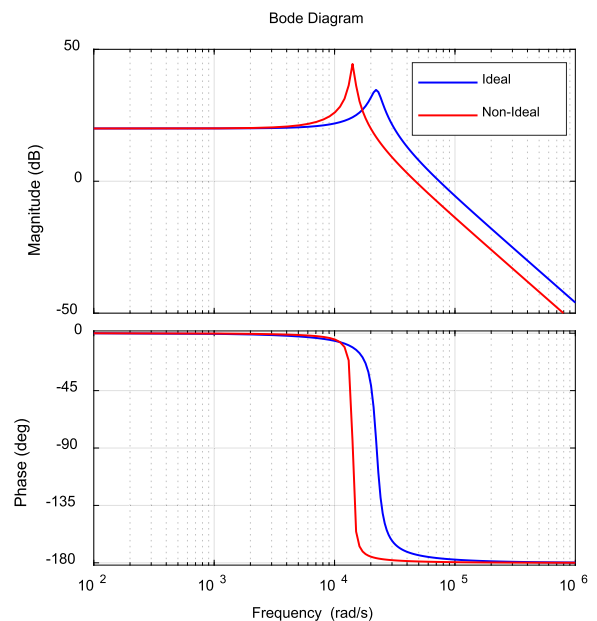


FIGURE 39. Bode Plot of the proposed with proposed prosecution open loop dc-dc converter (Ideal and Non-Ideal) at $T_s < t < 2T_s$.

open-loop condition is represented in A, B, C, and D matrices.

$$\frac{dx}{dt} = Ax + Bu \tag{100}$$

$$y = Cx + Du \tag{101}$$

where at $0 < t < T_s$ would be.

$$x = \begin{bmatrix} I_{RL1} \\ I_{RL2} \\ V_{C1} \end{bmatrix} \quad u = \begin{bmatrix} D \\ V_{D1} \\ V_{D2} \\ V_{D3} \\ V_{D4} \end{bmatrix} \tag{102}$$

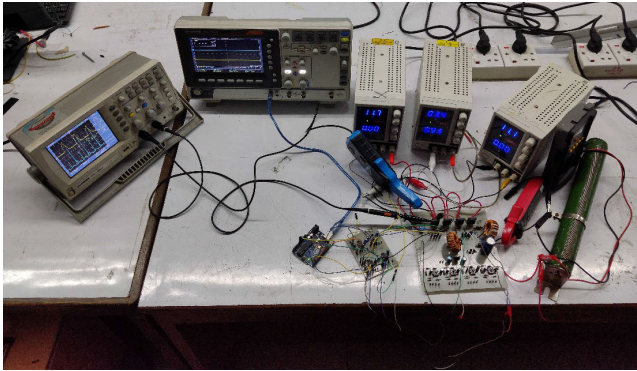
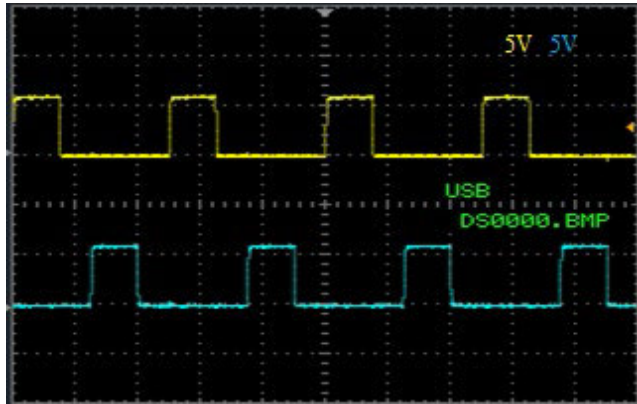
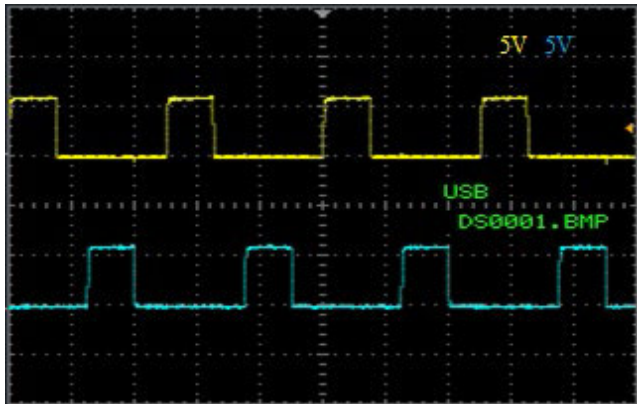


FIGURE 40. Hardware testing of the proposed DC-DC system with proposed prosecution.



(a)



(b)

FIGURE 41. Pulses of the proposed system with proposed prosecution before driver. (a) MOSFET one and three (b) MOSFET two and four.

$$A = \begin{bmatrix} A1 & A2 & A3 \\ A4 & A5 & A6 \\ A7 & A8 & A9 \end{bmatrix} \quad (103)$$

$$B = \begin{bmatrix} B1 & B2 & B3 & B4 & B5 \\ B6 & B7 & B8 & B9 & B10 \\ B11 & B12 & B13 & B14 & B15 \end{bmatrix}$$

$$C = [0 \ 0 \ 1] \quad D = [0]$$

$$A1 = \frac{-R_{L1} - R_{D3} - R_{F1} - R_{D1} - \frac{R \times R_{C1}}{R + R_{C1}}}{L1}$$

$$A2 = -\frac{\frac{R R_{C1}}{R + R_{C1}}}{L1}$$

$$A3 = -\frac{\frac{R}{R + R_{C1}}}{L1}$$

$$A4 = -\frac{\frac{R R_{C1}}{R + R_{C1}}}{L2}$$

$$A5 = \frac{-R_{L2} - R_{D4} - R_{F2} - R_{D2} - \frac{R \times R_{C1}}{R + R_{C1}}}{L2}$$

$$A6 = -\frac{\frac{R}{R + R_{C1}}}{L2}$$

$$A7 = \frac{1 - \frac{R_{C1}}{R + R_{C1}}}{C1}$$

$$A8 = \frac{1 - \frac{R_{C1}}{R + R_{C1}}}{C1}$$

$$A9 = -\frac{\frac{1}{R + R_{C1}}}{C1}$$

$$B1 = \frac{+V_g - V_{M1} - I_{RL1}R_{M1} + I_{RL1}R_{D1} + V_{D1}}{L1}$$

$$B2 = -\frac{1}{L1}$$

$$B3 = 0$$

$$B4 = -\frac{1}{L1}$$

$$B5 = 0$$

$$B6 = \frac{+V_g - V_{M2} - I_{RL2}R_{M2} + I_{RL2}R_{D2} + V_{D2}}{L2}$$

$$B7 = 0$$

$$B8 = -\frac{1}{L2}$$

$$B9 = 0$$

$$B10 = -\frac{1}{L2}$$

$$B11 = 0$$

$$B12 = 0$$

$$B13 = 0$$

$$B14 = 0$$

$$B15 = 0$$

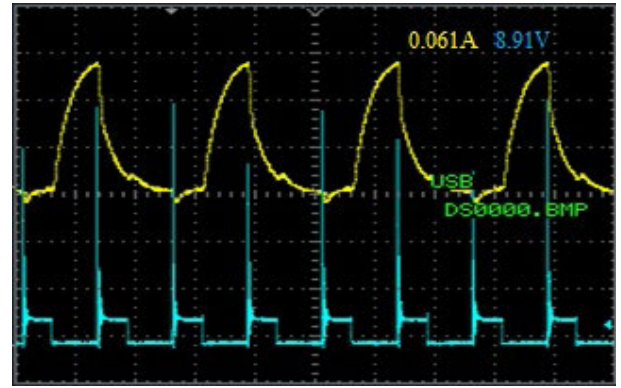
(104)

at $T_s < t < 2T_s$ would be.

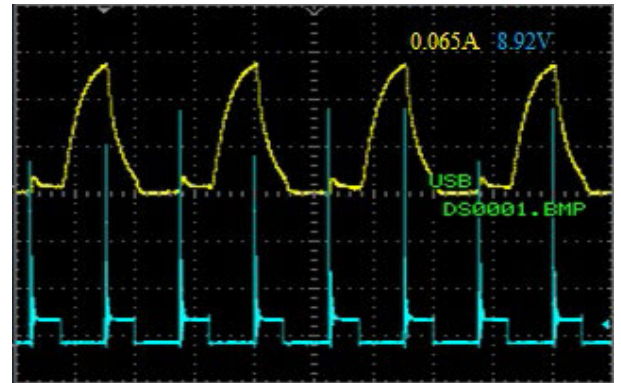
$$x = \begin{bmatrix} I_{RL1} \\ I_{RL2} \\ V_{C1} \end{bmatrix} \quad u = \begin{bmatrix} D \\ V_{D1} \\ V_{D2} \\ V_{D3} \\ V_{D4} \end{bmatrix} \quad (105)$$

$$A = \begin{bmatrix} A1 & A2 & A3 \\ A4 & A5 & A6 \\ A7 & A8 & A9 \end{bmatrix} \quad (106)$$

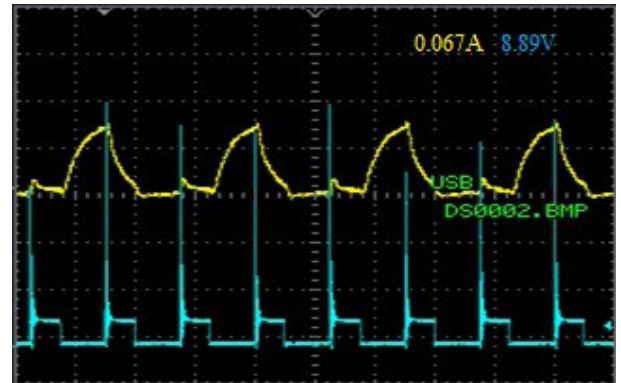
$$\begin{aligned}
 B &= \begin{bmatrix} B1 & B2 & B3 & B4 & B5 \\ B6 & B7 & B8 & B9 & B10 \\ B11 & B12 & B13 & B14 & B15 \end{bmatrix} \\
 C &= [0 \ 0 \ 1] \quad D = [0] \\
 A1 &= \frac{-R_{L1} - R_{D3} - R_{F1} - R_{D1} - \frac{R \times R_{C1}}{R + R_{C1}}}{L1} \\
 A2 &= -\frac{\frac{R R_{C1}}{R + R_{C1}}}{L1} \\
 A3 &= -\frac{\frac{R}{R + R_{C1}}}{L1} \\
 A4 &= -\frac{\frac{R R_{C1}}{R + R_{C1}}}{L2} \\
 A5 &= \frac{-R_{L2} - R_{D4} - R_{F2} - R_{D2} - \frac{R \times R_{C1}}{R + R_{C1}}}{L2} \\
 A6 &= -\frac{\frac{R}{R + R_{C1}}}{L2} \\
 A7 &= \frac{1 - \frac{R_{C1}}{R + R_{C1}}}{C1} \\
 A8 &= \frac{1 - \frac{R_{C1}}{R + R_{C1}}}{C1} \\
 A9 &= -\frac{\frac{1}{R + R_{C1}}}{C1} \\
 B1 &= \frac{+V_g - V_{M3} - I_{RL1}R_{M3} + I_{RL1}R_{D1} + V_{D1}}{L1} \\
 B2 &= -\frac{1}{L1} \\
 B3 &= 0 \\
 B4 &= -\frac{1}{L1} \\
 B5 &= 0 \\
 B6 &= \frac{+V_g - V_{M4} - I_{RL2}R_{M4} + I_{RL2}R_{D2} + V_{D2}}{L2} \\
 B7 &= 0 \\
 B8 &= -\frac{1}{L2} \\
 B9 &= 0 \\
 B10 &= -\frac{1}{L2} \\
 B11 &= 0 \\
 B12 &= 0 \\
 B13 &= 0 \\
 B14 &= 0 \\
 B15 &= 0
 \end{aligned} \tag{107}$$



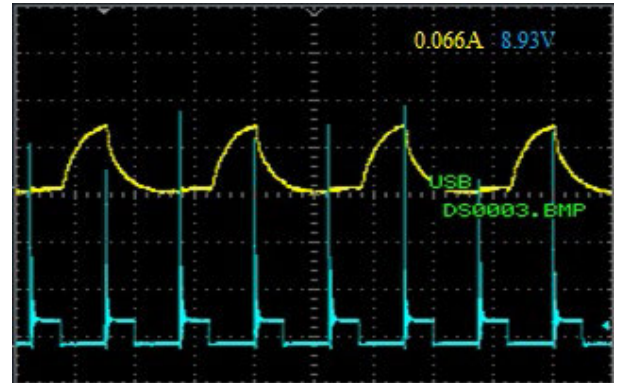
(a)



(b)



(c)



(d)

FIGURE 42. Consequence of MOSFETs current (yellow) and voltage (blue) in terms of the pulses (a) MOSFET one (b) MOSFET two (c) MOSFET three (d) MOSFET four.

After manipulating the above equations, the bode plots have been plotted in Figures 38 and 39. The plot implies that the phase margin for both ideal and non-ideal conditions are 3.5396 and 1.1353 degrees. Which leads the system to be stable.

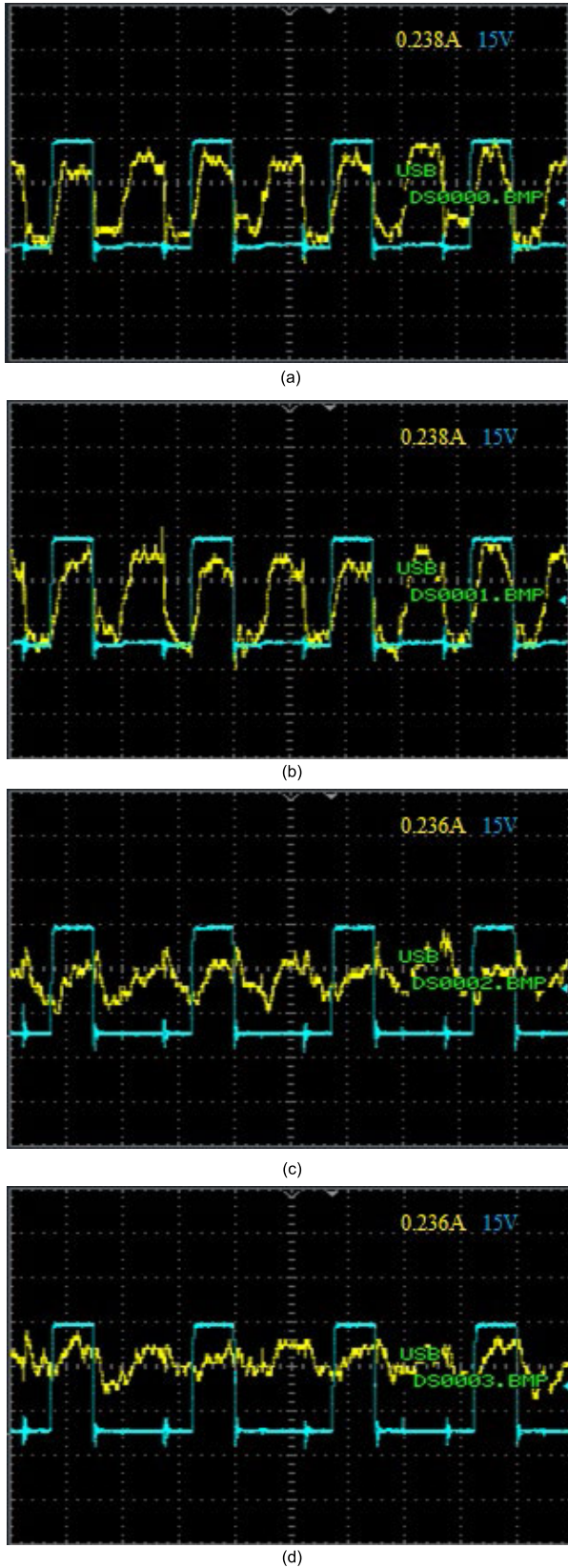


FIGURE 43. Consequence of inductors current (yellow) in terms of the MOSFETs pulses (blue) (a) Inductor one and MOSFET one (b) Inductor one and MOSFET three (c) Inductor two and MOSFET two (d) Inductor two and MOSFET four.

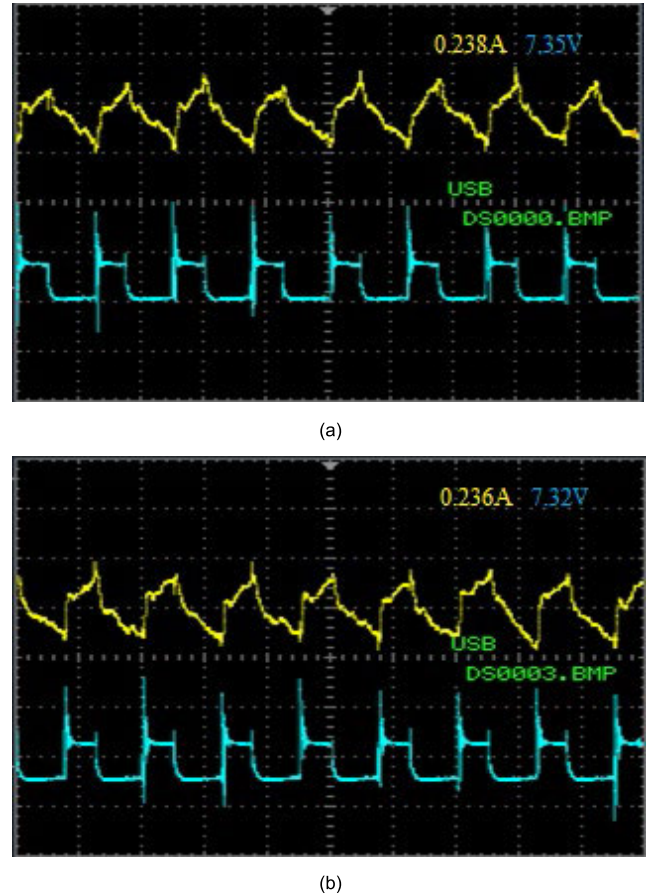


FIGURE 44. Consequence of inductors current (yellow) and voltage (blue). (a) Inductor one (b) Inductor two.

XV. LAB TEST OF HARDWARE PROTOTYPE OF PROPOSED SYSTEM

A hardware prototype of the proposed dc-dc converter in open loop conditions has been made and tested. The consequence is depicted in Figure 40.

The important parameters have given in Table 2 to verify the consequence of the proposed system with proposed prosecution.

The prosecution pulses are given in Figures 41 (a) and (b) as explained in the previous sections.

MOSFETs consequence in terms of the voltage and current are given in Figures 42. The phenomenon happening as explained in the previous sections. When the current goes down after some interval the adjacent MOSFETs do conduct and thus the voltage goes to zero and consequently the leakage power loss is minimized with the conduction and switching losses.

In Figures 43, the consequence in terms of the MOSFETs pulses and inductors current are illustrated. Since in between one complete pulse, the adjacent MOSFETs conduct, and each inductor current takes place even though in a non-conduction period in terms of one MOSFET and thus the conduction loss is minimized.

TABLE 2. Parameters of the hardware testing.

Parameters	Value
Input voltage	15V
Switching frequency	15.5kHz
Duty Cycle	0.3
DC inductor (L1, L2)	0.6mH
Output capacitor (C1)	1000uF

In Figures 44 the dc inductors' voltage and current are plotted. When positive voltage comes the inductor current increases and decays at a negative voltage.

XVI. CONCLUSION

This paper proposes a modified PI-controller-based high-gain DC-DC converter for EV charging applications. The steady-state analysis of the proposed converter both in ideal and non-ideal conditions shows the relation among input voltage, output voltage, and the prosecution. The power loss and thermal analysis of the MOSFETs manifest that the proposed prosecution has the ability to reduce the total power loss of the MOSFETs as well as temperature. For effective and economical operation, the DC and AC side inductors have been designed properly. The results state that the designed inductors stay underneath the saturation region, and the temperature rise is at an acceptable range. With the proposed converter and prosecution, the system can charge the lithium-ion battery with 152.1A while maintaining the overshoot and other factors. Besides, the power factor and the THD were achieved at 90% and 0.46% respectively. The frequency response of the dc-dc converter confirms the system's stability in ideal and non-ideal conditions. The analysis of the MOSFETs power loss and temperature profile confirms that the proposed system will be more reliable and operational than the conventional system.

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