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RESEARCH ARTICLE

A 0.78–0.91-THz Wideband Frequency Tripler With Harmonic-Matched Bias Network

KYEONGHO YEOM[1], HYUNJOON KIM[2], ILJIN LEE[3], AND SANGGEUN JEON[2], (Member, IEEE)

[1]Samsung Research, Seoul 06765, South Korea
[2]School of Electrical Engineering, Korea University, Seoul 02841, South Korea
[3]Samsung Electronics, Hwaseong 18448, South Korea

Corresponding author: Sanggeun Jeon (sgjeon@korea.ac.kr)

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ABSTRACT A 0.78–0.91-THz wideband frequency tripler is demonstrated using a 250-nm InP DHBT technology. Considering potential inaccuracy of the transistor model at the submillimeter-wave frequencies, a simple one-stage common-emitter topology is adopted for the wideband and stable operation. To enhance the output power and suppress the unwanted harmonics, a harmonic-matched bias network is used for dc feed at the output. The frequency tripler was measured with an on-chip probing method. Although an overmode waveguide probe was used, which imposes an additional measurement loss, a peak output power was measured as −28 dBm at 0.813 THz. The bandwidth for a −35-dBm output power ranges from 0.78 to 0.91 THz. The conversion loss is from 35.9 to 45 dB over the bandwidth. The chip area is 273 × 460 μm^2 and the dc power consumption is 22 mW.

INDEX TERMS Frequency tripler, InP DHBT, wideband submillimeter-wave source, WR-1.0 band.

I. INTRODUCTION

The submillimeter-wave band (0.3 to 3 THz) is considered as a promising solution to the bandwidth shortage occurred in the low-frequency bands. The high-speed communication and high-resolution imaging systems have been proposed as potential applications of the submillimeter-wave spectrum [1], [2], [3]. Recently, the lower end of the submillimeter-wave band has been actively developed owing to the advancement of transistor technologies. As a result, several submillimeter-wave frequency multipliers based on the transistors were reported in the WR-3.4 (220–325 GHz) [4], [5], [6], WR-2.2 (325–500 GHz) [7], [8], and WR-1.5 (500–750 GHz) bands [9], [10], [11].

However, as the frequency increases toward 1 THz, the transistor performance is rapidly deteriorated due to the limited f_{max} and enlarged parasitic effects. This makes it challenging to implement a transistor-based frequency source beyond 750 GHz. Therefore, there still have been only a few frequency multipliers reported in the WR-1.0 band (0.75–1.1 THz). A frequency quadrupler operating at 0.92–0.944 THz [12] and a transmitter including a frequency quintupler operating at 0.82–0.845 THz [13] were implemented using SiGe HBTs. Nevertheless, those WR-1.0 sources commonly suffer from a narrow bandwidth, which is no wider than a 3-% fractional bandwidth. Furthermore, the output power of those WR-1.0 sources were measured with a wave radiation method rather than a conventional physical probing method. The wave radiation method requires the information on the channel path loss and antenna gain used in the measurement setup. Therefore, this would limit the calibration accuracy and bandwidth of the measurement.

In this work, we propose a wideband WR-1.0 frequency tripler operating from 0.78 to 0.91 THz. A simple common-emitter (CE) topology is adopted to guarantee the stable operation of transistors. A harmonic-tuned output bias network enhances the third-harmonic output power while suppressing

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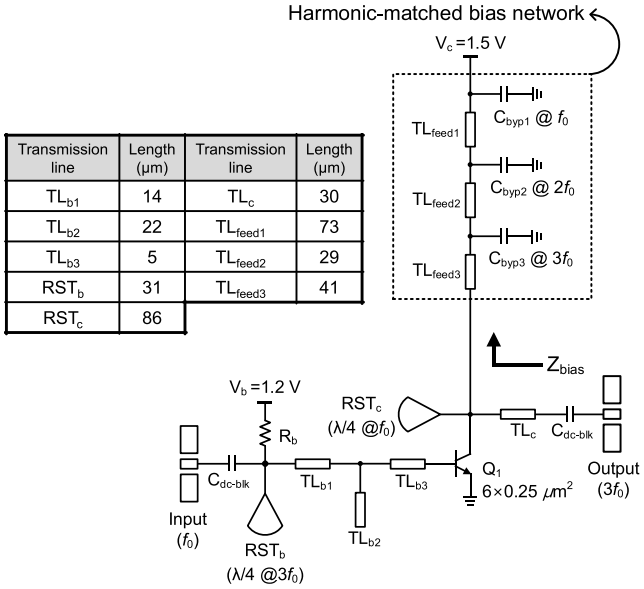


Transmission line	Length (μm)	Transmission line	Length (μm)
TL_{b1}	14	TL_c	30
TL_{b2}	22	TL_{feed1}	73
TL_{b3}	5	TL_{feed2}	29
RST_b	31	TL_{feed3}	41
RST_c	86		

FIGURE 1. Schematic of the WR-1.0 frequency tripler.

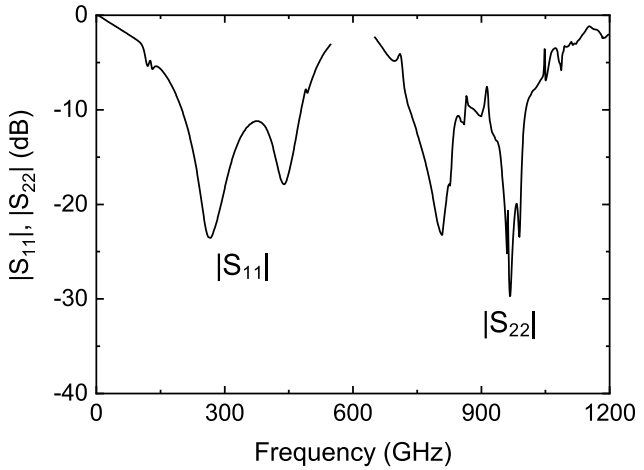


FIGURE 2. Simulated large-signal port-matching performance of the WR-1.0 frequency tripler at input signal level of 9 dBm.

unwanted frequency components. The WR-1.0 source was measured with an on-chip probing method. This requires no estimation of the channel path loss or antenna gain and allows for the wideband measurement.

II. DESIGN OF WR-1.0 FREQUENCY TRIPLER

Fig. 1 shows a schematic of the WR-1.0 frequency tripler. Given that the transistor modeling is commonly performed at low frequencies below 110 GHz, the model accuracy should be deteriorated in the terahertz regime. Furthermore, the parasitic reactive components of transistors become pronounced significantly as the frequency increases, thus degrading the transistor performance in the terahertz. Therefore, to guarantee the stable transistor operation against the modeling uncertainty and adverse parasitic effect of the transistors, a single-stage CE topology is simply employed for frequency multiplication. The transistor (Q_1) is biased at over-driven class-A operation for sufficient third-harmonic generation.

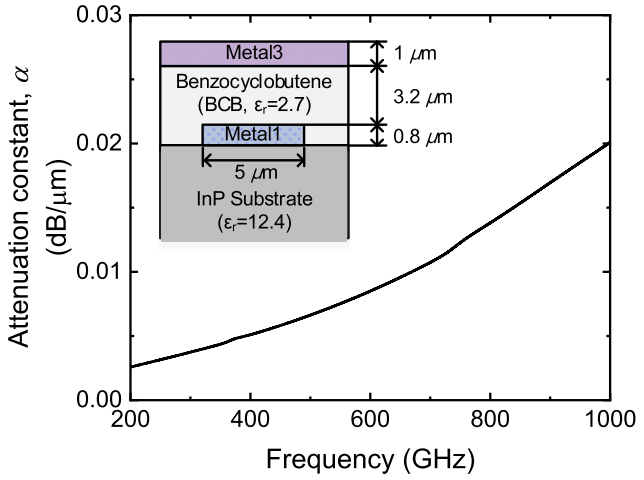


FIGURE 3. Geometry and attenuation constant of the 50-Ω inverted microstrip line.

The input is matched to 50 Ω at f_0 (nominally, 300 GHz) using a multi-L-section network consisting of the transmission lines (TL_{b1}–TL_{b3}) and a radial stub (RST_b). Both TL_{b2} and RST_b behave as a shunt capacitor at f_0, so that a low standing-wave ratio is achieved over a wide bandwidth. As shown in Fig. 2, the simulated large-signal $|S_{11}|$ is below −10 dB from 205 to 479 GHz. Furthermore, the RST_b presents a quarter wavelength at $3f_0$, thus behaving as a reflector to the third-harmonic signal that could be fed back from the output. According to the simulation, the output power is increased by 1.1 to 2.6 dB from 800 to 950 GHz due to the third-harmonic reflector. The transmission lines and stubs are implemented using an inverted microstrip structure where the ground is formed by the third metal (M3) whereas the signal line is made in the lowest metal (M1), as shown in Fig. 3. Therefore, the transistor can be directly connected to the transmission lines without via holes, thus eliminating an extra loss originated from the interconnection. The attenuation constant of the inverted microstrip line with a characteristic impedance of 50 Ω is 0.004 and 0.017 dB/μm at 300 and 900 GHz, respectively.

The transistor output is matched to 27 + j20.7 Ω at $3f_0$ (nominally, 900 GHz), which is a compromised impedance between the conjugate point for high return loss and the load-pull point for maximum power. The simulated $|S_{22}|$ shown in Fig. 2 presents a wideband characteristic, which is below -7.5 dB from 733 to 1004 GHz. A quarter-wave radial stub at f_0 (RST_c) is inserted to suppress the unwanted fundamental signal at the output. In principle, the RST_c is supposed to present a low impedance not only at f_0 but also at $3f_0$. This could suppress the desired output signal at $3f_0$, too, which is obviously undesirable. However, a full EM simulation with ADS Momentum® finds that the RST_c presents rather a high impedance at $3f_0$ due to the parasitic distributed components of the stub, thus not hindering the desired output signal from coming out at the output port. In Fig. 4, the magnitude of the input impedance of RST_c ($|Z_{in}|$) is simulated on the

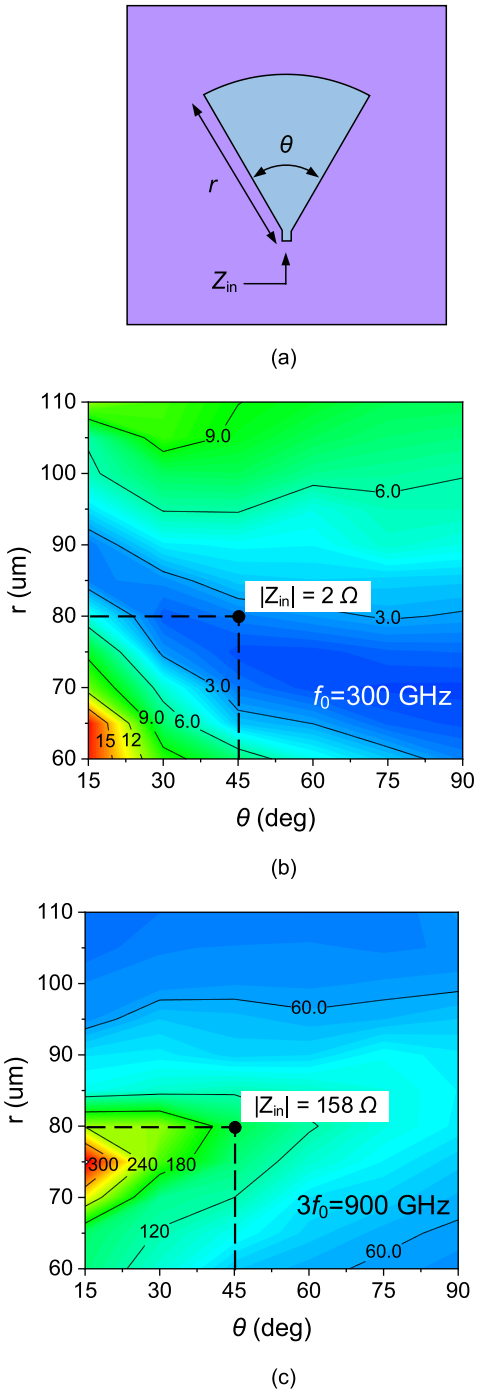


FIGURE 4. Dimensions of RST_c (a), $|Z_{in}|$ of RST_c at 300 GHz (b) and at 900 GHz (c).

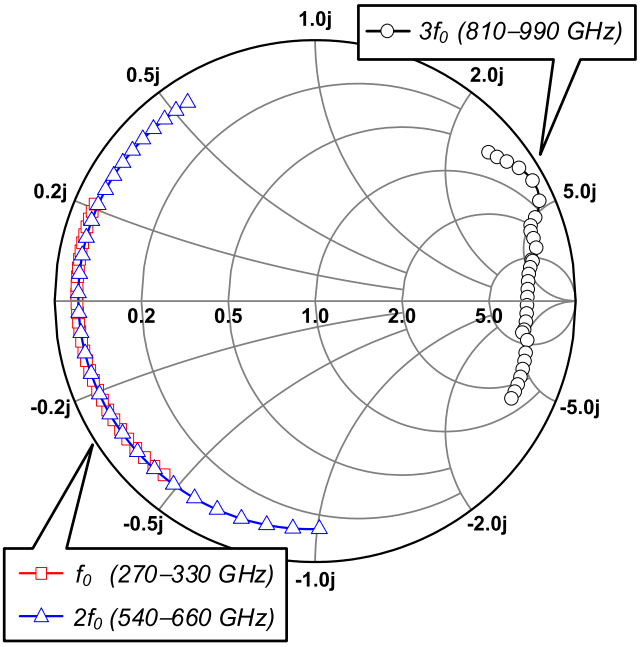


FIGURE 5. Simulated impedances of the harmonic-matched bias network (Z_{bias}) at f_0, $2f_0$, and $3f_0$.

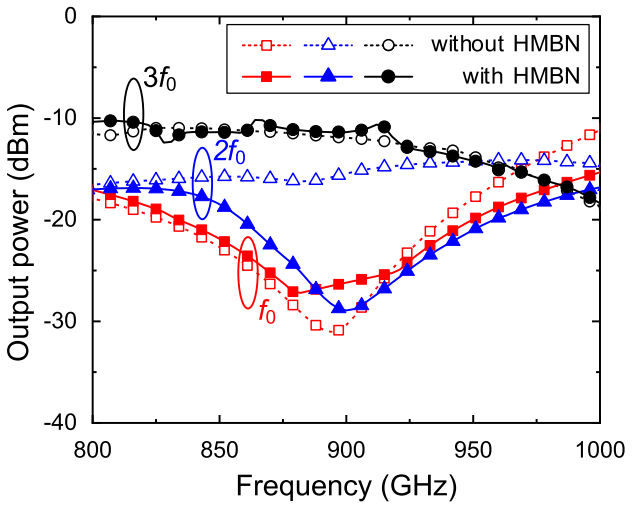


FIGURE 6. Simulated output power at f_0, $2f_0$, and $3f_0$ with and without the harmonic-matched bias network (HMBN).

r-θ plane at 300 and 900 GHz. r and θ represent the radius and central angle, respectively, of RST_c. Considering a trade-off between the fundamental suppression and 3rd harmonic output, an optimum point of r = 80 um and θ = 45° is chosen. This results in $|Z_{in}|$ = 2 and 158 Ω at 300 and 900 GHz, respectively. The finite impedance of RST_c at 900 GHz is rather exploited as an output impedance matching component.

The collector bias is supplied by a harmonic-matched bias network which suppresses the unwanted fundamental and second-harmonic components at the output. In Fig. 5, the input impedances of the bias network (Z_{bias}) are depicted at f_0, $2f_0$, and $3f_0$, respectively. At $3f_0$, a quarter-wave line (TL_{feed3}) and a bypass capacitor (C_{byp3}) constitute a high impedance of Z_{bias} which prevents the desired third-harmonic signal from leaking into the bias network. For example, $|Z_{bias}|$ is as high as 460 Ω at 900 GHz. On the other hand, the second transmission line (TL_{feed2}) and bypass capacitor (C_{byp2}) are optimized for presenting a low impedance of Z_{bias} at $2f_0$, which suppresses the undesired second-harmonic signal at the output. Finally, TL_{feed1} and C_{byp1} are optimized for a

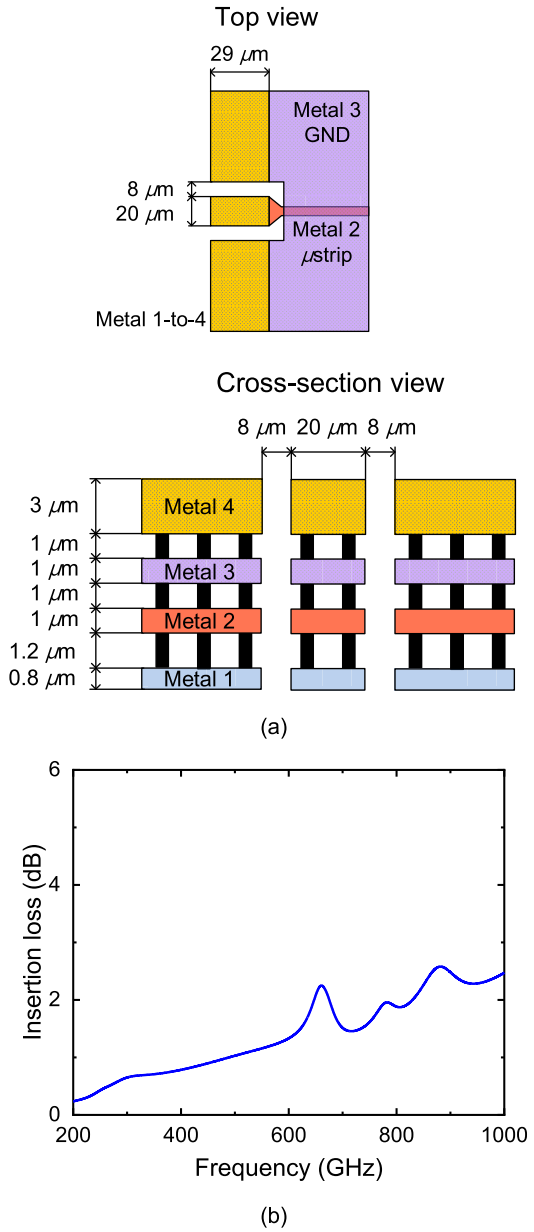


FIGURE 7. (a) Geometry and (b) simulated insertion loss of the on-chip RF probing pad.

low impedance at f_0. For example, $|Z_{bias}|$ is as low as 4 and 2.7 Ω at 300 and 600 GHz, respectively. As a result of the harmonic-matched bias network, the output power at $3f_0$ is enhanced whereas the unwanted frequency components at f_0 and $2f_0$ are suppressed. In Fig. 6, the simulated output power at f_0, $2f_0$, and $3f_0$ are shown with and without the harmonic-matched bias network. It is observed that the desired signal at $3f_0$ is rarely affected or rather enhanced at some frequencies by the bias network. On the other hand, the bias network significantly suppresses the output leakage at $2f_0$. For example, the leakage at $2f_0$ is suppressed by 18 dB when the output frequency at $3f_0$ is 900 GHz. The output leakage at f_0 is suppressed twice by the RST_c and the harmonic-matched bias network.

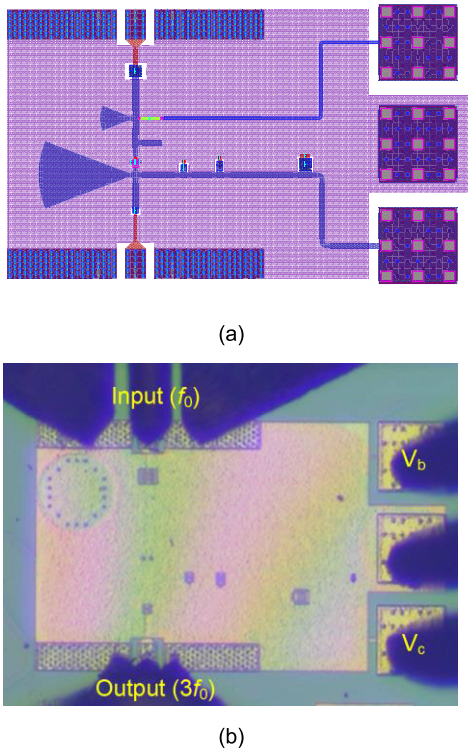


FIGURE 8. (a) Chip layout and (b) chip photograph of the WR-1.0 frequency tripler.

Facilitating the on-chip probing measurement, the terahertz probing pad was carefully designed to minimize the insertion loss. The geometry of the probing pad is depicted in Fig. 7(a). The pad size is determined to be 20×29 μm^2 which provides a minimum area that allows the probe tip contact while presenting a small shunt capacitance of 10 fF. The M2 signal line is transited to M1 after C_{dc-blk}. In Fig. 7(b), the simulated insertion loss of the probing pad is 2.5 dB at 900 GHz.

III. EXPERIMENTAL RESULTS

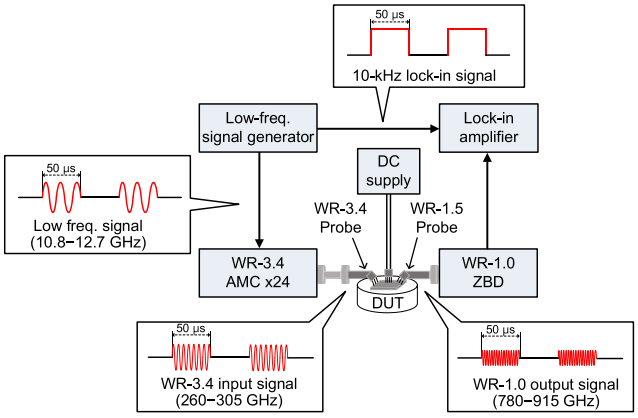
The frequency tripler was fabricated in a Teledyne 250-nm InP DHBT technology. The unity-gain frequency (f_T) and the maximum oscillation frequency (f_{max}) are 392 and 859 GHz, respectively [14]. The chip layout and photograph are shown in Fig. 8(a) and 8(b), respectively. The chip size is 273×460 μm^2 including the probing pads. The dc power consumption is 22 mW with the collector bias (V_c) of 1.5 V and base bias (V_b) of 1.2 V.

The chip was measured by an on-chip probing method. The block diagram and photograph of the measurement setup are shown in Fig. 9(a) and 9(b), respectively. The chip input is probed with a WR-3.4 GSG waveguide probe. The wideband input signal is generated by two individual WR-3.4 amplifier-multiplier-chain (AMC) modules. One AMC module is used for generating the frequency from 260 to 295 GHz and the other AMC module is for the frequency from 295 to 305 GHz. Each AMC module has a multiplication factor of 24 and thus is driven by a low-frequency signal generator from 10.83 to

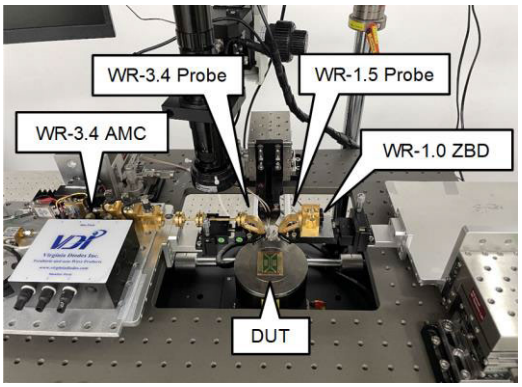
TABLE 1. Performance comparison with previous transistor-based WR-1.0 frequency multipliers.

Ref.	Technology	Topology	Multiplication factor	Output frequency (GHz)	P_{out} (dBm)	Conv. loss (dB)	P_{dc} (mW)	Area (mm^2)
[12]	130-nm SiGe BiCMOS	Differential CE + Patch antenna	×4	920 – 944	-29 – -17.3	25.3	5.7	0.37
[13]	250-nm SiGe BiCMOS	×3 + PA + ×3 + PA + ×5 + Patch antenna	×45	820 – 845	-40 – -17*	-	3700**	3.22**
This work	**250-nm InP DHBT**	**Single-ended CE**	**×3**	**780 – 915**	**-35 – -28**	**35.9–45**	**22**	**0.124**

*EIRP including an antenna gain of 10 dBi, **Transmitter including a WR-1.0 frequency quintupler



(a)



(b)

FIGURE 9. (a) Block diagram and (b) photograph of the measurement setup for the 3rd harmonic output power in the WR-1.0 band.

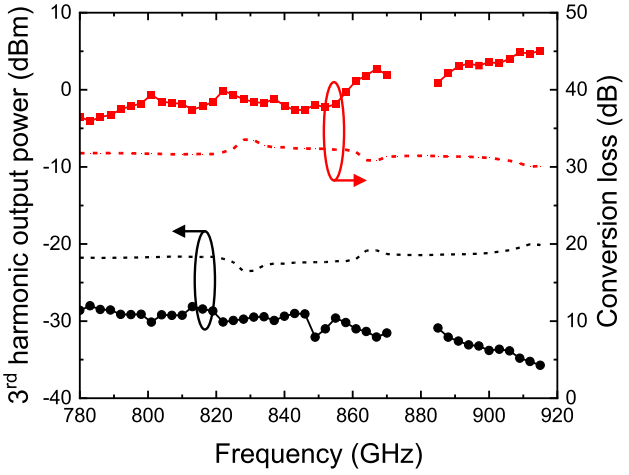


FIGURE 10. Measured (solid) and simulated (dashed) third-harmonic output power and conversion loss versus output frequency.

12.71 GHz. The drive signal is modulated by a 10-kHz periodic rectangular signal which behaves as a reference for lock-in measurement of the output power in the WR-1.0 band.

The chip output at 780 to 915 GHz is probed with a WR-1.5 GSG probe, which operates in an overmode at the WR-1.0 output frequencies. Therefore, an additional overmode loss is expected from the WR-1.5 waveguide. The output power is measured with a WR-1.0 zero-bias detector (ZBD) and a lock-in amplifier. The ZBD converts the WR-1.0 signal power to a dc output voltage with a responsivity of 820–1480 V/W. Then, a lock-in amplifier accurately reads the dc voltage, from which the output power of the tripler is calculated back according to the responsivity of the ZBD. A reference signal required for the lock-in operation, which is a 10-kHz rectangular signal, is provided by the input signal generator. The ground noise level of the lock-in measurement is -50.4 dBm, which was extracted from a frequency tripler with no input signal applied.

The WR-1.5 probe loss of 7.6 dB was calibrated out from the measured output power. However, the overmode loss of the WR-1.5 waveguide and the mode mismatch loss between the WR-1.5 waveguide and WR-1.0 ZBD were not calibrated. Therefore, it is expected that the actual output power available from the tripler should be higher than the reported power. It should also be noted that the fundamental and second harmonic signals are not included in the measured output power because they are cut off by the WR-1.0 ZBD that has a cutoff frequency higher than 600 GHz.

The measured third-harmonic output power and conversion loss versus the output frequency are shown in Fig. 10. The peak output power is -28 dBm at 813 GHz under the input power of 9.3 dBm. The output power is higher than -35 dBm over a wide bandwidth from 780 to 915 GHz. The conversion loss is from 35.9 to 45 dB over the bandwidth. In Table 1, this work is compared to previous transistor-based WR-1.0 frequency multipliers. Owing to the wideband port matching and on-chip probing measurement, this work exhibits the widest operating bandwidth. Although other work reported a higher output power or EIRP, the bandwidth is limited. Furthermore, it should be noted that the overmode and mode-mismatch loss

was not calibrated out during the measurement, which would otherwise increase the reported output power in this work.

IV. CONCLUSION

A transistor-based wideband THz source was reported for the future THz applications such as the high-speed communication and high-resolution imaging. A wideband impedance matching was performed at the input and output ports. The radial stubs and harmonic-matched bias network suppress the unwanted fundamental and second-harmonic components while enhancing the desired third-harmonic signal. The chip was measured with a physical probe contact method, exhibiting an output power higher than −35 dBm over a wide bandwidth from 780 to 915 GHz. An array of the frequency triplers configured for coherent power combining could be a potential way to further increase the output power.

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KYEONGHO YEOM received the B.S. degree in electronic engineering from Kwangwoon University, Seoul, South Korea, in 2019, and the M.S. degree in electrical engineering from Korea University, in 2021.

He is currently with Samsung Research, Seoul. His current research interests include millimeter-wave and terahertz integrated circuits and systems for communication applications.

HYUNJOON KIM received the B.S. degree in electronic convergence engineering from Kwangwoon University, Seoul, South Korea, in 2021, and the M.S. degree in electrical engineering from Korea University, Seoul, in 2023, where he is currently pursuing the Ph.D. degree in electrical engineering.

His current research interests include millimeter-wave and terahertz integrated circuits and systems.

ILJIN LEE received the B.S. and Ph.D. degrees in electrical engineering from Korea University, Seoul, South Korea, in 2013 and 2020, respectively.

He is currently with Samsung Electronics, Suwon, South Korea. His current research interests include millimeter-wave and terahertz integrated circuits and systems for wireless broadband communication applications.

SANGGEUN JEON (Member, IEEE) received the B.S. and M.S. degrees in electrical engineering from Seoul National University, Seoul, South Korea, in 1997 and 1999, respectively, and the M.S. and Ph.D. degrees in electrical engineering from the California Institute of Technology (Caltech), Pasadena, CA, USA, in 2004 and 2006, respectively.

From 1999 to 2002, he was a full-time Instructor of electronics engineering with Korea Air Force Academy, Cheongju, South Korea. From 2006 to 2008, he was a Research Engineer, where he was involved with CMOS phased-array receiver design. Since 2008, he has been with the School of Electrical Engineering, Korea University, Seoul, where he is currently a Professor. His current research interests include integrated circuits and systems at microwave, mm-wave, and terahertz bands for high-speed wireless communications and high-resolution imaging applications.