IEEE Access
Multidisciplinary ⋮ Rapid Review ⋮ Open Access Journal

Received 23 February 2023, accepted 10 March 2023, date of publication 15 March 2023, date of current version 24 March 2023.

Digital Object Identifier 10.1109/ACCESS.2023.3257331

RESEARCH ARTICLE

An Improved Modulation Method for Parallel Three-Level Rectifiers With Circulating Current Mitigation

YANFENG LI[1], HONGLIANG ZHANG[1,2], XIAO JING[1], AND AIGUANG ZHAO[1]

[1]Shandong Aotai Electric Company Ltd., Jinan 250101, China
[2]Department of Control, Shandong University, Jinan 250101, China

Corresponding author: Hongliang Zhang (18660138045@163.com)

This work was supported in part by the National Natural Science Foundation of China under Grant 62222309, and in part by the Natural Science Foundation of Shandong Province under Grant ZR2020YQ50 and Grant ZR2022JQ29.

ABSTRACT An improved modulation method is proposed for two parallel three-level interleaved rectifiers to reduce current harmonics and high-frequency zero-sequence circulating current, which uses sinusoidal pulse width modulation. First, a model of the two parallel rectifiers is constructed, and the main factor affecting the line current performance and zero-sequence circulating current is discussed. Second, the current harmonics are the priority optimization target to guarantee better line current performance. Finally, an exchange of the large common-mode voltage between two converters is made to reduce the high frequency zero-sequence circulating current based on the low current harmonics. Performance comparisons between the proposed method and existing methods in terms of total current harmonics, zero-sequence circulating current value and switching loss are made in the experiment, which confirm the effectiveness of the proposed method.

INDEX TERMS AC-DC power converters, closed loop systems, electrical engineering, multilevel converters, power industry, power conversion harmonics, pulse width modulation converters, rectifiers, three-phase electric power, voltage-source converters.

I. INTRODUCTION

Paralleled converter systems are widely applied to extend power ratings and improve system reliability [1], [2], [3], [4]. They have a wide range of applications in the electrical industry, such as renewable energy and motor drives [5], [6], [7]. To improve the current quality, an interleaved operation is employed to shift the angle between different modules [8]. In this way, the current ripple is reduced. This can reduce the size of the grid-side inductor. However, the circulating current is raised and can cause overcurrent and higher thermal stress for semiconductor devices and DC capacitors [9]. Normally, the zero-sequence circulating current (ZSCC) caused by the common mode voltage (CMV) difference flows through the DC and AC coupling points; therefore, extra filters are required to mitigate ZSCC [10]. These components increase costs, weight and volume, which are essential issues in many applications. There are some extensive discussions about closed loop control based on state-averaging algorithms to mitigate low-frequency ZSCC [11], [12], [13], [14]. However, they cannot be used in high-frequency ZSCC (HF-ZSCC) elimination.

Many researchers have studied methods to reduce HF-ZSCC and improve current quality [15], [16], [17], [18], [19], [9], [20], [21], [22], [23], [24], [25]. In [15], an interleaved zero-vector modulation scheme based on phase shifting the carrier of the fixed phase leg by π within the individual module is proposed to reduce the HF-ZSCC. The scheme also analyzes the harmonic spectrum of LF-ZSCC and then adopted a plug-in repetitive controller to eliminate the LF-ZSCC. This scheme is a useful tool to reduce ZSCC in parallel two-level converters. In [16], the authors introduce a line-current ripple minimization PWM method with a reduced ZSCC method in two-level converters, which

The associate editor coordinating the review of this manuscript and approving it for publication was Gerard-Andre Capolino.

used the nearest three vectors to reduce current harmonics and selects the voltage sequence with the lowest ZSCC using carrier-based modulation to achieve the goals. In [17], the authors use different voltage sequences in different sections to achieve low ZSCC. In [18], an interleaved discontinuous PWM (DPWM) method is proposed in two-level converters. An improved DPWM method is proposed in [19] that illustrates the detailed effect of switching states on ZSCC and currents. It can be adopted in any number of paralleled two-level converter units. Some modulation methods based on a three-level converter have been proposed. In [9], an analysis of phase disposition and alternative phase opposite disposition on common-mode voltage (CMV) is conducted. Mathematical models describing the circulating current in different switching sequences are included. It also calculates the peak-to-peak value and RMS value of the ZSCC and is a useful tool for designing CM filters. In [20], a carrier-based double reference PWM is proposed that uses the overlapping parts of each arm to reduce ZSCC. In [21], [22], and [23], a series of voltage state sequences are designed to reduce ZSCC in a paralleled NPC converter system. The two paralleled NPC converters can be seen as a five-level converter, and selecting a suitable voltage sequence can achieve a low ZSCC and good current quality. In [24], a two-degree-of freedom method is proposed that changes the carrier angle of each phase and shifts the carriers of the different converters to reduce ZSCC. In addition, MPC is also used to realize parallel interleaving technology [25], which avoids the cross traversal of vector candidates between two sets of windings and achieves a remarkable effect. However, it needs a large storage space. These methods are based on a shift angle of 180°. In fact, the current ripple is greatly reduced at a shift angle of 90° for different modulation indices [26].

Therefore, to reduce the calculation process, improve the current quality and reduce the ZSCC, this paper proposes a novel modulation method in parallel interleaved rectifiers. The main contributions of this article include these points.

1) For the two paralleled rectifiers, a mathematical model is established to analyze the effect of voltage vectors on the ZSCC and current ripple.

2) A novel modulation method is proposed with SPWM. With the proposed method, the CMV of each converter is distributed more equally, and the differences of each CMV are mitigated; thus, the ZSCC peak value is reduced significantly.

This article is organized as follows. Section II describes the basic structure of paralleled three-level rectifiers and shows the mathematical model of ZSCC in paralleled converters. The voltage sequence with an angle shift of 180° is analyzed in Section III. Section IV illustrates the proposed method. Finally, the experimental results verify the performance of the proposed method.

II. PARALLEL VOLTAGE SOURCE RECTIFIERS

The topology of paralleled three-level rectifiers is shown in Fig. 1. The grid-side of the two rectifiers is connected to the grid, while the DC-link of the rectifiers is connected to the same load. Each rectifier has three states: {2}, {1} and {0}. The input voltage of the rectifier can be expressed as

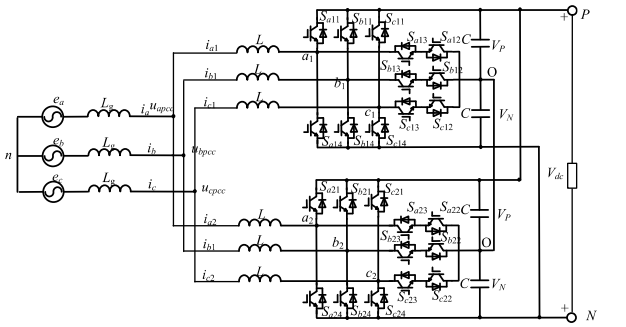

FIGURE 1. Topology structure of two-parallel three-level rectifiers sharing the same DC-link and AC-link.

TABLE 1. Relationship between switching states and input voltages.

Switching States (S_s)	ON Switches (i=1, 2; x=a, b, c)	Input Voltages (u_{xiO})
2	S_{xi1}, S_{xi2}	$V_{dc}/2$
1	S_{xi2}, S_{xi3}	0
0	S_{xi3}, S_{xi4}	$-V_{dc}/2$

$$u_{x_iO} = (S_s - 1) \times \frac{V_{dc}}{2}, \quad S_s = 0, 1, 2 \tag{1}$$

where V_{dc} is the DC-link voltage, u_{xiO} is the voltage between x_i and O point in Fig. 1. The relationship between the switching states and input voltage is shown in Table. 1.

Based on Table 1, each converter has 27 voltage space vectors. The complete voltage space vector diagram of a single three-level converter is shown in Fig. 2.

Selecting the neutral point of the DC-link capacitor as the reference point, based on Kirchhoff's voltage law (KVL), the model of the i-paralleled three-level converter is expressed as

$$e_x = L_g \frac{di_x}{dt} + L\frac{di_{xi}}{dt} + u_{x_iO} + u_{On} \tag{2}$$

where e_x is the phase voltage, i_x is the total current, i_{xi} is the current in each phase, and u_{On} is the voltage between O and n. Considering the three-phase balanced grid, (2) can be added up to 0, so the CMV of the i-paralleled three-level rectifier can be expressed as

$$u_{zi} = -\frac{1}{3}\sum_{x=a,b,c} u_{xiO} = -(\frac{1}{3}\sum_{x=a,b,c} L\frac{di_{xi}}{dt} + u_{On}), \quad i = 1, 2 \tag{3}$$

where u_{zi} is the CMV of the i-rectifier.

The ZSCC i_{zi} of the i-paralleled three-level converter can be expressed as

$$i_{zi} = \frac{1}{2L}\int (u_{z1} - u_{z2})dt \tag{4}$$

Based on (2) and (3), the equivalent CM circuit of paralleled converters is presented in Fig. 3(a). Fig. 3(b) shows the equivalent differential mode (DM) circuit of the paralleled converters, where u_{dmai} represents the DMV of a phase in the i-converter, i_{dmai} is the corresponding DM current and i_{dmx}

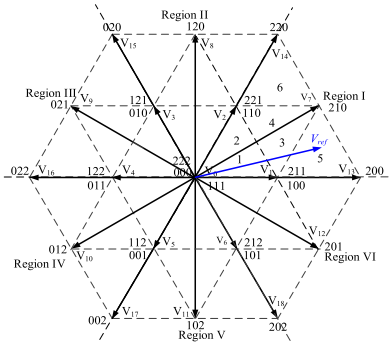

FIGURE 2. Voltage space vector diagram of a single three-level rectifier.

is the line current of the x phase. According to the KVL, the two paralleled legs of the a phase can be equivalent to a single source u_{dma} and an impedance $L/2$, which is the same for phase b and phase c [27].

The DM voltage of the i-paralleled converter can be expressed as

$$u_{dmai} = u_{a_iO} - u_{zi} \tag{5}$$

The equivalent voltage source is expressed as

$$u_{dma} = \frac{1}{2}(u_{dma1} + u_{dma2}) \tag{6}$$

Therefore, the DM model for each phase can be expressed as

$$e_a - L_g\frac{di_{dma}}{dt} = u_{dma} + \frac{1}{2}L\frac{di_{dma}}{dt} \tag{7}$$

Based on (7), the input current is determined by the voltage e_a-u_{dma}; thus, the parallel system can be seen as a single-phase converter from each input grid side. Both DMV and CMV are related to voltage u_{xiO}, thus controlling the u_{xiO} of two paralleled rectifiers to achieve low ZSCC and improve input current.

III. CURRENT RIPPLE ANALYSIS WITH CLASSICAL SVM

Based on Fig. 3(a) and (b), the single-phase equivalent circuit of the interleaved rectifier is shown in Fig. 3(c), where u_{On} can be expressed as [19]

$$u_{On} = -\frac{1}{6}\sum_{x=a,b,c} u_{x1O} - \frac{1}{6}\sum_{x=a,b,c} u_{x2O} \tag{8}$$

Therefore, the voltage on inductor L can be expressed as

$$L\frac{di_{ai}}{dt} = u_{apcc} - u_{aiO} - u_{On} \tag{9}$$

For the parallel rectifiers, this satisfies $i_a = i_{a1} + i_{a2}$. Thus, the current ripple of the input current can be analyzed from the current in the first rectifier and second rectifier.

Take the reference voltage in Region I-5 as the example in Fig. 2. The nearest three vectors 100, 200, 210 and 211 are selected to synthesize voltage V_{ref}. In addition, the dwell times of small vectors (100, 211) are the same. The voltage sequence and current ripple are shown in Fig. 4(a), where i_{a1} represents the instantaneous current of a phase in the first

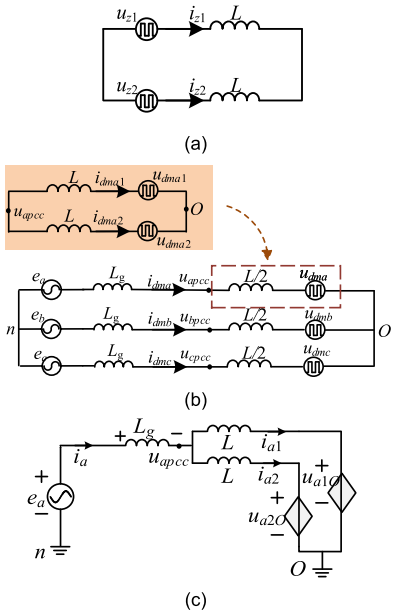

FIGURE 3. Equivalent circuits of two-parallel three-level rectifiers sharing the same DC-link and AC-link. (a) equivalent CM circuit, (b) equivalent DM circuit, (c) single-phase equivalent circuit of interleaved rectifier.

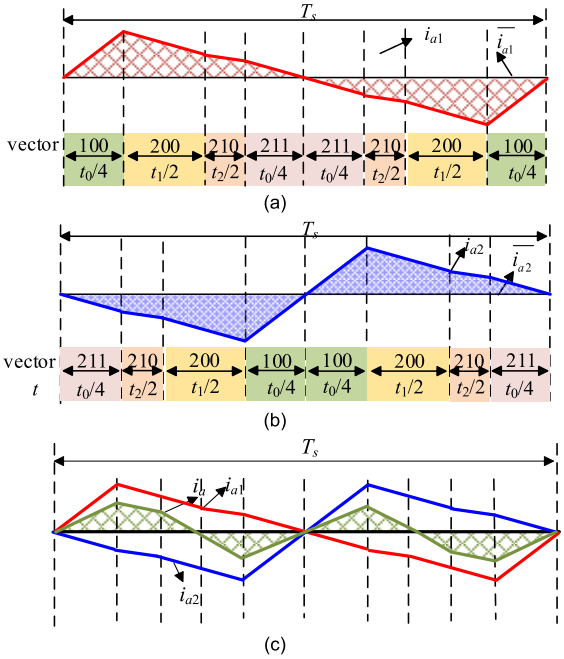

FIGURE 4. Current ripple with carrier phase shifted by 180° when the reference voltage is in Region I-5. (a) Current ripple of the first converter, (b) current ripple in the second converter, and (c) current ripple of the total current.

rectifier, $\overline{i_{a1}}$ stands for the average current in a carrier period, and t_0, t_1 and t_2 are the action times of the voltage space vectors. The ripple frequency is the same as the switching frequency.

The paralleled converters share the same reference voltage, so the voltage vectors are the same. In the conventional 180° carrier phase shift method, the voltage sequence and current of the a phase in the second rectifier are shown in

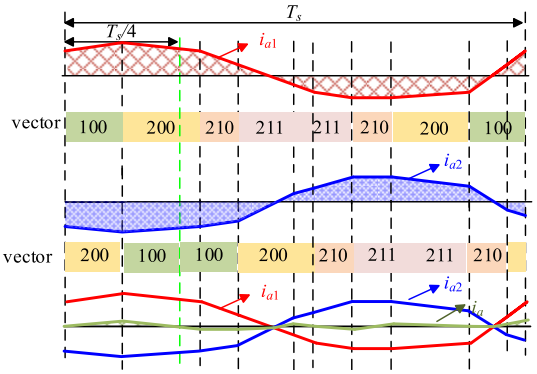

FIGURE 5. Current ripple with carrier phase shifted by 90° when the reference voltage is in Region I-5.

Fig. 4(b), where i_{a2}represents the instantaneous current of the a phase in the second rectifier and $\overline{i_{a2}}$ stands for the average current in a carrier period. The voltage sequence is changed to 211-210-200-100, which is shifted 180° compared with the first converter.

The input current of paralleled rectifiers is the sum of i_{a1} and i_{a2}, which is shown in Fig. 4(c). Here, i_a is the instantaneous input current of a phase of interleaved rectifiers. It is clearly seen that the input current ripple of interleaved rectifiers is the sum of the input currents of two rectifiers, which share twice the switching frequency.

IV. NOVEL MODULATION METHOD

A. ZSCC ANALYSIS WITHCARRIER PHASE SHIFTED BY 90°

As analyzed above, the amplitude of the current ripple is the sum of the two currents when applying the carrier phase shift by the 180° method in the interleaved rectifiers. The b phase and c phase are the same as the a phase. Thus, the conventional 180° phase-shift method to reduce the current ripple is limited. An effective method to reduce the input current ripple is modifying the phase-shifted angle to 90° in the second rectifier.

Assume that the reference voltage is located in Region I-5, as shown in Fig. 2. The voltage vector sequence is 100-200-210-211, and the corresponding current ripple is shown in Fig. 5. For another leg of the a phase in the interleaved rectifiers, the vectors lag $T_s/4$ behind the first rectifier. The input current of the interleaved rectifiers is the sum of the two legs, which is shown in Fig. 5. It is clearly seen that the current ripple amplitude is significantly reduced using the carrier phase-shifted by 90°, as the current ripples of the two legs in a phase are canceled most of the time in a period.

A simulation using 90° and 180° carrier phase-shift methods is shown in Fig. 6. It is clearly shown that the current harmonics are reduced from 1.7% to 1.59% when using the 90° carrier phase-shift method, which verifies the analysis above.

As analyzed above, using the 90° carrier phase-shifted method can reduce the current harmonics. In addition, the method can achieve a lower ZSCC compared with the 180° carrier phase-shifted method [29]. Therefore, we select the 90° carrier phase-shift method.

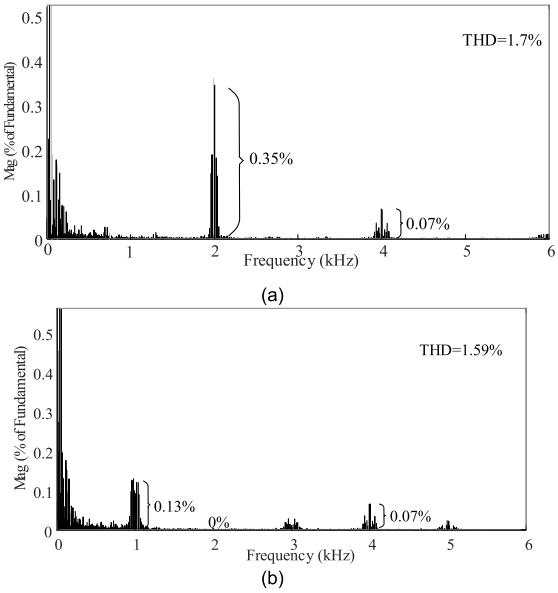

FIGURE 6. Current spectrum and THD value comparison of current i_a in different phase shift methods. (a) simulation results in the 180° carrier phase-shifted method (b) simulation results in the 90° carrier phase-shifted method.

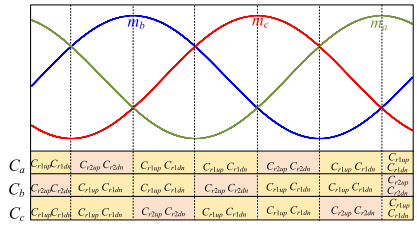

FIGURE 7. Carrier selection operation of rectifier 1 in a fundamental cycle (m_a, m_b, m_c represent three reference voltages).

TABLE 2. Voltage vectors and their CMV values.

CMV	Region I	Region II	Region III	Region IV	Region V	Region VI
$-V_{dc}/2$	000	000	000	000	000	000
$-V_{dc}/3$	100	010	010	001	001	100
$-V_{dc}/6$	110	110	011	011	101	101
	200	020	020	002	002	200
0	111	111	111	111	111	111
	210	120	021	012	102	201
$V_{dc}/6$	211	121	121	112	112	211
	220	220	022	022	202	202
$V_{dc}/3$	221	221	122	122	212	212
$V_{dc}/2$	222	222	222	222	222	222

B. REDUCTION OF HIGH FREQUENCY ZSCC

According to (3), the CMV of all voltage vectors is shown in Table 2.

The high-frequency ZSCC is from the instantaneous CMV difference in the interleaved converters, and its change rate

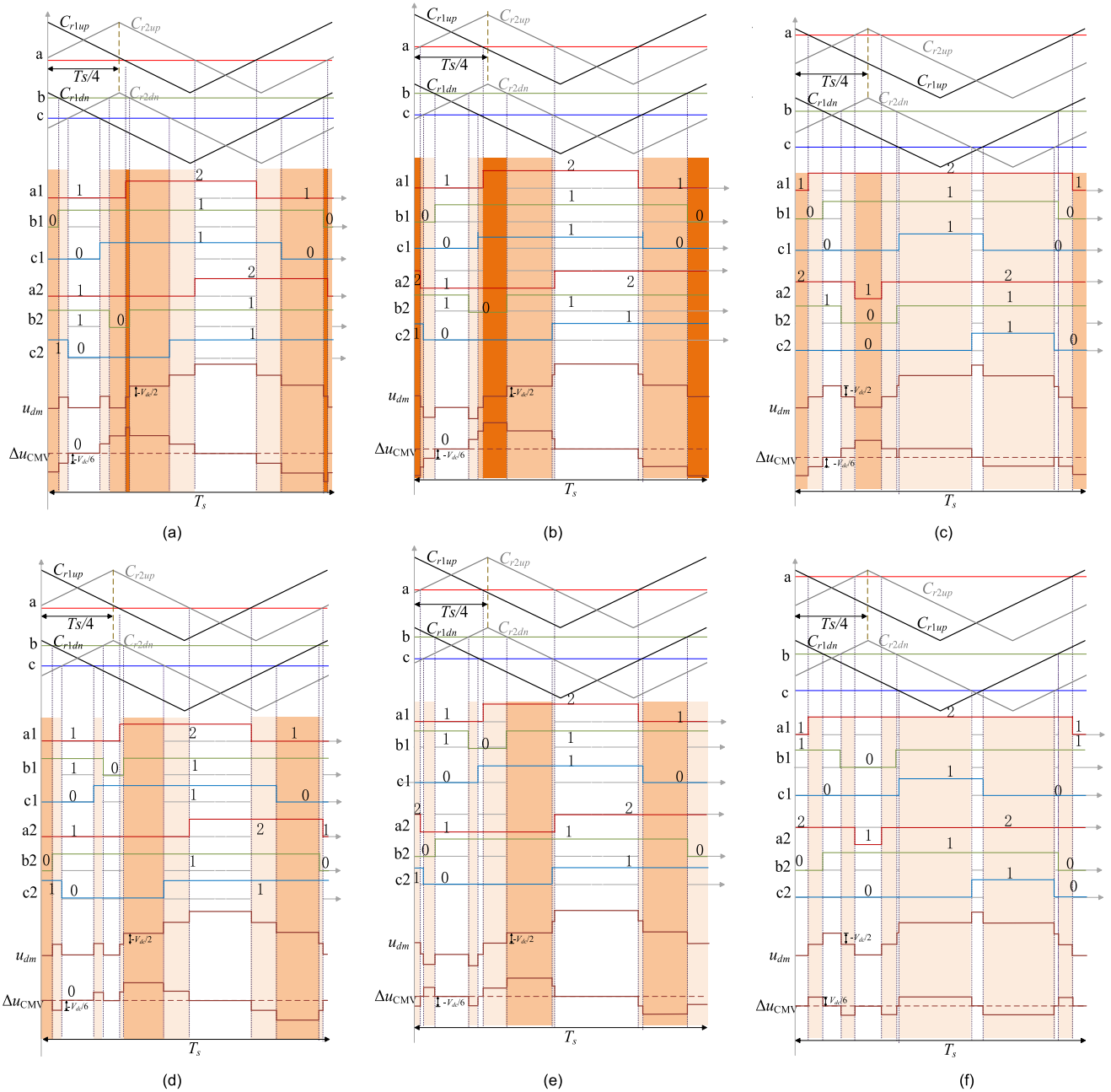

FIGURE 8. DM voltage u_{dm} and CM voltage difference Δu_{CMV} of parallel NPC rectifier when the voltages are in different regions of different methods. (a) voltages of 90° carrier phase shift in Region I-1, (b) voltages of 90° carrier phase shift in Region I-3, (c) voltages of 90° carrier phase shift in Region I-5, (d) voltages of proposed method in Region I-1, (e) voltages of proposed method in Region I-3, (f) voltages of proposed method in Region I-5 (a1,a2, b1, b2, c1, c2, represent switching signals).

can be expressed as [30]

$$l\frac{di_{cir}}{dt} = \Delta u_{CMV} = \frac{V_{dc}(S_{sa1} - S_{sa2} + S_{sb1} - S_{sb2} + S_{sc1} - S_{sc2})}{2L} \tag{10}$$

As discussed above, the 90° carrier phase-shift method can achieve a lower current ripple. Meanwhile, as discussed by the state-of-the-art ZSCC suppression methods, it is essential to maintain low ZSCC change rates to suppress ZSCC.

Fig. 7 shows the carrier selection results of converter 1, and the results are inversed for converter 2, where C_a, C_b, and C_c represent the carrier selection. Based on Fig. 8, C_{r2up} and C_{r2dn} are the carriers that lag C_{r1up} and C_{r1dn} at 90°, respectively. It can be seen that the proposed method exchanges the carrier in the same phase of two rectifiers, leading to a more equal CMV distribution. Fig. 8 shows the carrier comparison results when the reference voltage is in Region I-1, Region I-3 and Region I-5, where the carrier is interleaved by 90°. Fig. 8(a) and (b) and (c) show the results with the 90° carrier phase-shift method. Fig. 8(d), (e) and (f)

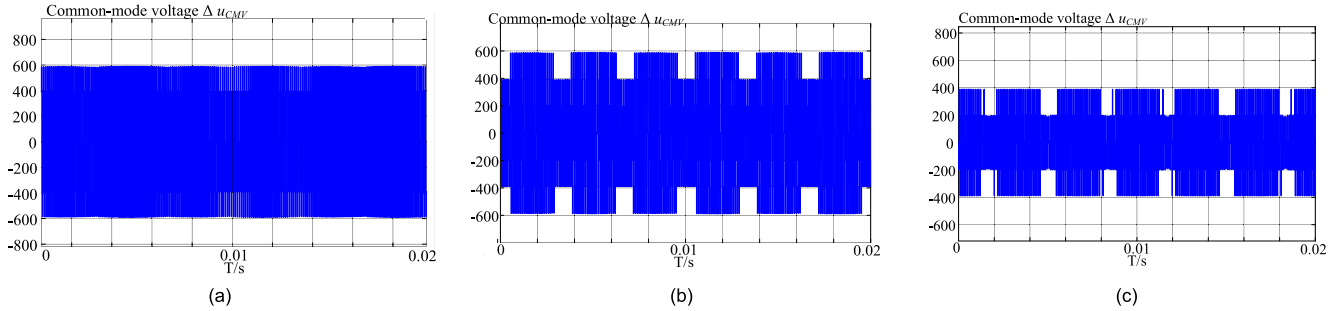

FIGURE 9. Simulation results of common mode voltage Δu_{CMV} of different methods. (a) Method-1, (b) Method-2, (c) Method-3.

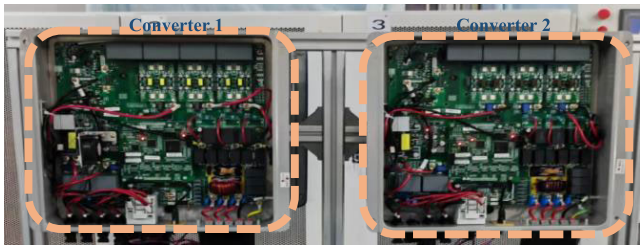

FIGURE 10. Experimental platform for two paralleled rectifiers.

TABLE 3. Parameters for simulation and experiment.

Quantity	Symbol	Unit	Value
Grid voltage	e_a, e_b, e_c	V	110
Rectifier-side Filter	L	mH	2
Grid-side Filter	L_g	mH	1
Fundamental frequency	f_g	Hz	50
Switching frequency	f_s	kHz	10

show the results of using the proposed method. For the voltage reference in Region I-1, the maximum CMV of the 90° carrier phase-shift method is $1/2V_{dc}$ and the minimum is $-1/2V_{dc}$, but the maximum CMV of the proposed method is $1/3V_{dc}$ and the minimum is $-1/3V_{dc}$, which means that the proposed method has a smaller CM variation. In Region I-3, the maximum of the 90° carrier phase shift is $1/2V_{dc}$, using the proposed method, the value is reduced to $1/3V_{dc}$. As for the CMV in Region I-5, the value is reduced to $1/6V_{dc}$ from the original value $1/3V_{dc}$. Besides, the proposed method does not change the CMV from the load. Similar results can be verified from other regions for all voltage space vector diagrams.

V. VERIFICATION AND DISCUSSION

To confirm the correctness of the theoretical analysis and effectiveness of the proposed method, a simulation is constructed using the parameters in Table 3. The effects of different methods are compared. Method-1 is the conventional 180° carrier phase-shifted method. Method-2 is the 90° carrier phase-shift method. Method-3 is the proposed method.

The common mode voltage Δu_{CMV} of different methods when the modulation index is 0.7 is shown in Fig. 9. The proposed method has the smallest voltage, so the ZSCC will be smallest.

A parallel three-level converter platform is constructed as shown in Fig. 10. The control schemes are implemented with DSP2812 and CPLD. The parameters for the experiment are also shown in Table 3.

A. OUTPUT PERFORMANCE

The experimental results for different methods in different modulation indices are expressed in Figs. 11–14, where i_a is the grid current, i_{a1} is the input current of the first rectifier, i_{a2} is the current in the second rectifier, and $3i_z$ is three times the ZSCC, which is the sum of three-phase currents. It can be seen that these methods have significant differences in ZSCC when m = 0.3. Method-1 has the maximum value in the ZSCC peak of 0.65 A, which is higher than that of the other methods. Method-3 has the lowest ZSCC value. When m = 0.5, the ZSCC in Method-1 is maximum, and Method-3 has the minimum ZSCC peak. A similar trend is observed when m = 0.8 and m = 1. It can be seen that in three methods, the proposed method can achieve the lowest ZSCC peak value in different modulation indices.

Fig. 15 summarizes the results of the line current THD value. The current THD value is similar in the three methods when m is less than 0.6. It can be seen that the proposed method has the same performance in the current THD value compared with Method-2.

Fig. 16 shows the experimental results of the ZSCC peak value. The proposed method can significantly reduce the ZSCC. The proposed method can achieve a 50% reduction in the maximum ZSCC peak compared with Method-1 and Method-2. Therefore, through a comparison of the experimental results of the current THD value and ZSCC peak value, the effectiveness of the proposed method is verified.

B. POWER LOSS

The total loss of parallel rectifiers under different methods is shown in Fig. 17, which is carried out by PLECS simulation. To acquire approximate results in the experiment and simulation, we chose the same switching device 10-FZ12NMA080SH01 from Vincotech to operate the simulation. The datasheet of the switching device is shown on the website from Vincotech [28].

When the modulation index is 0.4, as shown in Fig. 17(a), the switching loss and conduction loss are almost the same

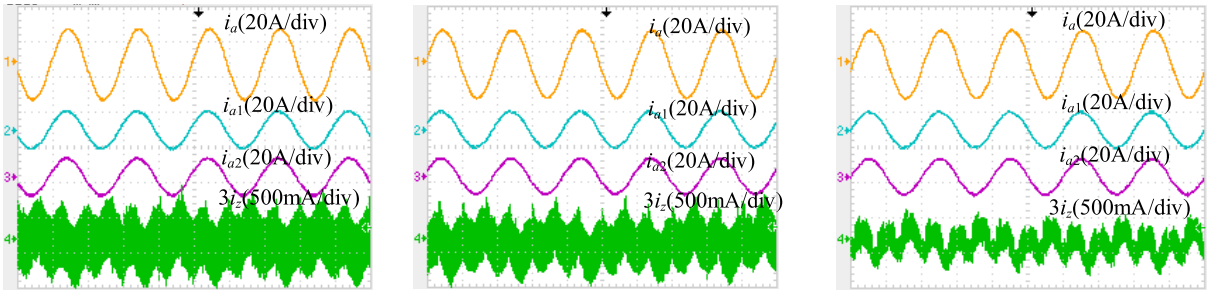

FIGURE 11. Experiment results of current i_a, i_{a1}, i_{a2}, $3i_z$ when m = 0.3 in different methods. (a) Method-1, (b) Method-2, (c) Method-3. (Current i_a presented in yellow, current i_{a1} presented in blue, current i_{a2} presented in purple and current $3i_z$ presented in green.)

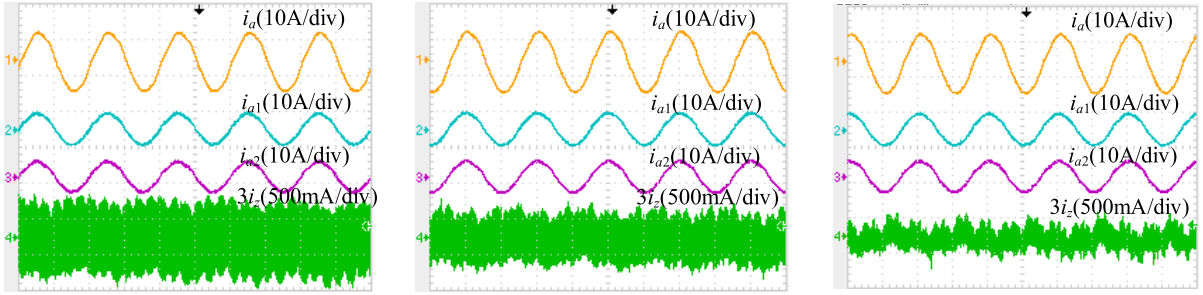

FIGURE 12. Experiment results of current i_a, i_{a1}, i_{a2}, $3i_z$ when m = 0.5 in different methods. (a) Method-1, (b) Method-2, (c) Method-3. (Current i_a presented in yellow, current i_{a1} presented in blue, current i_{a2} presented in purple and current $3i_z$ presented in green.)

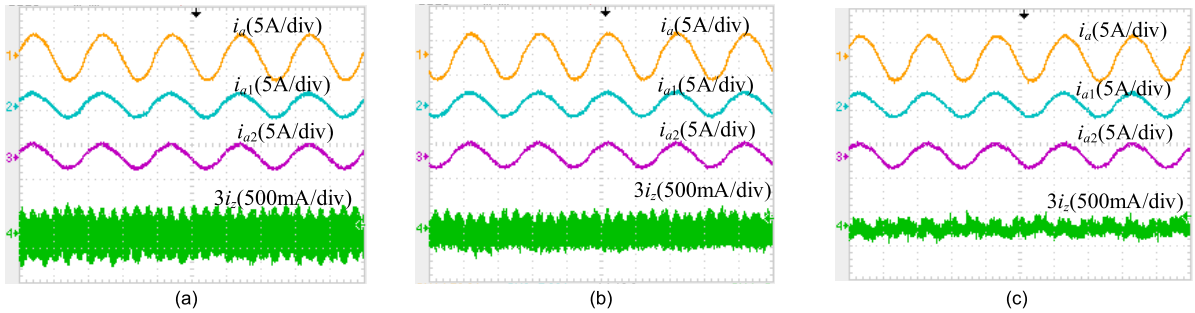

FIGURE 13. Experiment results of current i_a, i_{a1}, i_{a2}, $3i_z$ when m = 0.8 in different methods. (a) Method-1, (b) Method-2, (c) Method-3. (Current i_a presented in yellow, current i_{a1} presented in blue, current i_{a2} presented in purple and current $3i_z$ presented in green.)

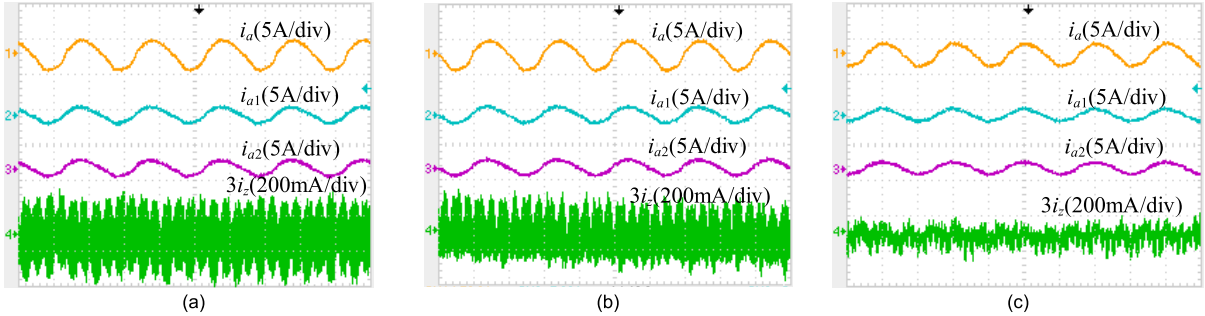

FIGURE 14. Experiment results of current i_a, i_{a1}, i_{a2}, $3i_z$ when m = 1 in different methods. (a) Method-1, (b) Method-2, (c) Method-3. (Current i_a presented in yellow, current i_{a1} presented in blue, current i_{a2} presented in purple and current $3i_z$ presented in green.)

for the three methods. Method-3 has a slight increase in total loss compared with Method-1. In Fig. 17(b), the modulation index is set at 0.8. The proposed method has a small advantage in total loss compared with Method-2. Therefore, it is found that the proposed method has a slight advantage in reducing ZSCC at high and low modulation indices.

The comparison of the harmonic components in the proposed method and limits of harmonic components established by IEC standards are shown in Fig. 18. The experiment is

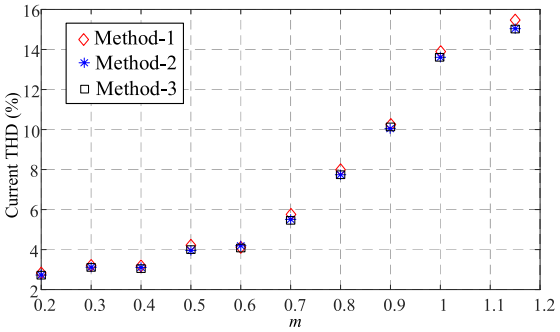

FIGURE 15. Line current THD value comparison of different methods when the modulation index varies.

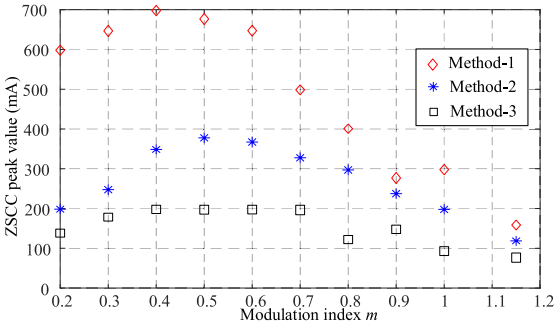

FIGURE 16. ZSCC peak value comparison of the three methods when the modulation index varies.

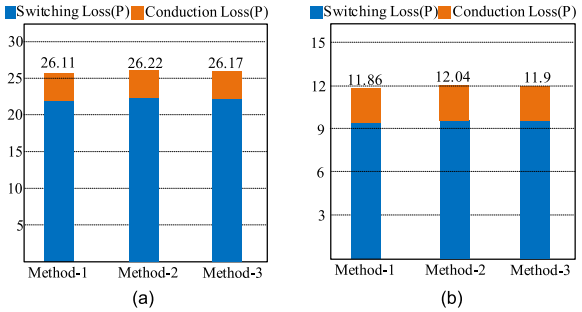

FIGURE 17. Semiconductor device loss in three methods for different modulation indices. (a) m = 0.4, (b) m = 0.8. (The value represents the sum of the switching loss and conduction loss.)

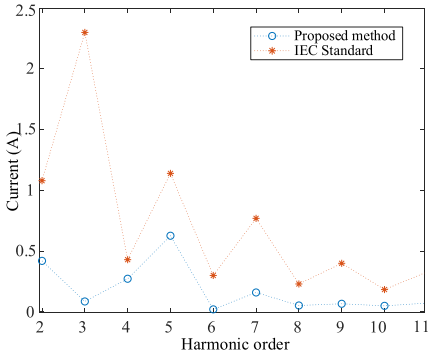

FIGURE 18. Comparison results of the proposed method and limits of harmonic components in the IEC standard.

conducted with a modulation index of 0.6 and a line current of 16 A. The output of the proposed method satisfies the requirements of the IEC standard.

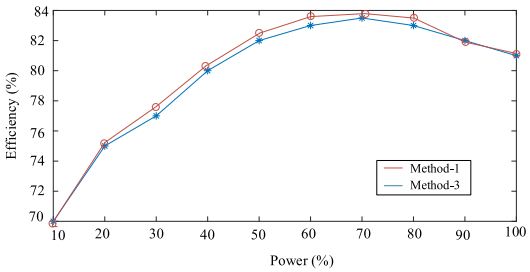

FIGURE 19. Efficiency comparison of Method-1 and Method-3.

Moreover, the efficiency curves of Method-1 and Method-3 are shown in Fig. 19. We can see that compared with the conventional 180° phase-shifted method, the proposed method has a slight efficiency reduction.

VI. CONCLUSION

The conventional 180° carrier phase-shifted method generates a larger HF-ZSCC, which will increase the current harmonics and affect the filter size. In this paper, a novel modulation method is proposed to reduce the ZSCC and current ripple in a parallel interleaved rectifier system. The main characteristics of the proposed method are as follows:

1) Use the 90° carrier phase-shift method to reduce the line current harmonics.

2) To reduce the HF-ZSCC, an exchange of pulses in large ZSCC is made in two converters. With the proposed method, the CMV of each converter is distributed more equally, and the differences of each CMV are mitigated; thus, the ZSCC peak value is reduced significantly.

The experimental results confirmed the benefits of the proposed method across a large modulation region.

REFERENCES

[1] X. Liu, T. Liu, A. Chen, X. Xing, and C. Zhang, "Circulating current suppression for paralleled three-level T-type inverters with online inductance identification," *IEEE Trans. Ind. Appl.*, vol. 57, no. 5, pp. 5052–5062, Sep. 2021.

[2] Z. Li, Z. Nie, and S. Ai, "Nonlinear modeling and improved suppression of zero-sequence circulating current for parallel three-level inverters," *IEEE J. Emerg. Sel. Topics Power Electron.*, early access, Jan. 13, 2023, doi: 10.1109/JESTPE.2023.3236797.

[3] Q. Li, Y. Ma, X. Zhao, D. Jiang, and Y. Zhang, "VSFPWM based on circulating current ripple prediction for ZVS in two paralleled grid-tied inverters with coupled inductors," *IEEE Trans. Ind. Electron.*, vol. 70, no. 1, pp. 39–51, Jan. 2023.

[4] X. Xing, Z. Zhang, C. Zhang, J. He, and A. Chen, "Space vector modulation for circulating current suppression using deadbeat control strategy in parallel three-level neutral-clamped inverters," *IEEE Trans. Ind. Electron.*, vol. 64, no. 2, pp. 977–987, Feb. 2017.

[5] V. Yaramasu and B. Wu, "Predictive control of a three-level boost converter and an NPC inverter for high-power PMSG-based medium voltage wind energy conversion systems," *IEEE Trans. Power Electron.*, vol. 29, no. 10, pp. 5308–5322, Oct. 2014.

[6] Z. Zhang, C. M. Hackl, and R. Kennel, "Computationally efficient DMPC for three-level NPC back-to-back converters in wind turbine systems with PMSG," *IEEE Trans. Power Electron.*, vol. 32, no. 10, pp. 8018–8034, Oct. 2017.

[7] J. Chen, H. Wu, J. Zhu, L. Li, and Y. Xing, "A three-phase AC/DC power system with paralleled active and passive rectifiers for low-frequency pulsed load applications," in *Proc. IEEE 9th Int. Power Electron. Motion Control Conf. (IPEMC-ECCE Asia)*, Nov. 2020, pp. 1595–1599.

[8] B. Wu, *High-Power Converters AC Drives*. Hoboken, NJ, USA: Wiley, Mar. 2006.
[9] Z.-X. Zou, F. Hahn, G. Buticchi, S. Gunter, and M. Liserre, "Interleaved operation of two neutral-point-clamped inverters with reduced circulating current," *IEEE Trans. Power Electron.*, vol. 33, no. 12, pp. 10122–10134, Dec. 2018.
[10] Y. Shi, Y. Zhang, L. Wang, and H. Li, "Reduction of EMI noise due to nonideal interleaving in a 100 kW SiC PV converter," *IEEE Trans. Power Electron.*, vol. 34, no. 1, pp. 13–19, Jan. 2019.
[11] A. Chen, Z. Zhang, X. Xing, K. Li, C. Du, and C. Zhang, "Modeling and suppression of circulating currents for multi-paralleled three-level T-type inverters," *IEEE Trans. Ind. Appl.*, vol. 55, no. 4, pp. 3978–3988, Jul./Aug. 2019.
[12] X. Xing, X. Li, C. Qin, J. Chen, and C. Zhang, "An optimized zero-sequence voltage injection method for eliminating circulating current and reducing common mode voltage of parallel-connected three-level converters," *IEEE Trans. Ind. Electron.*, vol. 67, no. 8, pp. 6583–6596, Aug. 2020.
[13] C. Jiang, Z. Quan, D. Zhou, and Y. Li, "A centralized CB-MPC to suppress low-frequency ZSCC in modular parallel converters," *IEEE Trans. Ind. Electron.*, vol. 68, no. 4, pp. 2760–2771, Apr. 2021.
[14] K. Kim, H.-J. Kim, D. Shin, J.-P. Lee, T.-J. Kim, J.-W. Baek, and D.-W. Yoo, "Design of current controller with circulation current reduction for parallel three phase voltage inverter," in *Proc. 19th Eur. Conf. Power Electron. Appl. (EPE ECCE Eur.)*, Sep. 2017, p. 1.
[15] S. He, A. Sun, and B. Liu, "Zero-sequence circulating current analysis and suppression for multimodular interleaved parallel inverters," *IEEE J. Emerg. Sel. Topics Power Electron.*, vol. 10, no. 6, pp. 7000–7013, Dec. 2022.
[16] Z. Zeng, Z. Li, and S. M. Goetz, "Line current ripple minimization PWM strategy with reduced zero-sequence circulating current for two parallel interleaved three-phase converters," *IEEE Trans. Power Electron.*, vol. 35, no. 7, pp. 6931–6943, Jul. 2020.
[17] Z. Zeng, Z. Li, and S. M. Goetz, "Optimal discontinuous space vector PWM for zero-sequence-circulating current reduction in two paralleled three-phase two-level converter," *IEEE Trans. Ind. Electron.*, vol. 68, no. 2, pp. 1252–1262, Feb. 2021.
[18] Z. Zeng, Z. Li, and S. M. Goetz, "A high performance interleaved discontinuous PWM strategy for two paralleled three-phase inverter," *IEEE Trans. Power Electron.*, vol. 35, no. 12, pp. 13042–13052, Dec. 2020.
[19] H. Xu, "Improved interleaved discontinuous PWM for zero-sequence circulating current reduction in three-phase paralleled converters," *IEEE Trans. Ind. Electron.*, vol. 68, no. 9, pp. 8676–8686, Sep. 2021.
[20] A. Tcai, Y. Kwon, S. Pugliese, and M. Liserre, "Reduction of the circulating current among parallel NPC inverters," *IEEE Trans. Power Electron.*, vol. 36, no. 11, pp. 12504–12514, Nov. 2021.
[21] W. Li, X. Zhang, and D. Xu, "Integrated modulation of dual-parallel NPC inverters with eliminated CMV," *IEEE Trans. Ind. Electron.*, vol. 69, no. 8, pp. 8113–8122, Aug. 2022.
[22] W. Li, X. Zhang, Y. Zhuang, G. Zhang, G. Wang, and D. Xu, "A five-level space vector modulation scheme for parallel operated three-level inverters with reduced line current distortion," *IEEE Trans. Power Electron.*, vol. 35, no. 10, pp. 11235–11249, Oct. 2020.
[23] W. Li, X. Zhang, Z. Zhao, G. Zhang, G. Wang, and D. Xu, "Implementation of five-level DPWM on parallel three-level inverters to reduce common-mode voltage and AC current ripples," *IEEE Trans. Ind. Appl.*, vol. 56, no. 4, pp. 4017–4027, Jul. 2020.
[24] Z. Quan and Y. W. Li, "Phase-disposition PWM based 2DoF-interleaving scheme for minimizing high frequency ZSCC in modular parallel three-level converters," *IEEE Trans. Power Electron.*, vol. 34, no. 11, pp. 10590–10599, Nov. 2019.
[25] M. Gu, Z. Wang, K. Yu, X. Wang, and M. Cheng, "Interleaved model predictive control for three-level neutral-point-clamped dual three-phase PMSM drives with low switching frequencies," *IEEE Trans. Power Electron.*, vol. 36, no. 10, pp. 11618–11630, Oct. 2021.
[26] R. Chen, "Modeling, analysis, and reduction of harmonics in paralleled and interleaved three-level neutral point clamped inverters with space vector modulation," *IEEE Trans. Power Electron.*, vol. 35, no. 4, pp. 4411–4425, Apr. 2020.
[27] T. Wang, C. Chen, P. Liu, T. Liu, Z. Chao, and S. Duan, "A hybrid space-vector modulation method for harmonics and current ripple reduction of interleaved Vienna rectifier," *IEEE Trans. Ind. Electron.*, vol. 67, no. 10, pp. 8088–8099, Oct. 2020.
[28] J. Niu, R. Chen, Z. Zhang, H. Gui, F. Wang, L. M. Tolbert, B. J. Blalock, D. J. Costinett, and B. B. Choi, "Analysis of circulating harmonic currents in paralleled three level ANPC inverters using SVM," in *Proc. IEEE Appl. Power Electron. Conf. Expo. (APEC)*, Mar. 2019, pp. 2481–2487.
[29] Z. Quan and Y. W. Li, "A three-level space vector modulation scheme for paralleled converters to reduce circulating current and common-mode voltage," *IEEE Trans. Power Electron.*, vol. 32, no. 1, pp. 703–714, Jan. 2017.
[30] L. Wei, J. McGuire, and R. A. Lukaszewski, "Analysis of PWM frequency control to improve the lifetime of PWM inverter," *IEEE Trans. Ind. Appl.*, vol. 47, no. 2, pp. 922–929, Mar. 2011.

YANFENG LI was born in Shandong, China, in 1986. He received the B.S. degree in applied physics from the Henan University of Science and Technology, Luoyang, China, in 2007, and the M.S. degree in electrical theory and new technology from Huaqiao University, Quanzhou, China, in 2010.

From 2010 to 2022, he was a Senior Power Engineer with Shandong Aotai Electric Company Ltd., which is a leading manufacturer of inverter welding and cutting equipments and solar inverters in China. His research interests include digital control systems, power electronics, DC/AC converters, and DC/DC converters.

HONGLIANG ZHANG was born in Shandong, China, in 1981. He received the M.S. degree from the School of Control Science and Engineering, Shandong University, Jinan, China, in 2007, where he is currently pursuing the Ph.D. degree in advanced manufacturing. His current research interests include multi-level inverters, micro-grid control technology, and renewable power generation.

XIAO JING was born in Shandong, China, in 1987. He received the B.S. degree in applied physics from the Qilu University of Technology, Jinan, China, in 2011, and the M.S. degree in control science and engineering from Shandong University, Jinan, in 2014.

From 2014 to 2022, he was an Intermediate Engineer with Shandong Aotai Electric Company Ltd. His research interests include digital control systems and high-power DC/AC converters.

AIGUANG ZHAO was born in Shandong, China, in 1985. He received the B.S. degree in automation from the University of Jinan, Jinan, China, in 2010.

From 2010 to 2022, he was a Power Electronics Engineer with Shandong Aotai Electric Company Ltd. His research interests include PV series string inverter, hybrid inverter, LLC converter, and digital control systems.