IEEE Access
Multidisciplinary ⋮ Rapid Review ⋮ Open Access Journal

Received 13 February 2023, accepted 7 March 2023, date of publication 10 March 2023, date of current version 17 March 2023.

Digital Object Identifier 10.1109/ACCESS.2023.3256079

RESEARCH ARTICLE

Broadband InGaP/GaAs HBT Doherty Power Amplifier IC Using Direct Interstage Power Division for Compact 5G NR Handset Module

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This work was supported by the Institute of Information and Communications Technology Planning and Evaluation (IITP) Grant funded by the Korea Government (MSIT) (Ku-band RF front-end module (RF-FEM) development) under Grant 2022-0-00938.

ABSTRACT This paper presents a 2.8-3.8 GHz broadband 2-stage fully differential Doherty power amplifier using direct interstage power division based on a 2-μm InGaP/GaAs HBT process for 5G new radio handset applications. A compact transformer-less interstage network is proposed for direct power division for carrier and peaking amplifiers. The power division ratio at the interstage is designed to dynamically vary according to the input power level to provide higher power gain and desired load impedance modulation. By utilizing the non-linear input reactance of the peaking amplifier, broadband dynamic power division circuits were designed for an operating frequency band of as broad as 1 GHz. In addition, active bias circuits for the peaking amplifier were optimized to have sufficient gain expansion, so that the overall AM-AM characteristics is as flat as possible. A broadband load modulation network using one transformer and two quarter-wave transmission lines is proposed. For the off-chip output transformer, impedance trajectory for the wide band impedance matching is presented using a T-equivalent circuit of the transformer. The self-inductance ratio of the transformer is optimized to maximize the bandwidth. Using the 5G new radio uplink signal with a signal bandwidth of 100 MHz, the implemented Doherty PA IC exhibited a power gain of 31.9 to 38.4 dB, PAE of 22.0 to 30.6%, and average output power of 26.0 to 27.8 dBm at a given ACLR of −33.0 dBc without pre-distortion.

INDEX TERMS InGaP/GaAs HBT, Doherty power amplifier, differential power amplifier, direct power division, transformer-less interstage, 5G new radio.

I. INTRODUCTION

To improve the efficiency of power amplifiers (PAs) for mobile handsets, supply modulation techniques have been widely used [1], [2], [3], [4]. The upcoming 5G new radio (NR) has higher data rates due to the increased signal bandwidth and modulation index. The modulated signal for the 5G NR has a signal bandwidth of more than 100 MHz. The wider the signal bandwidth, the more difficult it is to design the supply modulator for the envelope tracking method. In addition to the supply modulation techniques, several methods, such as harmonic control [5], [6], phase linearization [7], and stacked power cell methods [8], [9], have been reported to improve the performances of the PAs.

As the operating frequency increases, the performances can be further degraded due to the increased degeneration effect at the source of the transistor especially for the single-ended structure. To mitigate this source degeneration effect

The associate editor coordinating the review of this manuscript and approving it for publication was Olutayo O. Oyerinde.

and to increase the optimum load impedance, a differential structure can be used to take an advantage of its virtual ground [10], [11].

To further improve the back-off efficiency, Doherty PA IC's with improved efficiency at an average power level using the load impedance modulation have been reported [12], [13], [14], [15], [16], [17], [18], [19]. In [13], bandwidth limiting factors of the Doherty PA was analysed. Accordingly, Q factors of the λ/4 line and the post matching network at the load network were balanced to extend the bandwidth. In [14], asymmetric power cells for carrier and peaking amplifiers with uneven Wilkinson power divider were adopted for better load modulation. The Doherty PAs in [12], [13], and [14] consist of single-ended carrier and peaking amplifiers that are required to have very low optimum load impedance (about a few Ω) for the peak power level of 2-3 W with the supply voltage of about 3.0-4.8 V. Low optimum impedance can limit the bandwidth of the load modulation network (LMN) of the Doherty PAs. In [15], a Doherty PA based on a parallel plate coupler was proposed. However, it has a 3-section off-chip post matching network which makes the PA module bulky.

Compared to the Class-AB PAs, Doherty PAs generally have relatively lower power gain of up to 3 dB. Low gain degrades the power-added efficiency (PAE), and increases the burden of the driver PA. In [16], a differential structure was adopted for the carrier and peaking amplifiers. The power cell of each amplifier has increased optimum load impedance which can result in the wider bandwidth and lower loss of the load network. However, two off-chip transformers (TFs) are required to design the load network, which can make the module bulkier. A fully differential two-stage Doherty PA was proposed using differential pairs for both carrier and peaking amplifiers and two TFs for the interstage network [17]. Drive amplifiers are also based on a differential pair. Thus, the input network should be designed with a single-ended to double-differential TF or two TFs followed by a quadrature hybrid. However, those topologies require complex and bulky circuits for the input and interstage networks.

To divide the input power into the carrier and peaking amplifier paths in more compact form without a power divider, a direct input dividing method was proposed in [18] and [19] for a single-ended Doherty PA for a narrow frequency band. As the frequency band and bandwidth for the 5G systems are increased, research on broadband and a compact power dividing method for the differential Doherty PA becomes more and more important. In this paper, a broadband Doherty PA IC for 5G NR handsets, which was partially presented in [20], is proposed with a new compact differential two-stage structure. Both carrier and peaking amplifiers for the main stage are configured as differential, while only one differential drive stage is employed. Broadband load modulation network is designed using one off-chip TF and two quarter-wave transmission lines for the bandwidth of as broad as 1 GHz. Compared to the conventional impedance trajectory for a T-equivalent circuit of the TF, the trajectory of the proposed TF has a lower Q to have wider operating bandwidth. The self-inductance ratio of the primary and secondary turns is optimized to lower the Q for the broadband design.

For the differential drive stage, a direct interstage power dividing network without TF was designed to dynamically supply power to the carrier and peaking amplifiers. In addition, the interstage network supports dynamic power dividing ratio (PDR) between the carrier and peaking amplifiers according to the input power by utilizing the non-linear input reactance of the Class-C peaking amplifier. At a low power level, the PDR becomes high to drive more power to the carrier amplifier to mitigate power gain degradation. As the power level increases, the PDR is designed to be gradually reduced to have a desired load modulation operation by suppling more power to the peaking amplifier. The input admittances of both amplifiers are elaborately matched by the interstage network for 1 GHz operating bandwidth based on the constant conductance circles on the Smith chart. By utilizing this dynamic variation of the PDR, the AM-AM characteristics can be flattened, together with high gain expansion of the peaking amplifier.

The proposed broadband Doherty PA IC was implemented using a 2-μm InGaP/GaAs HBT process, and evaluated as a module using a laminate PCB. The design procedure of the proposed direct power division circuit at the interstage and the LMN are presented in detail. The proposed methods are verified using the simulated and measured performances in comparison to the previous state-of-the art configurations.

II. BROADBAND DOHERTY PA WITH DIRECT POWER DIVISION AT THE INTERSTAGE

A. FULLY DIFFERENTIAL DOHERTY PA

Fig. 1 shows three structures of the fully differential two-stage Doherty PAs. Fig. 1(a) shows a conventional structure that has two drive amplifiers for the carrier and peaking amplifiers. Most of the previous two-stage differential Doherty PAs has this structure [17], [30], [31], [32]. Thus, the interstage network requires two TFs, such as $TF_{int,c}$ and $TF_{int,p}$. Offset lines to compensate for the phase difference between the carrier and the peaking path can be deployed at the input of the drive stage of the peaking amplifier. Load impedances of the carrier and peaking amplifiers are modulated by LMN. Three TFs including a single-to-double differential TF should be used at the input and interstage, which could make the circuit bulkier. However, the overall performance of the Doherty PA can be further optimized by setting the biases of the two drive amplifiers differently [21]. Fig. 1(b) shows a simplified structure that has only one differential drive amplifier and fully differential carrier and peaking amplifiers. This structure is proposed in this work but is not a final form. It requires one input TF and one differential-to-double differential TF. An offset line is inserted at the input of the peaking amplifier. Since there is one drive stage for both carrier and peaking

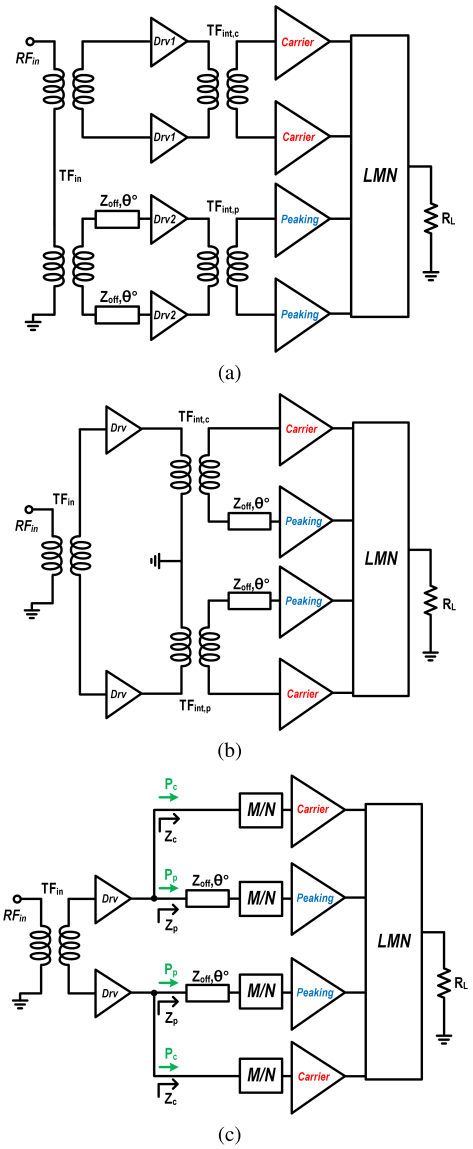

FIGURE 1. Structures of the fully differential 2-stage Doherty PAs: (a) using two drive amplifiers, (b) using one drive amplifier with interstage TFs, and (c) using one drive amplifier with direct interstage power division (proposed).

amplifiers, no separate bias tunability for the driver stage is available.

The proposed structure shown in Fig. 1(b) can be further simplified by applying the direct interstage power division method. Fig. 1(c) shows a new structure of the fully differential Doherty PA proposed in this work using the direct interstage power division method with no TF at the interstage. Instead of using TFs, relatively compact matching networks for the inputs of the carrier and peaking amplifiers are applied. The output current of the drive stage is directly divided according to the input impedances of the carrier and peaking amplifiers. Since the impedance of the Class-C peaking amplifier varies more dynamically according to the input power level, the PDR can be changed as well. The next sub-section explains how to design the circuit to take advantage of the dynamic PDR. The features of three fully differential Doherty PA structures are summarized and compared in Table 1.

TABLE 1. Comparison of the features for fully differential Doherty PAs.

Features	(a)	(b)	(c)
Number of drive amplifier (differential)	2	1	1
Number of TF at the input and interstage	3	3	1
Seperate bias tuning at the drive stage	Yes	No	No
Dynamic PDR	No	No	Yes

Fig. 2(a) shows a schematic of the proposed Doherty PA, showing all components, including parasitic capacitors (C_{out}). The input transformer (TF_{in}) is integrated on a chip and was designed using vertical coupling of two metal layers. It matches the input impedance of 9-j5 Ω with a simulated insertion loss of about 1.0-1.2 dB through the frequency band of 2.8-3.8 GHz. Using the interstage circuits based on series capacitors and shunt inductors, the power output of the drive amplifier is directly divided according to the input impedances of the carrier and peaking amplifiers. A 30 Ω quarter-wave line designed using a C-L-C structure is inserted at the input of the peaking amplifier for phase compensation. For the compact LMN, an output balun using a TF and two quarter-wave networks are used to provide load impedance modulation. A cross-coupled capacitor is added to the drive stage for higher gain. Parallel components connected to the same node can be merged to simplify the circuits. Fig. 2(b) shows a schematic of the proposed Doherty PA after circuit simplification. At the interstage, four shunt capacitors are merged, and are expressed as C_{int1}. Additionally, two shunt inductors and two shunt capacitors are merged, and are expressed as L_{int2}. L_{int3} at the low side supplies V_{cc1}, while L_{int3} at the high side is grounded using C_{byp}. At the collector of the carrier amplifier, a shunt capacitor including the parasitic capacitor (C_{out1}) is expressed as C_c. At the collector of the peaking amplifier, five capacitors including C_{out2} are merged into just one capacitor of C'_p.

B. GAIN EXPANSION AND DYNAMIC PDR

The Doherty PA has a relatively complicated mechanism for its AM-AM characteristics. For the low power level, since the peaking amplifier becomes relatively off, the AM-AM characteristics is mainly determined by the PDR at the input of the Doherty PA and the gain of the carrier amplifier. For the peak power level, the gain of the peaking amplifier additionally affects the AM-AM characteristics. PDR in this paper is defined as follows.

$$PDR = \frac{P_c}{P_p}, \tag{1}$$

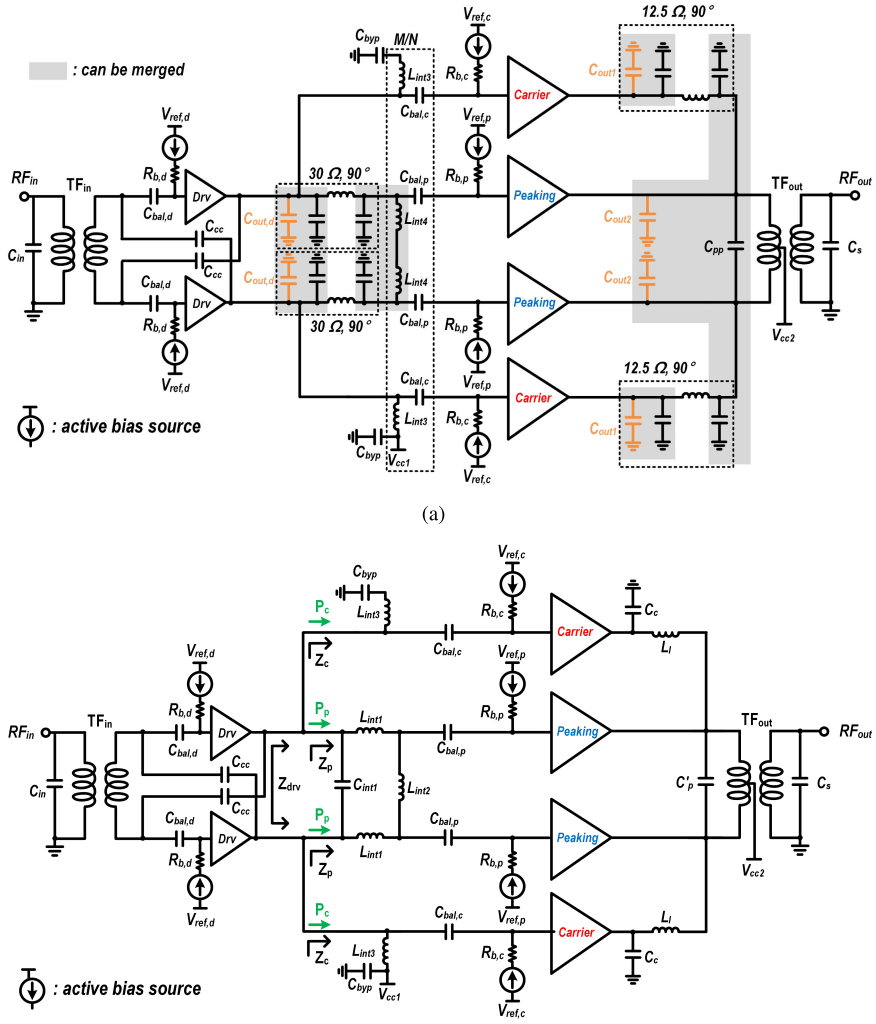

FIGURE 2. Schematics of the proposed Doherty PA (a) before, and (b) after circuit simplification.

where P_c and P_p are the input powers to the carrier and peaking amplifiers, respectively.

Fig. 3 shows a schematic of the active bias circuits for the carrier and peaking amplifiers. For PAs based on bipolar transistors, active bias circuits are required to supply current ($I_{b,c}$, $I_{b,p}$) to the base of the transistor, which affect RF performances. As the input RF power is changed, the DC current supplied from the bias circuits is also changed. The large signal operation is changed according to the DC current change as well. To simultaneously optimize the efficiency and linearity of the Doherty PA, the large signal characteristics of the carrier and peaking amplifiers should be differently optimized. The carrier amplifier needs to have linear operation with flat AM-AM characteristics until the peaking amplifier is turned on. On the other hand, the peaking amplifier is basically biased to have deep Class-C operation, which gives very low power gain, especially at the low power level. Therefore, as the input power increases, the gain expansion of the peaking amplifier should be high to maintain the overall AM-AM response of the Doherty PA to be as flat as possible. Hence, $R_{b,p}$ and $V_{ref,p}$ in the active bias circuits of the peaking amplifier are mainly optimized to provide as much high gain expansion characteristics as required.

Fig. 4(a) shows constant versus dynamic PDR according to the power level. A constant PDR (almost 1 or 0 dB) is obtained using an even power divider at the input of the main Doherty PA. The dynamic PDR is obtained from the design with direct interstage power division, which is presented in detail the next sub-section. Since the PDR varies gradually from about 3 dB to 1 dB for the dynamic PDR, higher gain can be achieved by supplying more power into the carrier amplifier at the low output power region. Since the PDR is still about 1 dB for the peak power level, the peaking amplifier should have high power gain at the peak power level to maintain flat AM-AM characteristics [22]. High power

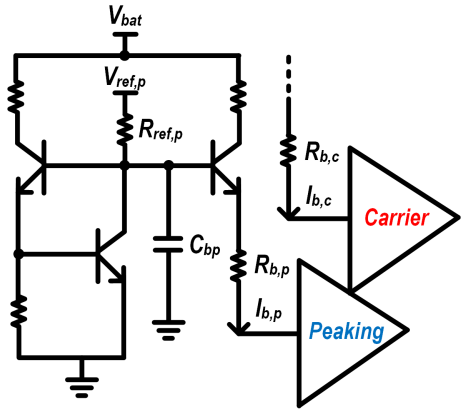

FIGURE 3. Schematic of the active bias circuits for the carrier and peaking amplifiers.

gain at the peak power level can be obtained by high gain expansion characteristics for Class-C amplifiers.

Fig. 4(b) shows the simulated gain and PAE for the main stage of the Doherty PA at 3.3 GHz with four cases with different bias resistor ($R_{b,p}$) values, bias points ($V_{ref,p}$), and PDR conditions for the peaking amplifier. $R_{b,c}$ and $V_{ref,c}$ are fixed at 52.5 Ω and 2.8 V, respectively, while C_{bp} is fixed as 2.7 pF. Fig. 4(b) shows the simulated gain of each carrier and peaking amplifier with four different cases. For case 1, bias resistors ($R_{b,p}$ and $R_{b,c}$) of the carrier and peaking amplifiers are the same as 52.5 Ω, and even power dividing with a constant PDR of about 0 dB is applied. The AM-AM characteristics is degraded due to the low gain of the peaking amplifier. For case 2, $V_{ref,p}$ of the peaking amplifier can be increased to increase the gain and to keep the AM-AM characteristics as flat as possible, which results in efficiency degradation at the back-off. To resolve this trade-off, the gain of the peaking amplifier can be expanded more according to the output power level by reducing $R_{b,p}$ without increasing $V_{ref,p}$ as shown in case 3. In this case, higher efficiency can be obtained even with very flat AM-AM characteristics compared to case 1. For case 4, the dynamic PDR scheme is additionally applied to have higher power gain. To make the AM-AM characteristics flat with the increased low power gain, $V_{ref,p}$ should be a little increased for the peaking amplifier to have higher power gain at the high power level than that of case 3. From Fig. 4, it can be known that the dynamic PDR and an appropriate level of power gain expansion of the peaking amplifier can increase the overall power gain, and can flatten the AM-AM characteristics of the Doherty PA.

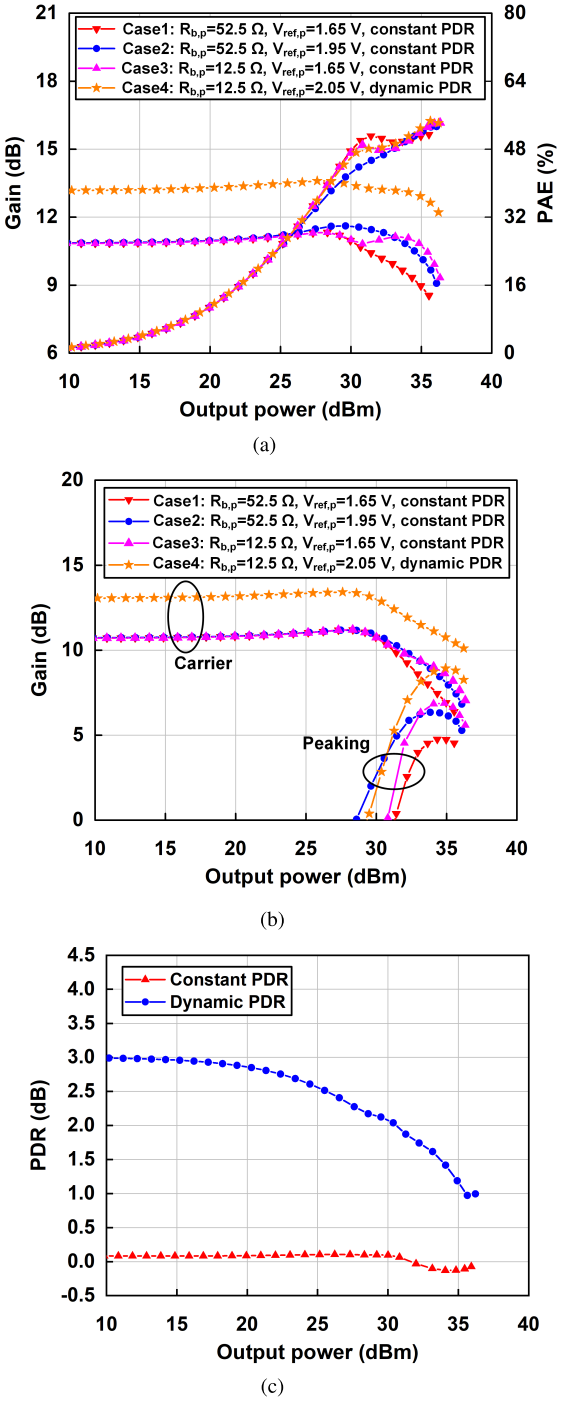

FIGURE 4. Simulated results of the main stage of the Doherty PA at 3.3 GHz: (a) overall gain and PAE for four different cases, (b) gain of each carrier and peaking amplifier, and (c) constant vs. dynamic PDR.

C. DIRECT INTERSTAGE POWER DIVISION FOR DYNAMIC PDR

Fig. 5 shows the schematic for the interstage and simulated impedance matching trajectories of the carrier amplifier in (b) and the peaking amplifier in (c). $Z_{b,c}$ and $Z_{b,p}$ are the input impedances of the carrier and peaking amplifiers, respectively. According to the input power levels, $Z_{b,p}$ significantly varies due to the strongly non-linear input capacitance of the Class-C peaking amplifier, while $Z_{b,c}$ varies much less. For the carrier amplifier, $Z_{b,c}$ is matched to Z_c using a series capacitor of $C_{bal,c}$ and a shunt inductor of L_{int3}. For the peaking amplifier, $Z_{b,p}$ is matched to be a higher impedance using a series capacitor of $C_{bal,p}$, and a shunt inductor of L_{int4}. Then, it is rotated to Z_p using a quarter-wave transmission line based on a C-L-C network. As shown, Z_p is wide-spread

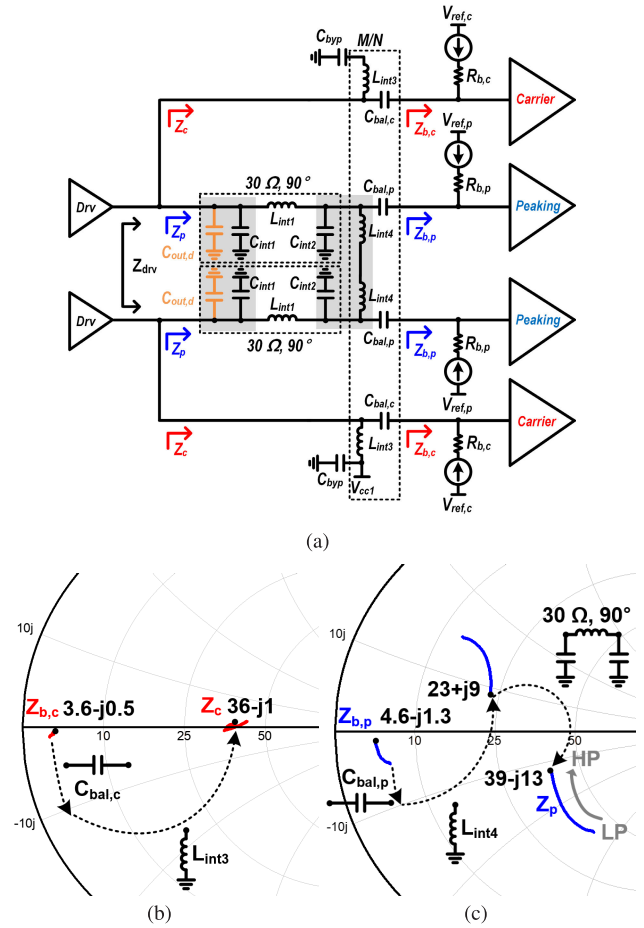

FIGURE 5. Schematic for the interstage and simulated impedance matching trajectories according to the output power levels at 3.4 GHz: (a) schematic, (b) matching for carrier amplifier, and (c) peaking amplifier.

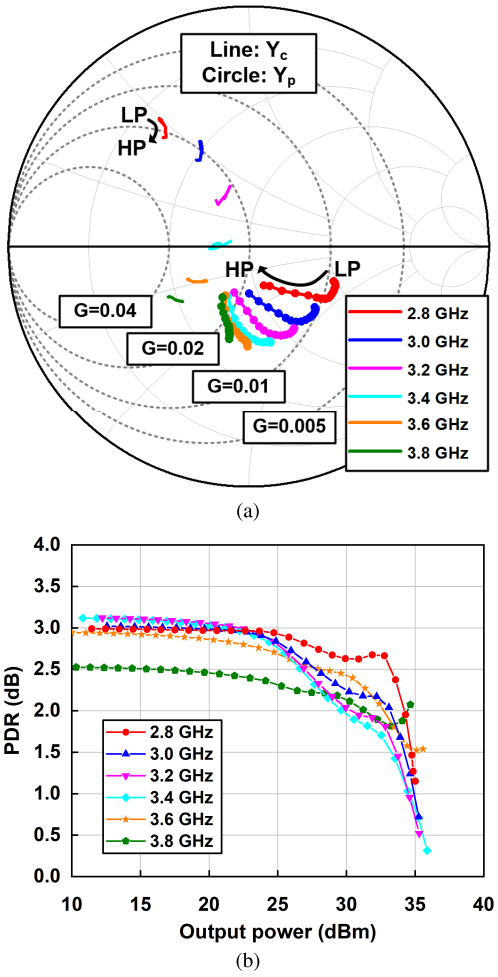

FIGURE 6. Simulated results of the direct interstage power dividing network for the frequency band of 2.8–3.8 GHz: (a) input admittances of Yc and Yp, and (b) PDR.

TABLE 2. Circuit parameters used in the simulation for the interstage network.

Parameter	Value	Parameter	Value
$C_{bal,c}$	4.4 pF	$C_{out,d}$	0.8 pF
$C_{bal,p}$	4.4 pF	L_{int1}	1.35 nH
C_{int1}	0.7 pF	L_{int3}	0.5 nH
C_{int2}	1.5 pF	L_{int4}	0.5 nH

according to the power levels of from the low power (LP) to the high power (HP). Circuit parameters used in the simulation for the interstage network are summarized in Table.

The admittances, Y_c and Y_p, are derived as follows.

$$Y_c = \frac{1}{Z_c} = \frac{1}{R_c + jXc} = G_c + jB_c, \tag{2}$$

$$Y_p = \frac{1}{Z_p} = \frac{1}{R_p + jXp} = G_p + jB_p. \tag{3}$$

Then, the PDR (or P_c/P_p) can be presented using Y_c and Y_p as follows.

$$P_c : P_p = \mathrm{Re}(Y_c) : \mathrm{Re}(Y_p) = G_c : G_p. \tag{4}$$

(4) shows that the ratio of P_c and P_p can be optimized by adjusting the ratio of the input conductances, G_c and G_p, using the component values used in the interstage matching network and offset line. The PDR can be dynamically changed since G_p of the Class-C peaking amplifier is a strong function of the input power level while G_c of the Class-AB carrier amplifier is not changed as much. For the low power level, a higher gain can be achieved by driving more power into the carrier amplifier using a high PDR. As the power level increases, the peaking amplifier becomes gradually turned on with decreasing PDR. The overall AM-AM characteristics can be optimized to be as flat as possible additionally using the gain expansion characteristics of the peaking amplifier.

Fig. 6 shows (a) the simulated admittances of Y_c and Y_p on the Smith chart, and (b) PDR for the direct interstage power dividing network for the frequency band of 2.8-3.8 GHz. Since PDR equals the ratio of G_c to G_p from (4), the ratio of G_c and G_p should be optimized for the low and high power levels using the parameters of the matching network and offset line at the interstage. At the low power level,

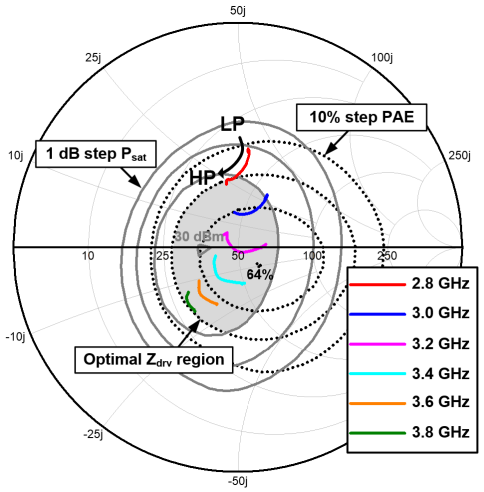

FIGURE 7. Simulated load impedance of the drive amplifier (Z_{drv}) for the 2.8-3.8 GHz band on PAE and output power contours.

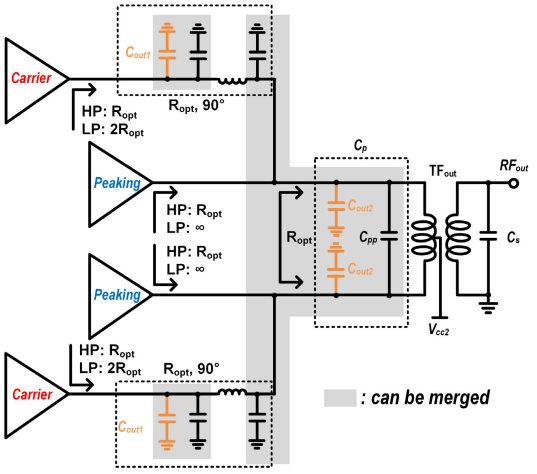

FIGURE 8. Proposed LMN for the HP and LP levels.

Y_c is matched to have a relatively large input G_c of about 0.02–0.03, while Y_p is matched to have a relatively small input G_p of about 0.01–0.015 to drive most of the input power to the carrier amplifier, as shown in Fig. 6(a). In contrast, for the high power level, Y_p has a gradual shift toward the increased input G_p, which results in a decreased PDR. The simulated PDR using the designed interstage direct power dividing circuits for the 2.8-3.8 GHz band in Fig. 6(b) shows 2.5-3.1 dB at the low power level and 0.3-2.0 dB at the peak power level, respectively.

Fig. 7 shows the simulated load impedance of the drive amplifier (Z_{drv}) from the low power to the high power level for the 2.8–3.8 GHz band on PAE and output power contours. The PAE and output power contours are extracted with 1 dB and 10% steps from the load-pull simulation, respectively. The contours are insensitive to the frequency variation since they are extracted at the current source plane of the drive amplifier. The optimal Z_{drv} region is determined to have an

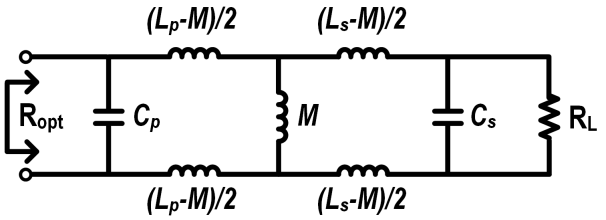

FIGURE 9. T equivalent circuit model of the output transformer including C_s and C_p.

output power of above 29 dBm and a PAE of above 44%. Z_{drv} is expressed as follows:

$$Z_{drv} = \frac{2Z_cZ_p}{Z_c + Z_p}. \tag{5}$$

For the target frequency band, almost all the Z_{drv}'s after including the direct power division circuits are inside the optimal region. This means that the drive amplifier is designed to supply sufficient input power to the main amplifier with high efficiency. For wider operating bandwidth, multi-section matching structure can be used for the interstage network. However, since there are four paths to be matched, the interstage network could be very bulky as the number of sections increases. Using only one-section matching network, the bandwidth of the drive amplifier is secured for high efficiency and power.

III. BROADBAND LOAD MODULATION NETWORK

A. BROADBAND OUTPUT TRANSFORMER

Fig. 8 shows the proposed LMN for the high and low output power levels. The output transformer (TF_{out}) with the tuning capacitors of C_s and C_p transforms the unbalanced load impedance of R_L to the balanced input impedance of R_{opt}. For appropriate load modulation in the wide frequency range, the output transformer network needs to provide the input impedance of R_{opt} in broad bandwidth. At the low output power level, the load impedance of each side of the carrier amplifier is set to $2R_{opt}$ as the peaking amplifier is turned off. A 90° transmission line having a characteristic impedance of R_{opt} transforms $R_{opt}/2$ to $2R_{opt}$ for each side of the carrier amplifier. At the high output power level, the 90° transmission line does not change the impedance. As a result, if the fundamental currents from all amplifiers are equal at the high power level, the load impedances of all the amplifiers become R_{opt}.

For the initial design stage, the T equivalent circuit model shown in Fig. 9 is very useful for extracting the design parameters. R_{opt} is the input impedance of the transformer and R_L is the load resistance. L_p and L_s are the self-inductances for the primary and secondary turns, respectively. M is the mutual inductance which can be expressed as follows:

$$M = k\sqrt{L_pL_s}, \tag{6}$$

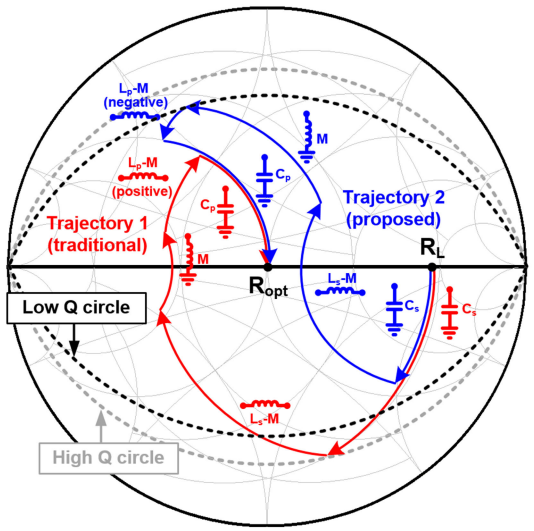

FIGURE 10. Two different impedance trajectories of the equivalent circuits for the output transformer including C_S and C_P on the Z-Y Smith chart.

where k is a coupling coefficient of the primary and secondary turns. If n is defined as the self-inductance ratio between L_s and L_p, then M is expressed as follows:

$$L_s = nL_p, \tag{7}$$

$$M = k\sqrt{n}L_p. \tag{8}$$

Accordingly, n can be rewritten using (8) as:

$$n = \frac{1}{k^2}\frac{M^2}{L_p^2}, \tag{9}$$

where k is between 0 and 1. As a result, the three relationships between n and k^2 according to the relationship between L_p and M can be derived as follows:

$$n < \frac{1}{k^2}, \text{ if } M < L_p, \tag{10}$$

$$n = \frac{1}{k^2}, \text{ if } M = L_p, \tag{11}$$

$$n > \frac{1}{k^2}, \text{ if } M > L_p. \tag{12}$$

For three different cases shown in (10)-(12), since the equivalent circuits have different impedance matching trajectories, they could exhibit different bandwidth.

Fig. 10 shows two different impedance trajectories from the load impedance of R_L to the input impedance of R_{opt} using the T equivalent circuit model. Trajectory 1 based on (10) shows the conventional design for the equivalent circuit [25]. A large C_s is used to move R_L at a resistance smaller than R_{opt}. Then, the imaginary part of the impedance is shifted through constant resistance circles and a constant conductance circle to the inductive region using three inductors of L_s-M, M, and L_p-M. Then, the admittance with a negative susceptance can be matched to R_{opt} using C_p. However, due to the large C_p, the Q of the network is likely to be high, which can limit the

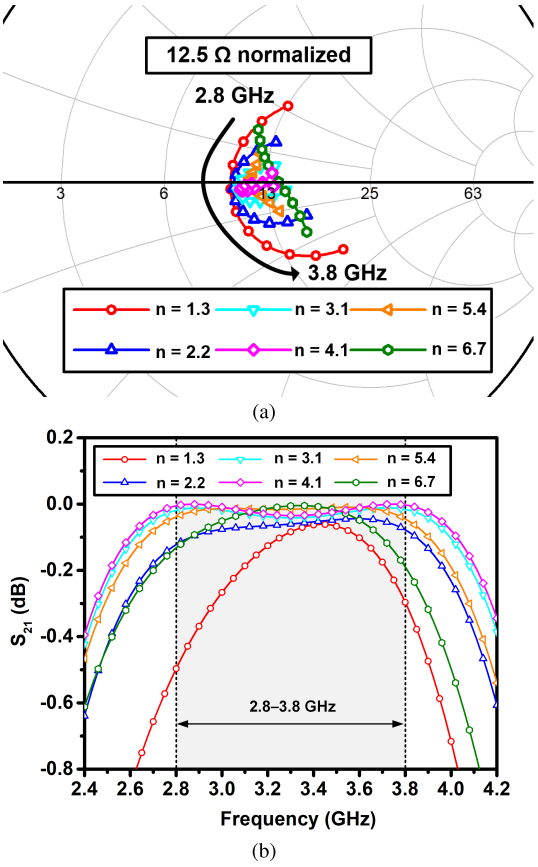

FIGURE 11. Simulated results using the T equivalent circuit model according to the self-inductance ratio of n: (a) input impedance, and (b) S_{21}.

bandwidth. (11) is the boundary between (10) and (12). For this condition, L_p-M becomes zero, while C_p and M are resonated out at the center frequency. Trajectory 2 based on (12) shows the trajectory for the proposed broadband transformer design. A smaller C_s is applied to shift R_L through a constant conductance circle to have a resistance between R_{opt} and R_L. Next, the impedance is moved to have a positive reactance using two series and shunt positive inductors of L_s-M and M. Then, L_p-M, which is a negative value, shifts the impedance counter-clockwise through a constant resistance circle to have a conductance value of $1/R_{opt}$. Finally, C_s is used to match the impedance to R_{opt}. For the Trajectory 2, the Q is decided by the impedance at the inductive region. However, the Q of the Trajectory 2 is lower than that of the Trajectory 1, which results in broader bandwidth. To optimize the parameter values of the equivalent circuit with practical consideration, the initial coupling coefficient should be appropriately estimated. It depends on the dielectric constant, thickness of the dielectric layer, structure, and so on. For a vertically-coupled off-chip transformer on a PCB, a coupling coefficient of about 0.5-0.6 can be obtained, while on-chip transformers generally have coefficients of more than 0.6 thanks to the thinner dielectric layer [23], [24], [25], [26], [27]. In this design, an initial coupling coefficient of 0.57 is selected after a few EM simulations using a 6-layer laminate. Therefore,

TABLE 3. Circuit parameters for various values of n used in the simulation based on the T equivalent circuit model.

n	1.3	2.2	3.1	4.1	5.4	6.7
k	0.57	0.57	0.57	0.57	0.57	0.57
$L_p\ (nH)$	0.738	0.561	0.477	0.421	0.38	0.38
$L_s\ (nH)$	0.941	1.252	1.521	1.745	2.06	2.545
$C_p\ (pF)$	3.63	4.89	5.86	6.76	7.68	7.94
$C_s\ (pF)$	3.21	2.35	1.9	1.62	1.35	1.14

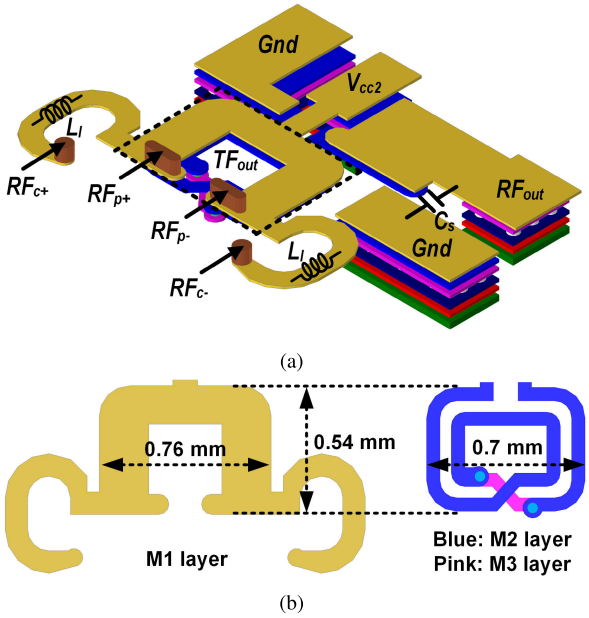

FIGURE 12. Layouts of the LMN using a 6-layer laminate: (a) overall 3D view, (b) top view of the three metal layers of M1, M2, and M3.

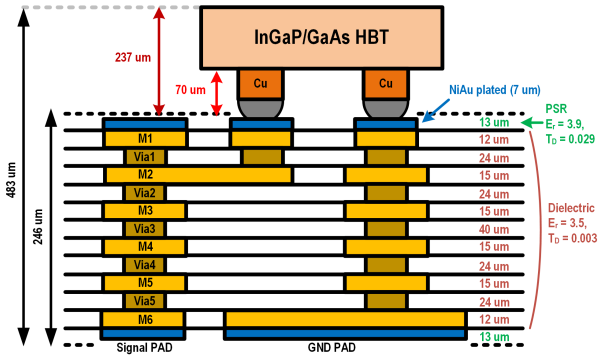

FIGURE 13. Vertical structure of the 6-layer laminate with the InGaP/GaAs HBT IC.

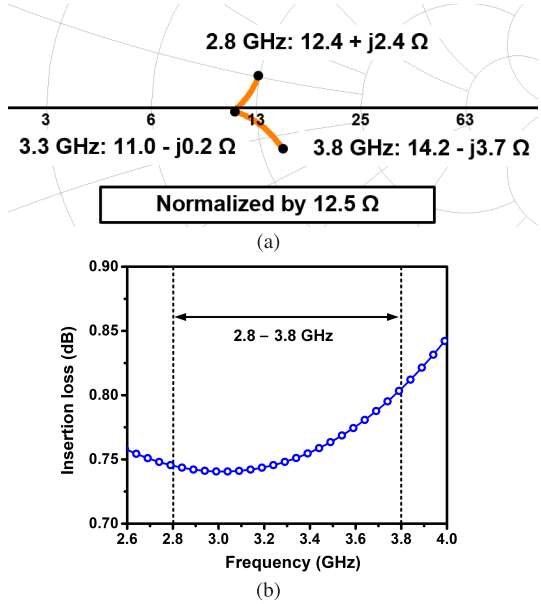

FIGURE 14. Simulated performances of the TF_{out}: (a) input impedance and (b) insertion loss.

according to (10)-(12), if n is smaller than 3.1, the equivalent circuit follows Trajectory 1; otherwise, if n is larger than 3.1, it follows Trajectory 2.

Fig. 11 shows the simulated results using the T equivalent circuit model according to the self-inductance ratio of n: (a) input impedance and (b) S_{21}. Table 3 summarizes the circuit parameters used in the simulation. At first, k was fixed at 0.57. By changing the value of n, L_s and L_p are determined to have as wide a bandwidth as possible, while considering practical implementation rules. Considering the layout including PA I/O PADs, a minimum achievable value of L_p was determined as 0.38 nH. Then, C_s and C_p values can be found for real-to-real impedance transformation. For n of 1.3 and 2.2, the bandwidth can be limited by a large C_s value (Trajectory 1 in Fig. 10). Accordingly, the input impedances are greatly deviated from R_{opt}, especially at the upper and lower ends of the frequency band, which results in a significant drop of S_{21}. For n of 3.1 (boundary of Trajectories 1 and 2), wider bandwidth can be achieved due to a smaller C_s value. When n becomes 4.1 (Trajectory 2), the input impedances are concentrated around R_{opt} for the 2.8-3.8 GHz frequency band, which results in flat response of S_{21}. As n grows to 5.4 or 6.7, C_s decreases, but L_s should be greatly increased. Too large L_s also limits the bandwidth by having too much reactance, which results in increased Q. Hence, as shown in Fig. 11, the bandwidth can be reduced for a too large value of n, as well.

B. DESIGN OF THE LOAD MODULATION NETWORK

Fig. 12(a) shows an overall 3D view of the LMN using a 6-layer laminate. TF_{out} was designed to have a 1:2 turn ratio with n of 4.1 (L_p=0.421 and L_s=1.745 nH). A wide M1 layer and relatively narrow M2 layer are vertically coupled for high self-inductance ratio. Core size of the TF_{out} is $0.76 \times 0.57\ mm^2$. For the quarter-wave transmission line at the LMN, two L_l's are implemented on the laminate only using M1 layer. Fig. 12(b) shows the top view of the M1, 2, and 3 layers. V_{cc2} is supplied through the center-tap of the TF_{out}. Only one off-chip capacitor (C_s) significantly simplifies the LMN. 3D EM for the laminate board with bump

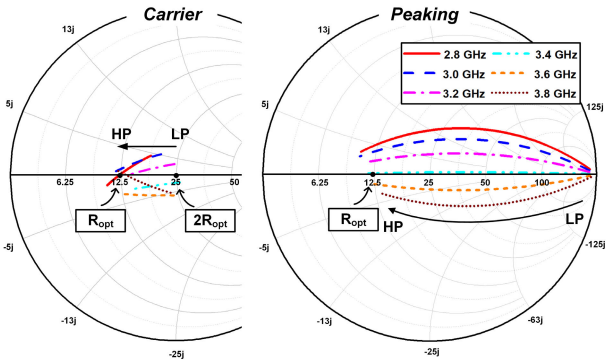

FIGURE 15. Simulated impedance modulation of the LMN from the low- to high-power level.

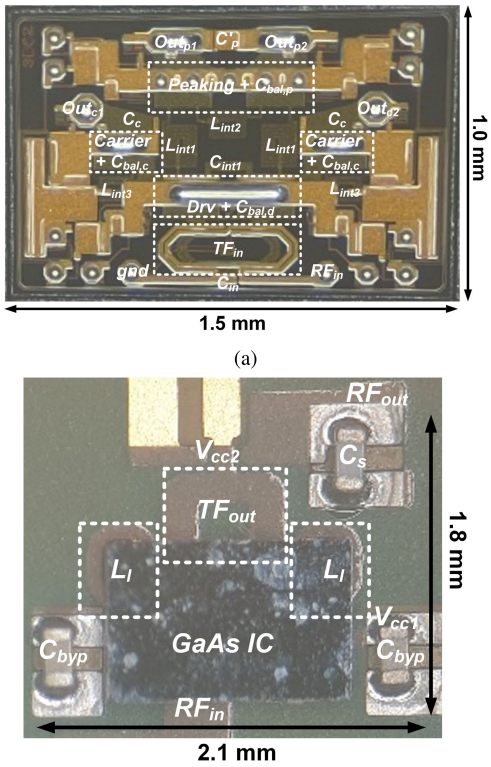

FIGURE 16. Photographs of the implemented Doherty PA: (a) an IC using InGaP/GaAs HBT process, and (b) a module using a 6-layer laminate.

pillars is simulated using ANSYS's HFSS. Fig. 13 shows the vertical structure of the 6-layer laminate with a flip-chip InGaP/GaAs HBT IC. I/O PADs of the PA IC are connected to the M1 layer through the bumps. The height of the PA module is 483 μm.

Fig. 14(a) shows the simulated input impedance of the TF_{out}. The target input impedance is 12.5 Ω for the whole frequency band of from 2.8 to 3.8 GHz. Just a little positive and negative reactance values are added at the lower and high ends of the broad frequency band. In addition, as shown in

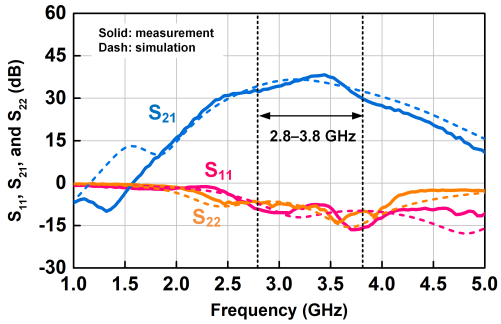

FIGURE 17. Measured S-parameters for the Doherty PA module (solid: measurement, dash: simulation).

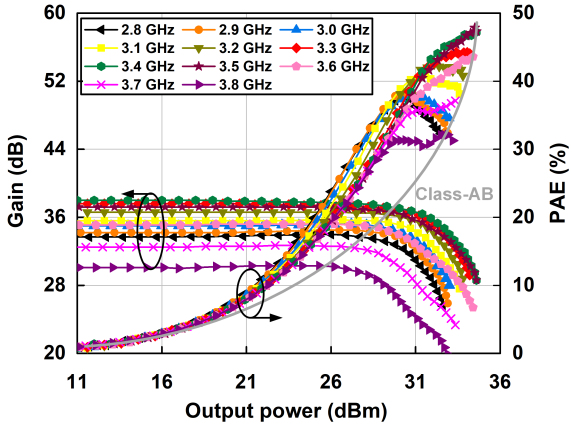

FIGURE 18. Measured gain and PAE for the Doherty PA module using a CW signal at the 2.8-3.8 GHz frequency band.

Fig. 14 (b), low insertion loss of from 0.74 to 0.81 dB was obtained including the chip capacitor, C_L.

Fig. 15 shows the simulated impedance modulation for the LMN according to the input power level. For the carrier and peaking amplifiers, the load impedances are modulated from $2R_{opt}$ to R_{opt} (from 25 to 12.5 Ω) and from a high impedance to R_{opt} (from ∞ to 12.5 Ω), respectively. Despite using a lumped quarter-wave transmission line at the LMN, the desired load modulation in the wide bandwidth of 2.8-3.8 GHz can be obtained using the broadband output transformer.

IV. IMPLEMENTATION AND MEASUREMENT RESULTS

To verify the design concept, the InGaP/GaAs PA IC and the module were implemented. Fig. 16(a) shows a photograph of the implemented Doherty PA IC using WIN semiconductor's 2-μm InGaP/GaAs HBT process. The emitter width for the carrier and peaking amplifiers is 3,200 μm each. The size of the IC is 1.5 × 1.0 mm^2. The PA IC is mounted on the module through flip-chip bonding process. Fig. 16(b) shows a photograph of the Doherty PA module based on 6-layer laminate. The size of the PA module is 2.1 × 1.8 mm^2. 65% of L_l area and some part of TF_{out} are implemented under the PA IC for compact module size. V_{cc2} is fed through the center-tap of the TF_{out}.

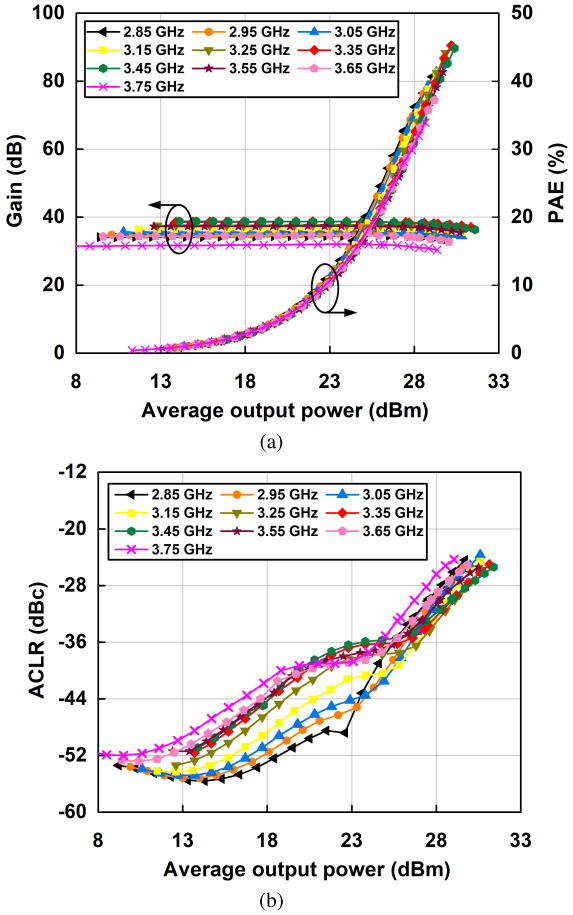

FIGURE 19. Measured performances for the Doherty PA module using the 5G NR signal at the carrier frequencies of 2.85-3.75 GHz: (a) power gain and PAE, and (b) ACLR.

Fig. 17 shows the measured S-parameters for the implemented Doherty PA module. For the target frequency band of 2.8-3.8 GHz, S_{21} of over 30 dB was obtained. The measured results are slightly different from the simulated results due to the inaccuracy of the device models and the imperfect EM simulations. Fig. 18 shows the measured gain and PAE of the Doherty PA module using a CW signal at the 2.8-3.8 GHz band. Saturation output power (P_{sat}) and peak PAE were obtained as 32.6-34.6 dBm and 32.2-47.3%, respectively. At the 6-dB back-off point, high PAE of 23.5-29.4% and high power gain of 30.1-38.0 dB were achieved.

Fig. 19 shows the measured performances of the Doherty PA module: (a) power gain and PAE, and (b) ACLR at the carrier frequencies of 2.85-3.75 GHz using the 5G NR signal based on QPSK DFT-spread OFDM with 270 resource blocks. The signal has a signal bandwidth of 100 MHz and a PAPR of 7.5 dB. Fig. 20 shows the measured average output power (P_{avg}), PAE, and error-vector magnitude (EVM) using the modulated signal for the center frequencies of 2.85-3.75 GHz. An average output power of 26.0-27.8 dBm, a power gain of 31.9-38.3 dB, and a PAE of 22.0-30.6% were achieved under the given ACLR of −33.0 dBc. An EVM of

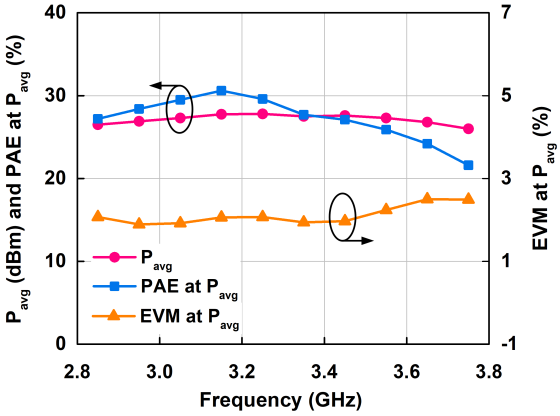

FIGURE 20. Measured P_{avg}, PAE, and EVM for the Doherty PA module using the 5G NR signal at the carrier frequencies of 2.85-3.75 GHz.

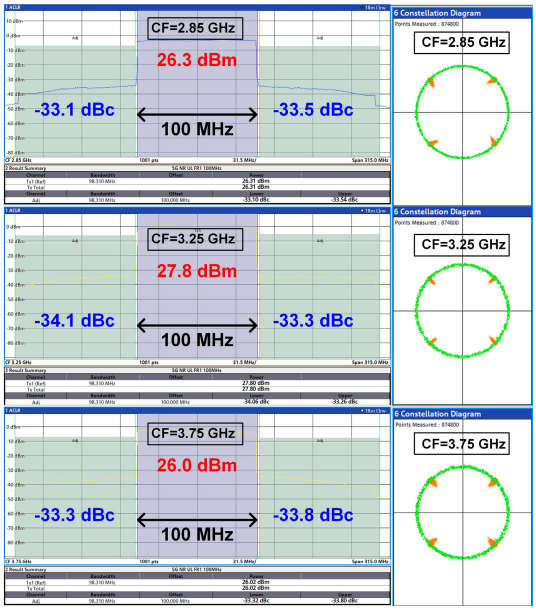

FIGURE 21. Measured channel power and constellation diagram for the Doherty PA module using the 5G NR signal at the carrier frequencies of 2.85, 3.25, and 3.75 GHz.

1.64-1.78% at P_{avg} was obtained. Captured channel power levels, ACLR levels, and constellation diagrams for the carrier frequencies of 2.85, 3.25, and 3.75 GHz are shown in Fig. 21.

The measurement results of the proposed differential DPA are summarized and are compared to the previously published InGaP/GaAs HBT PA ICs in Table 4. For the Doherty PA ICs in [14], [15], and [16], high-efficiency was obtained by applying digital pre-distortion methods to have increased linear output power. High back-off efficiency and the widest fractional bandwidth (FBW) of 30.7% were achieved even without DPD in this work. In addition, the implemented PA module has a smaller size, compared to the sizes of the previous modules in [15] and [16].

TABLE 4. Performance summary and comparison to the previously reported InGaP/GaAs HBT PA ICs.

Reference	**This work**	[8]	[10]	[11]	[13]	[14]	[15]	[16]	[19]
Frequency (GHz)	**2.8-3.8**	1.55-2.65	2.3	5.15-5.85	1.6-2.1	2.4-2.5	3.3-4.2	2.2-2.7	1.85
Structure	**2-stage differential Doherty**	2-stage single cascode	2-stage differential	2-stage differential	3-stage single Doherty	2-stage single Doherty	3-stage single Doherty	2-stage differential Doherty	2-stage single Doherty
FBW (%)	**30.7**	54.3	-	12.8	27.3	4.1	24.2	20.2	-
Modulation scheme	**NR QPSK OFDM**	LTE 16-QAM	LTE	LTE QPSK	LTE	WLAN 64-QAM	NR QPSK OFDM	NR QPSK OFDM	LTE 16-QAM
Signal BW (MHz)	**100**	10	10	20/40	10	40	100	100	100
PAPR (dB)	**7.5**	7.5	7.3	6.7/8.3	7.5	-	-	-	7.5
Supply Voltage (V)	**4.5**	10.0	4.7	3.3	4.5	5.0	3.8	5.5	3.5
P_{avg} (dBm)	**26.0-27.8**	26.7-27.7	24.8	24.1-24.4/ 22.2-22.8	27.5	26.0	27.8	30.5	26.0
PAE$_{@Psat}$ (%)	**32.2-47.3**	40.2-54.3	27.6	40.4-44.5	-	-	-	-	50.0*
PAE$_{@Pavg}$ (%)	**22.0-30.6**	30.9-38.4	14.3	19.3/12.3	>30	21.0	>35.0	>35.5	42.0
Gain (dB)	**31.9-38.3**	23.7-31.6	26.0	>25.9	27.5-32.5*	29.0	33.0-36.0*	24.0*	27.8
ACLR (dBc)	**<-33.0**	-30.0	-40.4	-33.0	-31.0	-50.7	<-35.0	-35.0	-37.0
EVM (%)	**1.64-1.78**	-	-	-	3.8	0.79	-	-	3.8
Using DPD	**No**	No	No	No	No	Yes	Yes	Yes	No
PA die size (mm^2)	**1.5×1.0**	1.0×1.0	3.0×1.5	1.55×0.9	1.4×1.4	-	1.1×1.1	1.0×1.15	1.2×1.2
Module area (mm^2), type	**2.1×1.8, laminate**	34.0×21.0, COB**	- COB	- COB	- COB	- COB	3.5×2.5*, laminate	2.6×2.2, laminate	- COB

*Graphically estimated, **chip-on-board

V. CONCLUSION

In this paper, a broadband 2-stage Doherty PA using a direct interstage power division method using a 2-μm InGaP/GaAs HBT process for 5G new radio handset application is presented. The transformer-less interstage network for dynamic PDR is proposed for the frequency band of 2.8-3.8 GHz (FBW of 30.7%). To design compact interstage and load networks, shunt passive components that share common nodes are merged. For linear operation, the active bias circuits of the peaking amplifier were optimized to provide a flat AM-AM response. In addition, the broadband load modulation network using one transformer and two quarter-wave transmission lines was designed. Based on a T equivalent circuit model, the self-inductance ratio between the primary and secondary turns of the transformer was optimized to maximize the operating bandwidth. The proposed Doherty PA module was implemented using a 6-layer laminate. The PA IC was assembled using a flip-chip bonding process. For the 5G NR uplink signal having a signal bandwidth of 100 MHz and a PAPR of 7.5 dB, a high gain of 31.9-38.4 dB, a PAE of 22.0-30.6%, and an average output power of 26.0-27.8 dBm were obtained under an ACLR of −33.0 dBc without DPD.

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