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RESEARCH ARTICLE

Magnetic Design of a 3-Phase SiC-Based PV Inverter With DC-Link Referenced Output Filter

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ABSTRACT The use of Silicon carbide (SiC) devices represents an improvement in terms of size, weight and efficiency of power converters. However, SiC-based solutions present high dv/dt and di/dt on the switching events, increasing the common-mode noise injected into the grid. To reduce the common-mode noise, three-phase inverters with a DC-link referenced output filter are widely considered in photovoltaic (PV) inverters connected to the grid. However, if the filter is DC-link referenced the inductor ripple is larger, and this must be considered for the AC inductor filter design. This work shows, on a PV inverter, the impact of that DC-link referenced filter on the current ripple of the inductor, and the improvement achieved with the use of SiC devices, increasing the switching frequency. A comparison in terms of weight, size, losses and materials costs is presented for different core materials and configurations.

INDEX TERMS DC-AC, silicon carbide, grid-connected, PV inverter, AC filter inductors.

I. INTRODUCTION

Grid-connected photovoltaic (PV) inverters represent the connection of the DC bus created by the PV panels and the AC grid, where the power is injected. Together with the cost, their efficiency, volume and weight represent the figures of merit of these converters. The most used for medium and high power systems is the three phase inverter. In this power range, after several years with 1000 V DC as the standard voltage level of the PV string, the market is moving to a new high voltage trend up to 1500 V DC. With 1000 V DC PV panels, 400 V AC line-to-line voltages are used on the grid side. However, with the increase of DC voltage up to 1500 V, 690 V AC or even 800 V AC have appeared on the market. With this increment in the voltage it is possible to manage higher power installation points without increasing the current, and therefore the employed copper [1], [2], [3].

Grid-tie inverters must fulfill power quality regulations such us IEEE 519 [4], with maximum individual harmonics up to 3% and total harmonic distortion of 5%. This has an impact on the inverter design in terms of switching frequency, AC filter design, and also in terms of converter topology. Two main converter topologies are found in the literature for these two DC voltage levels: two-level and multilevel (above all, 3-level) topologies.

For medium power inverters around 100 kW designed with Si-based IGBTs, 2-level topologies lead to switching frequencies around 5-10 kHz being limited by the semiconductor losses [5], [6], [7]. With 3-level topologies it is possible to use IGBTs with lower voltage rate, resulting in lower losses and then, higher switching frequencies. Despite of being well-known in the literature, 3-level (and multilevel) topologies present some challenges such us complex control, higher number of devices, electro-mechanical design, potentially (or even) destructive switching states, among others [6]. Therefore, two-level converters are preferred by many power electronics developers.

One the one hand, 2-level inverters for 1000 V DC PV systems are based on 1200 V switching devices. 1000 V DC represents the maximum DC voltage of the PV string,

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at zero current according to the I-V curve of the PV string. Therefore, the nominal power (i.e. current) condition appears between 600-800 V DC, resulting in sufficient voltage margin up to 1200 V for the device.

On the other hand, for 1500 V DC PV systems, the use of 2-level topologies is not so common. Besides obtaining lower losses and higher switching frequencies, the use of 3-level topologies ensures high reliability on the semiconductors due to cosmic ray effects [8], [9], [10]. For this reason, power electronics suppliers, like SEMIKRON uses CAL type diodes on the 2-level designs [11].

Recently, important semiconductor manufacturers have introduced new modules (with new packages) based on Silicon-carbide (SiC). Nowadays, for typical device voltages up to 1200 V or 1700 V, SiC is a technology whose benefits are having important impact in the PV market [12]. Despite of the higher cost of the SiC devices in comparison with its Si counterparts, the benefits in terms of efficiency, size, weight and reliability of SiC-based solutions, are gaining attention of the PV inverters market. [5]. Recent works such as [13] and [14] show how despite of having higher cost on the SiC devices, the reduction on the passives can compensate that, and in addition how with SiC an inverter can be 3-10 times lighter compared with its Si-based version, reducing the installation costs. Manufacturers, like Kaco [15] also highlight this aspect with the Blueplanet 125 TL3, a 1500 V DC inverter that uses SiC devices.

In addition, new SiC devices of 1200 V and 1700 V show better behavior under cosmic ray radiation [16] in comparison with Si-based ones. This aspect makes possible the use of newest 1700 V SiC samples on the 1500 V DC PV system with a 2-level topology [17] rather than 3-level topologies; and it encourages the use 1200 V SiC samples on 1000 V DC PV systems. Recently, the new 2000 V class SiC devices have been introduced [18], being also an improved and well suited choice for 1500 V DC PV system.

The characteristics of these SiC technology allows higher switching frequencies, which results in a higher overall efficiency and smaller power modules. The switching frequency has a direct impact on the sizing of AC filter inductors, that can represent the heaviest and biggest element in the power range of 80-120 kW, The increment in the switching frequency results in a reduction of volume, weight and cost. However, SiC devices have higher dv/dt and di/dt, resulting in a increment on the converter EMC/EMI noise.

The use of a DC-link referenced AC output filter, also known as "Modified LCL filter" (MLCL) in [19], represents a prominent choice for common mode noise attenuation. Since it is confined in the converter [20] the noise is limited on the grid, and on the PV panels side. With this configuration, no new modulation strategies are needed, and differential-mode and common-mode filtering is obtained with the same passive elements. In addition, over-voltages generated at the grid-side connection terminals due to cables length are also mitigated [19], [20] reducing the stress on the medium voltage distribution transformer of the PV installation. In addition, this configuration is more interesting for SiC-based inverters, where common mode current due to higher dv/dt is higher than with Si-based inverters, as it has been introduced before. Although galvanic isolation helps on the common mode noise attenuation, depending on National Standards (an their evolution), or specific requirements, galvanic isolation is needed or not, as is presented on [21], because it affects on the volume/weight and efficiency commented. Due to that, if it is not required, galvanic isolation is avoided.

But this MLCL filter configuration increases the inductor ripple under the same PV inverter conditions, affecting the weight and cost of the filter inductors. This work approaches this aspect using a 100 kW 2-level 2-phase inverter as case study.

First, in Section II it is shown how the current ripple on the AC filter inductor (L) is increased due to the DC-link referenced connection, and also the impact of increasing the switching frequency with the use of SiC devices. In Section III, the influence of L on the active and reactive power injection limits is introduced to see how with the use of SiC devices, theses limits can be improved. In Section IV the different alternatives more suitable for the magnetic design of L are presented, considering different switching frequencies, current ripple, DC and AC voltage levels and magnetic core materials. Finally, experimental results and the conclusions are presented in Section V and Section VI, respectively.

II. CURRENT INDUCTOR RIPPLE ON 2-LEVEL THREE PHASE INVERTERS

Figure 1(a) corresponds to a typical configuration where the DC voltage generated by the PV system (i.e. a string of panels) is connected to a 2-level pulse-width modulated (PWM) inverter, that works at a defined switching frequency (f_{sw}), generating a pulsated voltage on a, b, and c terminals. A differential mode LCL filter is used to attenuate the high frequency harmonics of the current injected into the grid, made up of the AC inductors L and capacitors C_f.

The total parasitic capacitance of the PV system is represented by C_{PV} also called leakage capacitance, which is connected between the DC bus negative terminal and ground. The grid is modeled, at the Point of Common Coupling (PCC) by a phase inductance (L_{grid}) and a Z_{grid} impedance to ground.

This yields to a simplified common-mode model like the presented on Fig. 1(b), where v_{cm} is a voltage source that represents the common-mode voltage generated in the converter. The common-mode loop is closed through ground, and then a common-mode current i_{cm} is flowing to the PV panel. The value of this i_{cm} is function of L_{grid}, and Z_{grid} which depends on the nature of the system.

For example, if a PV plant has a common (and unique) power inverter and the distribution medium-voltage transformer is just placed on the PCC (Fig. 1(a)), ideally it can be assumed that $Z_{grid} = \infty$, resulting in $i_{cm} \approx 0$. However, when other loads or systems supplied are connected

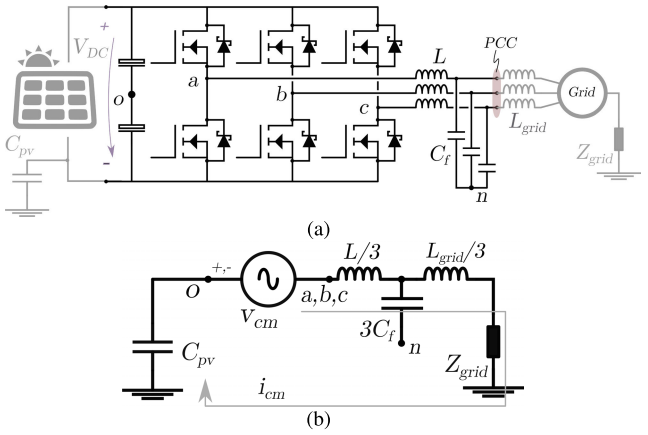

FIGURE 1. Representation of a three-phase PV inverter connected to the grid without a DC-link referenced filter.(a) 2-level 3-phase PV inverter. (b) Common-mode model.

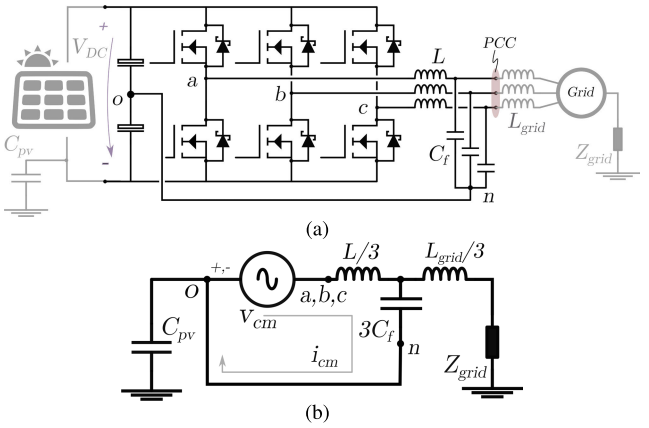

FIGURE 2. Representation of a three-phase PV inverter connected to the grid with a DC-link referenced filter(a) 2-level 3-phase PV inverter with DC-link referenced AC filter. (b) Common-mode model.

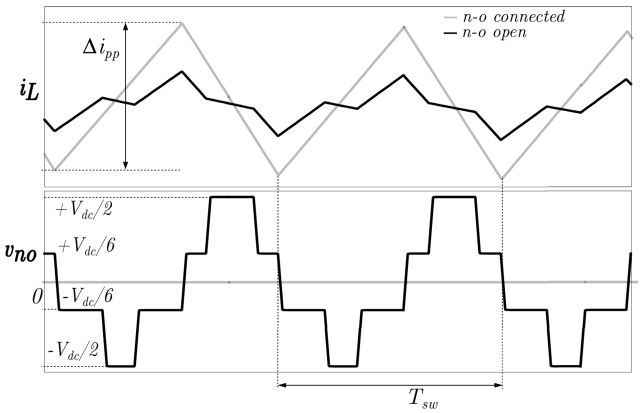

FIGURE 3. Differences on the current ripple in 2-level inverter between the traditional configuration (black waveforms) and with DC-link referenced output filter (gray waveforms). Top: inductor current. Bottom: voltage between neutral point (*n*) and DC bus neutral point (*o*).

at the PCC, e.g., another inverters of the same PV plant, or just the transformer is not needed, $Z_{grid} \ll \infty$. When it happens a non desirable common-mode current $i_{cm} > 0$ flows, which can damage the PV panel, the rest of the equipment connected to the PCC, and create electrical shock hazard [22], [23].

To avoid this problem, several new typologies with modified modulation strategies and configurations have been presented in the literature (like 4-legs 3-phase inverter, H8 topology, etc) [19], [24], [25], [26], [27]. Among other solutions, topologies with DC-link referenced AC filter, as the shown in Fig. 2(a) for the 2-level version, represent a reliable and simple alternative for common-mode current reduction [19], [28]. In this configuration, the dedicated common-mode filter needed on the most used solution presented on Fig. 1, can be relieved or even not needed [28]. In Fig. 2(a), the neutral point of the filter capacitors C_f (n) is connected to de DC bus neutral point (o). With this connection, the common-mode current loop is modified achieving a lower impedance loop through C_f accordinf to Fig. 2(b). In this manner, new elements are not introduced in the configuration of Fig. 2, in comparison with Fig. 1.

However, this connection between n and o affects the inductor current ripple, and therefore, the design of L and C_f (filter elements). This aspect is explained on Fig. 3, showing the switching periods in detail. Regardless $n-o$ connected or not connected, phase voltages v_{ao}, v_{bo} and v_{co} are the same. However, if $n - o$ is not connected, a v_{no} voltage appears between these terminals. This v_{no} voltage is generated by the switching of the three phases as it is presented on the bottom subplot of Fig. 3. Therefore, the inductor current waveform i_L of one phase is affected by this u_{no} voltage (i.e. the two other phases). Otherwise, if n and o are connected, $v_{no} = 0$ and the phases are not affected between them. Thus each phase is independent, resulting in the completely triangular inductor current.

The duty-cycle of the three phases a, b and c with a sinusoidal pulse-width modulation (SPWM) can be written as:

$$
\begin{aligned}
d_a &= \frac{1}{2} + \frac{1}{2} M \sin(2\pi f_{grid} t) \\
d_b &= \frac{1}{2} + \frac{1}{2} M \sin\left(2\pi f_{grid} t + \frac{2\pi}{3}\right) \\
d_c &= \frac{1}{2} + \frac{1}{2} M \sin\left(2\pi f_{grid} t - \frac{2\pi}{3}\right)
\end{aligned} \tag{1}
$$

where, f_{grid} is the grid frequency and M is the modulation index given by:

$$
M = \frac{2\sqrt{2} V_{grid}}{V_{DC}\sqrt{3}} \tag{2}
$$

being V_{grid} the line-to-line RMS voltage of the grid, and V_{DC} the DC bus voltage of the PV string. In this case, the peak-to-peak current ripple over the line-cycle will be given by:

$$
\Delta i_{pp,i} = V_{DC} \times \frac{d_i(1-d_i)}{f_{sw} L} \tag{3}
$$

where $i \in \{a, b, c\}$ and the duty-cycle $d_i \in [0, 1]$. With (1), expression (3) can by symplified as:

$$\Delta i_{pp} = \frac{V_{DC}(1 - M^2 \sin^2 \theta)}{4 f_{sw} L} \tag{4}$$

where $\theta \in [0, 2\pi]$, is the phase angle over the line cycle, whose maximum values occurs at $\theta = 0°$, being $\Delta i_{pp,max} = V_{DC}/4 f_{sw} L$.

The RMS value of this current ripple in each switching period ($T_{sw} = 1/f_{sw}$) is given by (5). Calculating the RMS value of the current ripple over the half-line cycle ($0 \leqslant \theta \leqslant \pi$) according to (6) the expression as function of V_{DC} and M is obtained.

$$\langle \Delta i_{pp,rms} \rangle_{T_{sw}} = \frac{\Delta i_{pp}}{2\sqrt{3}} = \frac{V_{DC}(1 - M^2 \sin^2 \theta)}{8\sqrt{3} f_{sw} L} \tag{5}$$

$$\begin{aligned} \Delta I_{pp,rms} &= \sqrt{\frac{1}{\pi} \int_{\theta=0}^{\theta=\pi} \langle \Delta i_{pp,rms} \rangle_{T_{sw}}^2 \, d\theta} \\ &= \frac{V_{DC}}{8\sqrt{3} f_{sw} L} \sqrt{1 - M^2 + \frac{3}{8} M^4} \end{aligned} \tag{6}$$

Considering that, the grid voltage V_{grid} is constant in the steady state, and V_{DC} is variable with the PV string power, $\Delta I_{pp,rms}$ is solved as function of V_{grid} and M using (2) in (6), resulting:

$$\Delta I_{pp,rms} = \frac{V_{grid}\sqrt{2}}{12 f_{sw} L} \sqrt{\frac{3}{8} M^2 - 1 + \frac{1}{M^2}} \tag{7}$$

This RMS (root mean square) value represents a steady state current representative of the inductor losses, considering the switching frequency harmonic components. However, the ratio $\Delta i_{pp,max}/\hat{I}_{grid}$ is commonly used to specify the inductance, where $\hat{I}_{grid}$ is the peak fo the grid current over the line-cycle given by $\hat{I}_{grid} = \sqrt{2} I_{grid}$. However, $\Delta i_{pp,max}$ only appears on the voltage zero-crossings ($\theta = 0°$) and does not depend on the modulation index M during operation, so $\Delta I_{pp,rms}$ represents more precisely the harmonics influence on the inductor losses, as is used in [20].

Using (4) and (6), it is possible to correlate $\Delta i_{pp,max}/\hat{I}_{grid}$ with the RMS factor $\Delta I_{pp,rms}/I_{grid}$ resulting:

$$\frac{\Delta I_{pp,rms}}{I_{grid}}[\%] = \frac{\Delta i_{pp,max}}{\hat{I}_{grid}}[\%] \times \sqrt{\frac{1 - M^2}{6} + \frac{M^4}{16}} \tag{8}$$

Then, these variables, $\Delta i_{pp,max}$ and above all $\Delta I_{pp,rms}$, have a key role on the inductor design. Reference values around 20-40% [29] or even higher like 50% in [30] can be used for $\Delta i_{pp,max}$, but the design that results on the best inductor in terms of weight, volume, cost and efficiency depends on the application, core material, etc [31]. This aspect is evaluated on Section IV, considering the peculiarities when $n - o$ terminals are connected.

As it has been introduced previously, in the case of no connection between n and o terminals, the peak-to-peak switching ripple in one phase is influenced by the two other phases. Works like [32], [33] study the analytical expression

TABLE 1. Characteristics of the Si-based 2-level PV inverter considered as reference.

Variable	Value
Operating DC input voltage V_{dc}, range	600 to 1000 V
Rated DC input voltage, V_{dc}	800 V
Rated AC grid voltage, V_{grid}	400 V_{ac}
AC filter inductor, L	360 μH
Rated AC grid frequency, f_{grid}	50 Hz
Switching frequency, f_{sw}	5 kHz
Max. apparent power, S_{max}	100 kVA

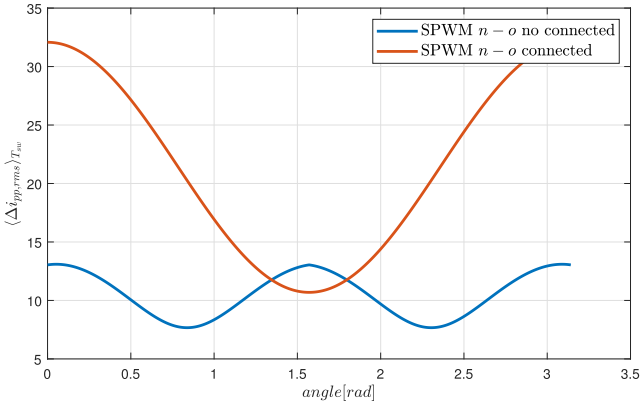

FIGURE 4. Inductor RMS current ripple $\langle \Delta i_{pp,rms} \rangle_{T_{sw}}$, in each switching period.

of the peak-to-peak current ripple of the inductor under this situation, and the expression to calculate the RMS current ripple under this situation is presented in [34].

A Si-based 2-level inverter has been considered as benchmarking design for comparison purpose (see Table 1). The inductance value has been decided as 360 μH considering the commercial products presented on [35] and [36] and assuming a 5 kHz switching frequency.

Figure 4 shows the RMS inductor current ripple ($\langle \Delta i_{pp,rms} \rangle_{T_{sw}}$) over the line cycle. Two different conditions are considered: with $n - o$ connection and without $n - o$ connection, both cases with sinusoidal pulsed-width modulation (SPWM), according to expression (1).

With the considered values, the RMS over the line cycle $\Delta I_{pp,rms} = 10.68\ A$ and $22.68\ A$ with and without $n - o$ connection, respectively. Thus, the current ripple is around the double due to the $n - o$ connection under the same operation conditions.

With the upgrade of the PV inverter using SiC devices, the impact of the neutral connection to the DC-bus midpoint can be partly compensated increasing the switching frequency. This aspect is illustrated on Table 2. Increasing the switching frequency up to 20 kHz with the help of SiC devices, and maintaining the $n - o$ connection, it is possible to reduce the inductance value to $L = 180\ \mu H$, and despite of that, the switching ripple obtained is 11.34 A, almost the same as the one obtained on the Si-based design used as

TABLE 2. Impact of the switching frequency value (f_{sw}) and the $n-o$ connection on the inductance (L) and RMS current ripple $\Delta I_{pp,rms}$.

V_{grid} [V]	V_{DC} [V]	L [μH]	$\Delta I_{pp,RMS}$ [A]	$n-o$ connected	f_{sw} [kHz]	Devices	$\frac{\Delta I_{pp,rms}}{I_{grid}}$ [%]	$\frac{\Delta i_{pp,max}}{\hat{I}_{grid}}$ [%]
400	800	360	10,68	No	5,00	Si	7.4	25.7
400	800	360	22,68	Yes	5,00	Si	15.8	54.6
400	800	360	11,34	Yes	10,00	Si/SiC	7.9	27.3
400	800	360	5,67	Yes	20,00	SiC	3.9	13.6
400	800	180	11,34	Yes	20,00	SiC	7.9	27.3
400	800	120	11,34	Yes	30,00	SiC	7.9	27.3

TABLE 3. Filter inductance values needed for different grid and DC bus voltages, considering $\Delta I_{pp,rms}$ as a 15% of the nominal grid voltage (I_{grid}). 5 kHz and 20 kHz switching frequencies are considered for Si-based and SiC based inverters, respectively, for a 100 kVA nominal power.

V_{grid} [V]	V_{DC} [V]	M	I_{grid} [A]	$\Delta i_{pp,Max}$ [A]	$\Delta I_{pp,rms}$ [A]	$\frac{\Delta i_{pp,max}}{\hat{I}_{grid}}$ [%]	L_{20kHz} [μH]	L_{10kHz} [μH]	L_{5kHz} [μH]
400	1000	0,65	144,34	93,63	21,65	46%	133	266	532
400	800	0,82	144,34	106,07	21,65	52%	94	188	376
400	650	1,00	144,34	122,87	21,65	60%	66	132	264
690	1500	0,75	83,67	58,36	12,55	49%	321	642	1284
690	1400	0,80	83,67	60,91	12,55	51%	287	574	1148
690	1200	0,94	83,67	67,92	12,55	57%	220	440	880
690	1150	0,98	83,67	84,02	12,55	59%	205	410	820
800	1500	0,87	72,71	55,46	10.83	54%	338	676	1352
800	1400	0,93	72,71	58,31	10.83	57%	300	600	1200
800	1300	1,00	72,71	61,44	10.83	60%	264	528	1056

reference (and without $n-o$ connection). As result, the same switching ripple is obtained despite of the $n-o$ connection, and with the improvements in terms of common-mode emission commented previously. The switching frequency of 10 kHz is considered as the limit where Si-based design can operate. In addition, the current ripple % mentioned before, $\Delta I_{pp,rms}/I_{grid}[\%]$ and $\Delta i_{pp,max}/\hat{I}_{grid}[\%]$, are also presented in Table 2.

Besides, Table 3 presents the filter inductance vales (L) needed for different grid (400, 690 and 800 V AC) and DC bus voltages of the PV plant (1000 V and 1500 V), considering $\Delta I_{pp,rms}$ as a 15% of the nominal grid current, I_{grid}, given by (7), considering a nominal power of 100 kVA. Also the ratio $\Delta i_{pp,max}/\hat{I}_{grid}$ is presented, that for $\Delta I_{pp,rms} = 15\%$ results around 50%, depending on the modulation index M, according to (8).

The values obtained for 400 V AC grid and 800 V DC bus voltage correspond to the reference case (c.f. Table 2), and requires an inductance value of 376 μH at 5 kHz, close to the L=360 μH considered previously.

The switching frequency of the PV inverters depends also on the power modules characteristics, the cooling system, point of optimum efficiency, etc. In this case, to illustrate the impact of different design variables, 5, 10 and 20 kHz have been considered. It is shown how in the worst case (1500 V DC bus and 800 V AC grid), 1.352 mH are needed with 5 kHz, and 338 μH with 20 kHz. Moreover, with lower DC bus voltages, lower values of L are needed, therefore the tendency of increasing the DC bus voltage (to 1500 V DC) results on higher inductance values. Nevertheless, the requirement of higher inductance can be mitigated increasing the switching frequency without a performance impact, thanks to SiC devices.

III. ACTIVE AND REACTIVE POWER INJECTION LIMITS

New PV inverters are requested to include, among other trends, smaller AC filter (i.e. inductors and capacitors) and improved grid support as reactive power [6].

The introduction of SiC devices on PV inverters has a direct impact on these mentioned requests. The increment of the switching frequency results in a direct decrement on the inductance value needed, and therefore in the size of the filter. And in addition, a lower inductance value has a positive influence on the reactive power injection limits of the inverter.

As it is presented on [37], [38], and [39], a PV inverter connected to the grid have a $P-Q$ (active and reactive) capability limits related to:

- grid voltage line-to-line, V_{grid}.
- DC bus voltage, V_{DC}, and the
- total impedance between converter and grid considering the filter and grid inductances, L and L_{grid}, respectively, $X = 2\pi f_{grid}(L + L_{grid})$,

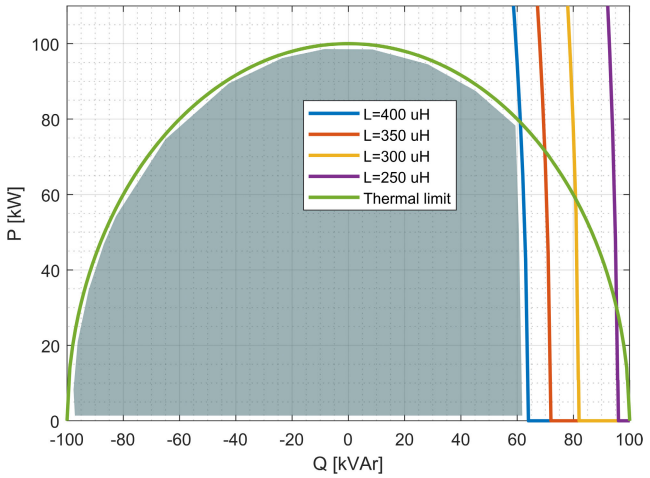

FIGURE 5. P-Q capability limit.

given by the next expression [39]:

$$P^2 + \left(Q + \frac{V_{grid}^2}{X}\right)^2 = \left(\frac{V_{grid} V_{conv}}{X}\right)^2 \tag{9}$$

where V_{conv} is line-to-line voltage on the converter terminals a, b and c. The highest value that can reach V_{conv} is $M \times \frac{V_{DC}\sqrt{3}}{2/\sqrt{2}}$ considering a maximum modulation index of $M = 1.15$ under Space-Vector PWM (SVPWM).

Furthermore, the thermal limit of the inverter is given by the maximum current that can be managed by the switching devices, that results on a maximum apparent power, S_{max}. Therefore, it must be fulfilled:

$$S_{max}^2 \geq P^2 + Q^2 \tag{10}$$

Expressions (9) and (10), with the values presented on Table 1 have been used to illustrate the impact of the inductor reduction on the P-Q capability limits. In this case, a lower DC-link voltage is considered ($V_{DC} = 600\ V$). Indeed, working under low solar radiance conditions or high ambient temperature [39]. This operating point is evaluated because represents a situation where P-Q limits are more restrictive. A range of $L = 250 - 400\ \mu H$ has been used, to see the influence of its value on the P-Q limits.

The results are plotted on Fig. 5, where the limits defined by S_{max} represents a circle centered at 0, according to (10). The area inside this circle represents the thermal operation of the inverter, but positive reactive power is limited by (9). In this case, considering the blue line defined by $L = 400\mu H$, the Q limit is around 60-64 kVAr, depending on the active power P demanded (between 0 and 80 kW). Reducing the inductance value to $L = 250\ \mu H$, Q limit increases up to 95 kVAr as it is shown on Fig. 5. With this inductance value reduction, the PV inverter can operate close the thermal limit (S_{max}) without affecting controllability at 600 V DC on the PV panel.

This aspect is an important advantage of the use of SiC on PV inverters connected to the grid, because increasing the switching frequency, the inductance value is decreased and the PQ capabilities are also improved, resulting in an improvement in the grid support, commented previously.

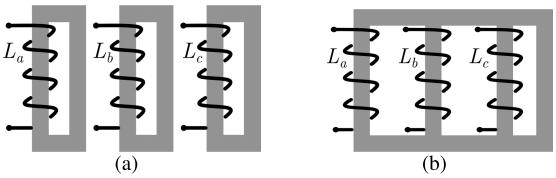

FIGURE 6. (a) 3 independent phase inductors. (b) 3 phase inductors in 3-limbs core.

IV. MAGNETIC DESIGN OF PHASE INDUCTORS

The connection of the terminals $n-o$ has an important impact in the consideration of the magnetic design of the AC inductor filter L. Three independent phase inductors (Fig. 6(a)) and 3 phase inductors in 3-limbs core (Fig. 6(b)) are well-known alternatives to be considered in the AC filter inductor design.

In both configurations, the behavior of the inductor is defined by (11), where $L_a = L_b = L_c = L_i$ is the self-inductance of each phase, and M is the mutual inductance between phase a, b and c. In a 3-independent inductors configuration, $L_i = L$ and $M = 0$. In a coupled design, the goal is to obtain $L_i \approx 2L/3$ and $M \approx L/3$ as it was presented on [40].

$$\begin{bmatrix} v_{La} \\ v_{Lb} \\ v_{Lc} \end{bmatrix} = \begin{bmatrix} L_a & -M & -M \\ -M & L_b & -M \\ -M & -M & L_c \end{bmatrix} \times \frac{d}{dt} \begin{bmatrix} i_a \\ i_b \\ i_c \end{bmatrix} \tag{11}$$

The common mode inductance, L_{cm} is due to $i_a = i_b = i_c = i_{cm}$, resulting in a common mode voltage $v_{cm} = v_{La} = v_{Lb} = v_{Lc}$. Considering (11), the common mode inductor is given by (12):

$$L_{cm} = \frac{v_{cm}}{di_{cm}/dt} = \frac{L_i - 2M}{3} \tag{12}$$

Under an ideal design with $M \approx L/3$ to have the maximum coupling between phases [40], common mode inductance is reduced ($L_{cm} \approx 0$). This common mode inductance must be considered in the common mode model presented on Fig. 2(b) when $n - o$ are not connected and in Fig. 1(b) when $n - o$ are connected, rather than $L/3$.

In the case of $n - o$ connection, it results in a high common mode ripple on the inductance, much higher than with 3-independent inductors, where $L_{cm} = L/3$. Due to that, three-phase three-column inductors are not recommended if output AC filter is DC-link referenced, as was introduced on the previous work [41], where 3-phase inductors in a 4-limb core are considered, because $L_{cm} = L/3$ too, and the core the materials needed (i.e. volume) can be lower. However, as it is depicted in that previous work, it represents a higher cost of manufacturing because no standard amorphous C-type cores can be used, and dedicated block cores are needed.

For the inductor core materials, with 100 kVA as nominal power, GO (grain-oriented) silicon steel H100-23 and

TABLE 4. Inductor design results for 1500 V DC, 690 V AC PV inverter.

$\Delta I_{pp,rms}/I_{grid}[\%]$	8%				8%				15%				15%			
$f_{sw}[kHz]$	10	15	20	30	10	15	20	30	10	15	20	30	10	15	20	30
Material	GO				Amorphous				GO				Amorphous			
Weight [kg]	26.3	21.1	22.1	38.8	33.9	23.9	16.8	15.0	26.5	21.6	38.8	94.9	23.9	16.6	13.3	9.1
Losses [W]	584	588	696	736	607	464	426	297	582	645	730	1,294	464	404	294	255
Volume [dm^3]	6.5	7.4	8.1	9.7	8.1	6.0	4.6	3.4	6.6	7.7	9.7	20.9	6.0	4.5	3.4	2.6
Cost [€]	113	94	100	165	466	327	223	198	114	97	165	391	200	160	120	98

Metglas amorphous alloy (2605SA) are considered. GO silicon steel is a common material used for Silicon based inverters at that power rate, for low switching frequencies around 5-10 kHz. Amorphous materials are well suited for higher switching frequencies where acoustic noise is reduced, having also high core saturation, but its cost is higher than silicon steel. However, increasing the switching frequency results on lighter and smaller inductors, so the cost can be partially compensated. With the aim of evaluating this aspect, several inductor designs have been considered for 3-independent inductors configuration with different switching frequencies (from 10 to 30 kHz), and different RMS peak to peak switching ripples ($\Delta I_{pp,rms}/I_{grid} = 8$ and 15%, that corresponds with values of $\Delta i_{pp,max}/\hat{I}_{grid}$ around 25 and 50%).

For the inductor design, the next design constraints have been considered:

- Cooper foils are used as conductor, with a current density up to 5 A/mm^2.
- Natural cooling.
- Air gap on the core is distributed on 3 separated gaps.
- Hot-spot temperature must be lower than 125 B:C.
- The cost of the materials considered are 5.59 €/kg, 15 €/kg for the Amorphous core, and 4 €/kg for the GO core.
- Isolation material, and structural/frame materials for the inductor manufacturing have not been considered.

A. INDUCTORS FOR A 1500 V DC TO 690 V AC PV INVERTER

The results obtained for a 1500 V 2-level 100 kW PV inverter are listed on Table 4 in terms on weight (kg), volume (dm^3), losses (W) and cost of materials (€). And these results are also plotted on Fig. 7 to see the trend line in the different variables considered. In the Fig. 7, the area where the Si-based inverters can typically operate for this topology is highlighted with a gray shadow, i.e., up to 10 kHz. And the rest of the area represents the area where SiC-based 2-level inverters can operate, higher than 10 kHz.

The preferred choice for a Si-based inverter (#Si-1500V) corresponds with a GO inductor design, because at low switching frequencies (up to 10 kHz), GO designs have a good balance between losses and size with a low cost, compared to amorphous-based designs. With $\Delta I_{pp,rms}/I_{grid} = 8 - 15\%$ (gray and dark-blue dotted lines) the designs are similar, being the cheapest design at this frequency.

It can be seen how the GO-based inductors have high losses under high current ripples and at the same is true with the increase of switching frequency. It results in the need of heavier cores to dissipate the losses, increasing the material costs. Going to switching frequencies of 20 kHz and higher, the tendency changes. The amorphous-based designs result in an inductor 50% (or more) lighter with also the same improvement in the losses. In addition, with amorphous design, higher switching ripples can be assumed because core losses are not the bottleneck, reducing L value needed. It results in high frequency designs with amorphous materials (suitable for SiC-based converters) whose cost of materials is similar to the GO-based design for low-frequency (Si-based converters), but with an important reduction in terms of weight, volume and also losses. The design selected for the SiC version is (#SiC-1500V).

B. INDUCTORS FOR A 1000 V DC TO 400 V AC PV INVERTER

The results obtained for a 1000 V 2-level 100 kW PV inverter are listed in Table 5, and designs are compared in Fig. 8 in the same format as before. It this case, it must be noticed that for the same power, at lower AC voltage (400 V rather than 690 V) the RMS current is higher. This higher current value results in higher inductor losses and weight, compared with the 1500 V PV inverter designs, being one of the reasons due to higher voltage range PV installation and gaining interest on the market. The conclusions are similar to the presented previously, where #Si-1000V is the best choice for Si-based low frequency inverter because despite of not having the best efficiency, it is the cheapest option. Under higher current ripples, amorphous materials are well suited under high switching frequencies, being #SiC-1000V the best choice for the SiC-based inverter.

For both voltage classes it must be highlighted that in this case, the cost of the materials is only considered. But is important to include also the cost is terms of manufacturing-tooling that the inductor manufacturers apply on the final cost.

V. EXPERIMENTAL RESULTS

With these simulations, it has been decided to manufacture the inductors with amorphous material, to work at 20 kHz switching frequency, having a compromise between the SiC-MOSFET losses and the inductor losses.

TABLE 5. Inductor design results for 1000 V DC, 400 V AC PV inverter.

$\Delta I_{pp,rms}/I_{grid}[\%]$	8%				8%				15%				15%			
$f_{sw}[kHz]$	10	15	20	30	10	15	20	30	10	15	20	30	10	15	20	30
Material	GO				Amorphous				GO				Amorphous			
Weight [kg]	72	146	213	504	32	27	21	18	137	250	358	800	28	20	17	10
Losses [W]	545	778	989	1,960	781	657	628	600	800	1200	1567	3560	593	546	492	473
Volume [dm^3]	13.7	26.3	35.4	77.0	6.1	4.7	3.7	3.0	26.3	42.0	59.0	120.0	4.8	4.0	3.4	3.0
Cost [€]	308	599	861	2,100	400	368	285	250	550	1150	1467	3501	369	300	226	200

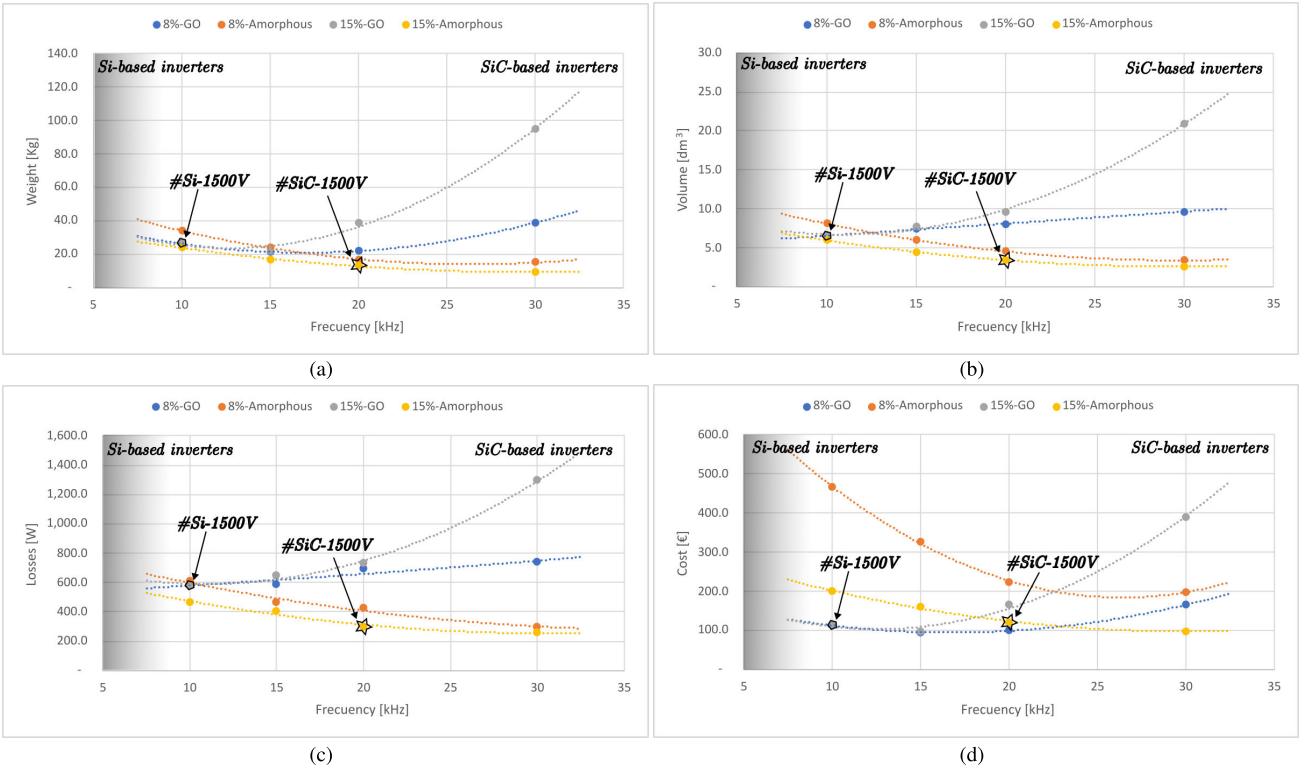

FIGURE 7. 1500 V DC to 690 V AC PV inverter: Three-independent solution evaluation with amorphous and GO steel material for different switching frequencies and inductor current ripple (a) Weight in kg. (b) Volume in dm^3. (c) Losses in W. (d) Cost of materials in €.

TABLE 6. Filter inductance values selected for a 100 kVA nominal power.

V_{grid} [V]	V_{DC} [V]	I_{grid} [A]	$\Delta i_{pp,Max}$ [A]	$\Delta I_{pp,rms}$ [A]	$\frac{\Delta i_{pp,max}}{\hat{I}_{grid}}$ [%]	$\frac{\Delta i_{pp,rms}}{I_{grid}}$ [%]	L_{20kHz} [μH]	Design
400	800	144,34	98,9	20,21	48%	14.1%	110	#SiC-1000V
690	1300	83.67	61,6	11,38	49%	13.6%	280	#SiC-1500V

The values selected are presented on Table 6. The steady state DC voltages considered for nominal power conditions (MPP on the PV panel) are 800 V and 1300 V in each voltage prototype.

The test-bench depicted in Fig. 9 has been used for the experimental evaluation. The AC inductors shown are the Design #SiC-1500V, and the 3-phase inverter, both for the 1500 V DC - 690 V AC system (see Fig. 9). Two different inverters have been developed (one per each voltage level) with a similar electro-mechanical design.

For the two inverter prototypes:

- **1500 V DC - 690 V AC system:** ST-Microelectronics, SCT20N170, 1700 V SiC-MOSFET samples have been used.
- **1000 V DC - 400 V AC system**: Wolfspeed 1200 V SiC-MOSFET modules, CAS325M12HM2, have been used.
- For both prototypes, low inductance Metallized Polypropylene Film (MKP) DC capacitors are used to manage expected di/dt and dv/dt around 28 $kV/\mu s$ and 15 $kA/\mu s$, respectively, as it was described in detail in [42] for the lower voltage PV inverter prototype.

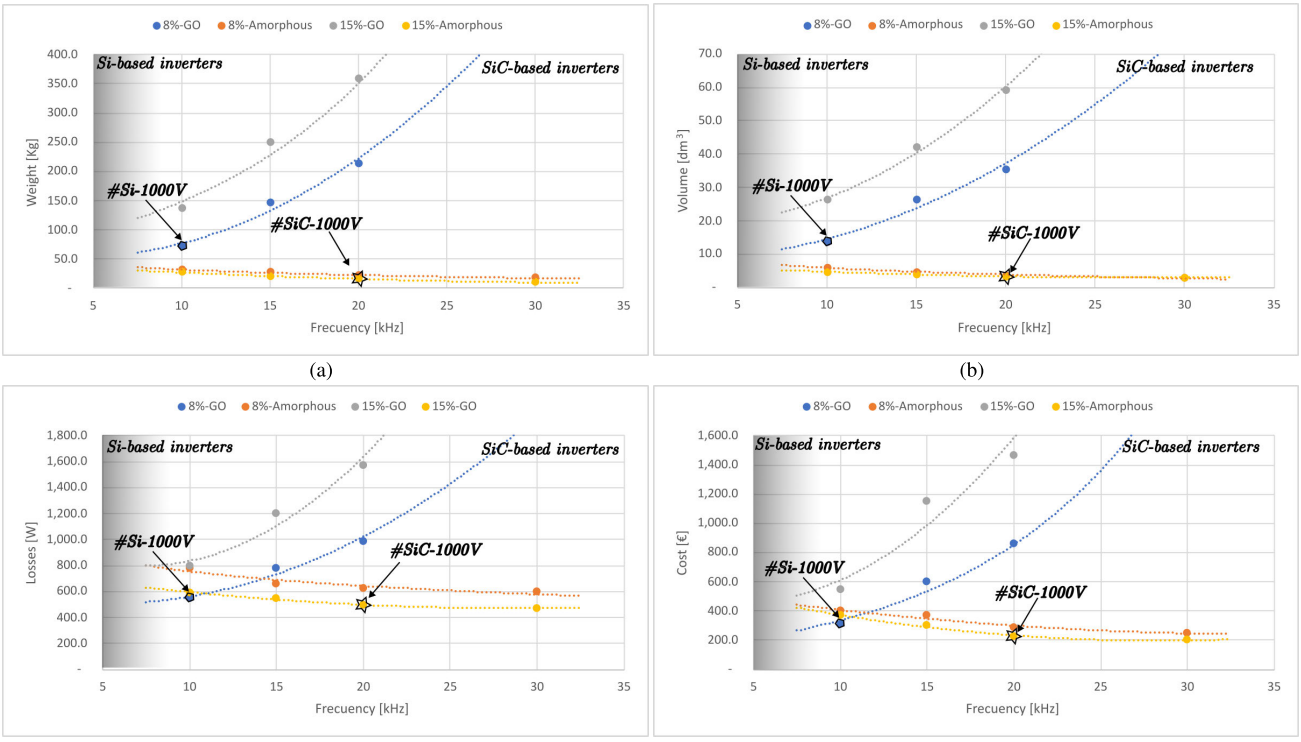

FIGURE 8. 1000 V DC to 400 V AC PV inverter: Three-independent solution evaluation with amorphous and GO steel material for different switching frequencies and inductor current ripple. (a) Weight in kg. (b) Volume in dm^3. (c) Losses in W. (d) Cost of materials in €.

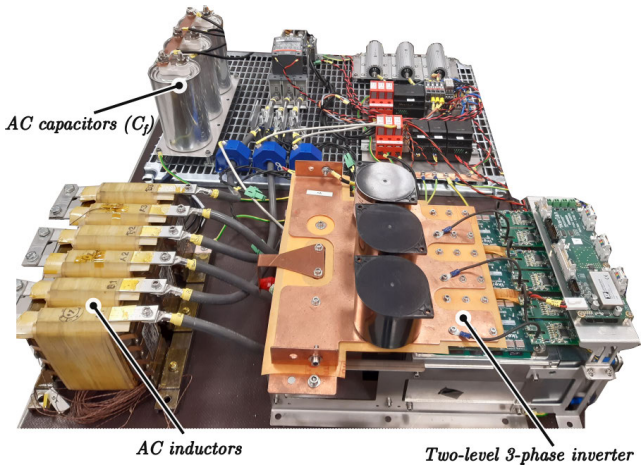

FIGURE 9. Laboratory test-bench.

The final manufactured inductors (#SiC-1500V and #SiC-1000V) have been manufactured by Elettromil, and are shown on Fig. 10. The final volume of these samples is 6.16 dm^3 for the Design #SiC-1000V, and 5.26 dm^3 for the Design #SiC-1500V, with a 20 kg and 18 kg weight, respectively. They have been tested under different power levels and the results are presented in Fig. 11. The results, at 100 kW nominal power, correspond with the values expected in Fig. 7 and 8. It is important to highlight that the losses at 690 V AC grid (design #SiC-1500V) have around the 50% power losses compared to 400 V AC grid (design #SiC-1000V), when in both cases the power level is the same, due the RMS current reduction on the inductors.

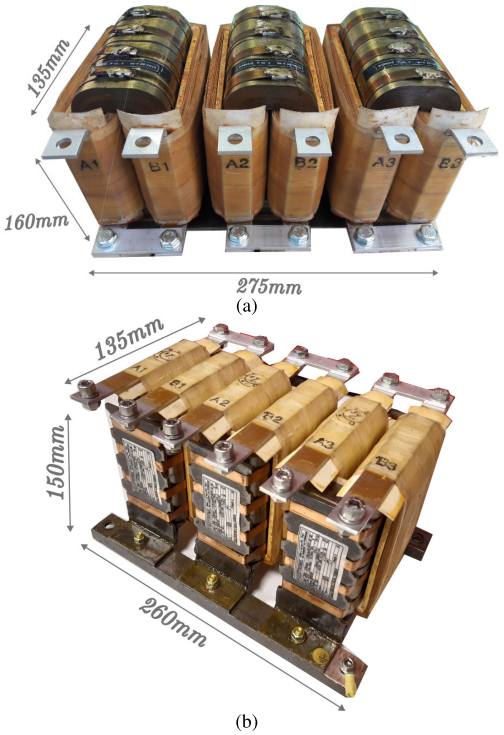

FIGURE 10. Inductors manufactured by Elettromil for the PV inverter prototypes. (a) Design #SiC-1000V. (b) Design #SiC-1500V.

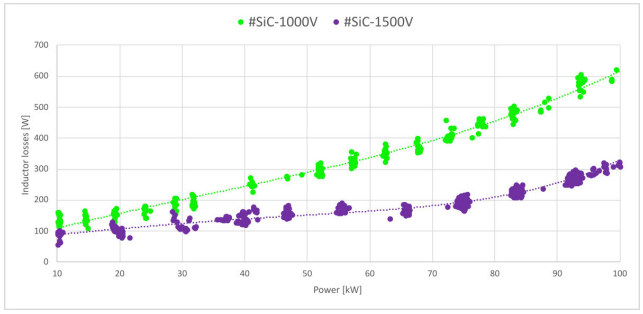

FIGURE 11. Losses measured on the AC filter inductors developed, at different output power levels.

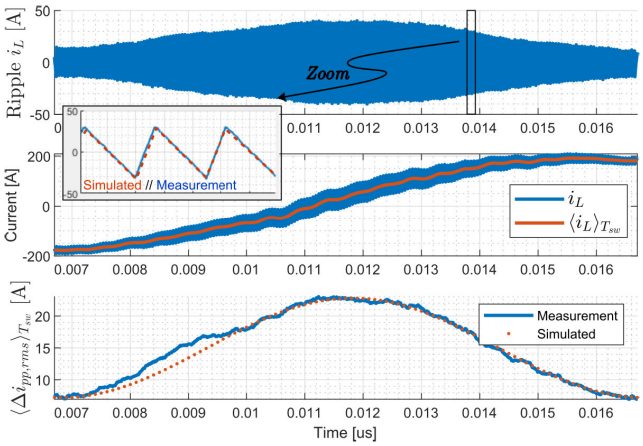

FIGURE 12. Measurements obtained with Design #SiC-1000V. Top: ripple component in the inductor current i_L with a zoom in compared with simulated waveform. Middle: inductor current i_L and switching period average of the current, $\langle i_L \rangle_{T_{SW}}$. Bottom: $\langle \Delta i_{pp,rms} \rangle_{T_{SW}}$ measured and simulated according to (5).

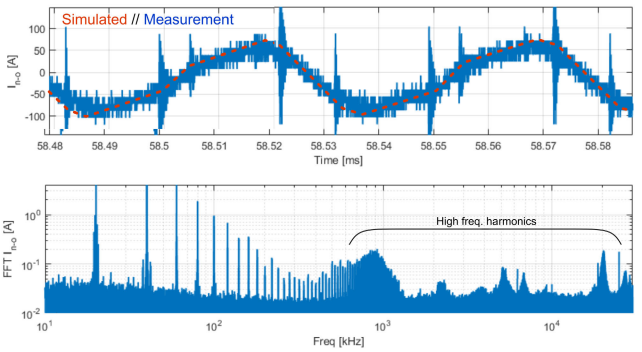

FIGURE 13. Current measurement obtained on the $n-o$ connection (i_{n-o}) with Design #SiC-1000V on que 1000 V DC to 400 V AC system. Top: Current measurement and simulated. Bottom: FFT of the current.

FIGURE 14. Current total harmonic distortion (THDi) measured on the grid side with the two developed converters.

In Fig. 12, the waveforms measured over a half-line cycle are presented for the 400 V AC prototype with #SiC-1000V inductors and under nominal power and voltage conditions. In the top figure, it is compared the measured current ripple waveform (in blue) with the simulated one (in orange) in PLECs. The middle plot shows the total inductor current (i_L) in blue, and the average current $\langle i_L \rangle_{T_{sw}}$ in each switching period. It can be appreciated that the RMS current ripple measured in each switching period ($\langle \Delta i_{pp,rms} \rangle_{T_{sw}}$) corresponds with the value obtained by (5), represented by orange dots in the figure.

The current measured on the neutral ($n-o$ connection) in the 400 V AC grid prototype is presented on Fig. 13 in the top plot. The measured current (in blue) is compared with the simulated one (in dotted orange line). The main difference between them is that there are no high frequency oscillations due to MOSFET switching, and therefore they do not appear in the simulation. The FFT of the measured current is plotted at the bottom of Fig. 13. It can be seen how the current waveform has harmonics at the switching frequency (20 kHz), and also at much higher harmonics due to the turn-on and off transitions commented, around 1 MHz and 20 MHz. With the $n-o$ connection, these high frequency components are confined on the converter, and are avoided on the grid and PV panel sides.

Considering the grid side, Fig. 14 shows the total harmonic distortion of the current injected to the grid for the two developed converters as function of the power. It can be seen that the results obtained in both designs are lower than 3% at power levels higher than 60 kW (a 60% of the nominal power).

VI. CONCLUSION

On 3-phase PV inverters, the AC filter inductor represents an element with an important impact on the weight, efficiency and cost of the converter. If in the PV converter the AC filter is DC-link referenced, there is an increment on the current ripple that can be compensated with the upgrade to SiC switching devices. This is analyzed on this work, and how the reduction of the AC filter inductors due to the use of these SiC samples improve the P-Q controllability limits of the PV inverter.

The paper also presents the different alternatives for the filter inductors, as function of the switching frequency, magnetic core materials and current ripple for a 100 kVA inverter. The results show how amorphous materials represents a interesting alternative at frequencies higher than 20 kHz, resulting in more efficient inductors, lighter and smaller with a material costs similar to the silicon steel (GO) solutions for Si-based

PV inverters. In addition, with amorphous materials higher ripples can be managed without penalizing inductor size or efficiency, due to the better characteristics at higher switching frequencies.

Two different inverter prototypes for 400 V and 690 V AC grids have been developed and tested. The experimental results validate the losses expected for the amorphous designs. For the same power rating, the higher grid voltage (400 V vs 690 V AC) results on lower current rating, and therefore on lower losses on the inductor (around the half of the losses).

The future works of this paper are focused on the common-mode currents injected to the system (grid and PV panels) with and without the the neutral wire connection.

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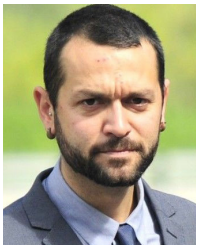

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