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RESEARCH ARTICLE

A New Single DC Source Five-Level Boost Inverter Applicable to Grid-Tied Systems

MILAD GHAVIPANJEH MARANGALU[1], NASER VOSOUGHI KURDKANDI[2], (Member, IEEE), PEYMAN ALAVI[3], SAEIDEH KHADEM[4], (Member, IEEE), HADI TARZAMNI[5], (Student Member, IEEE), AND ALI MEHRIZI-SANI[6], (Senior Member, IEEE)

[1]Faculty of Electrical and Computer Engineering, University of Tabriz, Tabriz 51666-16471, Iran
[2]Department of Electrical and Computer Engineering, San Diego State University, San Diego, CA 92182, USA
[3]School of Electrical Engineering and Computer Science, Penn State University, State College, PA 16801, USA
[4]Program of Electrical Engineering and Industrial Applied Mathematics, California State University Long Beach, Long Beach, CA 90840, USA
[5]Department of Electrical Engineering and Automation, Aalto University, 02150 Espoo, Finland
[6]Bradley Department of Electrical and Computer Engineering, Virginia Tech, Blacksburg, VA 24061, USA

Corresponding author: Hadi Tarzamni (hadi.tarzamni@aalto.fi)

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ABSTRACT In this paper, a single source five-level boost inverter has been proposed and analyzed. The proposed structure includes a five-level inverter and a single-input multi-output (SIMO) boost converter. In this structure, the DC link voltage has been controlled by controlling the implemented DC-DC boost converter. In addition, the inverter switching pattern has been obtained based on the pick current control (PCC) method. In order to test and prove the performance of the proposed structure, this system is tested with the local grid. Since the active and reactive powers have been controlled based on the PCC method, the generated energy in a renewable energy source can be transferred to the local grid with a controlled and high-quality current. In this paper, the proposed structure has been introduced and its operation in different modes has been analyzed completely. Furthermore, the design considerations of the required elements have been investigated. Also, the power loss analysis and the comparison results of the proposed converter with other similar structures have been presented. Finally, in order to test the practical performance of the proposed structure and prove the theoretical analysis, a 620 W laboratory prototype of this structure has been assembled and its performance with the local grid has been tested.

INDEX TERMS Multilevel inverter, DC–DC converter, peak current control (PCC).

I. INTRODUCTION

The multilevel inverters have been extensively studied in recent years and still are interesting for both academics and engineers. In the last ten years, research works have been concentrated on exploring new topologies for multilevel inverters. Therefore, a huge number of multilevel inverters with reduced circuit components have been presented in the literature. In these structures, the main purpose is reducing the number of the required power switches [1], [2], [3], [4] and DC voltage sources [5], [6], [7], [8], [9], [10]. In order to provide higher number of output voltage levels (high resolution), the presented inverters with reduced number of components contain considerably lower number of components in comparison with conventional inverters. However, in practical applications, the output voltage with considerable high voltage levels may not be required. On the other hand, almost in all the multilevel inverters with reduced number of components, some interesting features of the conventional multilevel inverters such as modularity may be lost. To provide high resolution with considerable number of voltage levels, this condition is even more intensified. Therefore, implementing multilevel inverters with high voltage levels may not be efficient practically.

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Although voltage boosting capability of the multilevel inverters is an interesting and useful feature for these inverters, this topic has not been investigated as widely as the component reduction topic. The presented topologies in [11], [12], [13], [14], [15], and [16] benefit from voltage boosting capability. In [11], a multilevel inverter with switched-battery based voltage bosting capability has been presented. In this topology, the implemented batteries get charge from the DC source and their series connections boost the inverter input voltage. Since more switching elements have been required to derive the mentioned switched-battery system, this structure suffers from high number of the switching elements. In [12], a thirteen-level inverter with voltage boosting capability has been introduced. In this inverter, the voltage boosting capability has been obtained based on the capacitors partial charging method. In order to obtain the expected voltage levels, the capacitors should be charged in different voltage levels. Consequently, this partial charging results in high total harmonic distortion (THD) of the output voltage. In [13], in order to achieve the voltage boosting capability, a Z-network has been added to the conventional cascaded H-bridge (CHB) multilevel inverter. In this structure, in order to implement only one Z-network for all the utilized H bridges, the utilized H-bridges are cascaded via low-frequency (LF) transformers which results in the overall system's high cost. The presented topology in [14] is a five-level inverter with eight power switches, two LF transformers, and a Z-network. In this structure, the voltage boosting capability has been provided by the separate DC-DC boost converter of each bridge. Since each bridge requires its DC source and DC-DC boost converter, this method cannot be efficient. Also, in order to modify the output voltage quality in lower output conditions, the idea of regulating the multilevel inverters DC voltage in response of changing the required output voltage magnitude has been presented in [15] and [16].

The presented five-level inverters in [17], [18], [19], and [20] require more than one DC source to provide the expected output voltages. However, the presented five-level inverters in [21], [22], [23], and [24] are capable of providing the expected output voltages with only one DC source. The introduced single source five-level inverters in [24] and [25] contain twelve and five power switches, respectively. Voltage boosting capability cannot be achieved by these structures. In [26], a new single DC source five-level inverter based on the fault tolerant method has been presented. This topology contains eight power switches and two power diodes. Similar to [24] and [25], the voltage boosting capability cannot be obtained by this topology.

In this paper, a single source multilevel inverter with boosting capability and lower number of components has been proposed. In this topology, the implemented converter in DC side has been analyzed and controlled based on the inverter's output voltage. Therefore, it is possible to improve the quality of the inverter's output voltage by regulating the DC sides voltages. Also, the PCC control method has been implemented to generate the inverter's switching pulses and regulate the active and reactive powers. In order to prove the performance of the proposed topology, a laboratory prototype of the introduced setup has been tested with the local grid and the results have been investigated. In this paper, the proposed topology, the operational modes of the introduced five-level inverter, control method of the implemented DC-DC converter, and control method of the proposed inverter have been presented in section II. The design of the implemented elements has been discussed in section III. In section IV, the power loss analysis of the proposed structure has been investigated. Also, a comparison study between the proposed five-level inverter and other related topologies has been presented in section V. In order to verify the dynamic response of the proposed inverter, some simulation results are provided in Section VI. Finally, in order to test the performance of the proposed setup and verify the claimed advantages of this structure, a 620 W laboratory prototype of the introduced structure has been assembled and the results have been investigated in section VII.

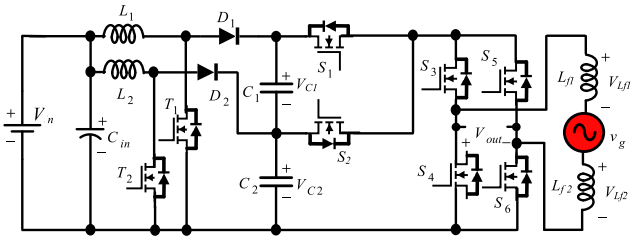


FIGURE 1. Proposed five-level boost inverter.

TABLE 1. Switching table of the proposed five-level inverter.

S_1	S_2	S_3	S_4	S_5	S_6	Switch / Voltage
1	0	1	0	0	1	V_{dc}
0	1	1	0	0	1	$V_{dc}/2$
0	0	1	0	1	0	0
0	1	0	1	1	0	$-V_{dc}/2$
1	0	0	1	1	0	$-V_{dc}$

II. PROPOSED TOPOLOGY AND IMPLEMENTED CONTROL SYSTEMS

In this section, the completely description of the proposed topology and its operation modes are presented. Also, the implemented control systems of the proposed inverter are provided.

A. PROPOSED TOPOLOGY

The schematic of the proposed topology has been illustrated in Fig. 1. This structure is a modified version of the presented inverter in [27]. Based on Fig. 1, the proposed structure is a combination of a SIMO DC-DC boost converter and a multilevel inverter. Since the inverter side is a five-level inverter, in the DC side, a single-input two-output DC-DC converter is required. The implemented five-level inverter is a six-switch inverter and this inverter is connected to the two

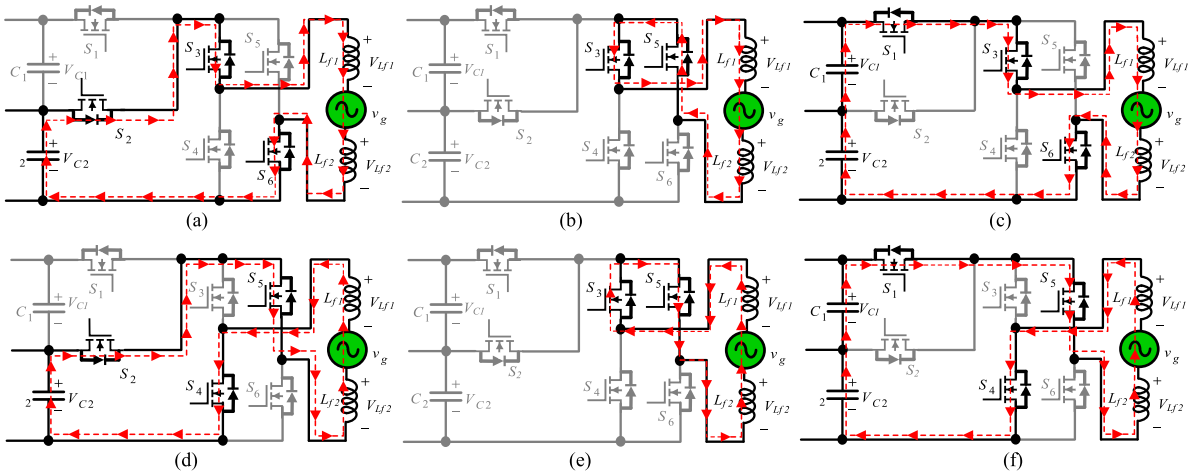


FIGURE 2. Operational modes of the proposed five-level inverter a) Mode 1, b) Mode 2, c) Mode 3, d) Mode 4, e) Mode 5, f) Mode 6.

output capacitors of the DC side. In Fig. 1, the implemented DC-DC converter contains two MOSFETs (T_1 and T_2), two inductors (L_1 and L_2), two power diodes (D_1 and D_2), and two output capacitors (C_1 and C_2). In this structure, two DC side output capacitors are the connection link between the DC side and inverter side. By controlling the implemented DC-DC converter, both the DC side output voltages (V_{C1} and V_{C2}) can be controlled autonomously. Therefore, by implementing a DC voltage source ($V_{in} = V_{dc}$), two non-isolated DC voltage sources have been obtained in the output of DC side. Since, autonomous control of the output DC voltages is possible, even with unequal power delivery from the output capacitors, the proposed structure can provide the desired performance. In fact, in the proposed structure, during a common cycle, the output capacitor C_2 transfers more power than output capacitor C_1. As a result, the mentioned feature is vital for the performance of the proposed structure. In Fig. 1, the implemented five-level inverter contains six power switches (S_1-S_6). The power switches S_1 and S_2 have been implemented to generate the output voltage levels. Also, the H-bridge part (switches S_3-S_6) has the responsibility of changing the voltage polarity to obtain the desired AC voltage in the output side of the inverter. Furthermore, the H-bridge switches (S_3-S_6) generate the zero-voltage level of the output voltage waveform. The switching states of the proposed inverter have been presented in Table 1. This pattern is obtained based on the pick current control (PCC) method. The detailed information about this method and obtaining the switching pattern has been presented in the control strategy subsection. In order to provide a five-level voltage waveform with equal steps, the voltages of the output capacitors (V_{C1} and V_{C2}) should be equal. In the proposed inverter, the DC link voltage ($V_{DC,link} = V_{C1} + V_{C2}$) can be regulated based on the required output voltage. Based on the switching pattern, the proposed inverter has six different operational modes and the equivalent circuits of these modes have been illustrated in Fig. 2.

B. PROPOSED FIVE-LEVEL INVERTER OPERATIONAL MODES

1) FIRST OPERATIONAL MODE

The equivalent circuit of the proposed inverter in the first operational mode has been shown in Fig. 2(a). In this mode, the power switches S_2, S_3, and S_6 are in on state. Therefore, the stored energy in the capacitor C_2 transfers to the output side and the current of the output inductor increases linearly. Also, due to off state of the power switch S_1, the capacitor C_1 does not conduct. As a result, the magnitude of the output voltage is equal to the voltage of the capacitor C_2 ($V_{out} = +V_{dc}/2$).

In this mode, the power switches voltage stresses can be obtained as follows:

$$V_{S1} = V_{C1} = V_{dc}/2 \tag{1}$$
$$V_{S4} = V_{S5} = V_{C2} = V_{dc}/2 \tag{2}$$

2) SECOND OPERATIONAL MODE

The equivalent circuit of the second operational mode is shown in Fig. 2(b). In this mode, the power switches S_3 and S_5 are in on state. Therefore, the output current is reduced and the zero-voltage level has been generated in the output voltage waveform.

3) THIRD OPERATIONAL MODE

Fig. 2(c) illustrates the equivalent circuit of the proposed structure in the third operational mode. In this mode, the power switches S_1, S_3, and S_6 are in on state. Furthermore, the capacitors C_1 and C_2 transfer energy to the output side simultaneously. As a result, the output voltage magnitude is equal to the DC link voltage ($V_{out} = +V_{dc}$).

The power switches voltage stresses can be achieved as follows:

$$V_{S2} = V_{C1} = V_{dc}/2 \tag{3}$$
$$V_{S4} = V_{S5} = V_{C1} + V_{C2} = V_{dc} \tag{4}$$

4) FORTH OPERATIONAL MODE

Fig. 4(d) shows the proposed inverter in the fourth operational mode. In this mode, the switches S_2, S_4, and S_5 are in on state. Consequently, the first negative voltage level in the negative half cycle has been generated and the output voltage is equal to $-V_{dc}/2(V_{out}= -V_{dc}/2)$. In this mode, the direction of the output current has been changed.

In this mode, the power switches voltage stresses can be obtained as follows:

$$V_{S1} = V_{C1} = V_{dc}/2 \tag{5}$$
$$V_{S3} = V_{S6} = V_{C2} = V_{dc}/2 \tag{6}$$

5) FIFTH OPERATIONAL MODE

Fig. 2(e) shows the proposed inverter in the fifth operational mode. Based on this figure, the power switches S_3 and S_5 are in on state. As a result, the zero voltage level of the output voltage has been generated in the negative half cycle.

6) SIXTH OPERATION MODE

Fig. 2(f) illustrates the equivalent circuit of the proposed inverter in the sixth operational mode. In this mode, the switches S_1, S_4, and S_5 are in on state. The output voltage is negative and the second voltage level of the negative half cycle has been generated. Therefore, the output voltage is equal to $-V_{dc}$ ($V_{out}= -V_{dc}$).

The power switches voltage stresses can be obtained as follows:

$$V_{S2} = V_{C1} = V_{dc}/2 \tag{7}$$
$$V_{S3} = V_{S6} = V_{C1} + V_{C2} = V_{dc} \tag{8}$$

C. DYNAMIC MODEL AND CONTROL METHOD OF THE IMPLEMENTED SIMO DC-DC CONVERTER

As discussed, a SIMO DC/DC converter has been implemented to provide two equal output voltages (V_{C1} and V_{C2}) from a single input DC voltage (V_{in}). The schematic of the implemented DC-DC converter without adding the proposed five-level inverter has been illustrated in Fig. 3. In order to control the output voltages (V_{C1} and V_{C2}) based on the switch's duty cycles (d_1 and d_2), the dynamic model of the implemented DC-DC converter can be described as follows:

$$\dot{x} = Ax + Bu, \quad y = Cx + Du \tag{9}$$

where x is the state space matrix, u is the input vector matrix, and y is the output vector matrix. In the implemented DC-DC converter, there are four energy storage elements (L_1, L_2, C_1, and C_2). Therefore, state space matrix, input and output matrixes can be described as follows:

$$x^T = \begin{bmatrix} i_{L1} & i_{L2} & v_{C1} & v_{C2} \end{bmatrix},$$
$$u^T = [v_{in}], \; y^T = [v_{C1} \; v_{C2}] \tag{10}$$

Analyzing the implemented DC-DC converter, the state space variables can be obtained as follows:

$$\frac{di_{L1}}{dt} = \frac{V_{in}}{L_1} + \frac{V_{C1} + V_{C2}}{L_1}(d_1 - 1) \tag{11}$$

$$\frac{di_{L2}}{dt} = \frac{V_{in}}{L_2} + \frac{V_{C2}}{L_2}(d_2 - 1) \tag{12}$$
$$\frac{dV_{C1}}{dt} = \frac{i_{L1}}{C_1}(1 - d_1) - \frac{V_{C1}}{R_{o1}C_1} \tag{13}$$
$$\frac{dV_{C2}}{dt} = \frac{i_{L1}}{C_2}(1 - d_1) + \frac{i_{L2}}{C_2}(1 - d_2) - \frac{V_{C2}}{R_{o2}C_2} \tag{14}$$

Based on small signal model, all the variables contain a DC part ($\bar{X}$, $\bar{Y}$, $\bar{U}$, $\bar{D}$) and an AC part ($\tilde{x}$, $\tilde{y}$, $\tilde{u}$, $\tilde{d}$). As a result, this equation can be written:

$$x = \bar{X} + \tilde{x}, \; y = \bar{Y} + \tilde{y}, \; u = \bar{U} + \tilde{u}, \; d_{1,2} = D_{\bar{1},2} + \tilde{d}_{1,2} \tag{15}$$

In this converter, the purpose is controlling the output voltages (V_{C1} and V_{C2}) by regulating the duty cycles (d_1 and d_2). Therefore, considering that the AC values are almost constant during a switching period and are noticeably smaller than DC values ($\bar{X} \gg \tilde{x}, \bar{Y} \gg \tilde{y}, \bar{U} \gg \tilde{u}, \bar{D} \gg \tilde{d}$), the small signal model of this converter can be rewritten as follows:

$$\dot{\tilde{x}} = A'\tilde{x} + B'\tilde{u}, \; \tilde{y} = C'\tilde{x} \tag{16}$$

where $\tilde{x}$, $\tilde{u}$, and $\tilde{y}$ can be described as follows:

$$\tilde{x}^T = \begin{bmatrix} \tilde{i}_{L1} & \tilde{i}_{L2} & \tilde{v}_{C1} & \tilde{v}_{C2} \end{bmatrix},$$
$$\tilde{u}^T = [\tilde{d}_1 \;\; \tilde{d}_2], \; \tilde{y}^T = [\tilde{v}_{Co1} \; \tilde{v}_{Co2}] \tag{17}$$

Now, considering (11-17), matrixes $A'(n\times n)$, $B'(n\times n)$, and $C'(m\times n)$ can be obtained as follows:

$$A' = \begin{bmatrix} 0 & 0 & \frac{(\bar{D}_1 - 1)}{L_1} & \frac{(\bar{D}_1 - 1)}{L_1} \\ 0 & 0 & 0 & \frac{(\bar{D}_2 - 1)}{L_2} \\ \frac{(1 - \bar{D}_1)}{C_1} & 0 & -\frac{1}{R_{o1}C_1} & 0 \\ \frac{(1 - \bar{D}_1)}{C_2} & \frac{(1 - \bar{D}_2)}{C_2} & 0 & -\frac{1}{R_{o2}C_2} \end{bmatrix} \tag{18}$$

$$B' = \begin{bmatrix} \frac{\bar{V}_{C1} + \bar{V}_{C2}}{L_1} & 0 & \frac{-\bar{I}_{L1}}{C_1} & \frac{-\bar{I}_{L1}}{C_2} \\ 0 & \frac{\bar{V}_{C2}}{L_2} & 0 & \frac{-\bar{I}_{L2}}{C_2} \end{bmatrix}^T \tag{19}$$

$$C' = \begin{bmatrix} 0 & 0 & 1 & 0 \\ 0 & 0 & 0 & 1 \end{bmatrix} \tag{20}$$

The schematic of the implemented pole placement control method [28] has been illustrated in Fig. 4. Considering, this figure, these equations can be written:

$$u = -K_x\tilde{x} - K_q q \tag{21}$$
$$\dot{q} = r - y = r - C'\tilde{x} \tag{22}$$

where q and r are the integrator's output and the reference signals of the output variables.

$$r(t)^T = [V_{C1,ref} \quad V_{C2,ref}] \tag{23}$$

Considering (22), these equations can be obtained:

$$\dot{q_1}(t) = V_{C1,ref} - V_{C1}, \quad \dot{q_2}(t) = V_{C2,ref} - V_{C2} \tag{24}$$

Implementing the described control method in a complete state controllable system, it is possible to shift the poles of the system to the desired locations by regulating the control matrixes [28], [29]. The controllability matrix can be defined as follows:

$$\begin{aligned}\Phi_c &= \left[B' \middle| A'B' \middle| A'^2B' \middle| \dots \middle| A'^{n-1}B'\right] \\ &= \left[B' \middle| A'B' \middle| A'^2B' \middle| A'^3B'\right]\end{aligned} \tag{25}$$

Now, the complete rank of the controllability matrix can guarantee the system's complete controllability. Therefore, the following condition should be fulfilled:

$$rank(\Phi_c) = n = 4 \tag{26}$$

Considering (16) and (22), the open-loop matrixes can be written as follows:

$$\begin{cases}\begin{bmatrix}\dot{\tilde{x}}(t)\\ \dot{q}(t)\end{bmatrix} = \begin{bmatrix}A' & 0\\ -C' & 0\end{bmatrix}\begin{bmatrix}\tilde{x}(t)\\ q(t)\end{bmatrix} + \begin{bmatrix}B'\\ 0\end{bmatrix}\tilde{u}(t) \\ \qquad + \begin{bmatrix}0\\ I\end{bmatrix} r(t) \\ y(t) = \begin{bmatrix}C' & 0\end{bmatrix}\begin{bmatrix}\tilde{x}(t)\\ q(t)\end{bmatrix}\end{cases} \tag{27}$$

$$\hat{A}' = \begin{bmatrix}A' & 0\\ -C' & 0\end{bmatrix}, \quad \hat{B}' = \begin{bmatrix}B'\\ 0\end{bmatrix} \tag{28}$$

Now, the new controllability matrix can be achieved as follows:

$$\begin{aligned}\overline{\Phi_c} &= \left[\hat{B}' \middle| \hat{A}'\hat{B}' \middle| \hat{A}'^2\hat{B}' \middle| \dots \middle| \hat{A}'^{n-1}\hat{B}'\right] \\ &= \left[\hat{B}' \middle| \hat{A}'\hat{B}' \middle| \hat{A}'^2\hat{B}' \middle| \hat{A}'^3\hat{B}'\right] \\ &= \left[\begin{array}{c|c|c|c} B' & A'B' & A'^2B' & \hat{A}'^3\hat{B}' \\ 0 & -C' & -C'A'B' & -C'A'^3B'\end{array}\right]\end{aligned} \tag{29}$$

$$\overline{\Phi_c} = \underbrace{\begin{bmatrix}B' & A'\\ 0 & q-C'\end{bmatrix}}_{M}\begin{bmatrix}I & 0\\ 0 & \Phi_c\end{bmatrix} \tag{30}$$

Now, the system is complete controllable when $rank(M)$ is equal to $n + m$:

$$rank(M) = n + m = 6 \tag{31}$$

Considering parameter values from Table 2, Six eigenvalues of $\hat{A}'$ have been achieved as follows:

$$e_{1,2} = 0, \quad e_{3,4} = -5.4 \pm 977.2i, \quad e_{5,6} = -7.9 \pm 2558.3i \tag{32}$$

All the eigenvalues should be completely shifted to the left side of the Jw axis. New desired locations for eigenvalues can be written as follows:

$$\begin{aligned}e'_{1,2} &= -45500, \quad e'_{3,4} = -5005 \pm 977.2i, \\ e'_{5,6} &= -1258 \pm 2558.3i\end{aligned} \tag{33}$$

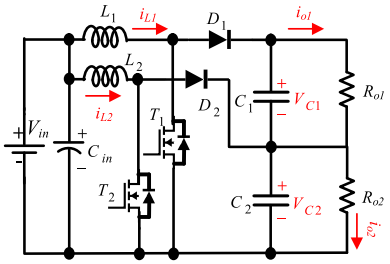


FIGURE 3. Schematic of the implemented DC-DC converter.

TABLE 2. Implemented components in the DC side .

Parameter	Type	Explanation
V_{in}	Fixed DC Voltage	100V
V_{C1}	Fixed DC Voltage	200V
V_{C2}	Fixed DC Voltage	200V
C_1 & C_2	Electrolytic	1000μF-250 V
L_1 & L_2	Ferrite Core	100 μH

Using the formula in MATLAB, to shift the eigenvalues to their new locations in the closed loop system, the control matrixes K_x and K_q can be obtained as follows:

$$K = [K_x, K_q] = \text{place}(\hat{A}', \hat{B}', e') \tag{34}$$

$$K_x = \begin{bmatrix}0.0134 & 0.00040.14280.0176\\ -0.0011 & 0.0257 & -0.2264 & 0.1299\end{bmatrix} \tag{35}$$

$$K_q = \begin{bmatrix}-117.2982 & -129.1656\\ 697.7264 & -164.3719\end{bmatrix} \tag{36}$$

Since the designed control method is type one, it is capable of tracking the input reference values without steady-state error.

Now, combining (22) and (27), the new system can be described as follows:

$$\begin{cases}\begin{bmatrix}\dot{\tilde{x}}(t)\\ \dot{q}(t)\end{bmatrix} = \begin{bmatrix}A' - B'K_x & -B'K_q\\ -C' & q0\end{bmatrix}\begin{bmatrix}\tilde{x}(t)\\ q(t)\end{bmatrix} + \begin{bmatrix}0\\ I\end{bmatrix} r(t) \\ y(t) = \begin{bmatrix}C' & 0\end{bmatrix}\begin{bmatrix}\tilde{x}(t)\\ q(t)\end{bmatrix}\end{cases} \tag{37}$$

Fig. 5 illustrates the bode diagrams of the implemented DC-DC converter. In this figure, the bode diagrams of the both output voltages (V_{C1} and V_{C2}) have been shown before and after implementing the described control method. Based on these bode diagrams, the gain margin (GM) values have been regulated to 11.24 and 17.06 for V_{C1} and V_{C2}, respectively. In addition, the values of the phase margin (PM) have been regulated to 78.89 and 77.08 for V_{C1} and V_{C2}, respectively. Therefore, both the GM and PM values are in the desired range (GM>10 and 60<PM<80) and the output voltages have been controlled based on duty cycles properly. Furthermore, in order to provide additional analysis of the control system, the Nyquist diagram of the implemented control method has been illustrated in Fig. 6.

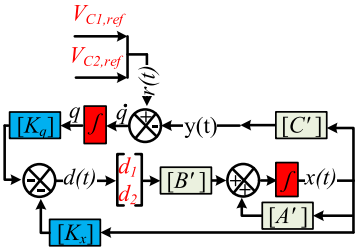


FIGURE 4. Schematic of the implemented control method of DC-DC converter.

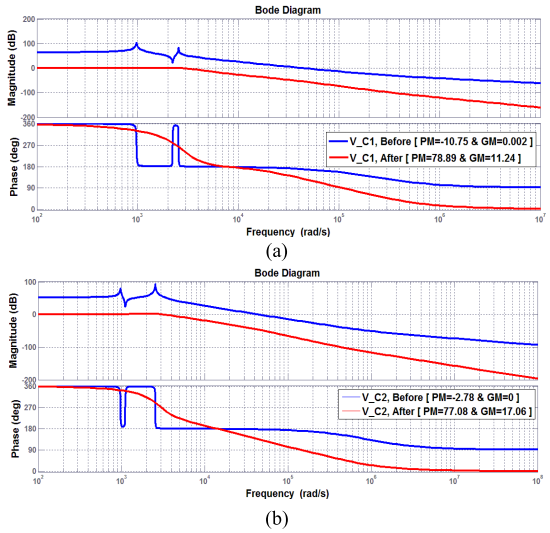


FIGURE 5. Bode diagrams before and after implementing control method (a) for V_{C1} (b) for V_{C2}.

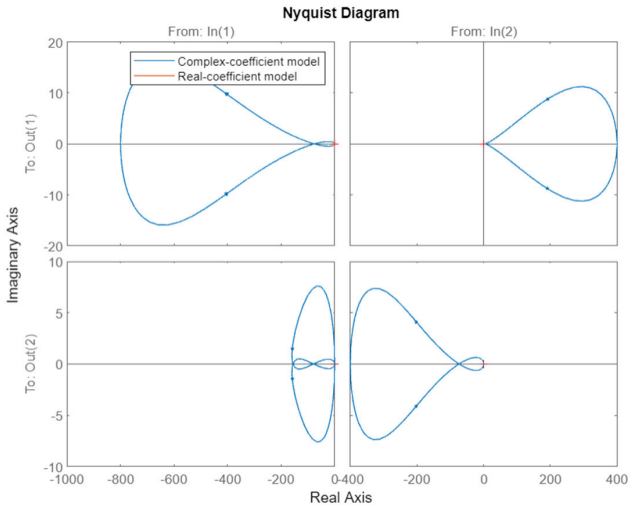


FIGURE 6. The Nyquist diagram of the implementing control method.

D. CONTROL STRATEGY OF THE PROPOSED FIVE-LEVEL BOOST INVERTER

In order to analyze and test the proposed inverter in the practical applications, its performance has been investigated in the grid-tied PV systems. In the proposed five-level inverter, the PCC method is implemented to obtain the switching pattern and control the active and reactive powers [30]. The schematic diagram of the applied control system for grid-tied application has been illustrated in Fig. 7. In this system, the reference injected current has been obtained based on the reference value of power (P_{ref}) and the reference reactive power (Q_{ref}). In addition, the magnitude and phase of the grid values have been obtained by the implemented phase-locked loop (PLL). Therefore, the current reference value and injected value have been compared in the current controller block and based on the PCC strategy, the appropriate gate pulses have been generated.

The reference and measured currents with the switches gate pulses have been shown in Fig. 8. In the current controller block, a special sampling time has been selected (T_{samp}). It should be mentioned that, the power switches work with different switching frequencies. As a result, two different frequencies can be described for the proposed inverter: the switches average switching frequency (f_{avg}) and the switching frequency of the inverter that can be seen from the load side (f_{inv}). The instantaneous slop of the output inductor current that acts like an L-type filter can be calculated by reflecting the switching frequency of the inverter. In this inverter, the switching frequency of the inverter is equal or less than the half of the sampling frequency. In the other word, the maximum switching frequency of the inverter is equal to half of the sampling frequency.

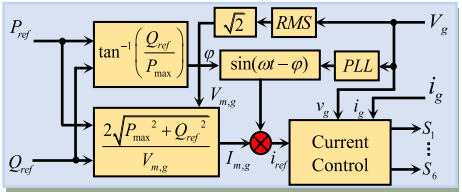


FIGURE 7. Control system of the proposed grid-tied inverter.

By comparing the measured and reference waveforms of the output inductor current which is the injected grid current (i_g), the switching pattern can be derived. During the positive half cycle, if the magnitude of the output voltage is less than half of DC link voltage ($V_{dc}/2$) for a certain sampling time (t_1) and the injected grid current is less than its reference value, the power switches S_2, S_3, and S_6 will start to conduct. Therefore, the output inductor current starts to increase linearly (First operational mode). In the next sampling period, if the injected grid current is more than its reference value (t_2), so the power switches S_3 and S_5 will be turned on and the output inductor current will be reduced (Second operational mode). Also, if the grid voltage (V_g) is higher than half of the DC link voltage ($V_{dc}/2$), the switching pattern will be different. In this condition, for a certain sampling time (t_3), if the injected grid current is lower than its reference value, the power switches S_1, S_3, and S_6 will be turned on (Third operational mode). In addition, at a certain

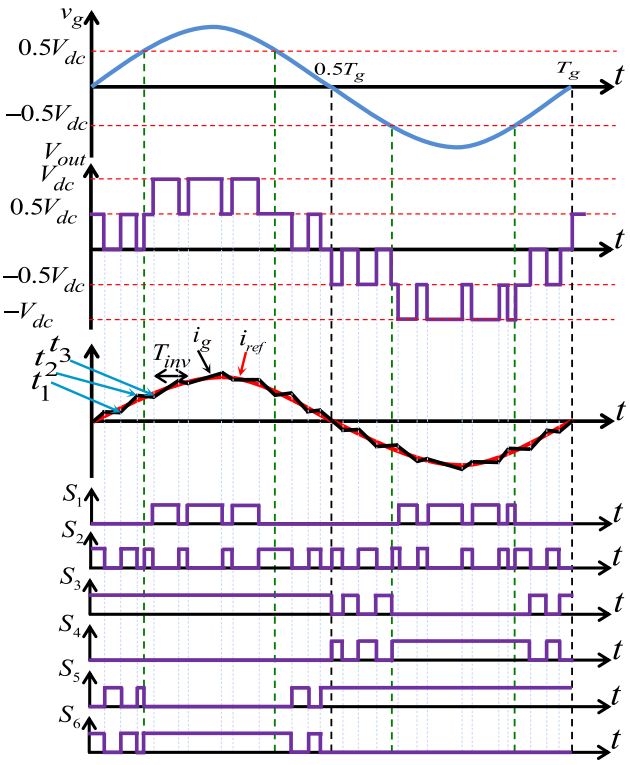


FIGURE 8. Reference and measured current with switches gate pulses.

sampling time (t_4), if the injected grid current is higher than the reference value, in order to decrease the output inductor current, the power switches S_2, S_3, and S_6 will be in on state (First operational mode). Also, in the negative half cycle, the switching pattern of the power switches can be obtained in a similar way. The flowchart of the implemented PCC strategy and logic circuit of the proposed method have been illustrated in Fig. 9(a) and (b). Based on this figure, by implementing this PCC strategy [31], the injected grid current is capable of tracking the reference current sinusoidal waveform properly.

In the third operational mode, considering the Volt-Second-Balance for the output inductor voltage waveform at a certain sampling period, the duty cycle and voltage gain of the inverter can be obtained as follows:

$$v_g = V_{m,g}\sin(\omega t) \tag{38}$$

$$i_g = I_{\mathrm{m,g}}\sin(\omega t - \varphi) \tag{39}$$

$$\int_0^{D_{inv}T_{inv}} (V_{dc} - v_g)dt + \int_{D_{inv}T_{inv}}^{T_{inv}} (V_{dc}/2 - v_g)dt = 0 \tag{40}$$

$$D_{inv} = \frac{V_{m,g}\sin(\omega t) - V_{dc}/2}{V_{dc}} \tag{41}$$

$$G = \frac{v_g}{V_{dc}} = D_{inv} + 1 \tag{42}$$

where φ, D_{inv}, $V_{m,g}$, and $I_{m,g}$ are the angle between the injected voltage and current, duty cycle of inverter, gird voltage pick value, injected current pick value, respectively.

III. DESIGN OF THE IMPLEMENTED COMPONENTS

In this section, the inductance values of output filter and inductor L_1, and L_2 are calculated. Also, the capacitance values of the capacitors C_1, and C_2 are calculated in the following:

A. INDUCTANCE VALUE OF OUTPUT FILTER

In this section, design of the implemented output inductor L_f has been presented.

$$L_f = L_{f1} + L_{f2}, \qquad L_{f1} = L_{f2} = L_f/2 \tag{43}$$

The output inductor current during a switching period can be written as follows:

$$i_{Lf}(t) = \frac{1}{L_f}\int_0^t V_{Lf}(t)dt + i_{Lf}(0) \tag{44}$$

Now, considering (40), the current ripple of the output inductor can be written as follows:

$$\begin{cases} \Delta i_{L_f} = \dfrac{1}{L_f}\displaystyle\int_0^{D.T_{inv}} (V_{dc} - v_g)dt \\ \Delta i_{L_f} = \dfrac{\left(V_{dc} - v_g\right) D_{inv}}{L_f . f_{inv}} \end{cases} \tag{45}$$

The inductance value of output filter can be calculated based on the inverter frequency and duty cycle as follows:

$$L_f = \frac{(V_{dc} - v_g)D_{inv}}{\Delta i_{Lf} . f_{inv}} \tag{46}$$

By substituting (41) into (46), the output inductor value can be obtained in terms grid voltage and DC link voltage as follows:

$$L_f = \frac{V_{dc}/2}{f_{inv}.\Delta i_{Lf}}\left(3v_g - V_{dc} - \left(\frac{v_g}{V_{dc}/2}\right)^2\right) \tag{47}$$

Therefore, considering (43), the values of the inductors L_{f1} and L_{f2} will be the half of the L_f value.

B. INDUCTANCE VALUE OF INDUCRORS L_1, AND L2

To calculate the inductance values of inductors L_1, and L_2 it is necessary to write the integral equations of the inductors current for a complete switching cycle as:

$$i_{Li}(t) = \frac{1}{L_i}\int_0^t V_{Li}(t)dt + i_{Li}(0) \quad ; \quad i = 1, 2 \tag{48}$$

By replacing (20) in (32) the inductance value of inductor L_2 can be obtained as:

$$L_2 = \frac{D_{boost}.V_{Li}}{\Delta I_{Li}.f_{SW}} \tag{49}$$

Note that, the duty cycle of DC-DC boost converter can be calculated as:

$$D_{boost} = \frac{V_{Ci} - V_{dc}}{V_{Ci}} \tag{50}$$

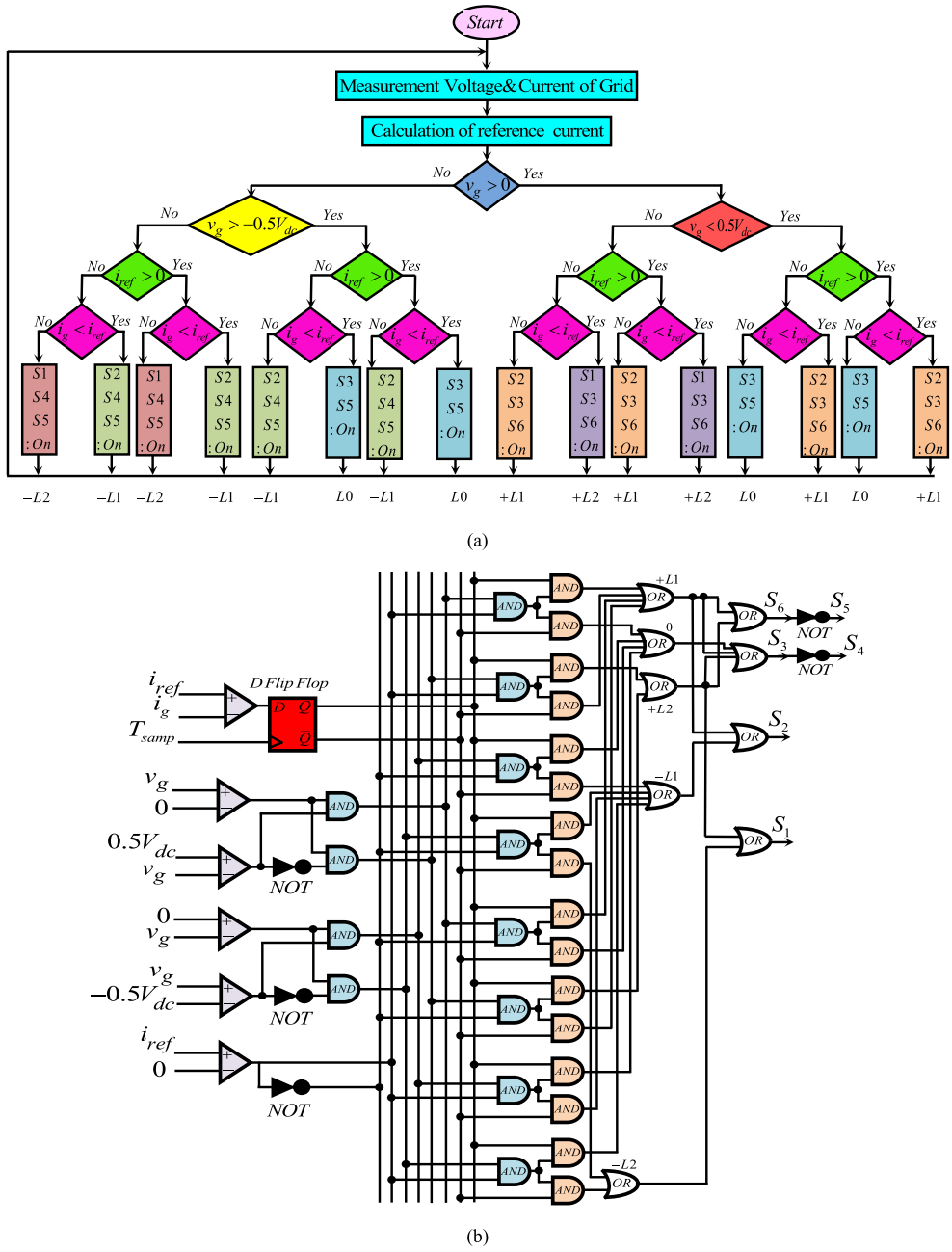


FIGURE 9. (a) Flowchart of the applied PCC strategy (b) logic circuit of the applied PCC strategy.

By placing (50) in (49) and considering the maximum value of current ripple for each inductor ($\Delta I_{Li,\max}$), the final inductance value of each inductor can be obtained as:

$$L_i = \frac{V_{Ci}.V_{dc}}{(V_{dc} + V_{Ci}).\Delta I_{Li,\max}.f_{SW}} \tag{51}$$

In the DC-DC boost converter, the passing current of inductor can be calculated as:

$$I_{Li} = \frac{I_{out}}{1 - D_{boost}} \tag{52}$$

The stored energy of each inductor (L_1 and L_2) can be obtained as follows:

$$W_{Li} = \frac{1}{2}L_i.I_{Li}^2 = \frac{1}{2}L_i\left(\frac{I_{out}}{1 - D_{boost}}\right)^2 \quad ; \quad i = 1, 2 \tag{53}$$

$$W_{Li} = P_{out}.t = \frac{P_{out}}{f_{SW}} \quad ; \quad i = 1, 2, \tag{54}$$

Using (53) and (54), the inductance equation of L_2 can be obtained as follows:

$$L_i = \frac{2\,(1 - D_{boost})^2\,.V_{Ci}^2}{f_{SW}.P_{out}} \quad ; \quad i = 1, 2 \tag{55}$$

Regarding (50), the inductance values of each inductor (L_1 and L_2) can be obtained based on the average value of output power (P_{out}), input voltage and switching frequency and expressed as follows:

$$L_i = \frac{2\,(V_{dc})^2}{f_{SW}.P_{out}} \quad ; \quad i = 1, 2 \tag{56}$$

C. INDUCTANCE VALUE OF OUTPUT FILTER

Considering Fig. 3 (b), in the third operation mode (see Fig. 2(c)) the passing current of the capacitor C_1 and C_2 are equal to the injected grid current (i_g). The voltage of capacitors can be obtained as:

$$V_{C1} = V_{C2} = \frac{1}{C}\int_0^t i_C(t)dt + V_C(0) \tag{57}$$

$$\Delta V_{C1} = \Delta V_{C2} = \frac{i_g}{C_1 f_{inv}} \cdot \left(\frac{v_g - V_{DC,link}}{V_{DC,link}}\right) \tag{58}$$

The peak value of ripple for each capacitor C_1 and C_2 are obtained when the voltage of the grid and the inductor L_f are been at the maximum point. Therefore, the value of capacitors C_1 and C_2 can be written as:

$$C_1 = C_2 = \frac{\mathrm{I}_{m,g}}{2\Delta V_{C,\max} f_{inv}} \cdot \left(\frac{V_{m,g} - V_{DC,link}}{V_{DC,link}}\right) \tag{59}$$

So, the final capacitance values of capacitors C_1, and C_2 can be obtained as:

$$C_1 = C_2 = \frac{\mathrm{I}_{m,g}}{2\Delta V_{C,\max} f_{inv}} \cdot \left(\frac{V_{m,g} - V_{dc}}{V_{dc}}\right) \tag{60}$$

IV. POWER LOSS ANALYSIS

In the proposed inverter, the total loss is equal to the summation of the component's conduction losses, switching losses, and power losses of passive components such as inductors and capacitors. As a result, total losses can be obtained as follows:

$$P_{Total} = P_C + P_S + P_{L,total} + P_{Cap,total} \tag{61}$$

A. CONDUCTION LOSSES

In the proposed inverter, the total conduction losses contain conduction losses of the power switches, power diodes, and implemented capacitors. Therefore, the average conduction losses of the proposed inverter can be calculated as follows:

$$\begin{aligned} P_{C,avg} = &\left[\frac{s(t)}{\pi}\int_0^{\pi}\left(V_S i(t) + R_S i^{\gamma+1} d\omega t\right)\right] \\ &+ \left[\frac{c(t)}{\pi}\int_0^{\pi} R_{Cap} i^2(t) d\omega t\right] \\ &+ \left[\frac{d(t)}{\pi}\int_0^{\pi}\left(R_D i^2(t) + V_D\right) d\omega t\right] \end{aligned} \tag{62}$$

where V_s and V_D are on-state drop voltage of the power switches and diodes, respectively. R_s, R_{cap}, and R_D are the internal resistances of the power switches, capacitors, and power diodes, respectively. Also, γ is a constant parameter which is related to the internal structure of the power switches. $s(t)$, $d(t)$, and $c(t)$ are the number of the power switches, power diodes, and capacitors, respectively.

B. SWITCHING LOSSES

In the power switches, a shift from on-state to off-state or vice versa always causes the switching losses. The switching pulses, voltage and current waveforms, and the switching losses waveform of the power switches have been illustrated in Fig. 10. Considering this figure, the power switches turn-on ($P_{S,on}$) and turn-off ($P_{S,off}$) losses can be obtained as follows:

$$P_{S,on} = \frac{N_{on}.E_{S,on}}{T_s} = \frac{(N_{on}f_s)\,(V_S I_S)}{6} t_{on} \tag{63}$$

$$P_{S,off} = \frac{N_{off} \times E_{S,off}}{T_s} = \frac{(N_{off}f_s) \times (V_S I_S)}{6} t_{off} \tag{64}$$

where $E_{s,on}$ and $E_{s,off}$ are the turn-on and turn-off losses per each time of the switch's turn-on and turn-off, respectively. N_{on} and N_{off} are the number of the switch's turn-on and turn-off per each time of the inverter's switching period. Therefore, the total switching losses can be written as follows:

$$P_S = P_{S,on} + P_{S,off} \tag{65}$$

C. POWER LOSSES OF USED PASSIVE COMPONENTS

In this section, the power losses of passive components such as inductors (L_1 & L_2) and capacitors (C_1 & C_2) and output filter inductors (L_{f1} & L_{f2}) are calculated. In order to calculate the power losses of inductors L_1, and L_2, the following equations should be considered:

$$P_{L1} = r_{L1} \times I^2_{L1,rms} \tag{66}$$

$$P_{L2} = r_{L2} \times I^2_{L2,rms} \tag{67}$$

where, $\mathrm{I}_{L1,rms}$ and $\mathrm{I}_{L2,rms}$ are the average value of passing current of inductors L_1 and L_2, respectively. Also, in the above equations, r_{L1}, and r_{L2} are the internal resistance of the inductors L_1, and L_2, respectively.

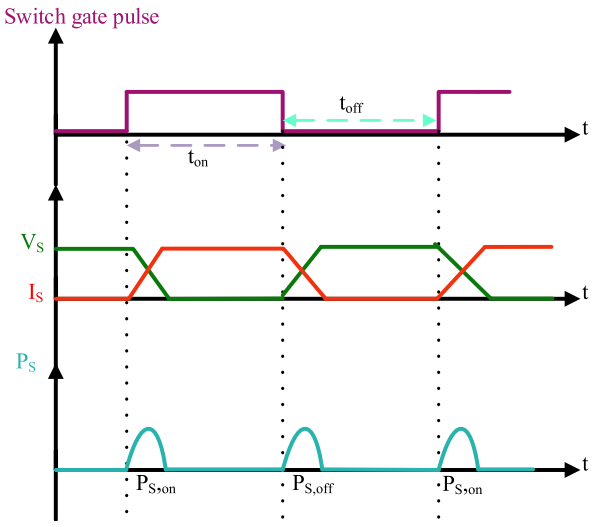


FIGURE 10. Switching gate pulse, voltage and current waveforms of power electronic switches, and switching losses waveform.

TABLE 3. Comparison of the proposed five-level inverter with other similar topologies.

Topology	Number of components				N_{Vdc}	Input voltage (V)	Voltage boosting	Voltage gain	P_{out} (W)	Total volume (cm^3)	Power density (W/cm^3)	Total cost ($)	Cost/P_{out} (%)	RPS	Eff (%)
	N_{SW}	N_D	N_{cap}	N_L											
[18]	8	7	2	3	3	100	Yes	2	600	854.21	0.71	284.3	47.39	No	86
[36]	8	1	2	0	1	200	Yes	2	1000	152.33	6.57	189.3	18.93	Yes	N.R
[37]	8	1	3	0	1	160	No	1	500	150.7	3.32	114.3	23	Yes	N.R
[33]	6	0	1	0	1	200	No	1	770	377.7	2.03	208.1	27	Yes	N.R
[35]	12	0	4	0	1	50	Yes	4	250	696.93	0.35	165.3	66.12	No	92
[38]	8	1	2	0	1	50	Yes	2	250	145.87	1.71	147.2	58	Yes	95.5
[39]	5	0	2	1	1	100	Yes	D / 1-D	200	1144.07	0.17	189.4	95	Yes	92.5
[48]	8	0	3	2	1	200	Yes	2	600	239.17	2.51	164.9	0.27	Yes	98.3
[34]	6	3	2	1	1	60	Yes	4	600	128.1	4.68	59.13	9.85	N.R	N.R
[6]	8	4	3	2	2	100	Yes	1.5	1000	537.5	1.86	151.8	15.18	Yes	95.5
[40]	6	2	2	0	1	200	Yes	2	1000	240.25	4.16	250.2	25.2	Yes	97.5
[41]	8	3	4	2	1	200	Yes	2.8	2000	906.93	2.21	694.9	34.74	N.R	91.0
[42]	7	1	1	1	1	200	Yes	2	1000	387.34	2.58	165.8	16.58	Yes	98.8
[43]	10	4	2	2	2	200	Yes	1.5	500	106.7	4.68	163.8	32.76	N.R	96.0
[44]	9	0	2	0	1	200	Yes	2	1000	106.61	9.37	74.1	7.41	Yes	98.6
[45]	6	0	2	2	1	100	Yes	2D / 1-D	200	356.4	0.56	85.72	43	No	94.5
[46]	10	0	1	1	1	100	Yes	2	360	113.87	3.16	150.3	41.7	No	97
[47]	11	0	2	2	1	360	No	1	1000	228.2	4.38	135.1	13.51	Yes	97.9
Proposed	8	2	2	2	1	100	Yes	4	620	146.4	4.24	151.7	24.4	Yes	97.6

Regarding Fig. 1, equivalent internal resistance of the output filter inductor can be calculated as follows:

$$r_{Lf} = r_{Lf1} + r_{Lf2} \tag{68}$$

Considering Fig. 2, it can be seen that the passing current through output filter is equal to injected current to the grid. So, the RMS value of passing current through the output filter can be obtained as:

$$I_{Lf,rms} = \left[\frac{1}{2\pi}\int_0^{2\pi} \mathrm{I}_{mg}^2 \sin^2(\omega t)\cdot d\omega t\right]^{1/2} = \frac{\mathrm{I}_{mg}}{\sqrt{2}} \tag{69}$$

Therefore, the power losses of the output filter can be calculated as follows:

$$P_{Lf} = r_{Lf} \times \left(\frac{\mathrm{I}_{mg}}{\sqrt{2}}\right)^2 \tag{70}$$

So, the total value of power losses of the used inductors in the proposed inverter can be obtained as:

$$P_{L,total} = P_{L1} + P_{L2} + P_{Lf} \tag{71}$$

In addition, to calculate the power losses of capacitors C_1 and C_2, the following equations should be used:

$$P_{C1} = r_{C1} \times I_{C1,rms}^2 \tag{72}$$

$$P_{C2} = r_{C2} \times I_{C2,rms}^2 \tag{73}$$

So, the total power losses of the capacitors can be calculated as follows:

$$P_{Cap,total} = P_{C1} + P_{C2} \tag{74}$$

where, $\mathrm{I}_{C1,rms}$, and $\mathrm{I}_{C2,rms}$ are the RMS values of passing currents of these capacitors. Also, in the above equations, r_{C1}, and r_{C2} are the internal resistance of the inductors C_1, and C_2, respectively.

V. COMPARISON

In this section, the proposed five-level inverter has been compared with some other similar five-level inverters. This comparison contains the number of implemented power switches, the number of implemented power diodes, the number of inductors and capacitors (except output filter), the number of required input DC sources, input voltage value (V), boosting capability, voltage gain, output power ($\mathrm{P}_{\mathrm{out}}$), total volume ($\mathrm{cm}^3$), power density($\mathrm{W/cm}^3$), total cost ($), cost/$\mathrm{P}_{\mathrm{out}}$ (%), reactive power supporting (RPS), and efficiency (Eff (%)). It should be mentioned that, the power density of the proposed inverter and other compared topologies can be obtained as:

$$\text{Power density}\ (\mathrm{W/cm}^3) = \frac{P_{\mathrm{out}}\,(W)}{\text{Volume}\,(cm^3)} \tag{75}$$

In (75), $\mathrm{P}_{\mathrm{out}}$ and volume are output power and total volume of each inverter. To calculate the total volume of each structure, the volume of each of the energy storage components (capacitors and inductor cores), the volume of semiconductors (switches and diodes), according to the data contained in the datasheet, have been added together numerically. The results of this comparison have been gathered in Table 3. Based on this table, the implemented power switches in [6], [18], [36], [37], [38], [41], and [48] to provide a five-level output voltage is equal to the proposed inverter. However, despite the proposed inverter, these structures need more than one DC input source. Also, despite the proposed inverter, inverters in [33] and [37] do not have the boosting capability. It should be noted that by adding additional boost converters to these structures, it is possible to add the boosting capability to them, but this approach can increase the number of implemented elements. Regarding Table 3, between most of the compared structures the proposed five-level grid-tied inverter has the maximum value of power density. The structures presented in references [18], [35], [45], and [46], unlike the proposed

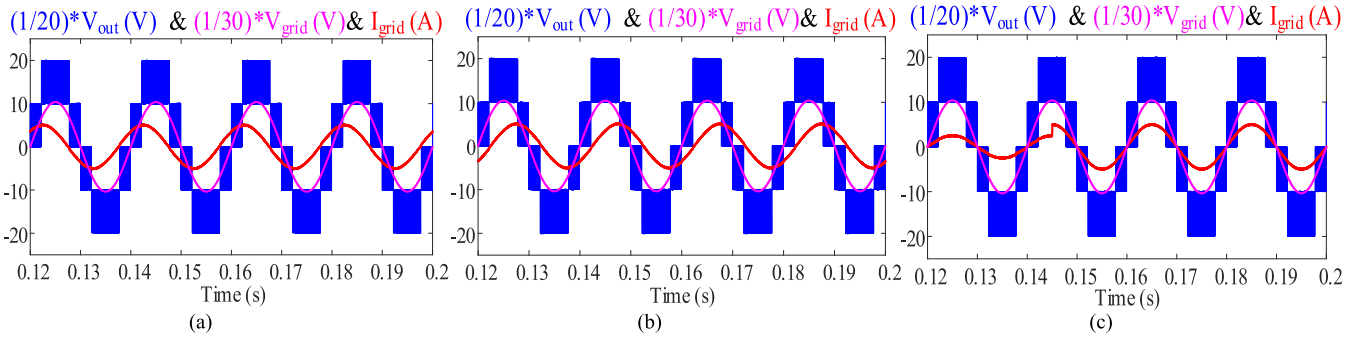


FIGURE 11. Output voltage (V_{out}), grid current (V_{grid}), and injected current into the grid (I_{grid}): (a) at 0.7 leading PF, (b) 0.7 lagging PF, (c) under step change in the active power.

structure, do not have the ability to control reactive power. Also, the cost of constructing the laboratory prototype of the mentioned structures is higher than the proposed inverter. Therefore, the proposed structure is economically viable.

Finally, it can be concluded that among the compared structures, the proposed inverter can provide features such as voltage boosting capability, reactive power control, high power density in a lower volume and cost.

VI. SIMULATION RESULTS TO VERIFY DYNAMIC RESPONSE OF THE PROPOSED INVERTER

In this section, to verify the accurate performance of the proposed five-level grid-tied inverter, the proposed inverter is simulated by using MATLAB/Simulink software. The simulation results are presented in different scenarios of injected active and reactive powers such as different conditions of power factor (PF), and step changes on the output active and reactive powers. Fig. 11 shows the output voltage (V_{out}), grid voltage (V_{grid}), and also injected current to the grid (I_{grid}). Considering Fig. 11(a), it can be seen that the output voltage of the inverter and the grid voltage are in same phase. Also, the phase angle between the grid voltage and the injected current into the grid is 45 degrees. So, Fig. 11(a) illustrated the grid voltage and injected current into the grid at 0.7 leading PF. Also, Fig. 11(c) illustrates the output voltage (V_{out}), grid voltage (V_{grid}) and injected grid current (I_{grid}) at unity power factor and step change on output active power. In Fig. 11(c), output power changes from 0.38 Kw to 0.77 Kw. Regarding Fig. 11(c), it can be verified that the proposed inverter along with its control system can support the step change on output power at unity PF. Fig. 12 (a) illustrates the output voltage, grid voltage and injected current to the grid under step change on phase angle of injected current to the grid. Regarding Fig. 12(a), the amplitude of the apparent power injected into the grid is constant and the step change has occurred in the phase angle of the injected grid current. In the other words, the operation of the inverter has changed from 0.7 leading PF condition to 0.7 lagging PF condition. Also, it can be verified that the proposed grid-tied inverter along with its control technique can support the step change on phase angle of injected current to the grid. Fig. 12(b) indicates the output voltage, grid voltage, and injected current to the grid waveforms under a step change on grid voltage. During this step change, the amplitude of grid voltage changes from 1 pu to 0.7 pu. However, during this step change in the grid voltage amplitude, the grid current maintains its steady state and follows its reference value. Also, Fig. 12(c) shows the output voltage, grid voltage, and injected current to the grid waveforms under a step change on grid voltage. During this step change, the amplitude of grid voltage changes from 0.7 pu to 1 pu. Considering Fig. 12(c), it can be seen that during this step change in the grid voltage amplitude, the grid current maintains its steady state and follows its reference value. Fig. 13 presents the output voltage, grid voltage and injected current to the grid under step change on phase angle of injected current to the grid. Based on Fig. 13(a), the phase angle changes from 0 degrees to 90 degrees. In the other words, the PF changes from 1 to zero with leading state. Under this condition, the proposed inverter absorbs the reactive power from the grid. Considering Fig. 13(b), the PF changes from 1 to zero with lagging state. Regarding this figure, the proposed inverter can only inject reactive power to the grid. Based on obtained simulation results, in addition to correct performance in non-unity power factor and in steady state, the inverter can also handle step change in non-unity PF.

In single-phase inverters, the injected power into the grid or load has a ripple twice the frequency of the grid voltage. In the case of the unit power factor, the instantaneous peak power injected into the grid is twice the average output power. Fig. 14 shows the grid voltage, grid current and injected power into the grid in the proposed inverter. It can be seen that the injected power into the grid has a frequency twice the frequency of the grid voltage. In order to be able to remove the power ripple from the input source, there are two methods:

- Active decoupled dc link
- Passive decoupled dc link.

In the active decoupled dc-link method, a separate dc-dc converter is needed to remove the power ripple from the input source [48], [49].

VII. EXPERIMENTAL RESULTS

In this section, in order to prove the theoretical analysis and the performance of the proposed five-level inverter, a 620 W laboratory prototype of this inverter has been assembled

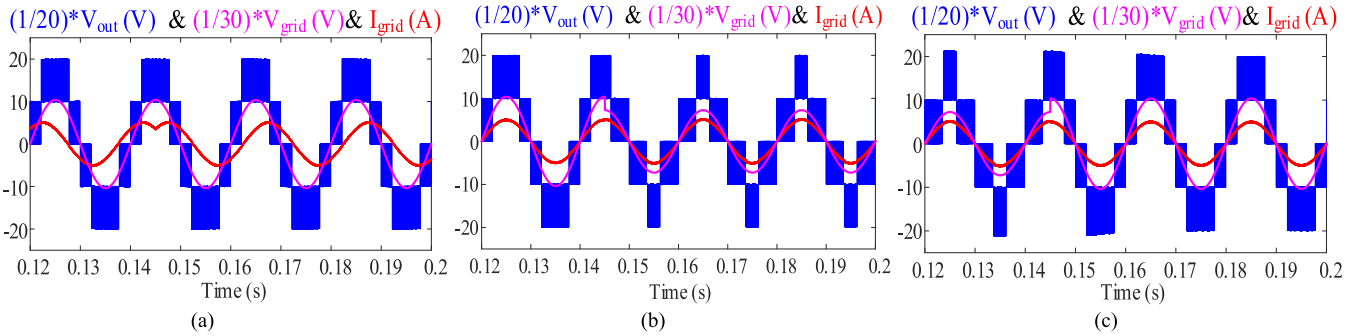


FIGURE 12. Output voltage (V_{out}), grid current (V_{grid}), and injected current into the grid (I_{grid}): (a) under step change on phase angle of injected current to the grid, (b) step change on V_{grid} from 1 pu to 0.7 pu, (c) step change on V_{grid} from 0.7 pu to 1 pu.

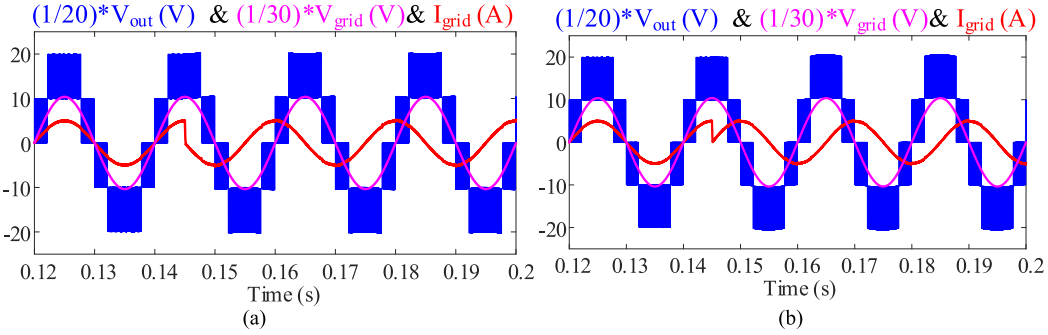


FIGURE 13. Output voltage (V_{out}), grid current (V_{grid}), and injected current into the grid (I_{grid}) under step change on phase angel of the injected current to the grid: (a) step change from PF = 1 to PF = 0 with leading state, (b) step change from PF = 1 to PF = 0 with lagging state.

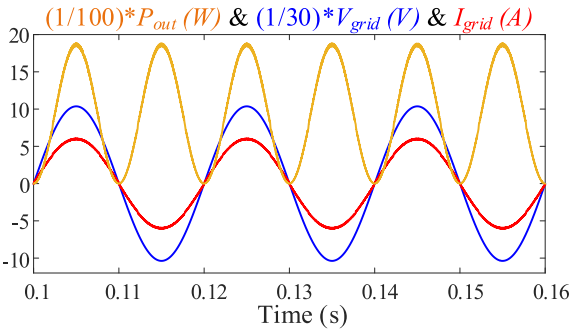
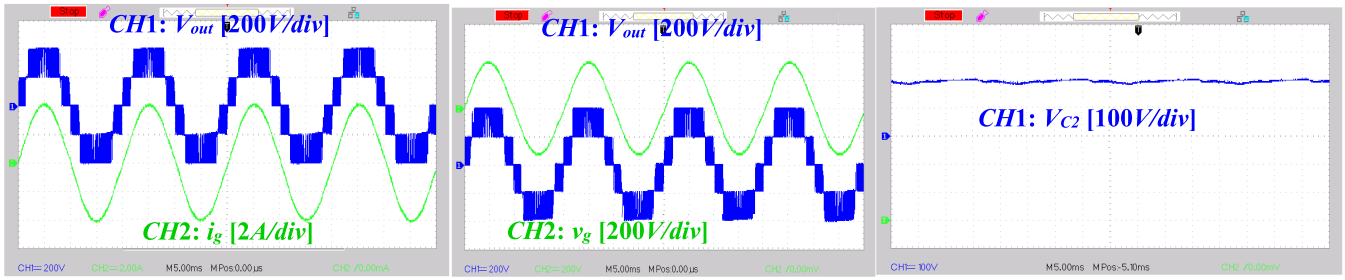


FIGURE 14. Grid voltage, grid current and injected power to the grid with double line frequency ripple.

TABLE 4. List of the implemented components and required descriptions of experimental prototype.

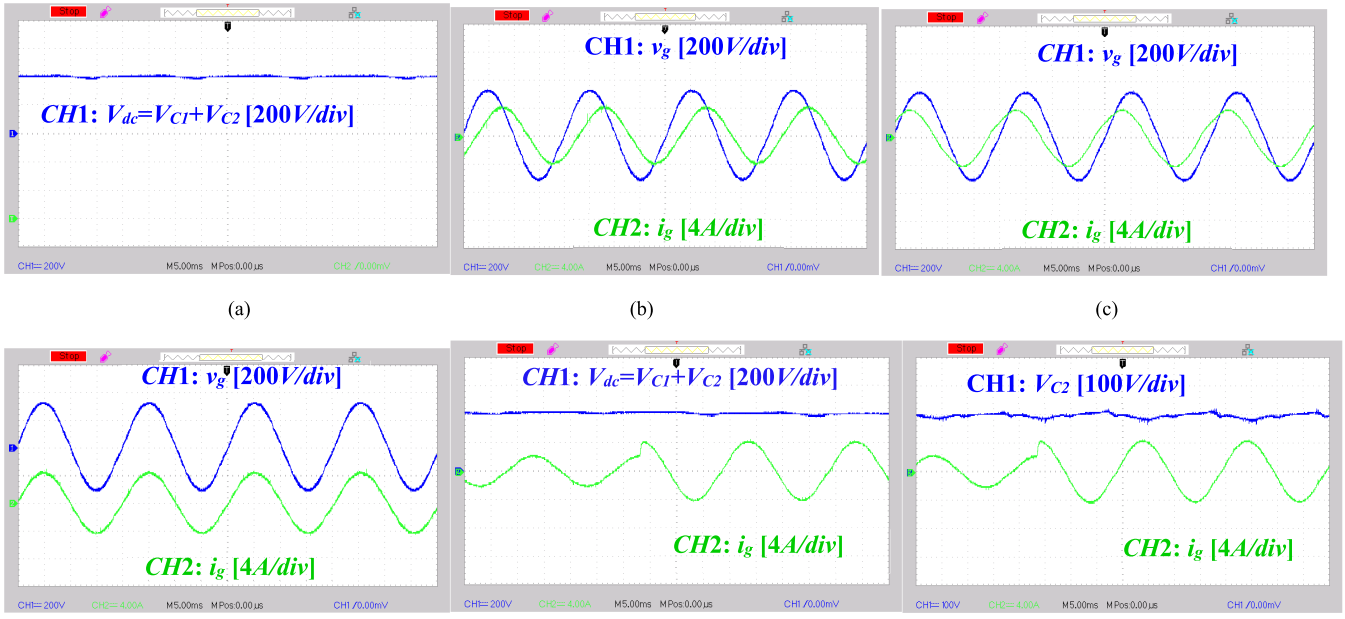
Circuit Element	Type	Explanation
S_1, S_2 S_3, S_4, S_5, S_6	IPW65R041CFD	650 V/47 A
Gate Driver	TLP 250	IC
Power Diode	C3D10060A	600 V/30 A
Current transducer	LA55P	Hall effect
Sampling time	25µs	-
Microcontroller	Beagle Bone Black	ARM
Grid frequency	50Hz	-
C_1 & C_2	Electrolytic	1000μF-250 V
L_1 & L_2	Ferrite Core	100 μH
L_{f1}=L_{f2}	Ferrite Core	1.4 mH

and its experimental results with the local grid have been extracted. In this prototype, the input power supply is 100 V and ARM microprocessor has been implemented to apply the PCC method. The values of the implemented parameter have been presented in Table 4. The output voltage of the inverter which is a Five-level voltage waveform with the sinusoidal injected grid current have been illustrated in Fig. 15(a). Based on Fig. 15(a), the proposed inverter is capable of tracking the reference current by the output inductor. The grid voltage waveform (50Hz) and the output voltage of the proposed inverter have been shown in Fig. 15(b). Considering Fig. 15(b), it can be concluded that output voltage of the inverter is properly synchronized with local grid voltage. As a result, Fig. 15(b) proves the proper performance of the proposed inverter with the designed PCC method. In the proposed structure, the DC link voltage is controlled based on the output voltage pick value. The voltage waveforms of the capacitor C_2 and DC link have been illustrated in Figs. 15 (c) and 16(a), respectively. Based on these figures,



(a) (b) (c)

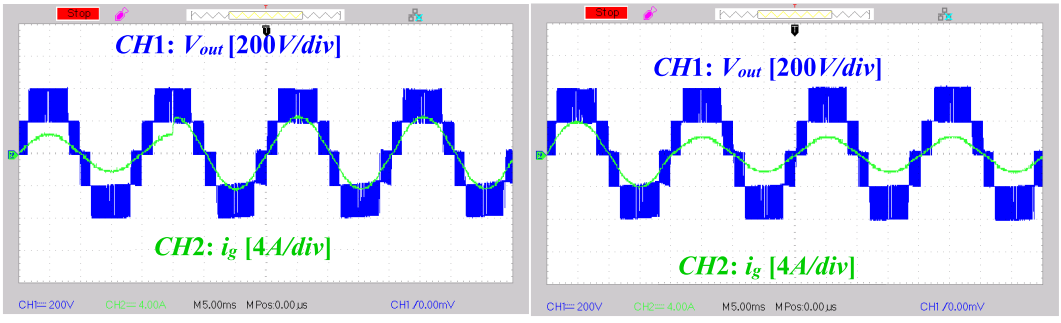
FIGURE 15. Experimental results: (a) five-level output voltage waveform (200V/div) with injected grid current (2A/div) (b) five-level output voltage waveform (200V/div) with the local grid voltage (200V/div), (c) voltage of capacitor C_2 (100 V /*div*).



(a) (b) (c)

(d) (e) (f)

FIGURE 16. Experimental results: (a) voltage of DC link (V_{dc} =V_{C1}+ V_{C2}) (200V/div), Grid voltage waveform and the injected current to local grid: (b) grid voltage (200V/div) and injected grid current (4A/div) under lagging PF (c) grid voltage (200V/div) and injected grid current (4A/div) under leading PF (d)grid voltage (200V/div) and injected grid current (4A/div) under unity PF, Dynamic performance of the proposed inverter under a step change in the amplitude of reference power (P_{ref}): (e) voltage waveform of DC-link, (f) voltage across capacitor C_2.



(a) (b)

FIGURE 17. Dynamic performance of the proposed inverter under a step change in the amplitude of reference power (P_{ref}): (a) Output voltage (200 V/div) and injected current (4 A/div); (b) Output voltage (200 V/div) and injected current (4 A/div).

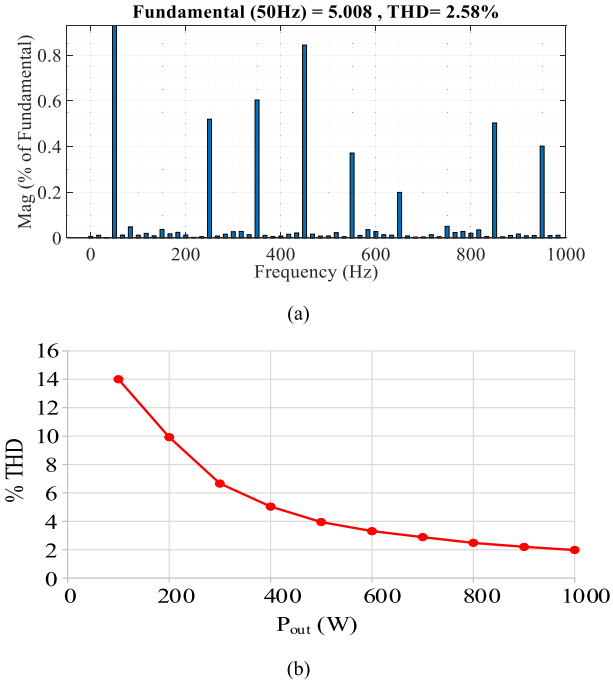


FIGURE 18. (a) Harmonic spectrum of the injected grid current, (b) THD of the grid current with the inverter operating at different power.

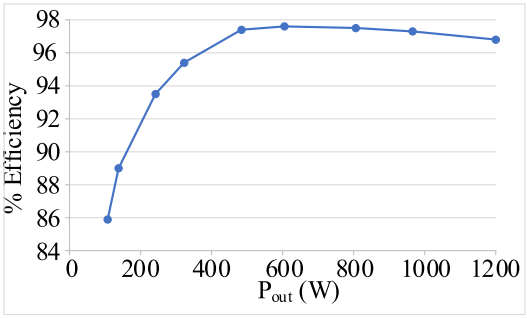


FIGURE 19. The efficiency curve of the proposed inverter working over the entire load range.

the voltage of capacitor C_2 is equal to 200V which is the half of the output voltage pick value. The capacitors voltages have been controlled and their values have been regulated based on the output voltage pick value. Based on the measured input and output powers of the inverter, the efficiency of the inverter part is 97.6%. As mentioned, the performance of the proposed inverter has been tested with the local grid. As a result, the proposed inverter can support the reactive power.

To prove this claim, the grid voltage and the injected grid current with different power factors including lagging, leading, and unit have been illustrated in Figs. 16(b)-16(d), respectively. These figures prove the capability of the proposed inverter with PCC method in generating sinusoidal injected current with different conditions of power factor. In order to investigate the dynamic response of the proposed inverter, step changes of the reference value of output power (P_{ref}) have been applied. In order to investigate the dynamic response of the proposed inverter, step changes of the reference value of output power (P_{ref}) have been applied. The experimental results of DC-link voltage and voltage of capacitor C_2, under the mentioned step change are illustrated in Figs. 16(e) and (f), respectively. Considering these figures, the step change of the $P_{ref}$is a change from 310 W to 620 W. Based on Figs. 16(e) and (f), the steady state voltage value of the DC-link and capacitor C_2, are 400 V and 200 V, respectively. The output voltage and injected grid current under the step change are presented in Fig. 17(a). Based on this figure, the step change of the P_{ref} is a change from 310 W to 620 W. The output voltage along with injected current to the grid under a step change of P_{ref} from 620 W to 310 W is shown in Fig. 17(b). Based on the obtained results under the step change condition, it can be concluded that the proposed inverter has a good dynamic response under a step change. In addition, to investigate the total harmonic distortion (THD) grid current, the harmonic spectrum of the injected current to the grid is obtained by using MATLAB/Simulink software and illustrated in Fig. 18(a). Regarding Fig. 18(a), it can be seen that the THD of grid current is around 2.58 %. Based on IEC 61000-3-2 and IEEE 1547.2-2008 standards the limit of THD of injected current to the grid is less than 5%. Therefore, the proposed inverter can pass these mentioned standards. Also, Fig. 18(b) illustrates the THD of the injected current to the grid at the different output power of the inverter. Considering this figure, it can be seen that the THD of the grid current at 620 W output power is 2.58%. Also, paying attention to this figure, it can be seen that by increasing the generated output power of the inverter, the THD value of injected current to the grid decreases so, the quality of the injected power to the grid increases. Finally, the measured efficiency curve of the proposed inverter at different output powers (100 W∼1200 W) is shown in Fig. 19. Considering Fig. 19, the maximum efficiency for the proposed inverter at 600 W is around 97.8%. Also, the efficiency of the proposed topology at 620 W is around 97.6 %.

VIII. CONCLUSION

In this paper, a five-level boost inverter with single DC source has been proposed. In the DC side of the proposed structure, a DC-DC boost converter has been implemented to transfer the required DC voltage from the single input DC source to the capacitors C_1 and C_2. In this structure, the implemented PCC method to derive the switching pattern has been explained. In addition, design of the implemented components and power losses analysis have been presented. The performance of the proposed inverter in terms of different parameters have been compared to similar structures. Furthermore, in order to verify the claimed advantages of the proposed structure, a laboratory prototype of the proposed structure has been tested with the local grid. Both the injected active and reactive powers have been controlled based on the PCC method.

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MILAD GHAVIPANJEH MARANGALU was born in Urmia, Iran, in 1992. He received the B.Sc. and M.Sc. degrees in power electrical engineering from Urmia University, Urmia, in 2014 and 2018, respectively. He has been a Visiting Researcher with the Department of Electrical Engineering and Mechatronics, Tallinn University of Technology, Tallinn, Estonia. He is currently a research assistant of power electronics. He has authored and coauthored 26 journals and conference papers. His current research interests include multilevel inverter, grid-tied photovoltaic inverter, high-step-up power electronic converters, control system of the multilevel inverter, and renewable energy systems.

NASER VOSOUGHI KURDKANDI (Member, IEEE) was born in Bostanabad, East Azerbaijan, Iran, in 1989. He received the B.Sc. degree in electrical engineering from Islamic Azad University, South Tehran Branch, Tehran, Iran, in 2011, and the M.Sc. and Ph.D. degrees in electrical engineering and power electronics from the University of Tabriz, Tabriz, Iran, in 2014 and 2019, respectively. From 2019 to 2020, he was a Postdoctoral Researcher with the University of Tabriz. In 2020, he joined the Tallinn University of Technology, Tallinn, Estonia, as a Postdoctoral Researcher. He has been a Postdoctoral Researcher with San Diego State University, since 2022. His current research interests include multilevel inverters, grid-connected PV inverters, DC–DC switched-capacitor and switched-inductor converters, fast charge station for electric vehicles, battery-based energy storage systems, and induction motor drives.

PEYMAN ALAVI was born in Urmia, Iran, in 1994. He received the B.Sc. degree in power electrical engineering from Shahid Beheshti University, Tehran, Iran, in 2016, and the M.Sc. degree in power electronics from the Department of Electrical and Computer Engineering, University of Tabriz, in 2019. His research interests include soft-switching methods, high-step-up power electronic converters, and designing and controlling power electronic converters.

SAEIDEH KHADEM (Member, IEEE) was born in Tabriz, Iran, in 1987. She received the B.Sc. and M.Sc. degrees in electrical engineering from the University of Tabriz, Tabriz, in 2013 and 2015, respectively. She is currently pursuing the Ph.D. degree in electrical engineering and industrial applied mathematics with California State University Long Beach, Long Beach, CA, USA. She is a Senior Advanced Electrical Engineer with Honeywell. Her research interests include power electronics, PV inverters, DC–DC converters, electric vehicle motor and controller design, power management, and model predictive control.

HADI TARZAMNI (Student Member, IEEE) was born in Tabriz, Iran, in 1992. He received the B.Sc. and M.Sc. degrees (Hons.) in power electrical engineering from the Faculty of Electrical and Computer Engineering, University of Tabriz, Tabriz, in 2014 and 2016, respectively. He is currently pursuing the dual Ph.D. degree in power electronics engineering with the School of Electrical Engineering, Sharif University of Technology, Tehran, Iran, and the Department of Electrical Engineering and Automation, Aalto University, Espoo, Finland. Since January 2021, he has been a Researcher with the Department of Electrical Engineering and Automation and the Department of Electronics and Nanoengineering, Aalto University. He has authored and coauthored more than 35 journals and conference papers. He also holds six patents in the area of power electronics. His research interests include power electronic converters analysis and design, DC–DC and DC–AC converters, high-step-up power conversion, soft-switching and resonant converters, and reliability analysis. He was a recipient of the Best Paper Award at the 10th International Power Electronics, Drive Systems and Technologies Conference (PEDSTC), in 2019. He has been awarded a three-year Aalto ELEC Doctoral School Grant, in 2021, and a Jenny and Antti Wihuri Foundation Grant, in 2022.

ALI MEHRIZI-SANI (Senior Member, IEEE) received the Ph.D. degree in electrical engineering from the University of Toronto, Toronto, ON, Canada, in 2011. He is currently an Associate Professor with Virginia Tech, Blacksburg, VA, USA. Previously, he was an Associate Professor with Washington State University, Pullman, WA, USA, and a Visiting Professor with the Graz University of Technology (TU Graz), Graz, Austria. From 2007 to 2011, he was a Connaught Scholar with the University of Toronto. His research interests include the power system applications of power electronics and the integration of renewable energy resources. He was a recipient of the 2018 IEEE PES Outstanding Young Engineer Award, the 2018 ASEE PNW Outstanding Teaching Award, the 2017 IEEE Mac E. Van Valkenburg Early Career Teaching Award, the 2017 WSU EECS Early Career Excellence in Research, the 2016 WSU VCEA Reid Miller Excellence in Teaching Award, the 2011 NSERC Postdoctoral Fellowship, and the 2007 Dennis Woodford Prize, for his M.Sc. thesis. He is an Editor of IEEE TRANSACTIONS ON POWER SYSTEMS, IEEE TRANSACTIONS ON ENERGY CONVERSION, and IEEE POWER ENGINEERING LETTERS.