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RESEARCH ARTICLE

Study on Distributed Power-Collection and Cascaded Boosting-Voltage Topology and Strategy for Offshore DC Station

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ABSTRACT Different from traditional concentrated power-collection and boosting-voltage (CPCB) topology adopted by HVDC station, this paper adopts a distributed power-collection and cascaded boosting-voltage (DPCB) topology for offshore DC station to collect DC power and boost DC voltage, which consists of multiple cascaded single active bridges (SABs). It has merits of strong DC-voltage boosting ability, low design difficulty and cost, and low system error rate. Three aspects are studied as follows. First, DPCB topology with its circuit equations is deduced step by step, and its operational mechanism is analysed under phase-shifting control method further. Second, PI control strategy is designed based on system small signal model, and system performance is analyzed by Bode diagram. Third, fault tolerance strategy with predicted power ratio is designed to keep DPCB station from breakdown when some SABs and generators are out of order, and enormous power difference occurs due to the factors of wind turbine location and windward. Finally, the feasibility and effectiveness of designed DPCB station with its strategy are verified by experiment results.

INDEX TERMS Distributed power-collection, cascaded boosting-voltage, SAB, fault tolerance, topology.

I. INTRODUCTION

Wind power is an important renewable energy [1], and the installation capacity of offshore wind generation has been increasing rapidly so far. Compared with HVAC, HVDC is more attractive and effective especially for offshore wind farm [2]. This paper mainly focuses on the topology, mechanism and strategy during normal operation and fault for offshore DC converter station.

The traditional concentrated power-collection and boosting-voltage (CPCB) topology is adopted in some AC and DC connected windfarms for offshore DC station.

Some topologies are applied in AC-connected windfarms in [3], [4], [5], [6], and [7]. In [8], a MMC grid-following state-space model is proposed to show clearly converter's dynamics in grid-forming mode. In [9], a small-signal stability model for MMC-Based DC Grids is proposed to obtain optimal values of slope coefficients and smoothing reactors. In [10], modular multilevel converter (MMC) topology is adopted to overcome the withstand voltage of IGBT in Fig. 1, which has merits of modular design and low voltage distortion. In [11], a flexible line commutated converter without AC filter is proposed to reduce DC station construction and filter loss. In [12], a hybrid DC converter that consists of diode rectifier and paralleled MMC is proposed to improve startup ability and performance. However, MMC has a complex structure with many submodules (SMs) of half-bridge or H-bridge, which needs numerous IGBTs and high system cost. Besides, power transformer is inevitable to boost voltage with big volume and weight, which does not benefit in construction and maintenance of large-scale offshore station.

Some topologies are mentioned in DC-connected offshore windfarms. Dual active bridge (DAB) is an important and basic converter, which is widely applied in medium-voltage DC converter, due to its merits of galvanic isolation and bidirectional power flow [13], [14], [15], [16], [17]. In [18],

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a multi-port DC-DC converter topology that consists of MMC and cascaded H-bridge is proposed for MVDC to improve HV bearing capacity and system reliability. In [19], an ISOP hybrid conversion topology based on resonant converters and DAB is proposed to reduce complexity of communication and control. In [20], a modified DAB dc/dc converter is proposed, which compensates reactive power by AC-sides capacitors to mitigate current stresses and losses. In [21], a DAB converter with auxiliary half-bridge circuit is proposed to achieve wide voltage gain. In [22], a DPS control with bidirectional inner phase shifts for DAB is developed to reduce the current surge in high-frequency transformer and stabilize output power. In [23], a multistring step-up resonant converter topology applied in MVDC grid is proposed to reduce switch voltage stress and loss. In [24], impulse commutated three-phase push–pull topology is proposed to enhance performance and efficiency of converter and reduce system cost. However, the mentioned above generator converter systems with high-frequency transformer are not suitable for offshore DC station to convert large-scale windfarm energy.

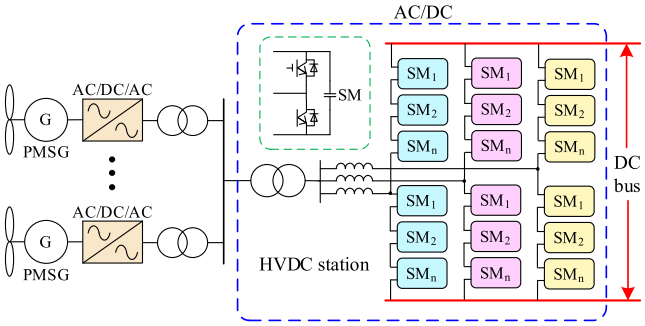

FIGURE 1. CPCB topology structure.

Besides, some fault tolerance strategies are broadly developed for MMC and DAB to make system operate safely in [25], [26], [27], [28], and [29], for their submodular faults might make the whole system break down. In [25], A hybrid series converter topology is proposed for HVDC that contains of a parallel and a series chain link per phase, to gain wide operation range and DC fault-tolerant capability. In [26], parallel multiple submodule topology is proposed to make MMC have large current operation ability and filtering effect on high frequency harmonics. In [27], system fault-tolerant configuration and fault detection and localization technique are proposed to improve system robust and fast response for both submodule and sensor faults of MMC. In [28], an inside capacitor-energy-storage fault tolerance method is proposed to eliminate DC fault current and maintain MMC stability. In [29], a ''primary-side lower power secondary-side bypass arm'' fault-tolerant method for DAB is proposed to improve system load-carrying ability after fault. In [30], a fault-tolerant DAB converter is proposed by reconfiguring central-tapped transformer and symmetrical auxiliary inductors to improve system reliability. In [31], an isolated modular multilevel DC-DC converter based on current-fed DAB is proposed to improve the ability of DC fault ride-though. However, the mentioned above fault tolerance schemes mainly depends on their bypass submodule or its redundant submodule in the MMC and DAB topology structure, which increases structure complexity and system cost.

Single active bridge (SAB) has the merits of no cycle-power and lower cost compared with DAB. Its topology and control strategy are mentioned in [32], [33], [34], and [35]. In [32], the series connection topology of SAB is proposed to collect DC power for wind farm, however, questions about its operation mechanism, power difference between SABs and fault tolerance do not be analyzed in detail. In [33], a fully modular control strategy is proposed to improve system reliability and achieve full modular design. In [34], an indirect I^2SOP DC-DC full-bridge converter system is proposed which adopts asymmetric pulse width modulation to reduce switch voltage stress and filter design difficulty. In [35], an ISOP converter system is proposed to achieve naturally sharing of input voltage and output current.

In this paper, different from traditional CPCB topology in HVDC station, the distributed power-collection and cascaded boosting-voltage (DPCB) topology is adopted for offshore DC converter station, and main contributions are as follows.

1) Structure and merits of DPCB is introduced in detail, and its operation mechanism is clearly analyzed under phase shifting control.
2) In order to make system operate stably, small signal model is built, and according to the model PI controllers are designed. In addition, system performance is analyzed based on Bode diagram.
3) Predicted power ratio and DC-voltage target adjustment algorithms are proposed to enhance system fault tolerance capacity without extra submodule. Finally, feasibility of adopted topology and strategy is verified by experiment.

And the paper is organized as follows. The system topology and operation analysis are explained in Section II. The system control strategy and fault tolerance are described in Section III. The system experiment is in Section IV. The conclusions are presented in Section V.

II. SYSTEM TOPOLOGY AND OPERATION ANALYSIS

Distributed power-collection and cascaded boosting-voltage scheme is adopted to collect DC power and boost DC voltage for offshore wind farm in Fig. 2, which is different from traditional CPCB scheme in Fig. 1. In this section, the DPCB topology with its merits is presented and compared with CPCB topology in detail. Besides, system equation is deduced and its operation mechanism is analyzed further.

A. SYSTEM TOPOLOGY STRUCTURE

In Fig. 2, the adopted DPCB station consists of multiple SABs with Diode bridge cascaded-connection at secondary-side and noninteractive H-bridges at primary-side, which collects distributed DC energy from wind generator and outputs high-voltage DC energy to DC bus. And SAB consists of

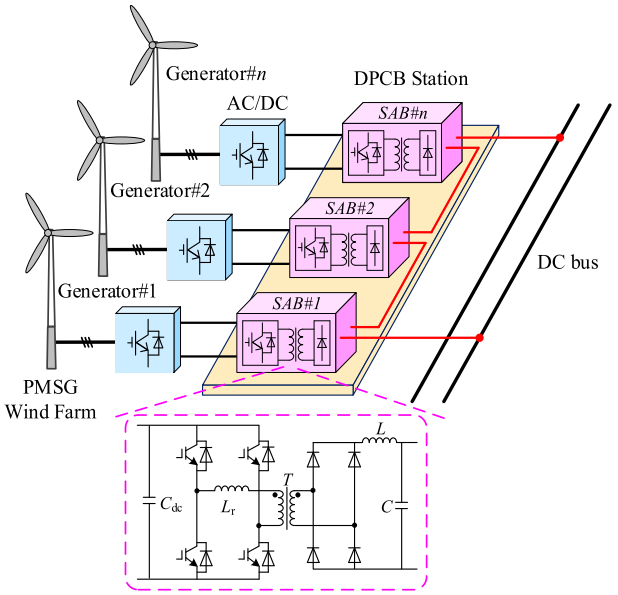

FIGURE 2. The DPCB topology structure.

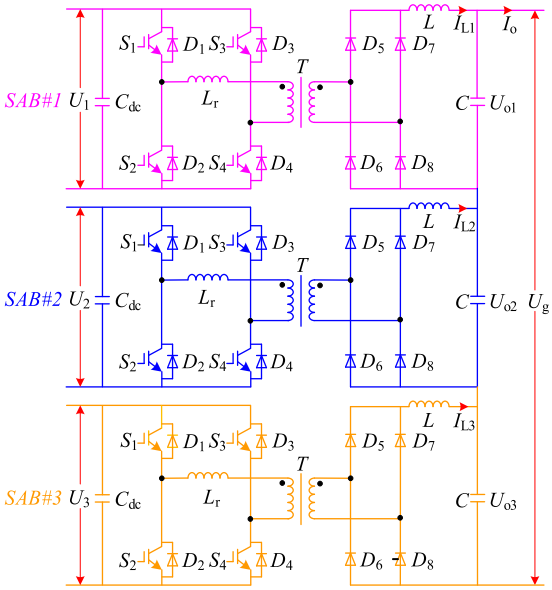

FIGURE 3. DPCB station circuit.

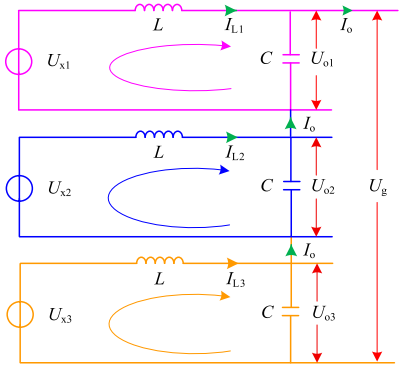

FIGURE 4. Submodular equivalent circuit diagram.

input capacitor (C_{dc}), filter capacitor (C), inductor (L), phase-shifting H-bridge (4-IGBT), high frequency transformer(T), and Diode-bridge (4-D).

Compared with traditional CPCB station, DPCB station might have some merits as follows.

1) Stronger DC-voltage boosting ability

In DPCB station, DC-voltage boosting method mainly depends on increasing the submodule quantity of wind generator and SAB, which is stronger and easier than the method by increasing the quantity of cascaded submodular H-bridges and step-up ratio of power transformer in CPCB station.

2) Lower design difficulty and system cost

SAB is the main system design without consideration of cascaded H-bridge at primary-side, IGBT and Diode withstand voltage, and circulating current restraining, which reduces IGBT and Diode quantities, system design difficulty, and system cost.

3) Lower system error rate

Submodular malfunction would lead to the whole system breakdown, while submodular malfunction in DPCB station would not due to the independent operation of each SAB, indicating that DPCB makes system operate more stable.

B. SYSTEM OPERATION MECHANISM

Taking DPCB station with 3 SABs for example, system operation mechanism is analyzed, and its circuit is shown in Fig. 3.

To analyze system conveniently, system circuit is equivalent in Fig. 4, where H-bridge, transformer and Diode-bridge are equivalent to a controlled voltage source (U_{xi}). Each submodule operates independently, without impact on other submodules except current harmonic.

And U_{xi} is determined by primary-side voltage of transformer (U_i) and fixed transformer ratio (n), which is expressed as

$$U_{xi} = \begin{cases} nU_i & S_1, S_4 \text{ or } S_2, S_3 \text{ on} \\ 0S_1 & \text{or } S_2 \text{or } S_3 \text{ or } S_4 \text{ on} \end{cases} \tag{1}$$

Ignoring system loss, the relationship of power, voltage and current of each SAB is expressed as

$$\begin{cases} P_{i1} = P_{o1} = U_{o1}I_o \\ P_{i2} = P_{o2} = U_{o2}I_o \\ P_{i3} = P_{o3} = U_{o3}I_o \end{cases} \tag{2}$$

$$\begin{cases} P_o = P_{o1} + P_{o2} + P_{o3} \\ U_g = U_{o1} + U_{o2} + U_{o3} \end{cases} \tag{3}$$

$$U_{oi} = \frac{P_{oi}}{\sum_{j=1}^{3} P_{oj}} U_g = \frac{P_{oi}}{P_o} U_g \quad i = 1, 2, 3 \tag{4}$$

where P_{i1}, P_{i2}, P_{i3} and P_{o1}, P_{o2}, P_{o3} are input and output power of each SAB; P_o is total system power; U_{o1}, U_{o2}, and U_{o3} are each SAB output voltage; U_g and I_o are DC bus voltage and current.

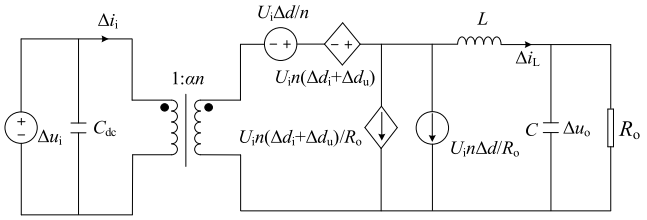

FIGURE 5. DPCB station circuit.

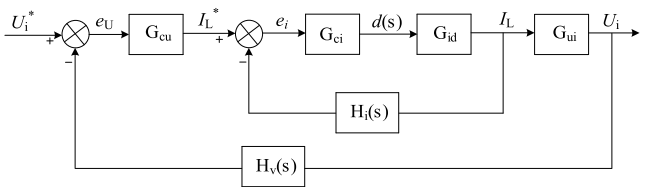

FIGURE 6. Dual cascaded control system diagram.

According to KVL and KCL, each SAB equation is given as

$$\begin{cases} I_{\mathrm{Li}} + C\frac{dU_{oi}}{dt} = I_{\mathrm{o}} \\ U_{\mathrm{xi}} - L\frac{dI_{\mathrm{Li}}}{dt} = U_{\mathrm{oi}} \end{cases} \tag{5}$$

where I_{Li} and U_{oi} are inductor current and output voltage.

From (5), the relationship between I_{Li} and I_{o} is obtained as

$$I_{\mathrm{o}} = I_{\mathrm{Li}} + C\frac{dU_{\mathrm{xi}}}{dt} - CL\frac{d^2I_{Li}}{dt^2} \tag{6}$$

Each average of I_{Li} is equal to I_{o}, and the difference of each I_{Li} depends on its second derivative and the derivative of U_{xi}.

Besides, phase shifting control is adopted to regulate U_{oi} by changing phase shifting angle (φ_{i}). And φ_{i} is the staggered angle between the PWM control signals of two diagonal IGBTs (S1, S4). Phase shifting ratio (α_{i}) is the ratio between φ_{i} and π, and expressed as

$$\alpha_{\mathrm{i}} = \frac{1}{\pi}\varphi_{\mathrm{i}} \tag{7}$$

And relationship of U_{oi}, U_{i} and α_{i} is given as (8). In addition, due to secondary-side duty-cycle loss, phase shifting ratio never reach 100%, and is always limited within its maximum value ($\alpha_{\max}$).

$$U_{\mathrm{oi}} = n\alpha_{\mathrm{i}}U_{\mathrm{i}}\ (\alpha_{\mathrm{i}} < \alpha_{\max}) \tag{8}$$

III. SYSTEM CONTROL STRATEGY AND FAULT TOLERANCE

System control strategy during normal and fault operation are designed to make system operate stably and safely. PI controllers are designed based on small signal model, and system performance is analyzed by Bode diagram. Besides, power difference impact on system operation is analyzed, and fault tolerance algorithm is designed to extend system operational range.

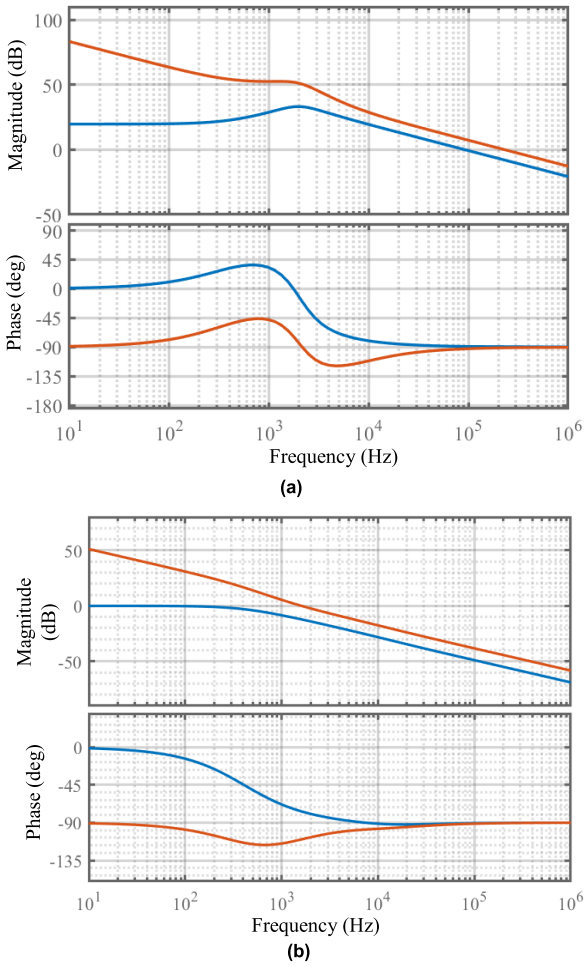

FIGURE 7. (a) Bode plots of current loop. (b) Bode plots of voltage loop.

A. SYSTEM CONTROL STRATEGY

1) SMALL SIGNAL MODELING

In order to analyze system conveniently, system small signal model of SAB is built in Fig. 5, where Δd_i and Δd_{u} are duty disturbances caused by output current and input voltage; Δd, Δi_{L}, Δu_{i} and Δu_{o} are disturbances of duty, inductor current, input voltage, and output voltage respectively. R_{o} is equivalent resistance, and equal to $R_{\mathrm{o}} = U_{\mathrm{i}}^2/P_{\mathrm{i}}$.

Δd_{i} and Δd_{u} are expressed as

$$\begin{cases} \Delta d_{\mathrm{u}} = \frac{4L_{\mathrm{T}}\alpha n^2}{T_{\mathrm{s}}U_{\mathrm{i}}R_{\mathrm{o}}}\Delta u_{\mathrm{i}} \\ \Delta d_{\mathrm{i}} = \frac{4n}{T_{\mathrm{s}}U_{\mathrm{i}}}\Delta i_{\mathrm{L}} \end{cases} \tag{9}$$

Based on KVL and KCL, small signal model is gained as

$$\begin{cases} \alpha n\Delta u_{\mathrm{i}} + nU_{\mathrm{i}}\left(\Delta d + \Delta d_{\mathrm{u}} + \Delta d_{\mathrm{i}}\right) = sL\Delta i_{\mathrm{L}} + \Delta u_{\mathrm{o}} \\ \alpha n\left(\Delta i_{\mathrm{i}} - sC_{\mathrm{dc}}\Delta u_{\mathrm{i}}\right) = \frac{nU_{\mathrm{in}}}{R_{\mathrm{o}}}\left(\Delta d + \Delta d_{\mathrm{u}} + \Delta d_{\mathrm{i}}\right) + \Delta i_{\mathrm{L}} \end{cases} \tag{10}$$

By assuming $\Delta u_i = 0$, transfer function $G_{id}(s)$ between Δd and Δi_L is obtained from (9) and (10) as

$$G_{id}(s) = \frac{\Delta i_L(s)}{\Delta d(s)} = \frac{nU_i}{LCs^2R_o + s\left[L + \frac{4L_rR_on^2C}{T_s}\right] + \frac{4n^2L_r}{T_s} + 1} \quad (11)$$

Similarly, by assuming $\Delta u_o = 0$, transfer function $G_{ui}(s)$ of Δu_{in} and Δi_L is expressed from (9), (10) and (11) as

$$G_{ui}(s) = \frac{\Delta u_i(s)}{\Delta i_L(s)} = \frac{T_sR_o\left(-LCR_os^2 - \frac{4n^2L_rCR_o}{T_s}s - 1\right)}{\alpha nT_sR_o + 4L_r\alpha n^3} \quad (12)$$

2) PI CONTROLLER DESIGN

Cascaded voltage and current PI controllers are designed to gain fast dynamic response and steady-state performance based on small signal analysis, which are expressed as

$$\begin{cases} G_{ci} = K_{ip} + \frac{K_{ii}}{s} \\ G_{cu} = K_{up} + \frac{K_{ui}}{s} \end{cases} \quad (13)$$

where K_{ip}, K_{up} and K_{ii}, K_{ui} are proportion and integral factors.

Besides, the whole system control diagram is showed in Fig. 6, where $H_i(s)$ and $H_v(s)$ are feedback coefficients.

In order to analyze the impact of PI parameters on system performance, the Bode plots are illustrated in Fig. 7 with system parameters in Table 2. The red and blue curves represent system frequency and phase responses with PI controllers or not. Their cutoff frequencies are 2000 and 1500 Hz with phase margins of 80 and 65 dB. System has enough phase margin and their curves cross the line of 0 dB with slope of -20 dB, which makes system have good stability.

B. SYSTEM FAULT TOLERANCE STRATEGY

1) SYSTEM FAULT TOLERANCE ALGORITHM FOR EXCESSIVE SAB POWER DIFFERENCE FAULTS

System fault tolerance algorithm is designed to keep DPCB station from breakdown caused by excessive SAB power difference. Due to the factors of wind turbine location and windward, each SAB power is different and might vary enormously, which makes power ratio exceed its allowance and low DC voltage out of control awfully. To avoid it, max power ratio is limited, and control target adjustment measure is taken as follows.

(1) Max power ratio for each SAB

Each power ratio of SAB (β_i) is defined with its output power and system total power, and the relationship between β_i and α_i, U_i, U_g is expressed from (4) and (7). And the max power ratio (β_{max}) is given when SAB operates at rated power.

$$\begin{cases} \beta_i = \frac{P_{oi}}{P_o} = \frac{n\alpha_iU_i}{U_g} \quad i = 1, 2, 3 \\ \beta_{max} = \frac{n\alpha_{max}U_{iN}}{U_{gN}} \end{cases} \quad (14)$$

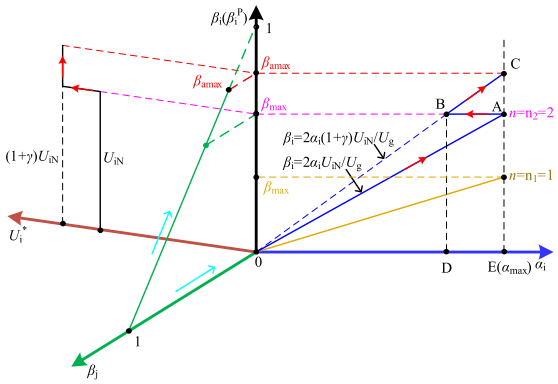

FIGURE 8. Variation curves of n, U_i^*, α_i, β_j with β_i.

where U_{iN} is the rated target of low-side DC voltage, and U_{gN} is rated DC bus voltage.

Besides, the relationship of each SAB power ratio (β_i) and the other power ratio (β_j) is satisfied as

$$\beta_i + \beta_j = 1 \quad (15)$$

β_i increases with the decreasing of β_j, and could not exceed its max value β_{max}, when power difference of SABs occurs due to the factors of wind turbine location and windward. The variation curve of β_i with β_j is illustrated in Fig. 8.

And the relationship between β_i and n and α_i is shown in Fig. 8, where β_i varies with n and α_i, and has its max value β_{max} when α_i reaches α_{max}. And the bigger n is, the bigger β_{max} is, which indicates that system could suffer from more power difference of SABs. When n varies from n_1 to n_2, β_{max} is increased by $(n_2\text{-}n_1)/n_1$.

Since n is determined in the platform construction, β_{max} could not be modified online any more, and could be increased only by the target adjustment (U_i^*) when α_{max} and n are fixed, which is designed as follows.

(2) DC-voltage target adjustment algorithm

In order to increase β_{max} and extend system operational range, DC-voltage target (U_i^*) at low side is adjusted and increased by γ when predicted power ratio (β_i^P) exceeds its max value β_{max}, otherwise it remains its original value in Fig. 8, and is adjusted as

$$\begin{cases} U_i^* = U_{iN}\beta_i^P \le \beta_{max} \\ U_i^* = (1+\gamma)\,U_{iN}\beta_i^P > \beta_{max} \end{cases} \quad (16)$$

From (14) and (16), the adjusted max power ratio (β_{amax}) and the difference ($\Delta\beta_{max}$) of β_{max} and β_{amax} are obtained as

$$\begin{cases} \beta_{amax} = \frac{n(1+\gamma)\alpha_{max}U_{iN}}{U_{gN}} \\ \Delta\beta_{max} = \beta_{amax} - \beta_{max} = \frac{n\gamma\alpha_{max}U_{iN}}{U_{gN}} \end{cases} \quad (17)$$

Taking $n = n_2 = 2$ for example, DC voltage target adjustment procedure is illustrated in Fig. 8. When β_i^P exceeds β_{max}, U_i^* is adjusted from U_{iN} to $(1+\gamma)U_{iN}$, as a result, max power ratio changes from β_{max} to β_{amax}. Accordingly, operational point of α_i varies from A to B instantaneously. Then, β_i changes along B-C line in the range from β_{max} to

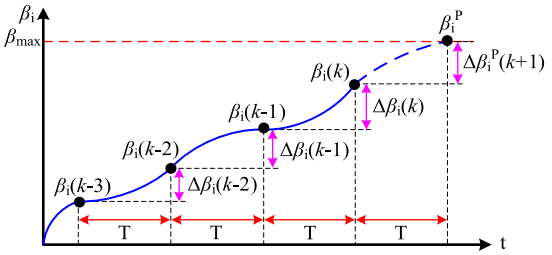

FIGURE 9. Predicted β_i curve.

β_{amax}, when α_i varies from D to E. And values of α_{max}, β_{max} and γ are listed in Table 1.

(3) Predicted power ratio algorithm

In order to prevent system from breakdown beforehand and improve its fault tolerance ability, the predicted power ratio (β_i^P) is vital and calculated by the current power ratio ($\beta_i(k)$) and its variations ($\Delta\beta_i^P(k+1)$) in Fig. 9, which is designed as

$$\begin{aligned}\beta_i^P &= \beta_i(k) + \Delta\beta_i^P(k+1) \\ &= \beta_i(k) + [Q_1\Delta\beta_i(k) + Q_2\Delta\beta_i(k-1) + Q_3\Delta\beta_i(k-2)]\end{aligned} \tag{18}$$

where $\Delta\beta_i(k)$, $\Delta\beta_i(k\text{-}1)$ and $\Delta\beta_i(k\text{-}2)$ are the previous power ratio variations respectively; Q_1, Q_2, Q_3 are weight factors; T is prediction period.

2) SYSTEM SELF-RECOVERY ABILITY ANALYSIS DURING SUBMODULAR (GENERATOR AND SAB) MALFUNCTION

When submodule (generator and SAB) breaks down, its output voltage U_{oi} could decrease with P_i and even to 0 V according to (2) and (4), and the other SAB's output voltages would increase according to (3) with the limitation of (8). Besides, each low-side DC voltage (U_i) could track its target by (13), and DPCB DC station still delivers the power of rest generators to DC bus normally without auxiliary submodules. When submodular malfunction is cleared, its output voltage U_{oi} could increase with P_i, and all system variables could recover to original states by themselves.

C. WHOLE CONTROL STRATEGY

The whole system control block diagram is shown in Fig.10.

IV. SYSTEM EXPERIMENT

In order to verify the feasibility and effectiveness of DPCB topology and control strategy, system experimental platform based on dSPACE is built which consists of 3 SABs, DC-bus system, and emulated DC wind power system in Fig. 11. Emulated DC wind power system consists of DC battery and 3 DC-DC converters controlled by DSP to output variable DC power. Programmable DC power supply is adopted to emulate DC bus system. Besides, the system and control parameters are listed in Table 1 and 2.

Three cases are carried out to verify system mechanism, operation performance and fault tolerance ability.

Case 1: System operational mechanism is verified and analyzed when system operates at rated power.

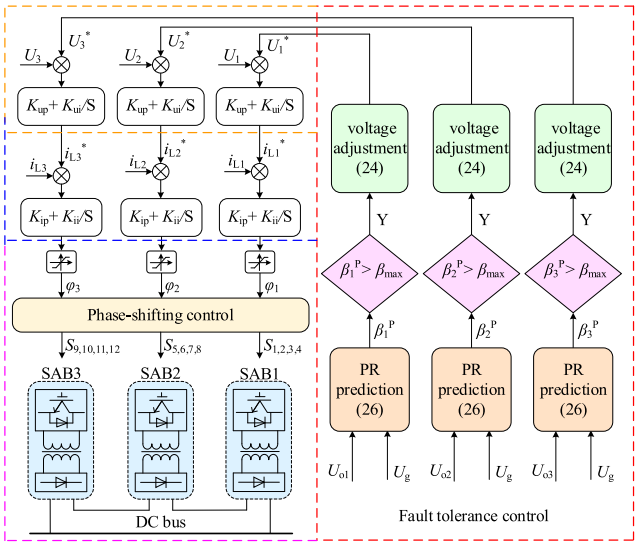

FIGURE 10. Control block diagram of DPCB topology.

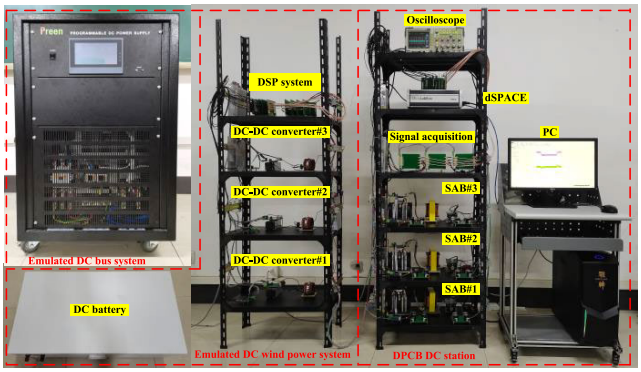

FIGURE 11. System experimental platform.

TABLE 1. System parameters.

Symbol	Quantity	Value
U_{iN}	Rated low DC voltage	50 V
U_{gN}	Rated DC bus voltage	180 V
P_N	SAB rated power	500 W
n	Transformer ratio	2
f_s	Switching frequency	10 kHz
L_r	Leakage reactance	56 μH
L	Filter inductance	153 μH
C	Filter capacitor	1000 μF
C_{dc}	Input capacitor	1000 μF

Case 2: System steady and transient performance is verified and analyzed during input power variation and DC bus voltage fluctuation, which emulates the cases of wind power variation and DC bus disturbance.

Case 3: System fault tolerance ability is verified and analyzed during system malfunction, which emulates the cases of generator malfunction, and excessive SAB power difference faults due to the location and windward of wind turbine.

In addition, system fault parameters are presented in Table 3.

The system experiment results are shown in Fig. 12-16, where the orange, pink, blue, and purple current curves

TABLE 2. System control parameters.

Symbol	Quantity	Value
K_{up}	Voltage loop proportion factor	50
K_{ui}	Voltage loop integral factor	4000
K_{ip}	Current loop proportion factor	100
K_{ii}	Current loop integral factor	7000
α_{max}	Maximum phase shifting ratio	0.95
β_{max}	Maximum power ratio	0.53
β_{amax}	Adjusted maximum power ratio	0.5565
γ	Voltage adjustment factor	0.05
Q_1	Weight factor of prediction equation	0.2
Q_2	Weight factor of prediction equation	0.3
Q_3	Weight factor of prediction equation	0.5
H_v	Voltage feedback coefficient	1/50
H_i	Current feedback coefficient	1/50

represent I_{L1}, I_{L2}, I_{L3} and I_o respectively; The cyan, magenta, and gray voltage curves represent U_{o1}, U_{o2}, and U_{o3} respectively; The red, green, and yellow curves of low DC voltage represent U_1, U_2, and U_3 respectively, and black curve represent voltage target; Besides, the blue, magenta and cyan curves of power ratio represent β_1, β_2 and β_3 in Fig.12-15. The magenta, red and black curves represent β_1, β_2 and β_3 respectively, and the blue, green and cyan curves represent β_1^P, β_2^P and β_3^P in Fig. 16.

A. SYSTEM OPERATIONAL MECHANISM ANALYSIS

Experiment system results are shown in Fig. 12 when system operates at rated power.

In Fig. 12(a), I_{L1}, I_{L2}, I_{L3}, and I_o keep at 7.8 A stably with errors of 0.19 and 0.1 A respectively; U_{o1}, U_{o2}, and U_{o3} keep at 60 V stably with error of 0.003 V; U_1, U_2, and U_3 track their target of 50 V stably with error of about 0.0005 V.

In Fig. 12(b), the variation curves of U_{T1}, I_{Lr1}, I_{L1}, I_{C1} and I_o for SAB#1 in a control period are illustrated. With switch states (S_1, S_4) changing to 1 synchronously, the magenta curve (U_{T1}) is 100 V; The blue and cyan curves (I_{Lr1}, I_{L1}) increase from 0 to 15.9 A, and from 7.6 to 7.96 A; The purple and orange curves (I_{C1}, I_o) decrease from 0.21 to -0.12 A, and from 7.9 to 7.7 A. After 27 μs, S_1 turns off, and U_{T1} drops to 0 V; I_{Lr1} and I_{L1} decrease to 0 and 7.67 A within 23 μs, while I_{C1} and I_o increase to 0.21 and 7.9 A. System variations in next 50 μs are similar to that in previous 50 μs, except the polarities of U_{T1} and I_{Lr1}.

B. SYSTEM STEADY AND TRANSIENT PERFORMANCE ANALYSIS

1) SYSTEM PERFORMANCE ANALYSIS DURING INPUT POWER VARIATION

Experiment system results are shown in Fig. 13 when 3 SAB powers decrease from 525, 500 and 475 W to 500, 475 and 450 W within 0.05s.

With input power decreasing, I_{L1}, I_{L2}, I_{L3}, and I_o decrease from 7.8 A with errors of 0.13, 0.16, 0.2 and 0.11 A, to 7.42 A with errors of 0.14, 0.18, 0.23 and 0.12A in 0.05 s. Their current ripples are consistent with (6) due to different current and voltage of each SAB.

TABLE 3. System fault parameters.

Fault	Max power ratio (β_{max})	DC bus voltage (U_g)	Power ratio (β_i)
DC bus fluctuation	0.53	186 V	0.35
Generator malfunction	0.53	180 V	0.51
Excessive SAB power difference	0.53	180 V	0.538

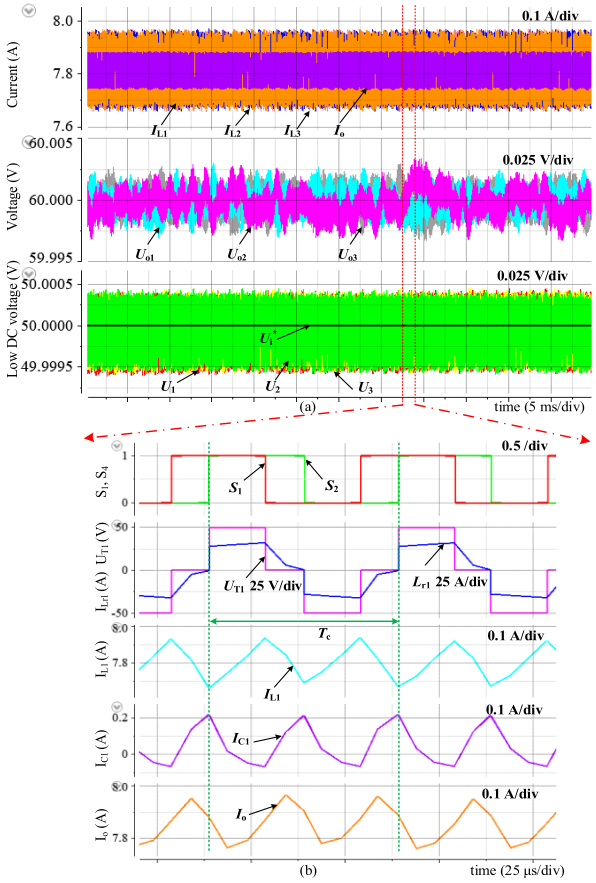

FIGURE 12. The variations of $U_{o1,2,3}$, $I_{L1,2,3}$, I_o and $U_{1,2,3}$, U_{T1}, $S_{1,4}$.

U_{o1}, U_{o2}, and U_{o3} always keep at 63.2, 60, and 56.8 V, which are related each SAB power and consistent with (4). U_1, U_2, and U_3 track their target stably at 50 V with error of 0.0005 V. β_1, β_2, and β_3 keep at 0.351, 0.333, and 0.316, which is consistent with (14).

2) SYSTEM PERFORMANCE ANALYSIS DURING DC BUS FLUCTUATION

Experiment system results are shown in Fig. 14 when DC bus fluctuates from 180 to 189 V, then to 180V in 0.05 s.

When DC bus voltage suddenly increases by 9 V, I_{L1}, I_{L2}, I_{L3}, and I_o decrease from 7.8 to 7.4 A within 0.05 s; U_{o1}, U_{o2}, and U_{o3} increase by 3.2, 3 and 2.8 V, due to their power ratios of 0.351, 0.333 and 0.316.

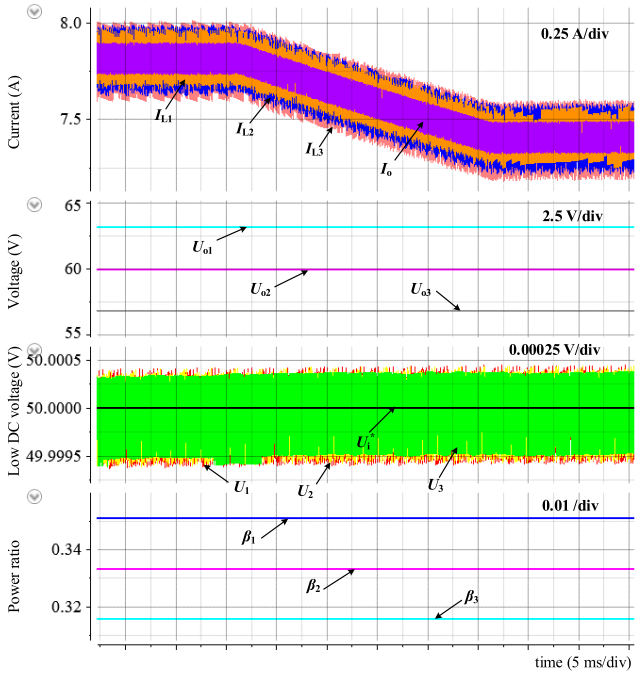

FIGURE 13. The variations of $U_{o1,2,3}$, $I_{L1,2,3}$, I_o and $U_{1,2,3}$ with input power.

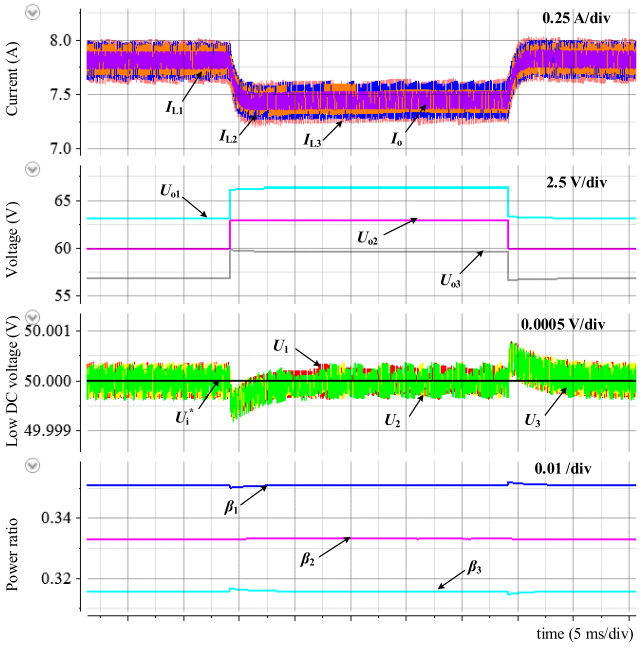

FIGURE 14. The variations of $U_{o1,2,3}$, $I_{L1,2,3}$, I_o and $U_{1,2,3}$ with DC bus voltage.

When DC bus voltage increases to 180 V normally, $I_{L1,2,3}$ and $U_{o1,2,3}$ recover to their original values within 2.5 ms.

Besides, U_1, U_2, and U_3 track their targets and keep stable at 50 V with their max errors of 0.001 V during DC bus fluctuation.

Therefore, system has good steady-state and transient performance, during the variations of input power and DC bus voltage.

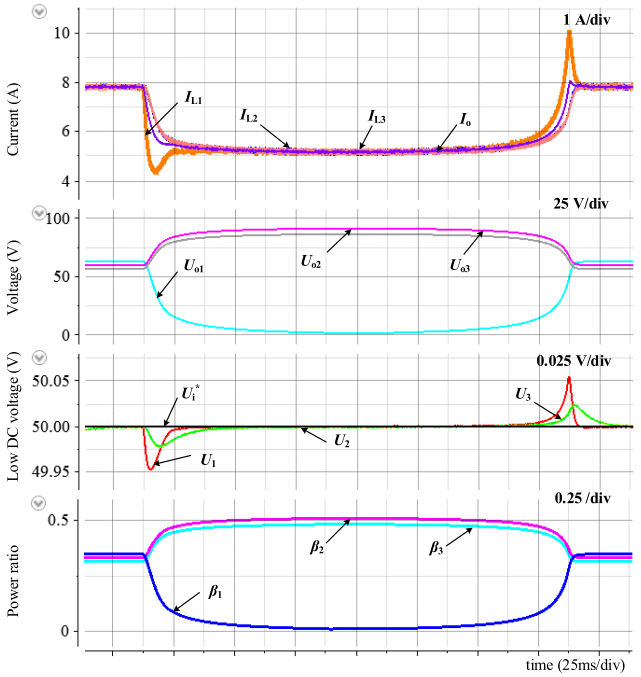

FIGURE 15. The variations of $U_{o1,2,3}$, $I_{L1,2,3}$, I_o and $U_{1,2,3}$ with SAB fault.

C. SYSTEM FAULT TOLERANCE ABILITY ANALYSIS

1) SYSTEM FAULT TOLERANCE ABILITY ANALYSIS FOR GENERATOR MALFUNCTION

Experiment system results are shown in Fig. 15 when generator #1 breaks down and recovers after 0.2 s.

When fault occurs, input power of SAB#1 disappears. U_{o1} decreases from 63 to 0 V, and β_1 varies from 0.351 to 0. However, its low-sides DC voltage (U_1) still tracks its target of 50 V stably. And I_{L1}, I_{L2}, I_{L3}, and I_o decrease gradually from 7.8 to 5.2 A within 0.15 s; U_{o2} and U_{o3} increase from 60 to 91.5 V, and from 57 to 88.5 V; Accordingly, β_2, and β_3 change from 0.333 to 0.51, and from 0.316 to 0.48 under the limitation β_{max} of 0.53. U_2 and U_3 always track stably their targets of 50 V.

When generator #1 recovers, all system variables also return to its original values within 0.15 s. These results are consistent with previous system self-recovery ability analysis.

Therefore, when system submodule breaks down and recovers, with the max power ratio limitation, the DPCB station operates stably, and still delivers the power of rest generators.

2) SYSTEM FAULT TOLERANCE ABILITY ANALYSIS FOR EXCESSIVE SAB POWER DIFFERENCE FAULTS

Experiment system results are shown in Fig. 16, when SAB#1 power rapidly rises in 0.05 s, and after 0.15 s, SAB#1 power recovers to its original value in 0.05 s.

When SAB#1 power rises rapidly, the other SAB power ratio decreases relatively. β_1^P, β_2^P, and β_3^P change from 0.351, 0.333 and 0.316 to 0.538, 0.235, 0.224, and accord with

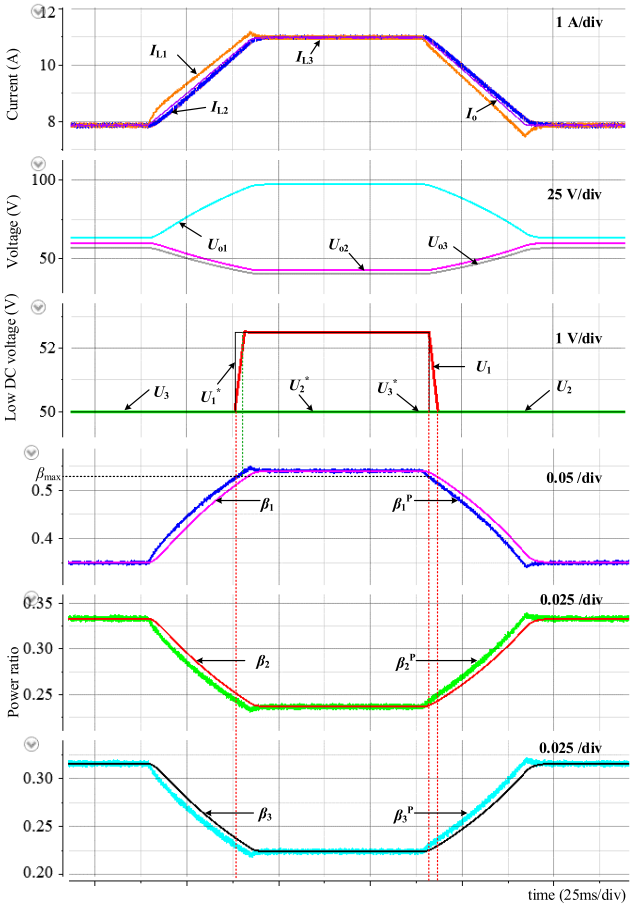

FIGURE 16. The variations of $U_{o1,2,3}$, $I_{L1,2,3}$, I_o and $U_{1,2,3}$ when β_1 exceeds β_{max}.

β_1, β_2, and β_3, which verifies the predicted power ratio algorithm.

When β_1^P exceeds β_{max}, U_1^* varies from 50 to 52.5 V, which is consistent with DC-voltage adjustment algorithm (16). Under the proposed fault tolerance strategy, system still operates stably. I_{L1}, I_{L2}, I_{L3}, and I_o increase from 7.8 to 10.9 A within 0.05 s. U_{o1}, U_{o2}, and U_{o3} change from 63.2, 60 and 56.8 V to 97.1, 42.6 and 40.3 V. U_1, U_2, and U_3 track their targets stably.

Besides, when SAB#1 power recovers to original value, all system state variables ($I_{L1,2,3}$, I_o, $U_{o1,2,3}$, $U_{1,2,3}$, $\beta_{1,2,3}^P$, U_1^*) vary to their original values in 0.005 s.

Therefore, the proposed fault tolerance and predicted power ratio algorithms could make system operate stably and safely.

V. CONCLUSION

Based on above experiment results, following conclusions might be drawn.

1) System operational mechanism is analyzed and verified for the DPCB topology when system operates at the rated power.

2) System steady and transient performance is improved by PI controllers which are designed based on system small signal model, when each input generator power varies and DC bus voltage fluctuates.

3) Proposed fault tolerance strategy makes system operate safely and enhances system fault tolerance ability when sub-modular malfunction and excessive SAB power difference faults occur.

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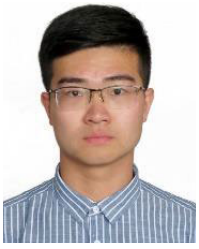

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