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RESEARCH ARTICLE

Three-Phase Hybrid Converter With Simultaneous DC and AC Outputs

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ABSTRACT A novel topology of three-phase hybrid converter (TP-HC) which can supply simultaneously both DC and AC loads is presented. This topology is obtained by adding three switches to T-type three-level inverter. Consequently, this converter can achieve one group of DC/DC power transformation and another three-phase three-level AC voltage outputs with adjustable amplitude. The topology and operation modes of the proposed hybrid converter are introduced. Then the working principle and the available switching states of converter are analyzed, including current path, output phase voltage level and blocking voltage of different switching states. The characteristics of three typical hybrid converters are compared. A strategy combining time-sharing modulation and virtual space vector modulation (VSVPWM) is adopted to realize simultaneous DC and AC outputs of the converter. Then the capacitance voltage balance of the DC link is realized. In order to simplify the modulation strategy, a carrier based on pulse width modulation (CBPWM)strategy is proposed. Then, boost ratio of this converter is analyzed in detail. Finally, the feasibility of the proposed topology and the effectiveness of modulation strategy are verified by simulation and experiment.

INDEX TERMS CBPWM, DC and AC outputs, hybrid converter, three level, time-sharing modulation strategy.

I. INTRODUCTION

Nowadays, with the development and high penetration of technologies such as solar photovoltaic, battery energy storage systems [1], charging stations for electric vehicles and AC/DC microgrids, hybrid AC/DC power systems are more demanded [2]. The research fields including how to realize the flexibility and diversity of AC/DC power supply, converter structure integration, the function expansion of a single converter and the transmission efficiency improvement for converter, have become increasingly hot topic.

The existing hybrid AC/DC converters are usually improved based on the boost DC/DC converters. The switch boost inverter (SBI), proposed in [3], is a hybrid converter topology, which can supply simultaneous single-phase DC and AC loads. However, it has a discontinuous input current and five controlled switches. The continuous input current is obtained in boost derived hybrid converter (BDHC) reported in [4], which is derived from single-switch boost converter by replacing its controlled switch with a voltage-source-inverter bridge network. Although the BDHC has lesser number of components as compared to SBI, it has a low voltage gain [5]. A current-fed source inverter (CFSI) is discussed to overcome the issues mentioned above [6]. The problem of instability in hybrid converter easily occur when load is heavy. The reason for this problem is the presence of a right half-plane zero (RHPZ) in the control-to-dc output voltage transfer function, which results a nonminimum phase system [7]. Then, a minimum phase dual output hybrid converter (DOHC) is proposed in [8], which can operate at a high load current while maintain closed-loop stability. However, it is only capable of supplying single-phase hybrid AC/DC system. In addition, more passive elements are required in DOHC topology.

The hybrid converters mentioned above have standalone AC/DC transmission path. Consequently, the switches suffering from high voltage stress result in an increase of cost

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and switching losses [9]. The converter structure integration and multiplex switches are appropriate ideas to solve this problem. In [10], nine switches converter (NSC) topology is used to generate three-phase AC power and three standalone DC power supply simultaneously. Although the number of switches decreases dramatically, the output phase voltage of NSC has only two levels [11]. Compared to three-level voltage, the harmonics and dv/dt of two-level voltage are high, which limits the improvement of waveform quality and the reduction of passive filters size [12]. T-type three-level converter plays an appropriate role in DC/AC power conversion of hybrid converter, due to less switches and shorter conduction paths than the neutral-point-clamped three-level converter (NPC-TLC).

In the field of renewable energy applications, the DC bus voltage is constantly changing [13], [14]. Therefore, as the energy interface between source and charge, the power electronic converter needs to integrate the function of bidirectional DC/DC voltage adjustment [15]. The integrated converter combines a bidirectional DC/DC converter circuit with a single-phase or three-phase inverter [16]. The idea of multiplexing switches is introduced into the topology construction of hybrid converter in this paper. Low DC voltage utilization rate is a common problem in integrated converter, which limits its application as terminal voltage sources [17]. This problem is mainly caused by the coupling between DC/DC transformation and DC/AC transformation. In order to maintain a certain DC duty ratio, the AC modulation interval cannot occupy the whole switching cycle [18]. With the increase of system level, the redundant voltage will bring greater switching loss and system cost. To solve this problem, an active split source inverter (ASSI) is proposed in [19], which combined with a feasible modulation strategy. ASSI can improve not only the utilization rate of DC voltage, but also the system efficiency. Compared with the two-stage topology, the three-phase switches of the integrated hybrid converter can share the heavy current required by load and reduce the risk of shoot-through [20], [21], [22]. In addition, the application of three-phase interleaved converter can realize three-phase switches phase shift conduction and reduce the current ripple of input DC side [23], [24].

Based on the research results above, a novel hybrid three-level converter is proposed in this paper, with a view to increasing the number of AC outputs levels, lowering voltage stress and integrating functions of dc/ac and dc/dc power conversions. In the case of a single DC power supply, the converter can achieve a set of three-level AC output with adjustable amplitude and three-phase step-down DC with controllable amplitude simultaneously. In the case of three DC power supply, a group of amplitude adjustable three-phase boost three-level AC output is realized. This article is organized as follows. In Section II, the topology structure and working principle of the proposed three-phase hybrid converter are mainly introduced. In Section III, a modulation strategy combining time-sharing modulation idea and virtual space vector modulation is described. In order to avoid the complicated calculation of modulation process, a carrier modulation strategy (CBPWM) based on virtual space vector modulation (VSVPWM) is proposed. The boost ratio of the hybrid converter is discussed in Section IV. Simulation and experiment results are given in Section V. Finally, the conclusion is summarized in Section VI.

II. TOPOLOGY AND OPERATION PRINCIPLE OF HYBRID CONVERTER

A. TOPOLOGY OF HYBRID CONVERTER

As shown in Fig. 1, the proposed hybrid converter has three ports, including two DC ports (U_{dc}, u_{dc}) and an AC port (u_{ac}). The topology of the proposed hybrid three-level converter is shown in Fig. 2. The topology consists of 15 switches and two capacitors (C_1 and C_2) which are connected in series at U_{dc} of the DC port. The three-phase bridge legs of the converter are all composed of 5 insulated gate bipolar transistors (IGBT) $S_{x1} \sim S_{x5}$ and antiparallel coupled diodes, where $x \in \{A,B,C\}$. The converter is regarded as a combination of T-type three-level inverter and bidirectional DC/DC converter.

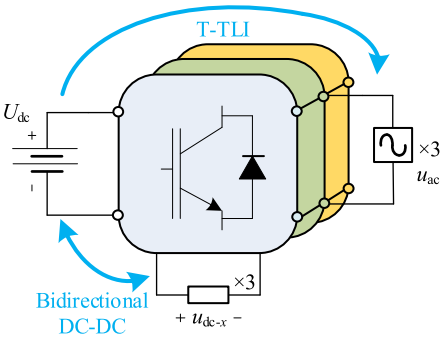

FIGURE 1. Schematic diagram of three-phase hybrid converter.

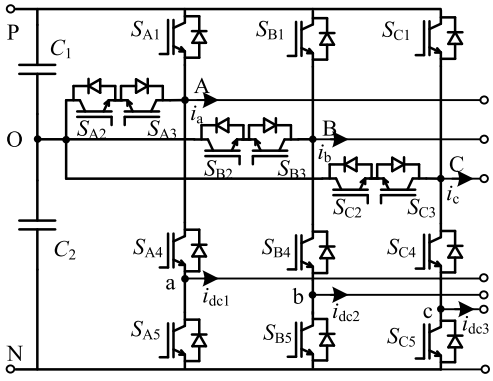

FIGURE 2. Topology of three-phase hybrid converter.

The converter has two operating modes. When the converter operates in mode 1, as is shown in Fig. 3, the DC port (U_{dc}) of the converter is connected to the DC source. Then AC port (u_{ac}) of the converter outputs a set of three-level AC with

adjustable amplitude and DC port (u_{dc}) outputs three-phase step-down DC (u_{dc-A}, u_{dc-B}, u_{dc-C}) respectively. When the converter operates in mode 2, as is shown in Fig. 3, the DC port (u_{dc}) of the converter is connected to the DC source and then voltage rising is completed at the U_{dc} of the DC port. The AC port (u_{ac}) of the converter outputs a set of step-up three-level AC with adjustable frequency and amplitude.

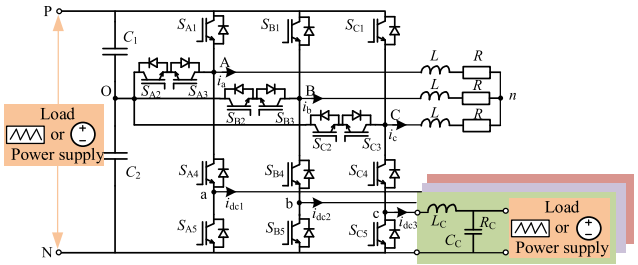

FIGURE 3. Operating mode of three-phase hybrid converter.

B. OPERATING PRINCIPLE

The operating mode 1 of the proposed hybrid three-level converter has four switching states which are respectively depicted in Fig. 4(a)-(d) (phase A as an example).

Switching state 1: Switches S_{A1}, S_{A2} and S_{A5} are in the on state. The AC and DC flow paths are shown in Fig. 4(a). At this time, the phase voltage u_{AO} is $U_{dc}/2$. Inductor L_A, DC load, capacitor C_A and diodes of S_{A3} form a circuit loop. During this process, inductor L_A discharges and the DC port voltage u_{aN} is 0. The blocking voltage of S_{A4} and S_{A3} are U_{dc} and $U_{dc}/2$ respectively.

Switching state 2: Switches S_{A2}, S_{A3} and S_{A5} are in the on state. The AC and DC flow paths are shown in Fig. 4(b). At this time, the phase voltage u_{AO} is 0 and the DC port voltage u_{aN} is 0. The blocking voltage of S_{A1} and S_{A4} are both $U_{dc}/2$.

Switching state 3: Switches S_{A3}, S_{A4} and S_{A5} are in the on state. The AC and DC flow paths are shown in Fig. 4(c). At this time, the phase voltage u_{AO} is -$U_{dc}/2$ and the DC port voltage u_{aN} is 0. The blocking voltage of S_{A1} and S_{A2} are U_{dc} and $U_{dc}/2$ respectively.

Switching state 4: Switches S_{A1}, S_{A2} and S_{A4} are in the on state. As shown in Fig. 4(d), the phase voltage u_{AO} is $U_{dc}/2$ and the DC port voltage u_{aN} is U_{dc}. It is worth noting that the DC circuit loop is changed. and the inductor L_A is charged during this process. The blocking voltage of S_{A3} and S_{A5} is $U_{dc}/2$ and U_{dc} respectively. The relationship between switching states and the port voltage is summarized in Table 1.

Different from operating mode 1, operating mode 2 takes u_{dc} of the DC port as input. As shown in Fig. 5, mode 2 is obtained by replacing the capacitor at u_{dc}port in mode 1 with DC voltage source. The voltage is stepped up at U_{dc} of the DC port and then three-phase three-level boosted voltage is acquired at u_{ac}.

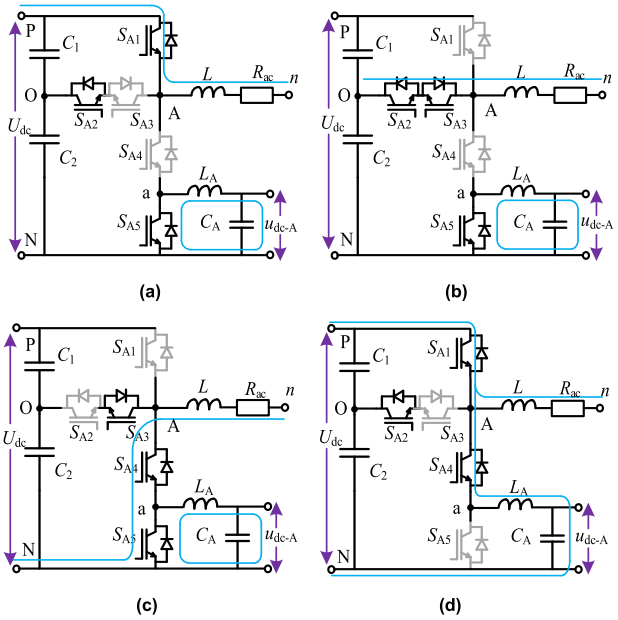

FIGURE 4. Switching state of operating mode 1. (a) $u_{AO} = U_{dc}/2$, $u_{aN} = 0$. (b) $u_{AO} = 0$, $u_{aN} = 0$. (c) $u_{AO} = -U_{dc}/2$, $u_{aN} = 0$. (d) $u_{AO} = U_{dc}/2$, $u_{aN} = U_{dc}$.

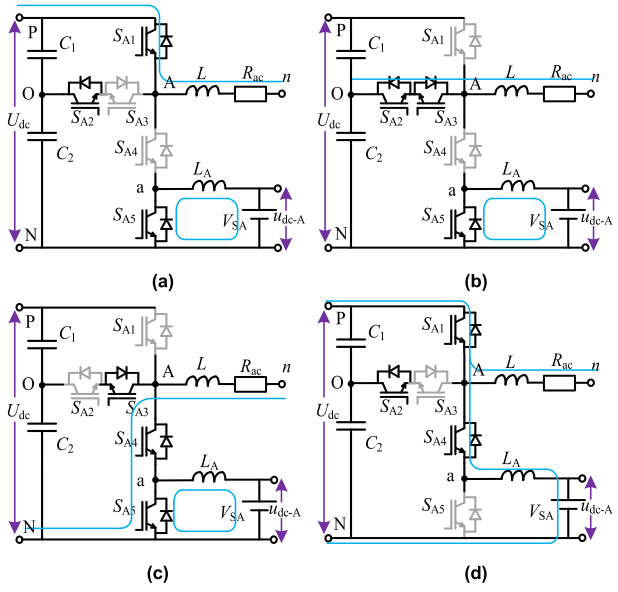

FIGURE 5. Switching state of operating mode 2. (a) $u_{AO} = U_{dc}/2$, $u_{aN} = 0$. (b) $u_{AO} = 0$, $u_{aN} = 0$. (c) $u_{AO} = -U_{dc}/2$, $u_{aN} = 0$. (d) $u_{AO} = U_{dc}/2$, $u_{aN} = U_{dc}$.

In terms of switching voltage stress, switches S_{A1}, S_{A4} and S_{A5} withstand the maximum voltage U_{dc}, and switches S_{A1}, S_{A2}, S_{A3} and S_{A4} suffer from voltage $U_{dc}/2$. The voltage stress of dual-output hybrid converter (DOHC) in [8], cascade boost converter and T-type inverter (CBT) and the proposed TP-HC in this paper are analyzed. Then the analysis

TABLE 1. Relationship between the switching states and the port voltage.

Switching state	S_{x1}	S_{x2}	S_{x3}	S_{x4}	S_{x5}	u_{AO}	u_{aN}
1	ON	ON	OFF	OFF	ON	$U_{dc}/2$	0
2	OFF	ON	ON	OFF	ON	0	0
3	OFF	OFF	ON	ON	ON	$-U_{dc}/2$	0
4	ON	ON	OFF	ON	OFF	$U_{dc}/2$	U_{dc}

results are shown in Table 2. In order to realize three-phase output, more diodes and passive elements are needed to form DOHC topology. Although stable three-phase output and three-level AC voltage can be accomplished by CBT topology, the number of elements required is not least. Among the three typical hybrid converter, the three-phase hybrid converter proposed (TP-HC) in this paper demand the less number of devices that suffer from the bus voltage U_{dc}, which accounts for only 60% of switches in total. The output AC line voltage is three level and the waveform quality is improved.

TABLE 2. Comparison of typical three-phase hybrid converter.

	Tri-Parallel-DOHC [8]	*CBT* [10]	*TP-HC*
Switch No.	12	18	15
Diode No.	3	0	0
Inductor No.	9	3	3
Capacitor No.	12	2	2
Total components No.	36	23	20
Switches blocking U_{dc} No.	12	12	9
AC voltage level	2	3	3

III. MODULATION STRATEGY OF TP-HC

A. VSVPWM STRATEGY BASED ON TIME-SHARING IDEA

A strategy for TP-HC combining time-sharing modulation and virtual space vector modulation is proposed in this paper. The inverter stage and chopper stage of the three-phase hybrid converter operate alternately in one switching cycle to obtain a set of three-phase AC outputs and three sets of DC outputs simultaneously.

Zero vector and large vector have no effect on the balance of neutral point voltage. Therefore, when constructing the virtual space vector, the zero vector and the large vector keep the modulus and direction of the original vector unchanged. Each small vector always comes in pairs, as a positive or negative vector. When the reference voltage vector is synthesized, these two small vectors are equivalent. But they have opposite effects on the neutral point voltage. Hence, this property of small vector is used to reconstruct a new small vector. The new vector needs to satisfy (1). Taking the vector in sector A as an example, the following

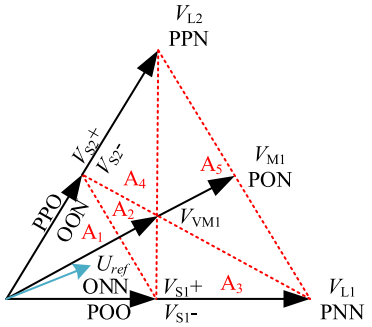

FIGURE 6. Virtual space vector diagram of sector A.

can be obtained:

$$\begin{cases} V_{S1} = (V_{S1+} + V_{S1-})/2 \\ V_{S2} = (V_{S2+} + V_{S2-})/2 \\ V_{VM1} = (V_{S1+} + V_{M1} + V_{S2+})/3 \end{cases} \tag{1}$$

According to (1), the reconstructed small vector is composed of a positive small vector and a negative small vector. The virtual medium vector consists of two small vectors and one medium vector, each accounting for one-third. Set the three-phase reference voltage as

$$\begin{bmatrix} u_{a\text{-ref}}(t) \\ u_{b\text{-ref}}(t) \\ u_{c\text{-ref}}(t) \end{bmatrix} = U_m \cdot \begin{bmatrix} \cos(\omega t + \phi) \\ \cos(\omega t + \phi - 2\pi/3) \\ \cos(\omega t + \phi + 2\pi/3) \end{bmatrix} \tag{2}$$

where, U_m, ω and φ are the amplitude, angular frequency and initial phase of the voltage sinusoidal reference signal respectively. The reference voltage vector of AC output can be expressed as:

$$U_{ref} = \frac{2}{3}\left(u_{a-ref} + u_{b-ref}e^{j\frac{2\pi}{3}} + u_{c-ref}e^{j\frac{4\pi}{3}}\right) \tag{3}$$

Fig. 6 shows the virtual space vector diagram of sector A. The selection method of the fundamental vectors used in synthesizing the reference voltage follows the principle of the nearest three vectors. Taking sub-sector A_1 as an example, V_0, V_{S2} and V_{S3} are selected to synthesize U_{ref}. Expression of the volt-second equilibrium principle is

$$\begin{cases} U_{ref} = V_{S1}d_1 + V_{S2}d_2 + V_0d_3 \\ 1 = d_1 + d_2 + d_3 \end{cases} \tag{4}$$

According to (4), the expression of duty cycle can be solved. Table 3 lists all duty cycle expressions for sector A and d_1, d_2 and d_3 are the corresponding duty cycles of the three effective vectors in each sub-sector respectively. Then, the effective switching time in other vectors is definite.

The parameter above in the inverter stage is obtained, the chopper stage is analyzed as following. The D means duty cycle in chopper stage. It means that during the period of DT_S,

TABLE 3. Duty ratio of sector A_N.

A_n	d_1	d_2	d_3
A_1	$2\sqrt{3}U_{ref}\sin(\pi/3-\theta)/U_{dc}$	$2\sqrt{3}U_{ref}\sin\theta/U_{dc}$	$1-2\sqrt{3}U_{ref}\sin(\pi/3+\theta)/U_{dc}$
A_2	$6U_{ref}\sin(\pi/6+\theta)/U_{dc}-1$	$2-6U_{ref}\cos\theta/U_{dc}$	$-3+6\sqrt{3}U_{ref}\sin(\pi/3+\theta)/U_{dc}$
A_3	$2-6U_{ref}\sin(\pi/6+\theta)/U_{dc}$	$3\sqrt{3}U_{ref}\sin\theta/U_{dc}$	$3U_{ref}\cos\theta/U_{dc}-1$
A_4	$3\sqrt{3}U_{ref}\sin(\pi/3-\theta)/U_{dc}$	$2-6U_{ref}\cos\theta/U_{dc}$	$-1+3U_{ref}\sin(\pi/6+\theta)/U_{dc}$
A_5	$3U_{ref}\cos\theta/U_{dc}-1$	$3U_{ref}\sin(\pi/6+\theta)/U_{dc}-1$	$3-3\sqrt{3}U_{ref}\sin(\pi/3+\theta)/U_{dc}$

TABLE 4. Summary of equations.

	u_{Sx1}	u_{Sx2}	u_{Sx5}
OOOPPP*	$2(1-D)\frac{u_{min}-u_{max}}{U_{dc}}+1-2D$	-1	$1-2D$
NOOOPP*	$2(1-D)\frac{u_{min}-u_{mid}}{U_{dc}}+1-2D$	$2(1-D)\frac{u_{max}-u_{mid}}{U_{dc}}-1$	$1-2D$
NNOOOP*	$1-2D$	$2(1-D)\frac{u_{max}-u_{min}}{U_{dc}}-1$	$1-2D$

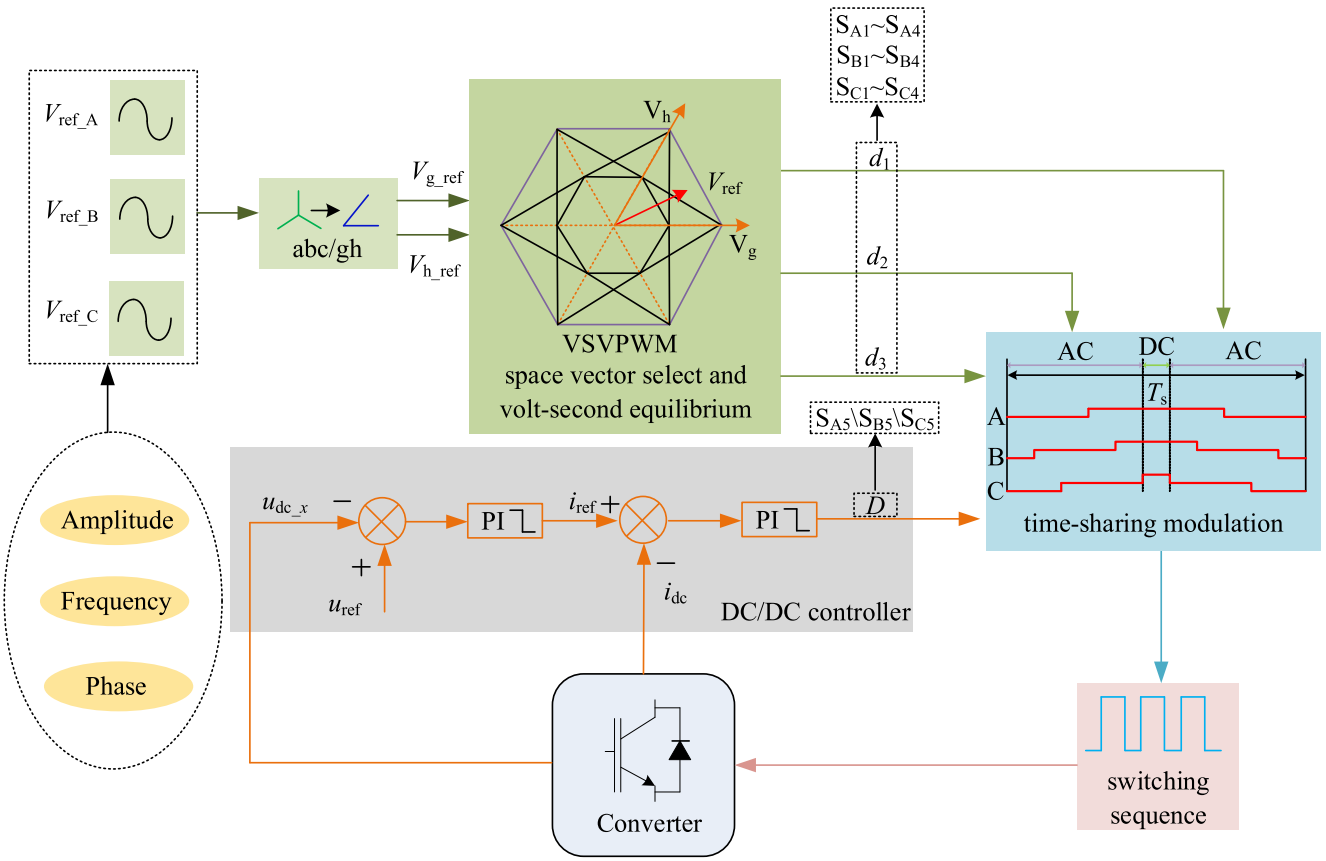

FIGURE 7. The overall control block diagram of the TP-HC.

DC output port in operating mode 1 supplies power to the resistive load through a low-pass filter composed of inductor L_x and capacitor C_x. In operating mode 2, the inductor L_x discharges and plays the role of pumping voltage. D is acquired

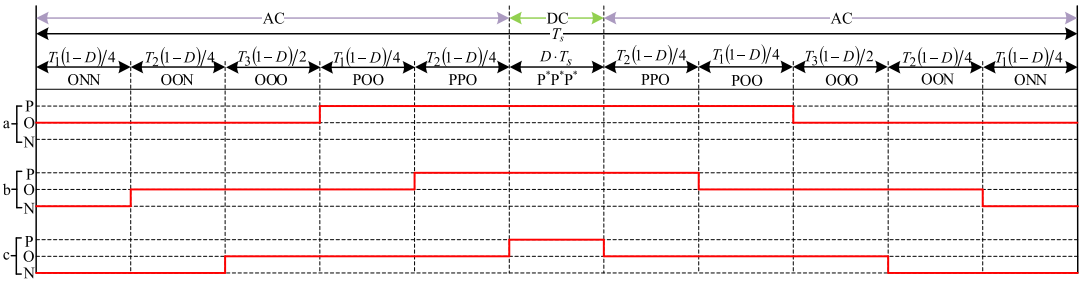

FIGURE 8. Switching sequence and dell time in a switching cycle.

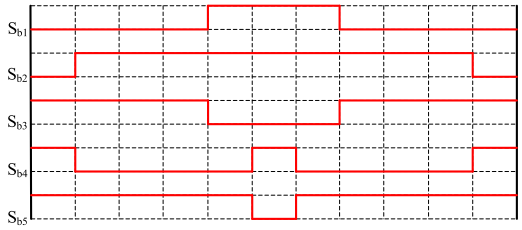

FIGURE 9. Driving signal of switches phase B in a switching cycle.

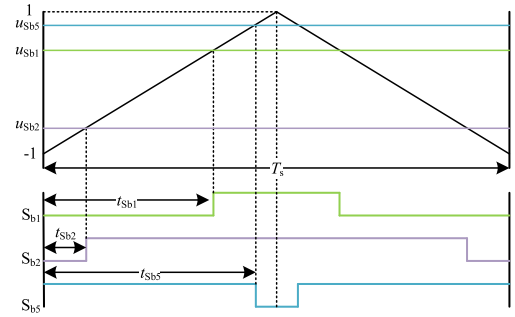

FIGURE 10. Driving signals and modulation waves of phase B.

by DC/DC controller. The voltage and current at DC ports is used to calculate D in DC/DC controller. The overall control diagram is illustrated in Fig. 7. Thus, a set of three-level AC output with adjustable amplitude and three-phase DC with controllable amplitude are acquired simultaneously. The switching state of 15 insulated gate bipolar transistors is determined by the corresponding working state of AC output and DC output.

Modulation index M can be defined as:

$$M = \sqrt{3} \cdot U_{\mathrm{m}} \Big/ U_{\mathrm{dc}} \tag{5}$$

where, U_{m} is the amplitude of AC output reference phase voltage; U_{dc} is the amplitude of DC bus voltage. During the period of DT_{S}, the output voltage at AC port is zero vector and the output voltage $u_{x\mathrm{N}}$at DC port is U_{dc}. During the period of (1-D)T_{S}, the output voltage at AC port is valid and the output voltage $u_{x\mathrm{N}}$ at DC port is 0. Therefore, the relationship between the amplitude of the AC output line voltage u_{ac} and the DC bus voltage U_{dc} meets (6) in the range of $M \leqslant 1$.

$$u_{\mathrm{ac}} = M \cdot U_{\mathrm{dc}} \cdot (1 - D) \tag{6}$$

where, D is the duty cycle in chopper stage of the converter; When the modulation index $M \leqslant \sqrt{3} \Big/ 3$, the output voltage at AC port will degenerate to two levels. The range of $M > 1$ belongs to the over-modulation and will no longer satisfy (6). The amplitude of AC output and DC output in operating mode 1 always restrict each other, because the higher amplitude of AC output is obtained at the cost of duty cycle D which determines the amplitude of DC output. In order to obtain larger DC output, (1-D)T_{s} should be smaller, that means, the effective time of AC output is compressed and the effective value of AC output is reduced. This is the characteristic of the modulation strategy of three-phase hybrid converter based on time-sharing modulation idea. However, the above characteristics is exactly used to maximize the boost ratio of the converter in operation mode 2. Because the duty cycle D of the converter in operating mode 2 is inversely proportional to the DC voltage gain, the smaller D is, the higher the DC voltage gain is. At the same time, the smaller D is, the larger (1-D)T_{s} and the larger amplitude of the AC output voltage is. The common result of these two effects is to further increase the AC output amplitude. Obviously, this situation is beneficial to the output of both AC and DC ports, which is also an advantage of the converter in operating mode 2.

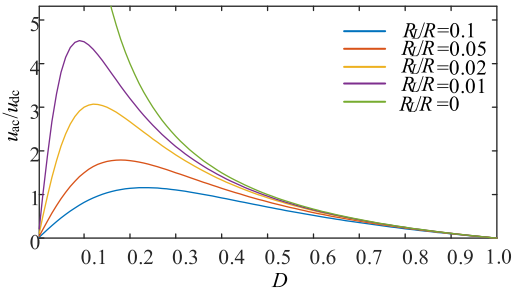

FIGURE 11. Boost ratio varying with D.

B. CBPWM STRATEGY

The virtual space vector modulation strategy needs to clear the specific position of the reference vector and also needs

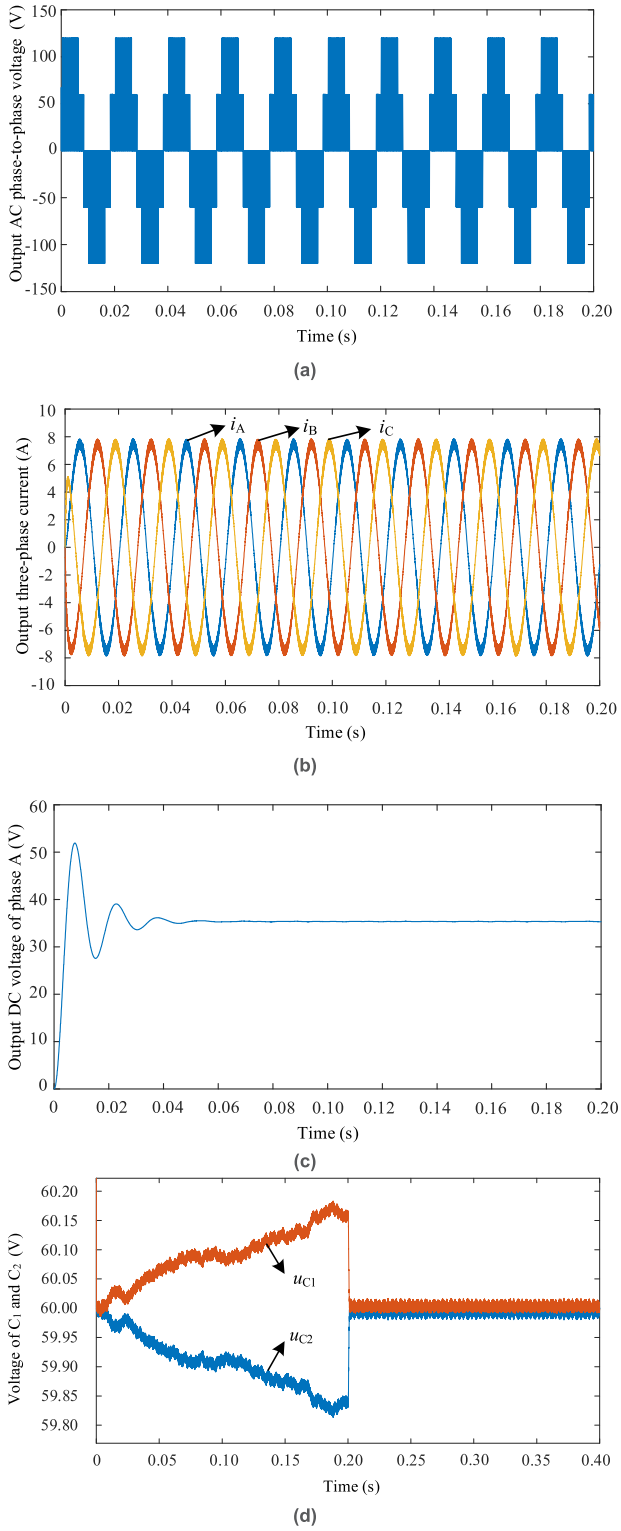

FIGURE 12. Simulation results in operating mode 1. (a) Line voltage v_{AB} from AC port. (b) Load current i_{ABC} from AC port. (c) Output voltage from one of DC ports. (d) Capacitors voltage in operating mode 1.

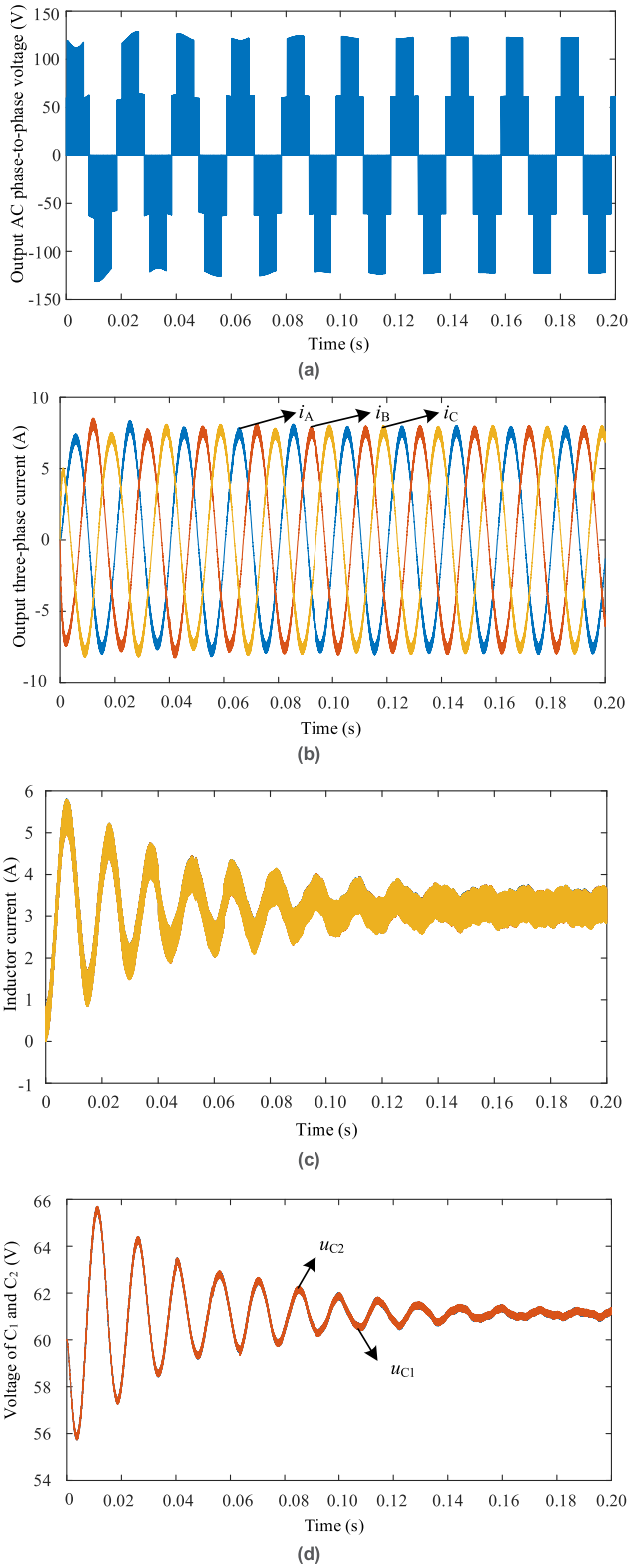

FIGURE 13. Simulation results in operating mode 2. (a) Line voltage v_{AB} from AC port. (b) Load current i_{ABC} from AC port. (c) Inductor current from DC ports. (d) Capacitors voltage in operating mode 2.

to calculate the action time in each sector. There are a lot of trigonometric functions in the process of duty cycle calculation and it is difficult to solve. Therefore, a CBPWM strategy based on virtual space vector modulation is proposed.

The switching sequence of the virtual space vector is not unique. In order to facilitate the implementation of CBPWM strategy, a switching period is divided into 11 segments. At the same time, as shown in Fig. 8, the optimized switching sequence is determined by considering preventing the voltage hopping and the symmetry of the switching sequence. It shows the switching details between AC output and DC output in one switching cycle. According to the switching state in Table 1, the driving signals of B-phase 5 switching tubes as shown in Fig. 9 can be obtained. Further analysis shows that driving signals S_{x3} and S_{x4} can be obtained by logical operation of S_{x1}, S_{x2} and S_{x5}. According to Fig. 9, the logical operation rules are as follows:

$$\begin{aligned} S_{x3} &= \bar{S}_{x1} \\ S_{x4} &= S_{x2} \mathrm{XOR} S_{x5} \end{aligned} \tag{7}$$

Therefore, it is only need to calculate the modulation waves that generate the driving signals S_{x1}, S_{x2} and S_{x5}. Fig. 10 shows the detailed calculation process of carrier modulation of phase B. The carrier is an isosceles triangle, whose period equal to the switching period and amplitude is between -1 and 1. The mathematical expression of the carrier is as follows:

$$u_{\mathrm{tri}} = \begin{cases} \frac{4}{T_S} t - 1, 0 \le t \le \frac{T_S}{2} \\ -\frac{4}{T_S} t + 3, \frac{T_S}{2} \le t \le T_S \end{cases} \tag{8}$$

As shown in Fig. 10, at the moment when the switching state changes, a vertical line is drawn upward to intersect the carrier at a point and a horizontal line is drawn past the point, representing the modulation wave of the switching signal. According to the above analysis content, the expression of switch switching time is as follows:

$$\begin{cases} t_{\mathrm{Sb1}} = \left(\frac{T_1}{4} + \frac{T_2}{4} + \frac{T_3}{2} \right) (1 - D) \\ t_{\mathrm{Sb2}} = \frac{T_1}{4} (1 - D) \\ t_{\mathrm{Sb5}} = \frac{T_s}{2} (1 - D) \end{cases} \tag{9}$$

By substituting (9) into (8), expressions of modulated waves u_{Sb1}, u_{Sb2} and u_{Sb5} can be obtained as follows:

$$\begin{cases} u_{\mathrm{Sb1}} = -2 (1 - D) \frac{u_{\mathrm{b}} - u_{\mathrm{c}}}{U_{\mathrm{dc}}} + 1 - 2D \\ u_{\mathrm{Sb2}} = 2 (1 - D) \frac{u_{\mathrm{a}} - u_{\mathrm{b}}}{U_{\mathrm{dc}}} - 1 \\ u_{\mathrm{Sb5}} = 1 - 2D \end{cases} \tag{10}$$

Similarly, the modulation wave expressions of phase A and phase C can be obtained. The calculation process of the modulation wave expression in other sub-sectors is the same as the above process. According to the analysis, there are only three kinds of deference switching sequences for each phase of the converter in a switching cycle and they are summarized in Table 4. Because carrier is symmetric, only half of the switching sequence is given. It can be seen that no matter which phase A, B and C corresponds to one of switching sequences, the expression of the modulation wave is the same.

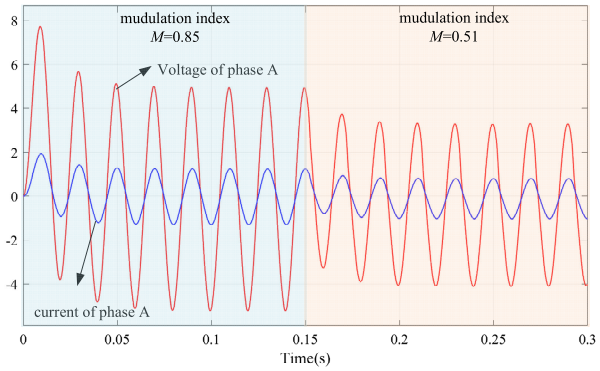

FIGURE 14. Load voltage and current waveforms of phase A from AC port vary with modulation index M.

In Table 4, $u_{\max}$, u_{mid} and $u_{\min}$ are shown as follows:

$$\begin{cases} u_{\max} = \max \left(u_{a-ref}, u_{b-ref}, u_{c-ref} \right) \\ u_{\mathrm{mid}} = \mathrm{mid} \left(u_{a-ref}, u_{b-ref}, u_{c-ref} \right) \\ u_{\min} = \min \left(u_{a-ref}, u_{b-ref}, u_{c-ref} \right) \end{cases} \tag{11}$$

According to the above content, CBPWM can greatly simplify the virtual space vector modulation method.

IV. BOOST RATIO

According to the conclusion derived in Part III above, the relationship between the amplitude of the AC output line voltage u_{ac} and the DC input voltage u_{dc} can be described by (12) when the current of the converter in operating mode 2 is continuous.

$$u_{\mathrm{ac}} = M \cdot u_{\mathrm{dc}} \cdot (1 - D) / D \tag{12}$$

The boost ratio is defined as:

$$\frac{u_{\mathrm{ac}}}{u_{\mathrm{dc}}} = M \cdot (1 - D) / D \tag{13}$$

Equation (13) shows that when the DC input voltage u_{dc} is unchanged and $0 < M < 1$, the amplitude of AC output voltage is mainly determined by D. Improving boost ratio in chopper stage means higher ratio of (1-D) /D. Theoretically, D can be arbitrarily small to achieve any amplitude of AC output voltage. However, it is not reasonable to produce an infinite output voltage. In fact, DC output voltage is zero when $D = 0$. The boost ratio is limited by the inductor resistance. Assuming that the inductive resistance is R_{L} and the load-side equivalent resistance is R, the relationship between u_{ac} and u_{dc} can be redefined in (14).

$$\frac{u_{\mathrm{ac}}}{u_{\mathrm{dc}}} = M \cdot (1 - D) \cdot \frac{1}{D} \cdot \frac{1}{\left(1 + \frac{R_{\mathrm{L}}}{RD^2} \right)} \tag{14}$$

Equation (14) is composed of the product of two parts, the first part is (13), which considers the inductance to be ideal. In the second part, the effect of inductance resistance R_{L} is considered. If R_{L} satisfies $R_{\mathrm{L}} \ll D^2 R$, the second part is approximately equal to 1. With R_{L} increases, more serious

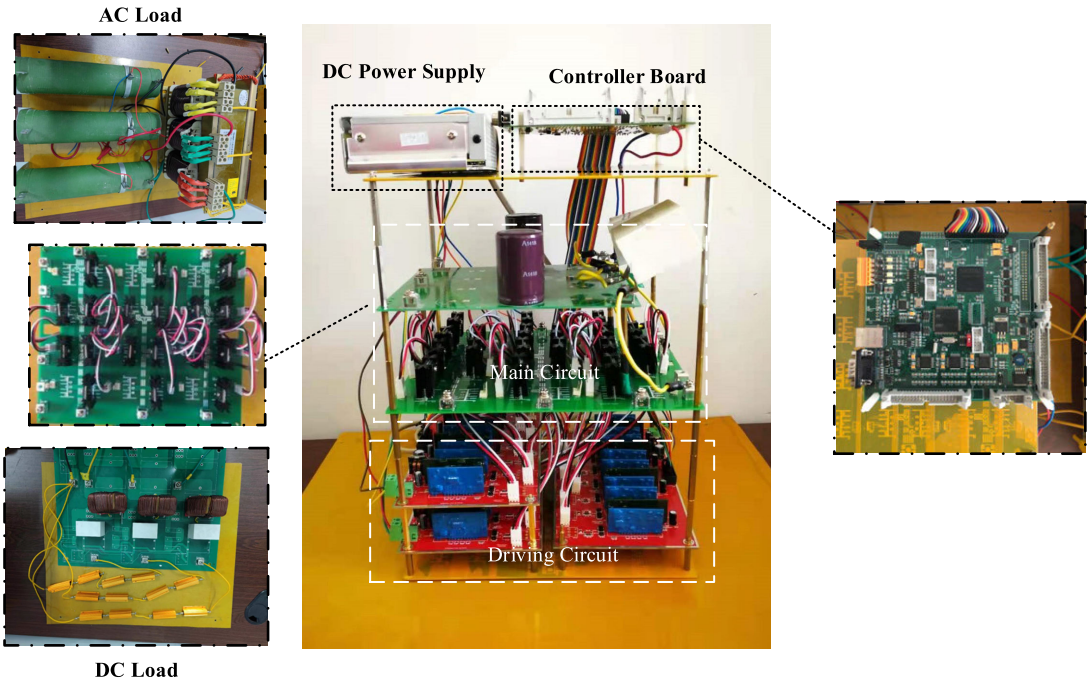

FIGURE 15. The three-phase hybrid converter prototype.

the boost ratio is limited. If M is set as 1, the curve of the boost ratio changing with D is shown in Fig. 11. It is known that the ratio of R_L/R determines the maximum value of boost ratio, which provides a reference for the optimal design of the converter.

V. SIMULATION AND EXPERIMENTAL RESULTS

A. SIMULATION RESULTS

The effectiveness of the proposed hybrid converter modulation method is verified by MATLAB/SIMULINK simulation. The simulation parameter is listed in Table 5. Fig. 12 shows the simulation results of the three-phase hybrid converter in operating mode 1, where $M = 0.8$, $D = 0.3$. Fig. 12(c) shows that value of u_{dc-x} is 36V when system enters steady state. Fig. 13 shows the simulation results of three-phase hybrid converter in operating mode 2, where $M = 0.8$, the amplitude of the three groups of DC voltage sources is 36V and $D = 0.3$, so the value of capacitors voltage at U_{dc} port reaches about 60V and U_{dc} reaches 120V after voltage boost. The waveforms illustrates that the adjustment time is about 0.15s. Fig. 14 shows load voltage and current waveforms of phase A from AC port after filtering vary with modulation index M from 0.85 to 0.51. It shows lagging power factor with constant AC output when load consists of resistance and inductance.

TABLE 5. Simulation parameter.

Description	*Value*
voltage of DC link	U_{dc}=120 V
upper/down capacitor	C_L=C_H=1000 uF
AC load	R_{ac}=5 Ω 、 L_{ac}=18 mH
Switching cycle	10 kHz
LC filter	L_{dc}=10 mH、 C_{dc}=500 uF
DC load	R_{dc}=10 Ω

B. EXPERIMENTAL RESULTS

It is further verified by building an experimental platform, which includes control board, main circuit and drive circuit, as shown in Fig.15. The control board for executing the control program includes high-performance DSPTMS320F28335 and programmable gate array EP4CE115F23I7N. The frequency of triangle carrier is set to 10kHz. Table 6 shows the relevant experimental parameters.

TABLE 6. Experimental parameter.

Description	*Value*
voltage of DC link	U_{dc}=200 V
upper/down capacitor	C_L=C_H=1000 uF
AC load	R_{ac}=10 Ω 、 L_{ac}=5 mH
Switching cycle	10 kHz
LC filter	L_{dc}=2 mH、 C_{dc}=30 uF
DC load	R_{dc}=40 Ω

Fig. 16 shows the experimental results of the three-phase hybrid converter in operating mode 1, where $M = 0.85$ and $D = 0.5$. Fig. 16(a) shows the waveform of output phase

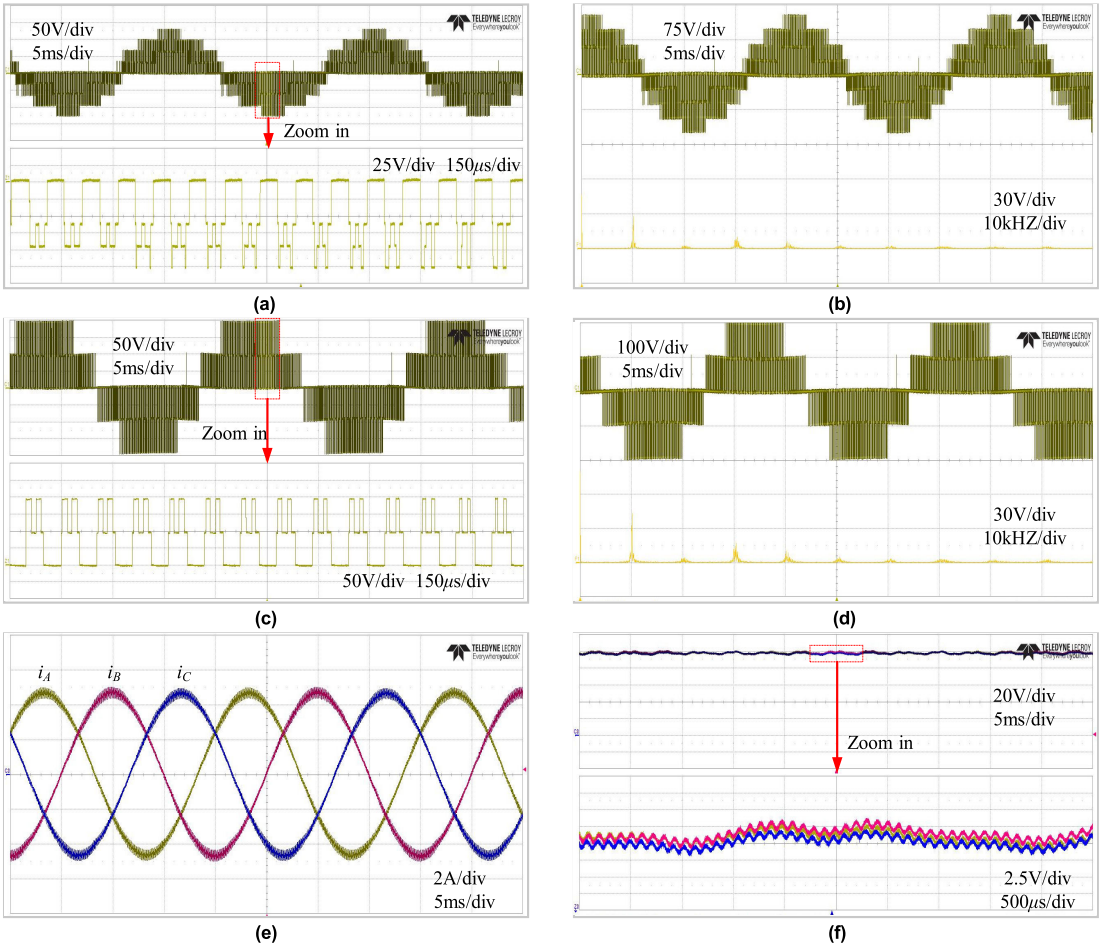

FIGURE 16. Experimental waveform in operating mode 1. (a) Phase voltage v_A from AC port and its zoom. (b) FFT of phase voltage v_A. (c) Line voltage v_{AB} from AC port and its zoom. (d) FFT of line voltage v_{AB}. (e) Load current i_{ABC} from AC port. (f) Output voltage from three groups of DC ports and their zooms.

voltage at AC port and its zoom. It is known that the phase voltage consists of 9 levels. Fig. 16(b) shows the Fourier analysis (FFT) of the phase voltage. The results show that the amplitude of the fundamental frequency wave of the phase voltage is about 47V and the theoretical value of the phase voltage is 49.1V. The experimental results are basically consistent with the theoretical value. Fig. 16(c) shows the waveform of line voltage and its zoom. The waveform shows that the line voltage consist of three levels: -U_{dc}/2, 0 and U_{dc}/2. Fig. 16(d) shows the Fourier analysis results of the line voltage. The result shows that the fundamental frequency wave amplitude of the line voltage is about 84V and the theoretical value of the line voltage is 85V. The experimental result is slightly smaller than the theoretical value, which is caused by the conduction resistance of the switching tube in the circuit. Fig. 16(e) shows the three-phase current waveform at the AC port, which is sine waves and its amplitude is about 5A. Fig. 16(f) shows the output DC voltage waveforms of three groups of DC ports and their zooms. The waveform shows that the output DC voltage amplitude is slightly less than 100V and its ripple amplitude is about 4V in steady state. Fig. 17 shows the experimental results of three-phase hybrid converter in operating mode 2, where $M = 0.85$, the amplitude of the three groups of DC voltage sources is 50V and $D = 0.25$, so the value at U_{dc} port reaches 200V after voltage boost. Fig. 17(a) shows the output phase voltage waveform of AC port and its zoom, which shows that there are 9 different levels. Fig. 17(b) shows the Fourier analysis of phase voltage, the results show that the amplitude of fundamental frequency phase voltage is about 70V and the theoretical value of phase voltage is 73.61V. The experimental results are basically consistent with the theoretical value. Fig. 17(c) shows the line voltage waveform and its zoom. The line voltage is composed of three levels. Fig. 17(d) shows the Fourier analysis of the line voltage. The results show that the fundamental frequency wave amplitude of the line voltage is 125V and the theoretical value is 127.5V. The experimental results are basically consistent with the

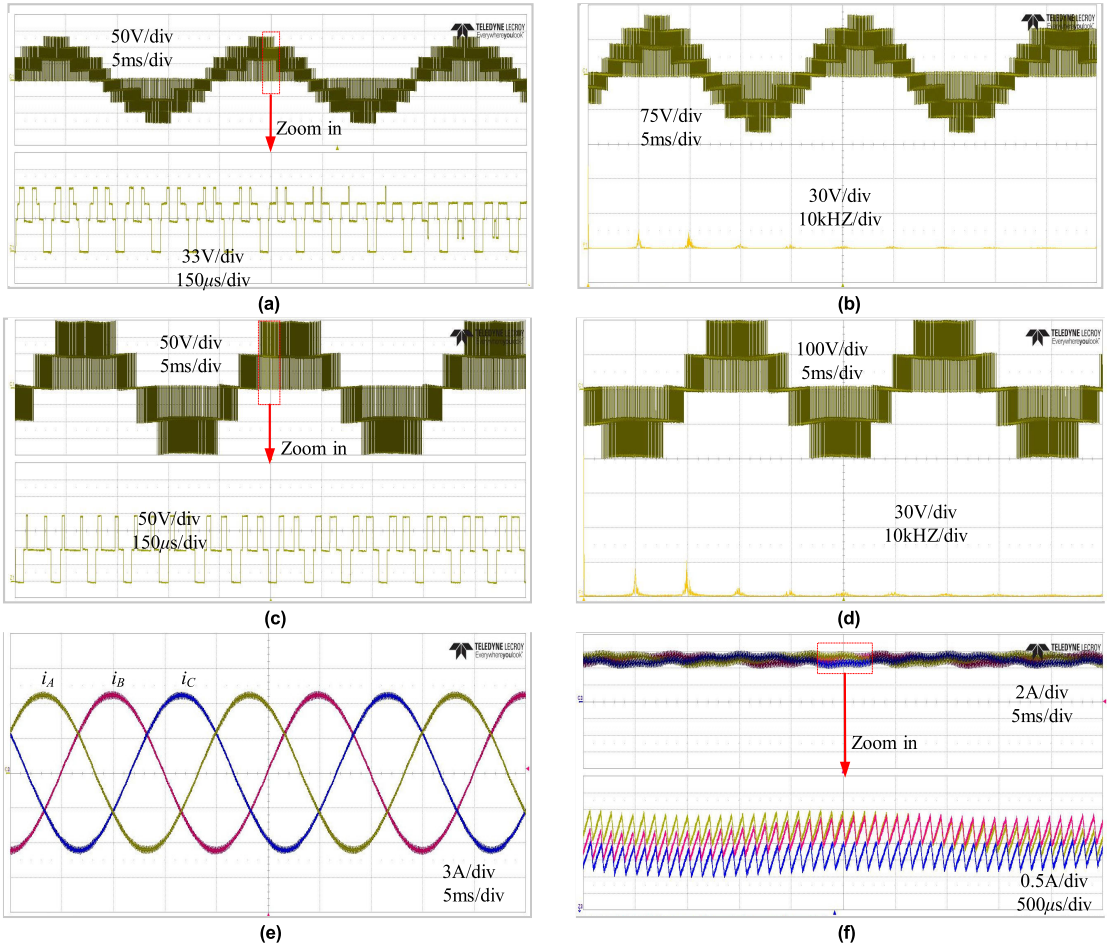

FIGURE 17. Experimental waveform in operating mode 2. (a) Phase voltage v_A from AC port and its zoom. (b) FFT of phase voltage v_A. (c) Line voltage v_{AB} from AC port and its zoom. (d) FFT of line voltage v_{AB}. (e) Load current i_{ABC} from AC port. (f) Output voltage from three groups of DC ports and their zooms.

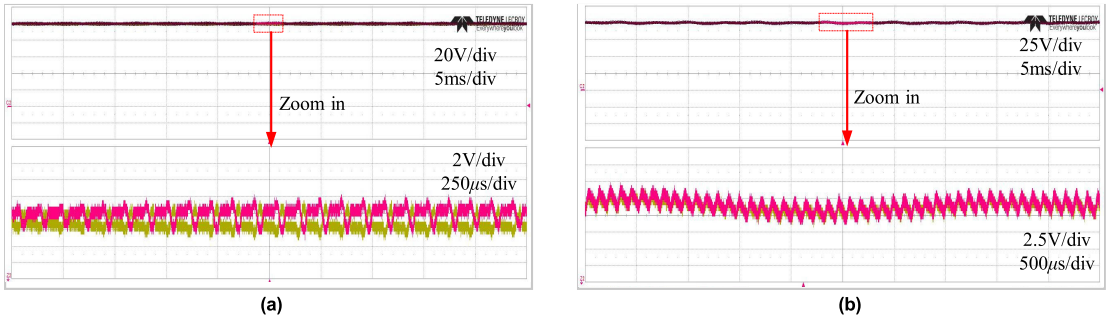

FIGURE 18. Voltage waveform of capacitors on DC link. (a) Capacitors voltage in operating mode 1 and its zoom. (b) Capacitors voltage in operating mode 2 and its zoom.

theoretical analysis. Fig. 17(e) shows the output three-phase current waveform, which shows that the current amplitude is about 6.5A. Fig. 17(f) shows the output currents of three groups of DC sources and their zooms. The waveform shows that the current amplitude fluctuates at 4∼6A. The ripple amplitude is within 2A and its fluctuation displays periodic regularity. Fig. 18(a) shows the waveform of the capacitor voltages on the DC link when hybrid converter is operating in mode 1. The waveform shows that the capacitor voltages on the DC link fluctuate around 100V and the difference between the voltages of two capacitors does not exceed 6V for utmost. Fig. 18(b) shows the waveform of the capacitor voltages on the DC link when the hybrid converter is operating in mode 2. The waveform shows that the capacitor voltages fluctuate around 100V and the difference between the voltages of capacitors not exceed 5V.

VI. CONCLUSION

In this paper, a novel three-phase hybrid converter topology is proposed. The converter adopts virtual space vector modulation strategy based on time-sharing modulation idea. A single DC power supply is used to realize a group of three-phase three-level AC output and three groups of DC output in operating mode 1. In addition, a group of three-phase boost three-level AC output is realized by using three groups of DC power supply in operating mode 2. In order to avoid the complicated calculation of action time and trigonometric function of space vector modulation, a CBPWM based on virtual space vector PWM is proposed in this paper and the modulation method is greatly simplified. Then the limiting condition of DC boost ratio is studied, which provides a reference for the subsequent research of DC boost capacity of hybrid converter. Compared with other existing hybrid converters, this converter has the advantages of more levels and more flexibility. Finally, the simulation and experimental results demonstrate the rationality of the proposed topology and the effectiveness of the control method.

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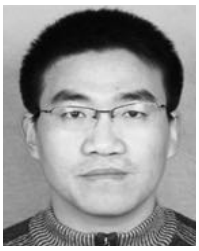

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