APPLIED RESEARCH

A Quadratic Buck-Boost Converter With Continuous Input and Output Currents

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ABSTRACT This study proposes a novel DC-DC converter topology that features a quadratic buck-boost voltage gain ratio. The quadratic gain of the converter enables it to achieve superior step-down or step-up capability when the duty cycle is higher or lower than 50 percent, as compared to conventional buck-boost converters. While there exist other quadratic buck-boost converters in the literature, the proposed converter offers unique features such as continuity of input and output currents, which reduces the current stress on the input and filter capacitors, making it a suitable option for renewable energy applications. Additionally, unlike its counterparts that have two high-side switches, the proposed converter features only one high-side and one low-side switch, allowing for a simpler gate-driver design. The proposed topology shares a common ground between the load and the source, and has the lowest stored energy with the same performance, indicating a compact size. Steady-state analysis has been conducted in both continuous and discontinuous conduction modes, and the controller design was studied with the aid of small-signal modelling. Simulation and experimental results from a 100 *W* prototype were used to validate claims and analyses.

INDEX TERMS dc-dc converter, low normalized semiconductor stress, quadratic buck-boost converter.

I. INTRODUCTION

Renewable energy resources, such as photovoltaic panels, require external equipment in the form of DC-DC power converters to regulate their voltage and bring it to a suitable level for connection to a DC-AC inverter and the power grid [1], [2], [3]. As shown in Fig. 1(a), transformer-based and transformer-less topologies are the two main categories of DC-DC power converters. Transformer-based converters can adjust their input voltage by the winding's turn ratio, providing increased voltage gain beyond that achievable by adjusting the duty cycle alone. Additionally, these converters isolate the input source and load, which protects sensitive loads from input-side faults. However, transformer-based converters suffer from disadvantages, such as large volume

and/or mass due to the use of high-frequency transformers and issues with leakage inductance. Furthermore, discontinuity of the input current can stress the filter capacitor, while the high current stress on the switch requires the use of snubber circuits, resulting in more components. Therefore, transformer-based converters are best suited for applications that require load and input source isolation [4], [5], [6], [7].

DC-DC converters are essential components in power electronic systems as they enable the transfer of electrical energy from one voltage level to another with high efficiency. Among the transformer-less DC-DC converter topologies, the buck, buck-boost, and boost converters are the fundamental topologies. The buck-boost converter can increase or decrease the input voltage level at its output terminal. The expected operating modes of this converter depend on the duty cycle, including step-up, step-down, and pass-through, which correspond to duty cycles above 50%, below 50%, and equal to 50%,

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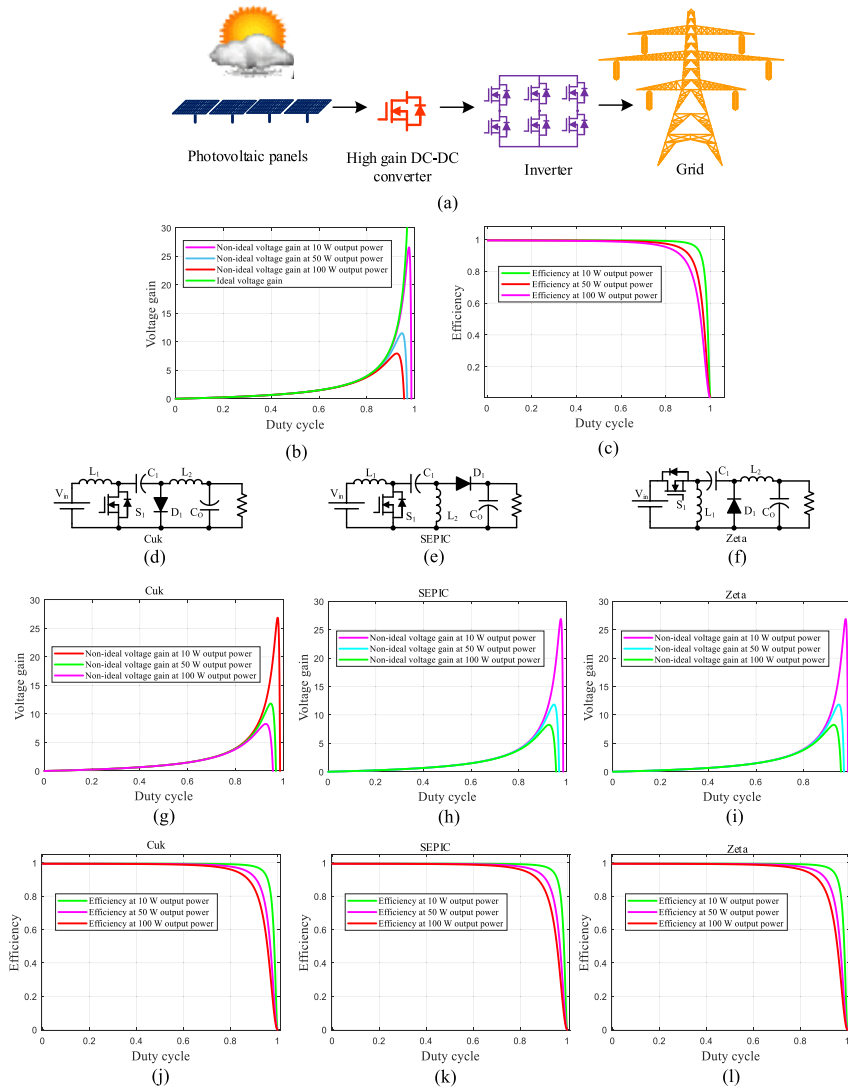
FIGURE 1. Illustration of the context and motivation for developing the proposed converter: (a) schematic of a converter connected to a photovoltaic panel, (b)-(c) voltage gain and efficiency of a conventional buck-boost converter vs. duty cycle for different power levels, (d)-(f) Cuk, SEPIC, and Zeta converters, and (g)-(l) voltage gain and efficiency of the Cuk, SEPIC, and Zeta converters vs. duty cycle for various power levels.

respectively. Due to its simple topology consisting of only one inductor, one capacitor, one switch, and one diode, the buck-boost converter has a high efficiency. However, there is still room for improvement, especially for renewable energy applications, such as discontinuity of input/output current, reverse polarity of the output voltage, and limited voltage gain range for high step-up/step-down requirements. Figs. 1 (b) and (c) illustrate these shortcomings. To address these issues, several converter topologies such as Cuk, SEPIC, and Zeta converters have been proposed, as shown in Figs. 1(d), (e), and (f), respectively. These converters have similar voltage gain ratios to the buck-boost topology. However, an increase in the output power, i.e., output current, significantly impacts the efficiency and voltage gain ratio, as demonstrated in Figs. 1(g)-(l). In other words, although Cuk, SEPIC, and Zeta

converters offer solutions for discontinuity issues in input and/or output current of buck-boost converters for renewable energy applications, a wide voltage gain range remains a topic of interest that could be addressed by using transformers or other voltage boosting techniques such as quadratic buck-boost converters.

High-gain converters are a solution to address the gain limitations of conventional topologies. One proposed topology combines the boost and positive output super lift Luo converter [1]. This topology provides a continuous input current and a common ground for the output and input source. However, it requires two switches and three diodes and has an inrush current issue that increases switching loss and current stress. Another proposed topology is the cascaded boost improvement [2]. This topology replaces the second

boost of the cascaded part with a positive output super lift Luo converter and uses a voltage multiplier cell (VMC) instead of an inductor in the super lift part to increase the voltage gain. However, the use of VMC brings two inrush currents that increase MOSFET's current stress and conduction loss. A similar topology [3] provides a voltage gain that is lower than [2] due to the use of only one voltage lift technique. However, it has a lower inrush current. An improved cascaded boost converter with voltage multiplier cells [4] uses a voltage lift technique that does not depend on the VMC and connects the input source and output capacitor with a diode to increase the voltage gain. However, the parallel and series connections of the capacitors cause inrush current issues that increase conduction loss and current stress. Another proposed converter [5] does not use the voltage lift technique and combines two boost converters. The voltage gain is less than [1], [2], [3], [4], but it does not have inrush current issues. However, the voltage stress of the second diode is higher than the output voltage, which is caused by the replacement of the first capacitor and diode in the first part. The proposed converter in [6] combines the conventional buck-boost and boost converters to provide a voltage gain that is the summation of the consisting parts. The output capacitor voltage is divided between two capacitors to reduce the output capacitor voltage stress. However, the input current ripple is increased, and the common ground of the input source and load is lost. Another proposed topology [7] is an improved boost converter with two VMCs that uses quadratic converters and voltage lift features to increase the voltage gain. The appeared inrush currents have less effect than previous ones, but the input current ripple is increased. The proposed topology in [8] is a combination of an improved boost converter with a VMC and a super lift Luo converter that improves the voltage gain but increases conduction loss and current stress due to inrush currents. A proposed topology [9] eliminates the common ground of the input source and load to increase the voltage gain but increases the input current ripple and the number of diodes, which decreases reliability.

Several converters have been proposed to improve the voltage gain and reduce the output capacitor voltage stress. One such converter proposed in [10] uses stacked boost converters to directly form the output voltage and decrease output capacitor voltage stress. However, this converter results in high input current ripple and a high-side switch. Another proposed converter in [11] improves upon the conventional boost converter with an improved switch structure but applies a voltage higher than the output voltage to the second diode. In [12], an improved cascaded boost topology uses a diode-capacitor-based voltage multiplier cell to provide high voltage gain at low duty cycle percentages but increases inrush currents after the first level. The proposed topology in [13] employs a positive output super lift Luo converter with a multiplier cell, resulting in double voltage lifting and increased voltage gain, but also produces high inrush currents. Finally, an improved buck-boost converter proposed in [14] uses a voltage multiplier cell to increase voltage gain but results in discontinu-

ous input/output currents and high output capacitor current stress. However, quadratic buck-boost converters proposed in [15], [16], [17], [18], [19], and [20] are capable of stepping up and down and providing continuous output current.

Based on recent research in power electronics, several quadratic buck-boost topologies have been introduced, such as those presented in [15], [16], [17], [18], [19], and [20]. Among them, the topology proposed in [15] combines a conventional buck-boost converter with a Cuk converter in the second stage, resulting in continuous input and output currents with negligible current stress on filter capacitors. However, it is important to note that the polarity of the output capacitor is changed due to the use of the buck-boost topology in the initial stage of power conversion, connecting the load and source to a common ground. On the other hand, the topology proposed in [16] is a cascaded version of two buck-boost converters, resolving the reversed polarity issue but with different switch types and non-continuous input and output currents. Similarly, the proposed topology in [17] combines the boost and Cuk topologies, resulting in continuous input and output currents but with high voltage and current stresses on both switches. While the proposed topology in [18] has the advantage of a low component count, it suffers from non-continuous input and output currents and different switch types. Finally, the topologies proposed in [19] and [20] utilize modified buck-boost converters with continuous input and output currents, providing a series connection of capacitors and input source acting as the output capacitor, and utilizing high-sided switches. There are other topologies such as [21] that benefit from a single switch but might have a higher voltage and/or current stress as well as a higher number of components.

This study presents a new topology of buck-boost converters with a quadratic voltage gain ratio, designed for renewable energy applications. The proposed topology is based on a combination of the boost and Zeta converters, resulting in the following contributions:

- Wide range of voltage gain ratio
- Continuous input and output current waveforms
- Same type of switches (i.e. N-type), simplifying the gate-driver circuit design
- Lower energy storage compared to existing quadratic buck-boost topologies, indicating the potential for a compact-size delivery
- Common ground of the load and input source

These contributions make the proposed topology highly beneficial for renewable energy applications, with a high voltage gain, continuous current waveforms, common input and output ground, and a simple gate-driving circuit design.

II. PROPOSED TOPOLOGY

The proposed converter topology is shown in Fig. 2(a) and consists of three inductors (L_1, L_2, and L_3), three capacitors (C_1, C_2, and C_o), two switches (S_1 and S_2), and
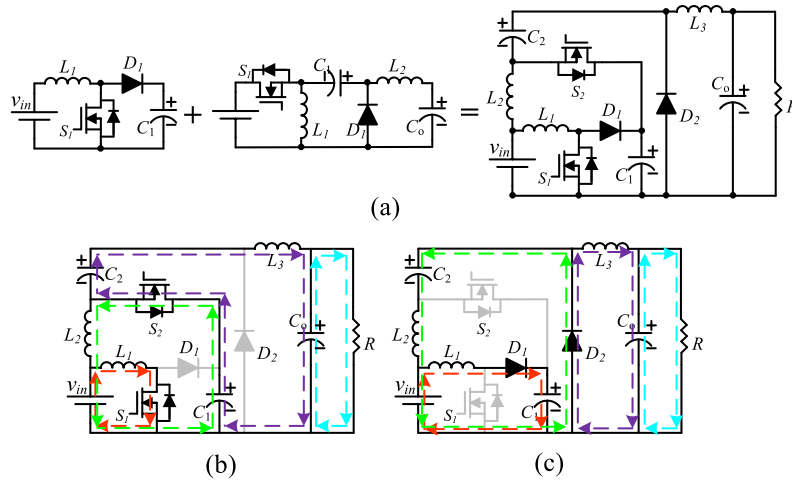
FIGURE 2. Proposed topology: (a) topology diagram, (b) equivalent circuit for the first mode, and (c) equivalent circuit for the second mode.
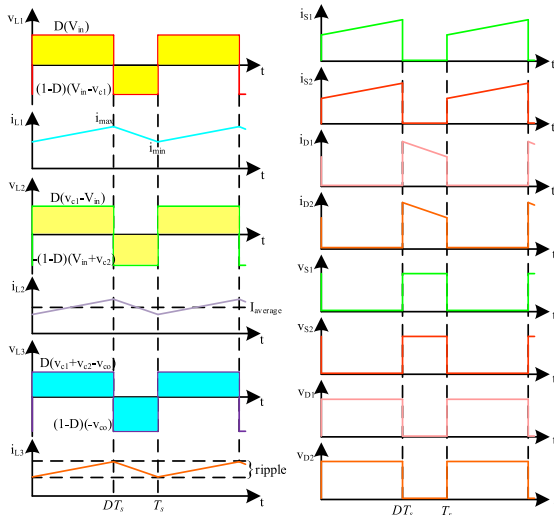

FIGURE 3. Inductors' current/voltage and semiconductors' current waveforms derived from theoretical expressions.

two diodes (D_1 and D_2). The topology combines the boost and zeta converter topologies and the switches are synchronously activated while the diodes are reverse-biased during switch activation. This results in two operating modes, with the inductors and capacitors, assumed to be sufficiently high-valued that the converter operates in the continuous conduction mode (CCM) and the applied voltage to the capacitors is constant. Specifically, the sum of the first and second inductor current provides the input current during both operating modes, leading to a continuous input current. In addition, the current flow through the third inductor provides a continuous output current waveform. Details of the operating modes are presented in the following subsections.

A. OPERATING MODES

The first operating mode occurs when both switches are ON, as shown in Fig. 2(b). In this mode, the first inductor's current flows through the first switch, and the remaining inductors'

current flows through the second switch. The voltage across all inductors is positive, and their magnetic field stores the energy. The energy is released by the electrical field of the first and second capacitors, while the third inductor's current charges the output capacitor and discharges it through the output current.

The second operating mode occurs when the switches are OFF, as shown in Fig. 2(c). In this mode, the inductors' flowing currents make the diodes forward-biased, and the inductors' voltage becomes negative, demagnetizing them and releasing their stored energy. The capacitors are charged in this mode, and they store energy in their electrical field. Fig. 3 shows the inductors' voltage/current and semiconductors' current waveforms based on the proposed concepts. The expressions for the voltage across inductors and current through capacitors are shown in (1).

$$
\begin{cases}
L_1 \dfrac{di_{L1}}{dt} = D(V_{in}) + (1-D)(V_{in} - v_{c1}) \\[2mm]
L_2 \dfrac{di_{L2}}{dt} = D(v_{c1} - V_{in}) - (1-D)(V_{in} + v_{c2}) \\[2mm]
L_3 \dfrac{di_{L3}}{dt} = D(v_{c1} + v_{c2} - v_o) - (1-D)(v_o) \\[2mm]
c_1 \dfrac{dv_{c1}}{dt} = -D(i_{L2} + i_{L3}) + (1-D)(i_{L1}) \\[2mm]
c_2 \dfrac{dv_{c2}}{dt} = -D(i_{L3}) + (1-D)(i_{L2}) \\[2mm]
c_3 \dfrac{dv_{c3}}{dt} = D(i_{L3} - I_o) + (1-D)(i_{L3} - I_o)
\end{cases}
\tag{1}
$$

B. VOLT-SECOND BALANCE

In the steady state, the inductors act as a short-circuit, meaning that the average voltage across them over a duty cycle is zero. This results in the equations for the inductor voltages in (1) being equal to zero. As a result, the average voltage across the capacitors can be expressed as (2).

$$
V_{c1} = \frac{V_{in}}{1-D}, \quad V_{c2} = \frac{2D-1}{(1-D)^2}V_{in}, \quad V_o = \left(\frac{D}{1-D}\right)^2 \tag{2}
$$

C. CHARGE-SECOND BALANCE

The duality of the last expression implies the charge-second balance, which means that capacitors behave as open circuits. This concept refers to the zero average currents of the capacitors over a duty cycle. Therefore, the current relation of capacitors in equation (1) becomes zero, and as a result, the average current of the inductors can be expressed using equation (3).

$$I_{L1} = \frac{D}{(1-D)^2}I_o, \quad I_{L2} = \frac{D}{1-D}I_o, \quad I_{L3} = I_o \quad (3)$$

D. THE BUCK-BOOST CAPABILITY

The voltage gain expression in equation (2) indicates that the proposed converter has the capability to operate as a step-up, step-down, or pass-through converter based on the duty cycle value. When the duty cycle is greater than 50 percent, the converter behaves as a step-up converter. Conversely, duty cycles lower than 50 percent cause the converter to operate as a step-down topology. Finally, at a duty cycle percentage of 50 percent, the converter operates in a pass-through mode.

E. VOLTAGE/CURRENT STRESS

The average current passing through the semiconductors during their conduction interval is defined as their current stress, while the voltage applied to the semiconductors during the inactivation and/or deactivation intervals is defined as their voltage stress. Therefore, the voltage and current stress values of the semiconductors can be expressed using equation (4).

$$\begin{cases} V_{S1} = V_{D1} = \dfrac{V_{in}}{1-D}, & V_{S2} = V_{D2} = \dfrac{D}{(1-D)^2}V_{in} \\ I_{S1} = \left(\dfrac{D}{1-D}\right)^2 I_o, & I_{S2} = I_{D1} = \dfrac{D}{1-D}I_o, \; I_{D2} = I_o \end{cases} \quad (4)$$

F. INDUCTOR/CAPACITOR CURRENT/VOLTAGE RIPPLE

The simplified forms of the inductors' current ripple and capacitors' voltage ripple can be expressed using equation (5). These factors are essential when selecting the circuit components.

$$\begin{cases} \Delta i_{L1} = \dfrac{DV_{in}}{f_sL_1}, & \Delta i_{L2} = \dfrac{D^2V_{in}}{(1-D)f_sL_2} \\ \Delta i_{L3} = \dfrac{D^2V_{in}}{(1-D)f_sL_3}, & \Delta v_{c1} = \dfrac{DI_o}{(1-D)f_sc_1} \\ \Delta v_{c2} = \dfrac{DI_o}{f_sc_2}, & \Delta v_{co} = \dfrac{D^2V_{in}}{8(1-D)f_sc_oL_3f_s^2} \end{cases} \quad (5)$$

III. DISCONTINUOUS CONDUCTION MODE (DCM)

The operation of a DC-DC converter in either continuous conduction mode (CCM) or discontinuous conduction mode (DCM) depends on the inductors' value and their average current. The value of the inductors affects the current ripple, which means that reducing the inductors' value increases the inductor current ripple, causing the converter to approach the
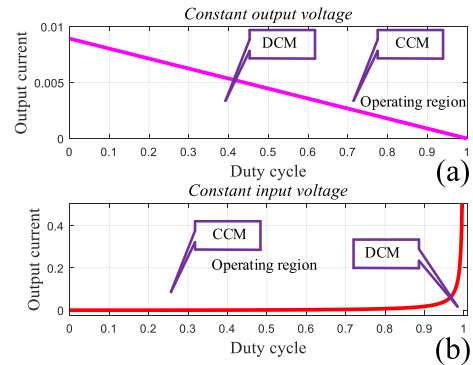

FIGURE 4. The operation of the converter in CCM and DCM: output current values with respect to the constant output and input voltages, where there is a transition from CCM to DCM.
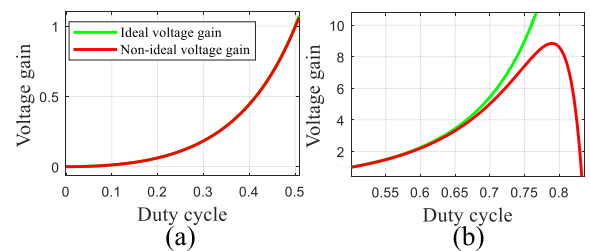

FIGURE 5. The ideal/non-ideal voltage gain, while: (a) duty cycle varies from 0% to 50% and (b) duty cycle varies from 50% to 100%.

boundary conduction mode (BCM). Therefore, each inductor should have a minimum value to ensure that the converter operates in CCM. It's worth noting that the minimum value of each inductor required to maintain the converter's operation in CCM, as per equation (5), can be expressed using equation (6).

$$L_1 > \frac{R(1-D)^4}{2D^2f_s}, \quad L_2 > \frac{R(1-D)^2}{2Df_s}, \quad L_3 > \frac{R(1-D)}{2f_s} \quad (6)$$

The operation of the converter in CCM or DCM is also affected by the average current of the inductor. If the average current of the inductor is less than half of the inductor's current ripple, the converter operates in DCM. It's important to note that the average current of the inductors depends on the average output current. The operation of the converter for different values of the output current and duty cycle is presented in Figure 4. Figure 4(a) represents a constant output voltage, while Figure 4(b) represents a constant input voltage. The voltage gain of the converter in DCM is not the same as that expressed in CCM. Therefore, other parameters need to be described. The duty cycle of the converter is represented by D and is defined as the ratio of the switch activation time to the switching period. Additionally, D_1 represents the ratio of the diode's conduction time to the switching period, while D_2 is defined as the ratio of all semiconductors' inactivation time to the switching period. It's worth noting that these
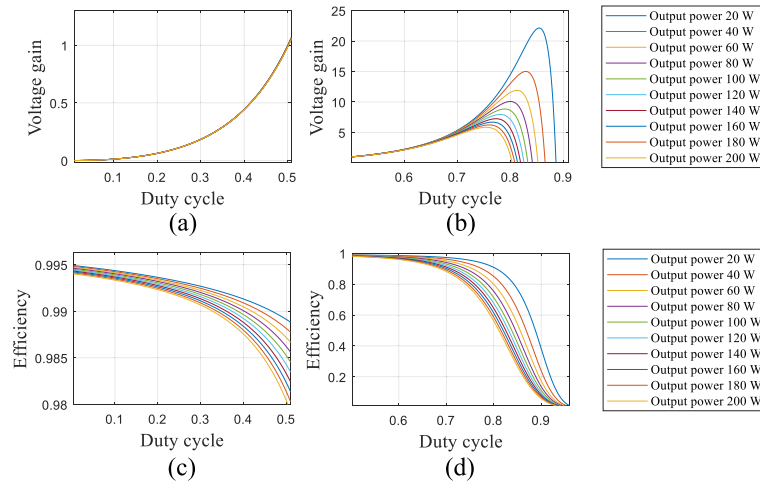
FIGURE 6. The output power effect on (a) voltage gain while the duty cycle varies from 0 to 50%, (b) voltage gain while the duty cycle varies from 50% to 100%, (c) efficiency while the duty cycle varies from 0 to 50%, and (d) efficiency while the duty cycle varies from 50 to 100%.
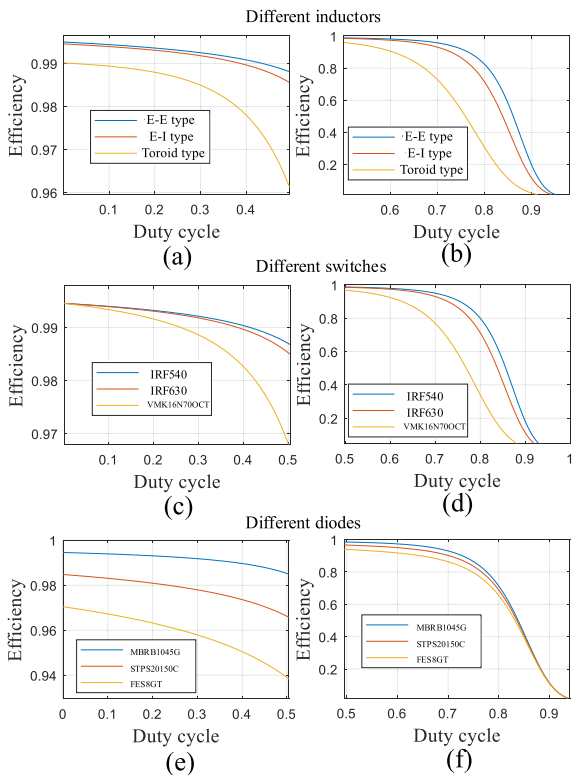

FIGURE 7. Efficiency variations for: (a)-(b) differnt inductor core types, (c)-(d) different switch types, and (e)-(f) different diode types.

parameters are related to equation (7).

$$D + D_1 + D_2 = 1 \qquad (7)$$

Based on the mentioned parameters, the governing equation of the voltage gain in DCM is expressed as (8).

$$\frac{V_o}{V_{in}} = \left(\frac{D}{D_1}\right)^2 \qquad (8)$$

IV. NON-IDEAL GAIN AND EFFICIENCY

The performance of the DC-DC converter is affected by the presence of non-ideal components, such as parasitic resistance in the inductors, switches, and diodes. The presence of these resistances results in a voltage gain that is different from the ideal voltage gain expressed in equation (2) and causes the practical output power to be lower than the input power. This, in turn, affects the efficiency of the converter. However, the parasitic resistance of the capacitors can be minimized by using Metallized Polyester Film Capacitors (MKT) or by connecting capacitors in parallel. The effect of these non-ideal components on the voltage gain can be expressed using equation (9).

In equation (9), the terms r_L, r_S, r_D, and R represent the equivalent series resistance of the inductors, switches, diodes, and load, respectively. The inclusion of these parasitic components results in three additional terms being added to the ideal voltage gain equation. Figure 5 illustrates the impact of non-ideal factors on the voltage gain, comparing the ideal and non-ideal voltage gain versus duty cycle variations. It can be observed that both curves are very similar up to a duty cycle of 70 percent, with a negligible difference. However, for duty cycles above 70 percent, the non-ideal voltage gain starts to fall more significantly, highlighting the impact of parasitic components at higher duty cycles.

The output power also has an impact on the non-ideal voltage gain. As shown in equation (9), an increase in output power decreases the value of R, resulting in the coefficients of the non-ideal part having a greater impact. This effect is validated in Figure 6 (a)-(b), where it can be observed that in non-ideal modes, higher output power ratings lead to a lower voltage gain at higher duty cycles compared to the ideal analysis.

To assess the efficiency of the converter, different types of losses must be considered. This study focuses on the

TABLE 1. Comparing different features of similar converters (the configurations are all non-isolated with quadratic and semi-quadratic voltage gain).

	Continuity of the input current	Continuity of the output current	Number of the inductors	Number of the capacitors	Number of the switches	Number of the diodes	Switch-type	Number of the low-side switch	Number of the high-side switch
Proposed	yes	yes	3	3	2	2	NMOS-NMOS	1	1
[15]	yes	yes	3	3	2	2	NMOS-PMOS	0	2
[16]	No	No	2	2	2	2	NMOS-PMOS	0	2
[17]	yes	yes	3	3	2	2	NMOS-PMOS	0	2
[18]	No	No	2	2	2	2	NMOS-PMOS	0	2
[19]	yes	No	2	2	2	2	NMOS-PMOS	0	2
[20]	yes	No	2	2	2	2	NMOS-PMOS	0	2

conduction loss of the inductors, switches, and diodes, as well as the frequency loss of the switches, depending on their types. It is important to note that the Foucault and hysteresis losses of the inductors have been disregarded, the frequency loss of the diodes has also been disregarded, and the conduction loss of the capacitor has not been taken into account. Nonetheless, it is worth mentioning that the conduction loss of the capacitor approaches zero for MKT capacitors. Equation (10) expresses the losses and efficiency formulae, where PL denotes the conduction loss of inductors, PSC is the conduction loss of switches, PSS is the frequency loss of MOSFETs, and PD is the conduction loss of diodes. Efficiency is affected by the duty cycle, output power, and component quality. Fig. 6 (c)-(d) presents the efficiency variations for different output power values while the duty cycle varies from 0 percent to 100 percent. It can be concluded that the high efficiency is not attainable when the duty cycle is set at a high value, along with an increase in the output power ratings.

Component quality is another factor that affects efficiency. Fig. 7 (a)-(b) presents the efficiency function according to different types of inductors, switches, and diodes. The comparison involves E-E, E-I, and toroidal types for inductors, IRF540, IRF630, and VMK16N70OC2 for different switches, and MBRB104G, STPS20150C, and FES8GT for diodes. As expected, the higher the internal resistance of the component, the lower the efficiency. This conclusion holds for all types of components, including inductors, switches, and diodes.

V. COMPARISON OF DC-DC CONVERTER TOPOLOGIES
Table 1 presents a comparison of the proposed converter topology with other recently suggested converters that use two switches and have quadratic voltage gain. Various topological aspects have been considered. It can be observed that the proposed converter has a continuous input current, as do the converters in [15], [17], [19], and [20]. Additionally, the proposed converter and converters [11] and [17] have a continuous output current. The proposed converter, like converters [15] and [17], uses three inductors and capacitors. It is worth noting that the number of switches and diodes is the same for all compared topologies. As another aspect of comparison, MOSFETs used in

DC-DC converters are classified into two categories: low-side and high-side. Low-side switches have less complicated drive circuits compared to high-side switches because their source is connected to the converter's ground, while high-side switches are connected to the load. The proposed converter has both high-side and low-side switches, while both switches in [15], [16], [17], [18], [19], and [20] are high-side. In addition, the MOSFETs of the proposed converter are of the same type, whereas those in [15], [16], [17], [18], [19], and [20] have a combination of N-type and P-type.

Table 2 reports the normalized voltage/current stress of the semiconductors. The output voltage of the converters is used as the reference value for voltage stress normalization, while the input current is used as the reference value for current stress normalization. The duty cycle percentage used in this table is 67 percent, providing a four-time voltage boost ratio. According to this table, except for [17], the voltage stress across the first switch is the same in all converters. The first switch's voltage stress in [17] is the highest. The voltage stress of the second switch and the first diode is the same in the proposed converter and [15], [16], [18], [19], [20], with the lowest value in [16]. The other voltage/current stress values are the same in all topologies.

$$
\begin{cases}
\dfrac{V_o}{V_{in}} = \left(\dfrac{D}{1-D}\right)^2 - \dfrac{r_L}{R}\left(\dfrac{D^6 - 2D^5 + 2D^4}{(1-D)^6}\right) \\
- \dfrac{r_S}{R}\left(\dfrac{D^6 - D^4 + D^3}{(1-D)^6}\right) - \dfrac{r_D}{R}\left(\dfrac{2D^5 - D^3 + D^2}{(1-D)^5}\right)
\end{cases}
$$

(9)

$$
\begin{cases}
P_L = \left(r_{L1}\dfrac{D^2}{(1-D)^4} + r_{L2}\left(\dfrac{D}{1-D}\right)^2 + r_{L3}\right)\dfrac{P_o}{R} \\
P_{SC} = \left(r_{s1}\dfrac{D^3}{(1-D)^4} + r_{s2}\dfrac{D}{(1-D)^2}\right)\dfrac{P_o}{R} \\
P_{SS} = \dfrac{P_o f_s(t_{OFF1} + t_{OFF2})}{2(1-D)} \\
P_D = \left(\dfrac{D}{1-D}V_{DF1} + V_{DF2}\right) \\
\eta = \dfrac{P_o}{P_o + P_L + P_{SC} + P_{SS} + P_D}
\end{cases}
$$

(10)

Table 3 presents various losses at the operating point. The output power is 100 W, the output current is 1 A, and the duty cycle is 67 percent. The conduction losses of the inductors are the same in the proposed converter and [15], [16], with the topology in [20] having the highest inductor losses. The conduction losses of the switches are the same in the proposed converter and [15], [16], [18], [19], [20], with the highest value belonging to [17]. A similar trend is observed for the switching losses of the MOSFETs. The conduction loss of the diodes is the same in all topologies. The proposed converter and [15], [16] have the highest efficiency, while the lowest value belongs to [20].

Table 4 reports the stored energy of inductors, which is related to the size of the converter. A lower stored energy corresponds to a smaller converter size. The stored energy is formulated using the output voltage (V_o), frequency (f_s), load value (R), and the percentage of the current ripple (k). In this case, the output voltage is 100 V, the frequency is 100 kHz, the load value is 100 ohm, the duty cycle is 67 percent, and the percentage of the current ripple is 30 percent. The stored energy of the proposed converter is lower than that of the other converters in [15], [16], [17], [18], [19], and [20]. Therefore, the proposed topology has the smallest size among the compared topologies.

Fig. 8 relates to Table 3 and shows a comparison of inductor, switch, and diode losses among different duty cycle percentages. The proposed converter has similar inductor loss as [15] and [16] at duty cycles below 70%, but lower than [18] and [19] and higher than [17] and [20]. At other duty cycle percentages, the proposed topology has lower inductor loss than [17] and [20], and similar to [15], [16], [18], and [19]. The switching loss of the proposed topology is similar to others, except for [16], which has lower switching loss at duty cycles below 70%. For other duty cycle percentages, the proposed topology has the lowest switching loss. All topologies have the same diode loss.

Fig. 9 shows a comparison of non-ideal voltage gain, which is the same for all topologies at duty cycles from 0% to 70%, except for [19]. The maximum voltage gain and corresponding duty cycle are the same for the proposed topology, [16], [18], and [20].

Fig. 10 compares the efficiency of the proposed converter and [15], [16], [17], [18], [19], [20] at different voltage and power levels. The efficiency of the proposed topology and [15] is higher than [18], [19], and [20] at duty cycles from 0% to 50% and lower than [16], [17]. At duty cycles from 50% to 75%, the efficiency of the proposed topology and [15], [16], [17], [18], [19] is similar.

Table 5 compares various losses of the proposed converter and [1], [2], [3], [4], [5], [6], [7], [8], [9], [10], [11], [12], [13], [14]. The proposed topology has higher extracted inductor loss than [1], [2], [3], [4], [5], [6], [7], [8] and [8], [9], [10], [11], [12], [13], and [14], but lower extracted switch loss than [2], [3], [4], [7], [8], [12], [13], and [14]. The diode conduction loss in the proposed converter is lower than [1], [2], [3], [4], [7], [8], [9], [12], [13], and [14], but higher than

[5], [6], and [11]. The proposed efficiency is higher than [2], [3], [4], [7], [8], [12], [13], and [14], but similar to [1], [5], [6], [9], [10], and [11].

Table 6 compares the normalized current stress of the semiconductors in various topologies, including the proposed one. The results show that all the semiconductors in [1] experience less current stress than the proposed topology, while in [2], the second diode has the highest current stress. However, the values in the other semiconductors are better than the proposed one. The topology in [3] causes higher current stress to the second diode but lower stress in the other components than the proposed one. The proposed topology in [4] only has a higher current stress, but the rest of the values are better than the proposed one.

Table 7 presents the normalized voltage stresses of the semiconductors in various topologies, including the proposed one. The results show that all the proposed topologies in [1], [2], [3], [4], [5], [6], [7], [8], [9], [10], [11], [12], [13], and [14] provide lower voltage stresses than the proposed topology. This is due to the higher voltage gain capability and component count, which allows for sharing higher voltages among numerous components, resulting in lower voltage stresses.

VI. SMALL SIGNAL ANALYSIS

The extracted equations in (1) provide the inductors' voltage and capacitors' current in both switch operating modes and can be used to derive the state-space equations and their corresponding matrices. Specifically, the inductors' current and capacitors' voltage can be treated as state variables. Using these variables, the state-space equations can be expressed as shown in equation (11).

$$\begin{cases} L_1 \dfrac{d<i_{L1}>}{dt} = d(V_{in}) + (1-d)(V_{in} - <v_{c1}>) \\ L_2 \dfrac{d<i_{L2}>}{dt} = d(<v_{c1}> - V_{in}) - (1-d)(V_{in} + <v_{c2}>) \\ L_3 \dfrac{d<i_{L3}>}{dt} = d<v_{c1} + v_{c2} - v_o> - (1-d)<v_o> \\ c_1 \dfrac{d<v_{c1}>}{dt} = -d<i_{L2} + i_{L3}> + (1-d)<i_{L1}> \\ c_2 \dfrac{d<v_{c2}>}{dt} = -d<i_{L3}> + (1-d)<i_{L2}> \\ c_3 \dfrac{d<v_{c3}>}{dt} = d<i_{L3} - \dfrac{V_o}{R}> + (1-d)<i_{L3} - \dfrac{V_o}{R}> \end{cases}$$

(11)

Applying small-signal perturbations to the duty cycle and forming the standard state-space matrices $\dot{x} = Ax + B\hat{d}$ and $y = Cx$, where C is simply denoted as [0 0 0 0 0 1], one can express (12), as shown at the bottom of page 11. A clearer step-by-step approach to obtain the model has been elaborated in [22].

The Bode diagram of the proposed converter has been obtained before and after compensation using the expressed relations, and is illustrated in Fig. 11. The compensator suitable for the proposed topology has been designed using the Sisotool in Matlab and is presented in (13), using Fig. 12,

TABLE 2. Comparing normalized semiconductors voltage/current stress.

	V_{s1}/V_o	V_{s2}/V_o	V_{D1}/V_o	V_{D2}/V_o	I_{s1}/I_{in}	I_{s2}/I_{in}	I_{D1}/I_{in}	I_{D2}/I_{in}	D
Proposed	$\frac{1-D}{D^2}=0.75$	$\frac{1}{D}=1.5$	$\frac{1-D}{D^2}=0.75$	$\frac{1}{D}=1.5$	1	$\frac{1-D}{D}=0.5$	$\frac{1-D}{D}=0.5$	$\left(\frac{1-D}{D}\right)^2=0.25$	67 %
[15]	$\frac{1-D}{D^2}=0.75$	$\frac{1}{D}=1.5$	$\frac{1-D}{D^2}=0.75$	$\frac{1}{D}=1.5$	1	$\frac{1-D}{D}=0.5$	$\frac{1-D}{D}=0.5$	$\left(\frac{1-D}{D}\right)^2=0.25$	67 %
[16]	$\frac{1-D}{D^2}=0.75$	$\frac{1}{D}=1.5$	$\frac{1-D}{D^2}=0.75$	$\frac{1}{D}=1.5$	1	$\frac{1-D}{D}=0.5$	$\frac{1-D}{D}=0.5$	$\left(\frac{1-D}{D}\right)^2=0.25$	67 %
[17]	$\frac{1}{D^2}=2.25$	$\frac{1}{D}=1.5$	$\frac{1-D}{D^2}=0.75$	$\frac{1}{D}=1.5$	1	$\frac{1-D}{D}=0.5$	$\frac{1-D}{D}=0.5$	$\left(\frac{1-D}{D}\right)^2=0.25$	67 %
[18]	$\frac{1-D}{D^2}=0.75$	$\frac{1}{D}=1.5$	$\frac{1-D}{D^2}=0.75$	$\frac{1}{D}=1.5$	1	$\frac{1-D}{D}=0.5$	$\frac{1-D}{D}=0.5$	$\left(\frac{1-D}{D}\right)^2=0.25$	67 %
[19]	$\frac{1-D}{D^2}=0.75$	$\frac{1}{D}=1.5$	$\frac{1-D}{D^2}=0.75$	$\frac{1}{D}=1.5$	1	$\frac{1-D}{D}=0.5$	$\frac{1-D}{D}=0.5$	$\left(\frac{1-D}{D}\right)^2=0.25$	67 %
[20]	$\frac{1-D}{D^2}=0.75$	$\frac{1}{D}=1.5$	$\frac{1-D}{D^2}=0.75$	$\frac{1}{D}=1.5$	1	$\frac{1-D}{D}=0.5$	$\frac{1-D}{D}=0.5$	$\left(\frac{1-D}{D}\right)^2=0.25$	67 %

TABLE 3. Comparing different losses and efficiency in 100 W.

	P_L	P_{sc}	P_{ss}	P_D	Efficiency
Proposed	$\frac{2D^4-6D^3+8D^2-4D+1}{(1-D)^4}\frac{r_L}{R}P_o=1.9W$	$\frac{2D^3-2D^2+D}{(1-D)^4}\frac{r_S}{R}P_o=0.69W$	$\frac{f_sP_ot_{OFF}}{1-D}=0.015W$	$\frac{V_{DF}I_o}{1-D}=1.5$	95.96 %
[15]	$\frac{2D^4-6D^3+8D^2-4D+1}{(1-D)^4}\frac{r_L}{R}P_o=1.9W$	$\frac{2D^3-2D^2+D}{(1-D)^4}\frac{r_S}{R}P_o=0.69W$	$\frac{f_sP_ot_{OFF}}{1-D}=0.015W$	$\frac{V_{DF}I_o}{1-D}=1.5$	95.96 %
[16]	$\frac{2D^4-6D^3+8D^2-4D+1}{(1-D)^4}\frac{r_L}{R}P_o=1.9W$	$\frac{5D^3-4D^2+D}{(1-D)^4}\frac{r_S}{R}P_o=1.5W$	$\frac{f_sP_ot_{OFF}}{1-D}=0.015W$	$\frac{V_{DF}I_o}{1-D}=1.5$	95.96 %
[17]	$\frac{3D^4-5D^3+7D^2-4D+1}{(1-D)^4}\frac{r_L}{R}P_o=2.187W$	$\frac{2D^3-2D^2+D}{(1-D)^4}\frac{r_S}{R}P_o=0.69W$	$\frac{f_sP_ot_{OFF}}{1-D}=0.015W$	$\frac{V_{DF}I_o}{1-D}=1.5$	95.06 %
[18]	$\frac{2D^2-2D+1}{(1-D)^4}\frac{r_L}{R}P_o=2.93W$	$\frac{2D^3-2D^2+D}{(1-D)^4}\frac{r_S}{R}P_o=0.69W$	$\frac{f_sP_ot_{OFF}}{1-D}=0.015W$	$\frac{V_{DF}I_o}{1-D}=1.5$	95.05 %
[19]	$\frac{2D^2-2D+1}{(1-D)^4}\frac{r_L}{R}P_o=2.93W$	$\frac{2D^3-2D^2+D}{(1-D)^4}\frac{r_S}{R}P_o=0.69W$	$\frac{f_sP_ot_{OFF}}{1-D}=0.015W$	$\frac{V_{DF}I_o}{1-D}=1.5$	95.05 %
[20]	$\frac{5D^2-4D+2}{(1-D)^4}\frac{r_L}{R}P_o=6.45W$	$\frac{2D^3-2D^2+D}{(1-D)^4}\frac{r_S}{R}P_o=0.69W$	$\frac{f_sP_ot_{OFF}}{1-D}=0.015W$	$\frac{V_{DF}I_o}{1-D}=1.5$	92.6 %

where the gain and phase margins are 8.72dB and 83.8deg, respectively, after compensation.

$$C(s) = \frac{0.52616}{s} \tag{13}$$

The compensator was designed by inputting the system parameters into the Sisotool toolbox and the compensator presented in (13) was obtained through trial and error to achieve the desired phase and gain margins.

To validate the theoretical findings, simulation and experimental results have been obtained and compared. In order to simulate the proposed topology, the values of the inductors and capacitors need to be determined. The equations for the inductors' current ripple and capacitors' voltage ripple are used to find the values of these components. Accord-

ing to power quality standards, an acceptable current ripple is between 20% and 40%, while the recommended voltage ripple is between 1% and 10%. For the built prototype, the current ripples and voltage ripples have been considered to be 30% and 5%, respectively.

To apply the percentage of the current and voltage ripples, the average inductors' current and capacitors' voltage must be determined. This is done by taking into account the duty cycle, input voltage, and output current. For the boost mode, the input voltage is 25 V, the output current is 1 A, and the duty cycle is 67%. For the buck mode, the input voltage is 100 V, the output current is 1 A, and the duty cycle is 33%. The average voltage across the capacitors and the average current through the inductors are obtained using the parametric equations presented in the previous sections, in particular
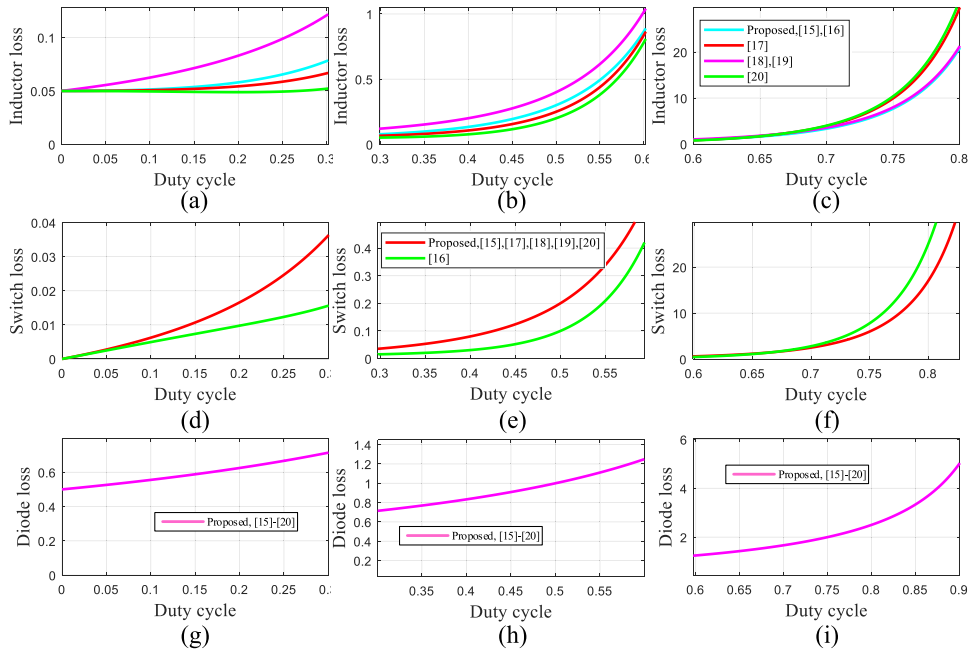
FIGURE 8. Comparing various losses: (a)-(c) inductor loss, (d)-(f) switch loss, and (g)-(i) to diode loss.

TABLE 4. Comparing the stored energy.

	Stored energy
Proposed	$(2-D)\dfrac{V_0^2}{2kf_sR} = 2.22mJ$
[15]	$2\dfrac{V_0^2}{2kf_sR} = 3.34mJ$
[16]	$2\dfrac{V_0^2}{2kf_sR} = 3.34mJ$
[17]	$2\dfrac{V_0^2}{2kf_sR} = 3.34mJ$
[18]	$2\dfrac{V_0^2}{2kf_sR} = 3.34mJ$
[19]	$2\dfrac{V_0^2}{2kf_sR} = 3.34mJ$
[20]	$2\dfrac{V_0^2}{2kf_sR} = 3.34mJ$
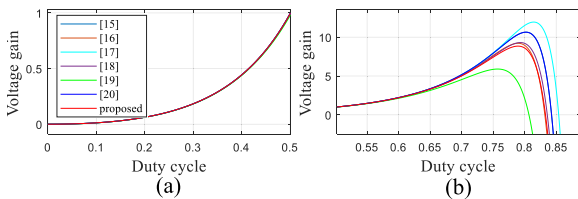
FIGURE 9. Comparing the non-ideal voltage gain, while the duty cycle varies: (a) from 0 to 50% and (b) from 50% to 100%.

using (2)-(4), and are expressed in (14) and (15), respectively.

$$Boost \begin{cases} V_{C1} = V_{C2} = 75V, & V_O = 100V \\ I_{L1} = 6A, I_{L2} = 2A, & I_{L3} = 1A \end{cases} \quad (14)$$
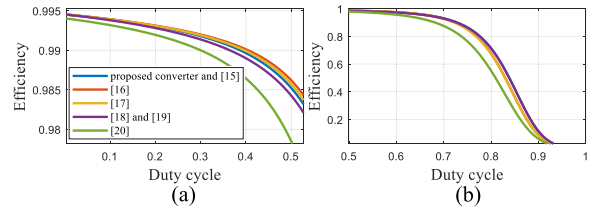

FIGURE 10. Comparing the non-ideal efficiency, while the duty cycle varies: (a) from 0 to 50% and (b) from 50% to 100%.

$$Buck \begin{cases} V_{C1} = 150, V_{C2} = 75V, & V_O = 25V \\ I_{L1} = 0.75A, I_{L2} = 0.5A, & I_{L3} = 1A \end{cases} \quad (15)$$

Using (14), and applying the voltage/current ripples yields the inductors' and capacitors' values as (16).

$$\begin{cases} L_1 = 3000\mu H, & L_2 = 2250\mu H, \ L_3 = 2222\mu H \\ C_1 = 10\mu F, & C_2 = 5\mu F, \ C_O = 0.062\mu F \end{cases} \quad (16)$$

VII. SIMULATION AND EXPERIMENTAL RESULTS

The selected switching frequency is 50 kHz to keep switching losses at a negligible level and to ensure that the wires and cores used in the prototype can handle the frequency. Table 8 summarizes all the parameters used in the simulations and the prototype. PLECS was used to extract the simulation results since it is suitable for power electronics, control, and microgrid projects. Figs. 13, 14, 15 and 16 show the simulation results of all the components' voltage and current waveforms. The capacitors' average voltage and inductors' current were calculated using (17) and (18), respectively,

TABLE 5. Comparing loss for [1], [2], [3], [4], [5], [6], [7], [8], [9], [10], [11], [12], [13], [14].

	P_L	P_S	P_D	D
[1]	$\frac{2D^2-6D+5}{(1-D)^4}\frac{r_L}{R}P_o=0.92$	$\frac{D^4-4D^3+5D^2-2D+1}{D(1-D)^4}\frac{r_S}{R}P_o=0.22$	$\frac{3-2D}{1-D}V_{DF}I_o=1.78$	0.36
[2]	$\frac{3D^2-10D+11}{(1-D)^4}\frac{r_L}{R}P_o=0.91$	$\frac{(1+2D-D^2)^2}{D(1-D)^4}\frac{r_S}{R}P_o=1.04$	$\frac{2D^2-7D+7}{(1-D)^2}V_{DF}I_o=4.1$	0.15
[3]	$\frac{2D^2-6D+5}{(1-D)^4}\frac{r_L}{R}P_o=2.71$	$\frac{1+D-D^2}{D(1-D)^4}\frac{r_S}{R}P_o=1.02$	$\frac{2D^2+5D+4}{(1-D)^2}V_{DF}I_o=7.4$	0.36
[4]	$\frac{2D^2-4D+6}{(1-D)^4}\frac{r_L}{R}P_o=0.59$	$\frac{(2D^2-4D+4)^2}{D(1-D)^4}\frac{r_S}{R}P_o=6.9$	$\frac{5-D}{1-D}V_{DF}I_o=2.9$	0.18
[5]	$\frac{D^2-2D+2}{(1-D)^4}\frac{r_L}{R}P_o=1$	$\frac{D^3-2D^2+2D}{(1-D)^4}\frac{r_S}{R}P_o=0.5$	$\frac{1}{1-D}V_{DF}I_o=1$	0.5
[6]	$\frac{2}{(1-D)^2}\frac{r_L}{R}P_o=0.62$	$\frac{2D}{(1-D)^2}\frac{r_S}{R}P_o=0.37$	$2V_{DF}I_o=1$	0.6
[7]	$\frac{2D^2-4D+4}{(1-D)^4}\frac{r_L}{R}P_o=3.8$	$\frac{(-D^2+2D+1)^2}{D(1-D)^4}\frac{r_S}{R}P_o=9.17$	$\frac{4D^2-7D+5}{(1-D)^2}V_{DF}I_o=6.7$	0.58
[8]	$\frac{3D^2-10D+9}{(1-D)^4}\frac{r_L}{R}P_o=0.45$	$\frac{(3-D^2)^2}{D(1-D)^4}\frac{r_S}{R}P_o=6.85$	$\frac{2D^2-11D+11}{(1-D)^2}V_{DF}I_o=5.5$	0
[9]	$\frac{D^2-2D+2}{(1-D)^4}\frac{r_L}{R}P_o=0.22$	$\frac{2D^2-2D+1}{D(1-D)^4}\frac{r_S}{R}P_o=0.4$	$\frac{4-3D}{1-D}V_{DF}I_o=2.15$	0.23
[10]	$\frac{D^2-2D+2}{(1-D)^4}\frac{r_L}{R}P_o=1$	$\frac{2D^3-6D^2+5D}{(1-D)^4}\frac{r_S}{R}P_o=0.2$	$\frac{2-D}{1-D}V_{DF}I_o=1.5$	0.5
[11]	$\frac{1+D^2}{(1-D)^4}\frac{r_L}{R}P_o=1$	$\frac{D^3-2D^2+2D}{(1-D)^4}\frac{r_S}{R}P_o=0.5$	$\frac{1}{1-D}V_{DF}I_o=1$	0.5
[12]	$\frac{D^2-2D+5}{(1-D)^4}\frac{r_L}{R}P_o=1.18$	$\frac{(1+2D-D^2)^2}{D(1-D)^4}\frac{r_S}{R}P_o=9.2$	$\frac{D^2-4D+5}{(1-D)^2}V_{DF}I_o=8.54$	0.58
[13]	$\frac{2}{(1-D)^2}\frac{r_L}{R}P_o=0.23$	$\frac{4}{D(1-D)^4}\frac{r_S}{R}P_o=3.1$	$\frac{4-2D}{1-D}V_{DF}I_o=2.5$	0.34
[14]	$\frac{D^2-2D+2}{(1-D)^4}\frac{r_L}{R}P_o=1.46$	$\frac{D(2-D)^2}{(1-D)^4}\frac{r_S}{R}P_o=1.4$	$\frac{1+D-D^2}{(1-D)^2}V_{DF}I_o=3.1$	0.55

and it was found that they were in good agreement with the assumed and obtained values, although some differences may be due to the circuit components' parasitic components in the simulation model. During the ON mode, the semiconductors pass current. Based on the considerations in this section and the theoretical equation derived in the second section, the average current values for the boost and buck modes are expressed as (19) and (20), respectively.

$$Boost \begin{cases} V_{C1}=72V, & V_{C2}=67V, \ V_O=94V \\ I_{L1}=5.25A, & I_{L2}=1.8A, \ I_{L3}=0.95A \end{cases} \tag{17}$$

$$\begin{bmatrix} \dot{i}_{L_1} \\ \dot{i}_{L_2} \\ \dot{i}_{L_3} \\ \dot{v}_{C_1} \\ \dot{v}_{C_2} \\ \dot{v}_{C_o} \end{bmatrix} = \begin{bmatrix} 0 & 0 & 0 & \frac{D-1}{L_1} & 0 & 0 \\ 0 & 0 & 0 & \frac{D}{L_2} & \frac{D-1}{L_2} & 0 \\ 0 & 0 & 0 & \frac{D}{L_3} & \frac{D}{L_3} & \frac{-1}{L_3} \\ \frac{1-D}{C_1} & \frac{-D}{C_1} & \frac{-D}{C_1} & 0 & 0 & 0 \\ 0 & 0 & \frac{1}{C_o} & 0 & 0 & \frac{-1}{RC_o} \end{bmatrix} x + \begin{bmatrix} b_{11} \\ b_{21} \\ b_{31} \\ b_{41} \\ b_{51} \\ b_{61} \end{bmatrix} \hat{d}$$

$$\begin{cases} b_{11}=\dfrac{V_{C1}}{L_1}, & b_{21}=\dfrac{V_{C1}+V_{C2}}{L_2}, \ b_{31}=\dfrac{V_{C1}+V_{C2}}{L_2} \\ b_{41}=-\dfrac{I_{L1}+I_{L2}+I_{L3}}{C_1}, & b_{51}=-\dfrac{I_{L2}+I_{L3}}{C_1}, \ b_{61}=0 \end{cases} \tag{12}$$

TABLE 6. Comparing current stresses for [1], [2], [3], [4], [5], [6], [7], [8], [9], [10], [11], [12], [13], [14].

	$\frac{I_{S1}}{I_{in}}$	$\frac{I_{S2}}{I_{in}}$	$\frac{I_{D1}}{I_{in}}$	$\frac{I_{D2}}{I_{in}}$	$\frac{I_{D3}}{I_{in}}$	$\frac{I_{D4}}{I_{in}}$	$\frac{I_{D5}}{I_{in}}$	$\frac{I_{D6}}{I_{in}}$	D
[1]	$D=0.36$	$\frac{1-D}{2-D}=0.44$	$\frac{1-D}{2-D}=0.44$	$\frac{(1-D)^2}{2-D}=0.28$	$\frac{(1-D)^2}{2-D}=0.28$				0.36
[2]	$\frac{1+2D-D^2}{3-D}=0.36$		$D=0.15$	$1-D=0.85$	$\frac{1-D}{3-D}=0.3$	$\frac{1-D}{3-D}=0.3$	$\frac{(1-D)^2}{3-D}=0.25$	$\frac{(1-D)^2}{3-D}=0.25$	0.15
[3]	$\frac{1+D-D^2}{2-D}=0.75$		$D=0.36$	$1-D=0.64$	$\frac{(1-D)^2}{2-D}=0.25$	$\frac{(1-D)^2}{2-D}=0.25$			0.36
[4]	$\frac{2D^2-4D+4}{D^2-2D+3}=1.24$		$\frac{2-2D}{D^2-2D+3}=0.62$	$\frac{D(1-D)}{D^2-2D+3}=0.05$	$\frac{(1-D)^2}{D^2-2D+3}=0.25$	$\frac{1-D}{D^2-2D+3}=0.31$	$\frac{1-D}{D^2-2D+3}=0.31$	$\frac{(1-D)^2}{D^2-2D+3}=0.25$	0.18
[5]	$D=0.5$	$D(1-D)=0.25$	$D(1-D)=0.25$	$(1-D)^2=0.25$					0.5
[6]	$\frac{D}{D+1}=0.37$	$\frac{D}{D+1}=0.37$	$\frac{1-D}{D+1}=0.25$	$\frac{1-D}{D+1}=0.25$					0.6
[7]	$\frac{1+2D-D^2}{2}=0.9$		$1-D=0.42$	$D=0.58$	$\frac{(1-D)(2D-1)}{2}=0.05$	$\frac{(1-D)^2}{2}=0.1$	$\frac{(1-D)^2}{2}=0.1$		0.58
[8]	$\frac{3-D^2}{2(2-D)}=0.75$		0.5	0.5	$\frac{1-D}{2}=0.5$	$\frac{2-D-D^2}{2}=1$	$\frac{1-D}{2}=0.5$	$\frac{(1-D)^2}{2(2-D)}=0.25$	0
[9]	$\frac{D}{D^2-3D+3}=0.1$	$\frac{1-D}{D^2-3D+3}=0.34$	$\frac{(2-D)(1-D)}{D^2-3D+3}=0.6$	$\frac{(1-D)^2}{D^2-3D+3}=0.26$	$\frac{(1-D)^2}{D^2-3D+3}=0.26$				0.23
[10]	$D(2-D)=0.75$	$D(1-D)=0.25$	$1-D=0.5$	$(1-D)^2=0.25$					0.5
[11]	$D(1-D)=0.25$	$D=0.5$	$D(1-D)=0.25$	$(1-D)^2=0.25$					0.5
[12]	$\frac{1+2D-D^2}{2}=0.9$		$\frac{1-D}{2}=0.21$	$\frac{1-D}{2}=0.21$	$\frac{1-D}{2}=0.21$	$\frac{1+D}{2}=0.79$	$\frac{(1-D)^2}{2}=0.1$		0.58
[13]	$\frac{1+2D-D^2}{2}=0.9$		$\frac{1-D}{2}=0.21$	$\frac{1-D}{2}=0.21$	$\frac{1-D}{2}=0.21$	$\frac{1+D}{2}=0.79$	$\frac{(1-D)^2}{2}=0.1$		0.34
[14]	1		$\frac{1-D}{D(2-D)}=0.56$	$\frac{1}{(2-D)}=0.68$	$\frac{1-D}{2-D}=0.31$				0.55

TABLE 7. Comparing voltage stresses for [1], [2], [3], [4], [5], [6], [7], [8], [9], [10], [11], [12], [13], [14].

	$\frac{V_{S1}}{V_o}$	$\frac{V_{S2}}{V_o}$	$\frac{V_{D1}}{V_o}$	$\frac{V_{D2}}{V_o}$	$\frac{V_{D3}}{V_o}$	$\frac{V_{D4}}{V_o}$	$\frac{V_{D5}}{V_o}$	$\frac{V_{D6}}{V_o}$	D
[1]	$\frac{1-D}{2-D}=0.44$	$\frac{1}{2-D}=0.68$	$\frac{1-D}{2-D}=0.44$	$\frac{1}{2-D}=0.68$	1				0.36
[2]	$\frac{2}{3-D}=0.7$		$\frac{1+D}{3-D}=0.4$	$\frac{1-D}{3-D}=0.3$	$\frac{1}{3-D}=0.35$	$\frac{1}{3-D}=0.35$	$\frac{2}{3-D}=0.7$	$\frac{2}{3-D}=0.7$	0.15
[3]	$\frac{1}{2-D}=0.6$		$\frac{D}{2-D}=0.22$	$\frac{1-D}{2-D}=0.38$	$\frac{1}{2-D}=0.6$	$\frac{1}{2-D}=0.6$			0.36
[4]	$\frac{2}{D^2-2D+3}=0.75$		$\frac{1-D}{D^2-2D+3}=0.31$	$\frac{1+D}{D^2-2D+3}=0.44$	$\frac{2}{D^2-2D+3}=0.75$	$\frac{1}{D^2-2D+3}=0.37$	$\frac{1}{D^2-2D+3}=0.37$	$\frac{2}{D^2-2D+3}=0.75$	0.18
[5]	$1-D=0.5$	1	$1-D=0.5$	$2-D=1.5$					0.5
[6]	$\frac{1}{1+D}=0.62$	$\frac{1}{1+D}=0.62$	$\frac{1}{1+D}=0.62$	$\frac{1}{1+D}=0.62$					0.6
[7]	0.5		$\frac{1-D}{2}=0.21$	$\frac{D}{2}=0.29$	0.5	0.5	0.5		0.58
[8]	$2-D=2$		$\frac{1-D}{2(2-D)}=0.25$	$\frac{1-D}{2(2-D)}=0.25$	$\frac{1-D}{2-D}=0.5$	$\frac{D}{2-D}=0.01$	$\frac{1}{2-D}=0.5$	$\frac{1}{2-D}=0.5$	0
[9]	$\frac{1-D}{D^2-3D+3}=0.34$	$\frac{1}{D^2-3D+3}=0.44$	$\frac{1-D}{D^2-3D+3}=0.34$	$\frac{1}{D^2-3D+3}=0.44$	$\frac{2-D}{D^2-3D+3}=0.78$				0.23
[10]	$1-D=0.5$	$D=0.5$	$1-D=0.5$	1					0.5
[11]	1		$\frac{1-D}{2}=0.21$	$\frac{1-D}{2}=0.21$	$\frac{1-D}{2}=0.21$	$\frac{1+D}{2}=0.79$	1		0.5
[12]	1	$1-D=0.5$	$1-D=0.5$	$2-D=1.5$					0.58
[13]	$\frac{2}{3-D}=0.75$		$\frac{1}{3-D}=0.38$	$\frac{1}{3-D}=0.38$	$\frac{2}{3-D}=0.75$	$\frac{2}{3-D}=0.75$			0.34
[14]	$\frac{1}{D(2-D)}=1.25$		$\frac{1-D}{D(2-D)}=0.56$	$\frac{1}{2-D}=0.68$	$\frac{1}{D(2-D)}=1.25$				0.55

$$Buck \begin{cases} V_{C1}=148.5V, & V_{C2}=76.5V, \ V_O=23.5V \\ I_{L1}=0.7A, & I_{L2}=0.45A, \ I_{L3}=0.95A \end{cases} \tag{18}$$

$$Boost \begin{cases} I_{S1}=4A, & I_{S2}=2A \\ I_{D1}=2A, & I_{D2}=1A \end{cases} \tag{19}$$

$$Buck \begin{cases} I_{S1}=0.25A, & I_{S2}=0.5A \\ I_{D1}=0.5A, & I_{D2}=1A \end{cases} \tag{20}$$

According to the simulation results, the semiconductors' average current is obtained as (21) and (22) for the boost and
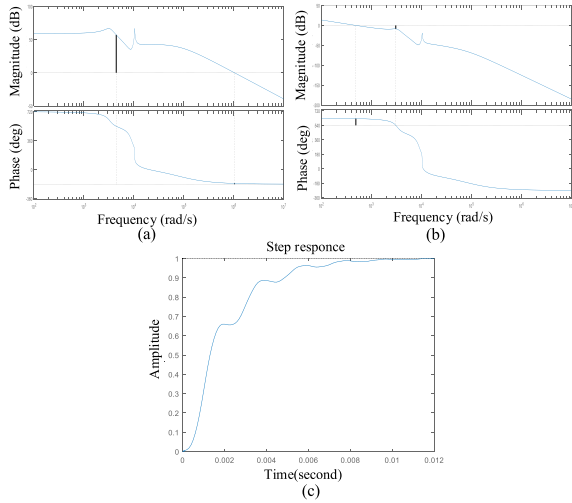
FIGURE 11. (a) Bode diagram before compensation, (b) bode diagram after compensation, (c) step response.
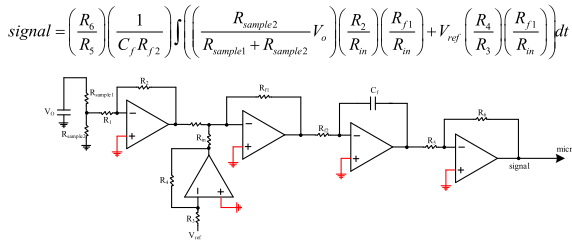
$$signal = \left(\frac{R_6}{R_5}\right)\left(\frac{1}{C_f R_{f2}}\right)\int\left(\left(\frac{R_{sample2}}{R_{sample1}+R_{sample2}}V_o\right)\left(\frac{R_2}{R_{in}}\right)\left(\frac{R_{f1}}{R_{in}}\right)+V_{ref}\left(\frac{R_4}{R_3}\right)\left(\frac{R_{f1}}{R_{in}}\right)\right)dt$$

FIGURE 12. Compensator implementation.

buck modes, respectively.

$$Boost \begin{cases} I_{S1} = 3.9A, & I_{S2} = 1.9A, \\ I_{D1} = 1.9A, & I_{D2} = 0.95A \end{cases} \quad (21)$$

$$Buck \begin{cases} I_{S1} = 0.22A, & I_{S2} = 0.44A, \\ I_{D1} = 0.44A, & I_{D2} = 0.95A \end{cases} \quad (22)$$

The compatibility between the values of the semiconductors' average current obtained from the theoretical equations and simulation results can be evaluated by comparing the corresponding values of (19) and (20) with (21) and (22). The small differences between these values are attributed to the variations in the inductors' current in the theoretical analysis and simulation results. During their OFF mode, the semiconductors are subjected to the applied voltage. The voltage stress on the semiconductors was analyzed and simulated, and the results are presented in (23) to (26) for the boost and buck modes, respectively.

$$Boost \begin{cases} V_{S1} = 75V, & V_{S2} = 150V, \\ V_{D1} = 75V, & V_{D2} = 150V \end{cases} \quad (23)$$

$$Buck \begin{cases} V_{S1} = 150V, & V_{S2} = 75V, \\ V_{D1} = 150V, & V_{D2} = 75V \end{cases} \quad (24)$$
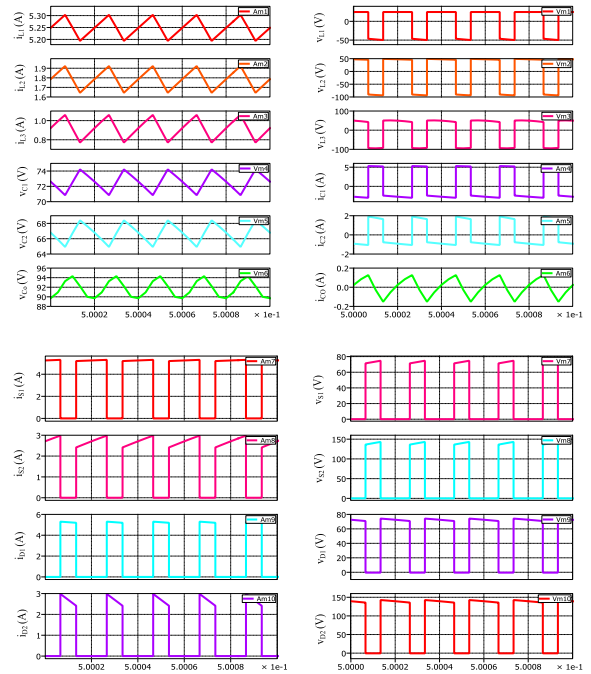
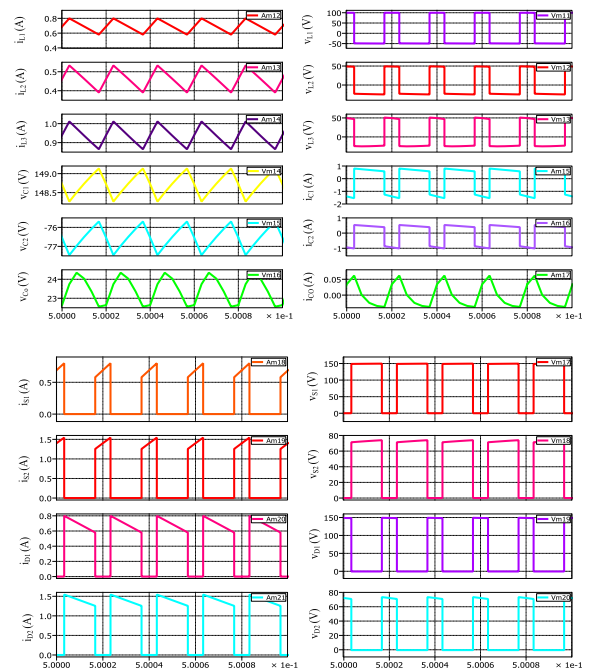**FIGURE 13.** Simulation results (Boost mode)- time unit is second.

FIGURE 14. Simulation results (Buck mode)-time unit is second.

$$Boost \begin{cases} V_{S1} = 72V, & V_{S2} = 145V, \\ V_{D1} = 72V, & V_{D2} = 145V \end{cases} \quad (25)$$

$$Buck \begin{cases} V_{S1} = 147V, & V_{S2} = 72V, \\ V_{D1} = 147V, & V_{D2} = 72V \end{cases} \quad (26)$$

The negligible differences between the corresponding values of equations (23) to (26) are attributed to the parasitic components assumed in the simulation.
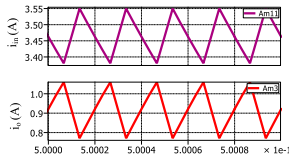
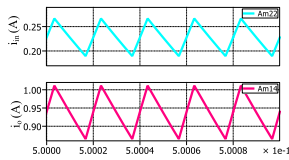**FIGURE 15.** Input/output current based on simulation in boost mode.

FIGURE 16. Input/output current based on simulation in buck mode.

TABLE 8. Design parameters.

	Buck mood	Boost mood
L_1	3000 μH	3000 μH
L_2	2250 μH	2250 μH
L_3	2222 μH	2222 μH
C_1	10 μF	10 μF
C_2	5 μF	5 μF
C_O	62 nF	62 nF
R	100 Ω	25 Ω
f_S	50kHz	50kHz
D	33%	67%
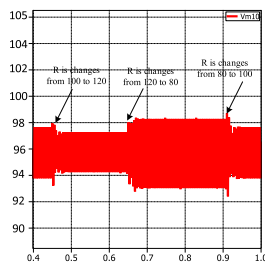
FIGURE 17. Simulation result: control method checking.

To further validate the simulation results and the analysis conducted, experimental results were extracted, consisting of all components' voltage and current waveforms. The controller performance was first tested in Simulink as shown in Fig. 17. The prototype and component values used were the same as those in the simulation design assumptions. The highest calculated values of the inductors and capacitors in the design considerations were used to make the prototype well-formed and well-designed. The inductor cores used were E-E typed, and Litz wires were employed in their structure to minimize the conductors' skin effect. All the capacitors used were of MKT types, which have lower ESR than electrolyte capacitors. This ensures that the capacitors' conduction loss is negligible, and the voltage gain and efficiency experience a lower voltage drop and loss. The MOSFETs used were IRF540, driven with IRF2110, which is capable of driving both the low-sided and high-sided switches, while the diodes used were 2015OCT. Figs. 18 and 19 present the extracted results from the prototype for both the boost and buck modes, respectively, while Figs. 20 and 21 illustrate the input/output currents based on the experimental results

for the boost and buck modes, respectively. Fig. 22 presents the dynamic analysis of the prototype, while Fig. 23 shows the prototype of the converter that was designed to operate at a power level of 100 W, which is a typical power range for applications such as portable devices, LED lighting, and auxiliary circuits in electric vehicles. Fig. 24 illustrates the appropriate connections of IRF2110 for both the low-sided and high-sided switches. The inductors' average current and capacitors' average voltage are reported in equations (27) and (28), respectively.

$$Boost \begin{cases} V_{C1} = 72V, \quad V_{C2} = 72V, V_O = 97V \\ I_{L1} = 5.8A, \quad I_{L2} = 1.9A, I_{L3} = 0.95A \end{cases} \quad (27)$$

$$Buck \begin{cases} V_{C1} = 148.5V, \quad V_{C2} = 76.5V, V_O = 23.5V \\ I_{L1} = 0.7A, \quad I_{L2} = 0.45A, I_{L3} = 0.95A \end{cases} \quad (28)$$

The reported values are in agreement with the corresponding simulation results and design considerations, with any minor discrepancies attributable to parasitic components in the circuit elements. A comparison of the reported values with simulation results and design considerations confirms the governing relationships of the inductors' average current and capacitors' average voltage. As shown in the experimental results, equations (29) and (30) represent the average current of the semiconductors for the boost and buck modes, respectively.

$$Boost \begin{cases} I_{S1} = 4A, \quad I_{S2} = 2A, \\ I_{D1} = 2A, \quad I_{D2} = 1A \end{cases} \quad (29)$$

$$Buck \begin{cases} I_{S1} = 0.25A, \quad I_{S2} = 0.5A, \\ I_{D1} = 0.5A, \quad I_{D2} = 1A \end{cases} \quad (30)$$

The reported values are consistent with the simulation results, and (31) and (32) provide an explanation for the applied voltage to the semiconductors during their OFF mode.

$$Boost \begin{cases} V_{S1} = 72V, V_{S2} = 145V, \\ V_{D1} = 72V, V_{D2} = 145V \end{cases} \quad (31)$$

$$Buck \begin{cases} V_{S1} = 147V, V_{S2} = 72V, \\ V_{D1} = 147V, V_{D2} = 72V \end{cases} \quad (32)$$

The reported values in this study are found to be compatible with the corresponding simulation results, which validate the theoretical relations of the circuit elements. All equations presented in the second section are also validated by the experimental results. Fig. 25 shows the voltage gain of the converter in the non-ideal mode of the circuit components based on theoretical equations, simulation results, and experimental outcomes. The voltage gain variations for the three figures are almost the same when the duty cycle is from 0 to 60 percent. However, beyond that point, differences can be observed due to approximations made during voltage gain analysis and calculation. Despite this, Fig. 26 validates the
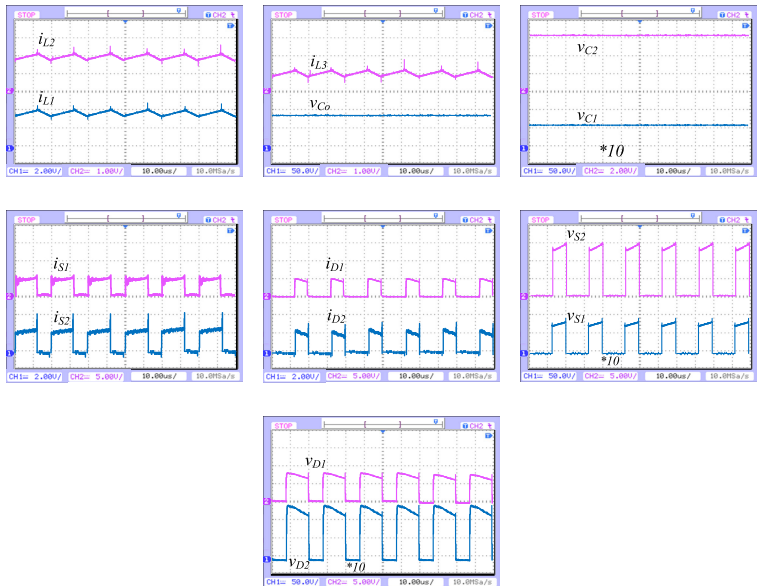
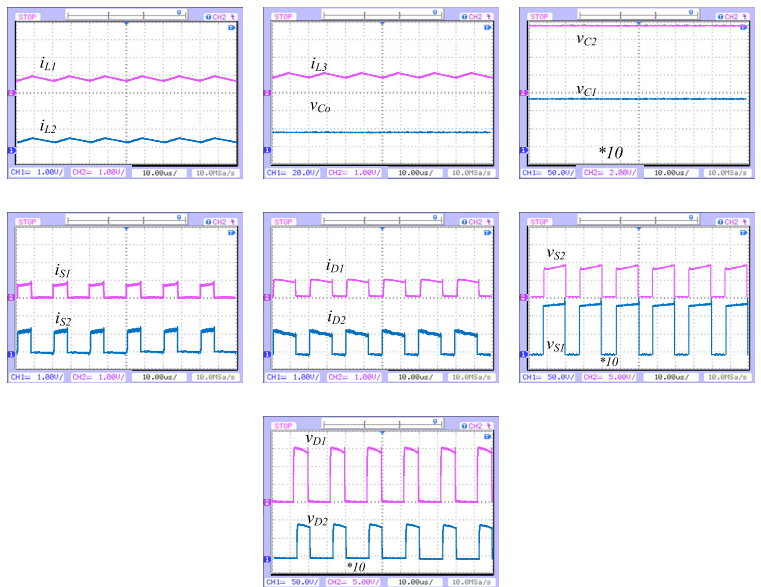**FIGURE 18.** Experimental results: boost mode.

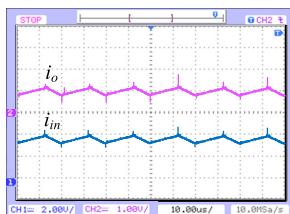**FIGURE 19.** Experimental results: buck mode.

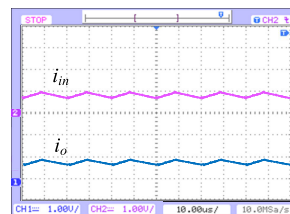**FIGURE 20.** Experimental results: input/output currents in the boost mode.

FIGURE 21. Experimental results: input/output currents in the buck mode.

expressed voltage gain in the non-ideal mode of the components.

Fig. 27 illustrates the efficiency of the proposed topology based on theoretical equations, simulation outcomes,

and experimental results. The efficiency values from the theoretical and simulation results are close, with negligible differences. However, the experimental results show lower efficiency due to hysteresis and eddy current loss of inductors,
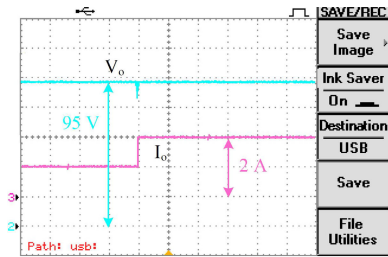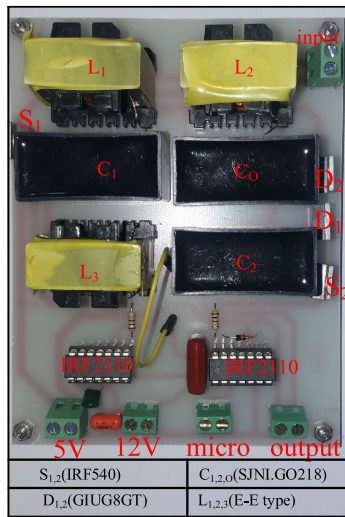
FIGURE 22. Experimental results: dynamic response.

FIGURE 23. The prototype of the converter.

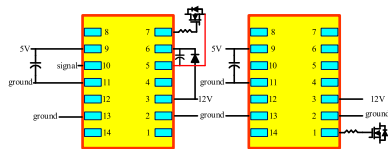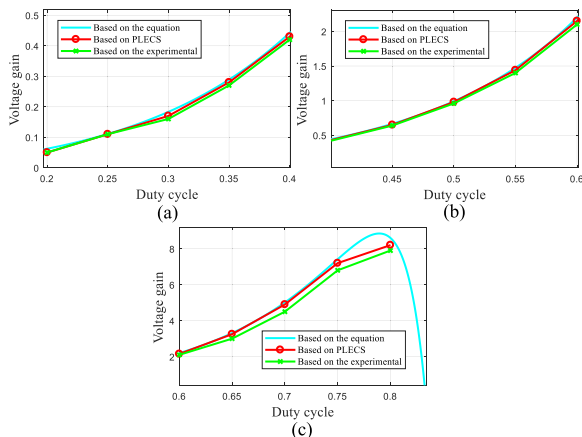| S$_{1,2}$(IRF540) | C$_{1,2,o}$(SJNI.GO218) |
| D$_{1,2}$(GIUG8GT) | L$_{1,2,3}$(E-E type) |

FIGURE 24. IRF2110.

FIGURE 25. Voltage gain based on the theory, simulation, and experiment, while the duty cycle varies: (a) from 20% to 40%, (b) from 40% to 60%, and (c) from 60% to 80%.
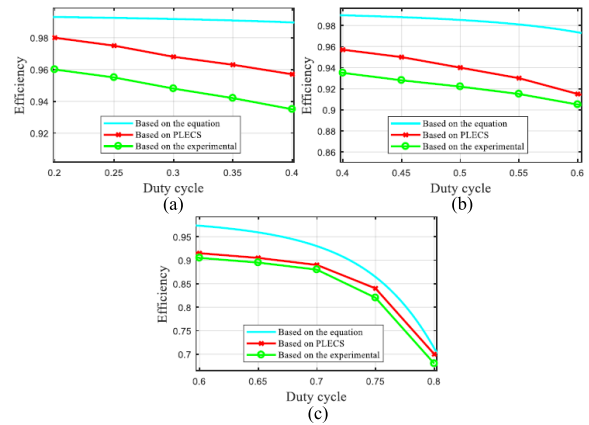

FIGURE 26. Efficiency variations versus the duty cycle variations: (a) from 20% to 40%, (b) from 40% to 60%, and (c) from 60% to 80%.

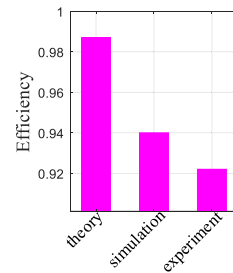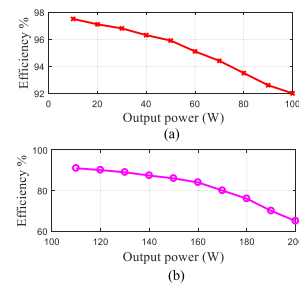**FIGURE 27.** Efficiency at the operating point.

FIGURE 28. Efficiency at the fixed duty cycle and varying output power.

as well as frequency loss of diodes. The graph presents efficiency variations when the power is 100 W, the duty cycle

is 67 percent, the output voltage is 100 V, and the switching frequency is 50 kHz. In Fig. 28, the efficiency of the converter is shown for a 67% duty cycle and varying output power from 10 W to 200 W according to the experimental results. It can be observed that higher output powers lead to efficiency drops due to increased losses.

Fig. 29 and Fig. 30 respectively present the variations of the converter's voltage gain and efficiency when different components are used. The E-E, E-I, and toroidal types are the different inductor types, with the E-E type providing higher inductance with less volume, resulting in increased power density. IRF540, IRF630, and VMK16N70OCT are the studied MOSFETs, with the first two suitable for low-voltage applications and able to withstand currents less than 20 A, while the last one is suitable for high-voltage applica-
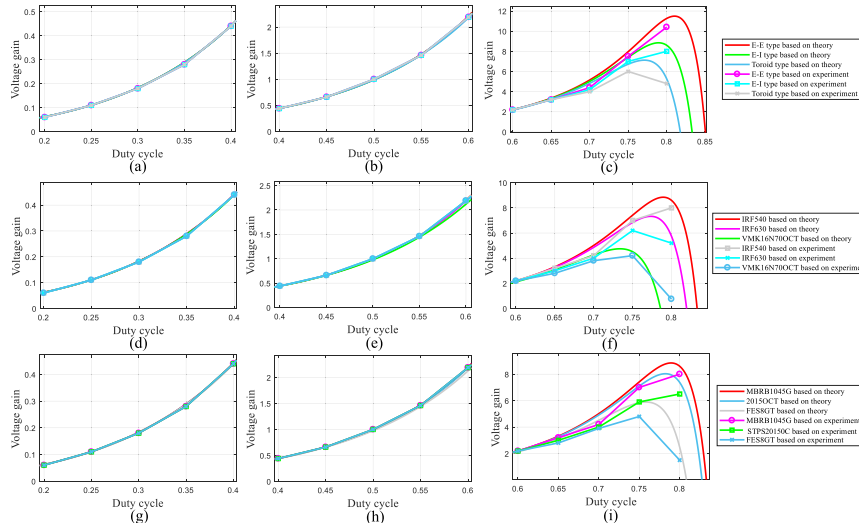
FIGURE 29. Sensitivity analysis of the voltage gain for: (a)-(c) different inductors, (d)-(f) different switches, and, (g)-(i) different diodes.
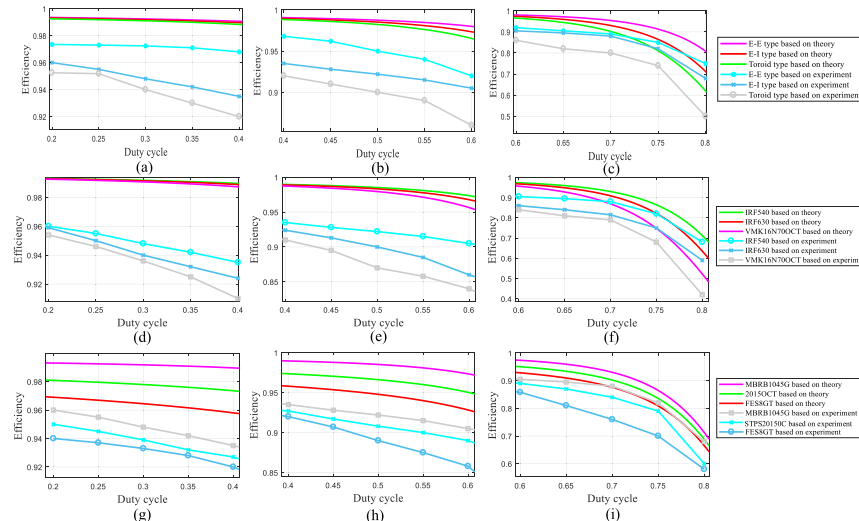

FIGURE 30. Sensitivity analysis of the efficiency for: (a)-(c) different inductors, (d)-(f) different switches and, (g)-(i) different diodes.

tions. MBRB1045G, STPS2015OCT, and FES8GT are the diodes used, with MBRB1045G providing low voltage drop, STPS2015OCT and FEST8GT suitable for low-current applications. Fig. 29(a)-(c), Fig. 29(d)-(f), and 29(g)-(i) respectively correspond to the variations of voltage gain versus duty cycle for different inductors, switches, and diodes. The same goes for Fig. 30(a)-(c), Fig. 30(d)-(f), and 30(g)-(i), which respectively correspond to the variations of efficiency versus duty cycle for different inductors, switches, and diodes. It is important to note that the higher the resistance, the higher the loss will be, leading to lower efficiency, as per the rule of thumb.

VIII. CONCLUSION

This research proposes a novel transformer-less quadratic buck-boost converter topology that offers higher voltage gain, and lower current stress on input and output capacitors. The proposed converter provides unique advantages, including high efficiency, small size, and common ground between the source and load. The steady-state behaviour of the converter was analyzed, and mathematical models for both ideal and non-ideal cases were derived. Simulation and experimental results obtained from a 100 W prototype validate the design, which has promising applications in various fields, such as renewable energy, automotive, and aerospace, where small size and high efficiency are critical requirements. The comprehensive analysis of the converter's steady-state behaviour and controller design provides a deeper understanding of the converter's performance.

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