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APPLIED RESEARCH

Leveraging Public Information to Fit a Compact Hot Carrier Injection Model to a Target Technology

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ABSTRACT The design of countermeasures against integrated circuit counterfeit recycling requires the ability to simulate aging in CMOS devices. Electronic design automation tools commonly provide this ability; however, their models must be tuned for use with a specific target technology. This requires data which is ideally provided by a fab. It may also be collected from a set of purpose-built test devices, a costly and time-consuming process. Here we describe a novel, low-cost, and rapid approach to tuning such models. Our iterative method leverages public domain data sourced from published studies to fit an aging model. Results are statistically validated against the target technology's specification. We demonstrate our approach by fitting a compact hot carrier injection degradation model for use with both core and I/O nMOSFETs from a specific 65 nm technology. Our resulting model parameter values are validated with a maximum error of 0.5 % with a 99 % confidence bound.

INDEX TERMS Aging, circuit simulation, degradation, hot carrier injection stress effect, integrated circuit modeling, iterative methods, semiconductor device reliability.

I. INTRODUCTION

The modern electronic industry relies on globally distributed supply chains of a size and complexity that it is difficult, if not impossible, for a company to fully control its supplier network. This has made the industry a tempting target for counterfeiters. Beyond the economic impact, on the scale of $100 billion annually [1], counterfeit electronic components can severely impact the safety and reliability of critical systems in areas such as health care, defense, and transportation [2]. Recycled components, where used components are recovered from waste and resold as new, are a particularly vexing class of counterfeits which have been identified by the U.S. Department of Defense as the greatest threat to the reliability of its systems [3].

Combatting counterfeiting through recycling requires identifying circuits which have begun to age but still operate within specifications. CMOS integrated circuits (ICs) are all affected by aging mechanisms which degrade their performance with use [4]. Eventually this degradation is significant enough that an aged circuit can no longer operate within specifications.

Electronic design automation (EDA) tools are equipped with facilities to simulate the effects of CMOS degradation mechanisms so that system lifetimes may be predicted. Since these modeling facilities can be used to predict performance degradation over time, they can be used in the design of recycling countermeasures. The degradation models are not generic and must be tuned to a target CMOS technology if they are to produce accurate results. Fabs are the authoritative source of degradation models and the data required to tune EDA models to their technologies, but this is sensitive information which they tightly control and do not always share with academic researchers. An alternative would be to build and characterize one's own test devices, a process which can be costly and time-consuming.

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As academics engaged in early-stage design exploration of recycling countermeasures we required the ability to tune a CMOS degradation model without relying on fab data nor the fabrication of test devices. In this work we propose a search based method for identifying aging model parameters that leverages public domain data. Results are validated by estimating lifetime statistics through Monte Carlo simulation for comparison against a target technology's specifications.

Though we demonstrate out method with a hot carrier injection (HCI) degradation model, it is not model specific. HCI is attractive for recycling countermeasures because it causes irreversible degradation in the form of a permanent shift in threshold voltage [5]. Charge carriers in a MOSFET's channel can gain substantial energy near the drain. These energetic carriers, traditionally called hot carriers, may end up being injected into the gate oxide. When this occurs the interface between the oxide and channel is damaged, causing a permanent shift in the threshold voltage. This has traditionally been described in longer channel devices by the lucky electron model where the driving force is the lateral electric field. Under this model peak HCI degradation is correlated with peak substrate current, which roughly occurs when $V_{GS} = \frac{1}{2} V_{DS}$. In devices with channel lengths shorter than about 250 nm hot carriers are better described by an energy driven model where the effect depends on the total available energy rather than the lateral electric field. Under this regime peak HCI degradation occurs when $V_{GS} = V_{DS}$ [5]. We focus on fitting the model to nMOSFETs since pMOSFETs are not seriously affected by HCI [5].

Our target technology is a 65 nm process from Taiwan Semiconductor Manufacturing Co., LTD (TSMC) [6]. Though this technology is now far from cutting edge it is still relevant. Mature CMOS technologies, which are defined as 40 nm and older, represent 54% of currently installed fab capacity [7]. They are reliable and dominate applications where safety is paramount, such as the automotive industry [7].

We also validated our results at the circuit level by matching the accuracy of a previously reported model [8] when simulating HCI degradation in an inverter.

Our contributions through this work are threefold.

1) We propose a general method for fitting a MOSFET degradation model to a target technology by leveraging public domain data. The solution produces results which are statistically validated against the target technology's specifications.
2) We demonstrate the application of our method by fitting an HCI model to TSMC's 65 nm core and I/O nMOSFETs.
3) We validate our result at the circuit level.

This paper is organized as follows. The model parameter search method, including validation, is presented in section II. Section III details the public domain data used. Our model fitting results are presented in section IV. In section V we validate our results at the circuit level by simulating HCI aging in an inverter. Finally, section VI gives our conclusions.

II. MODEL PARAMETER SEARCH PROCESS

We begin with a general, technology and degradation mechanism agnostic description of our process. We then discuss its use in tuning a HCI model for use with TSMC's 65 nm technology. There are two requirements for implementing our process. First is access to a target technology design kit, including SPICE model files and associated documentation. Second is that the degradation model of interest be of a compact parametric form, i.e. that it be a function of externally observable quantities such as terminal voltages and temperature.

Our parameter search process is iterative and consists of three steps. First, a free search parameter, which controls the search process, is adjusted. Second, a candidate solution is determined through a least-squares fit. Third, the candidate solution is validated. A new iteration is performed if the validation fails.

A. GENERAL DESCRIPTION

In order for a degradation model to accurately predict performance degradation in a target technology, the model needs to be tuned to the technology. This means identifying appropriate values for the model's parameters. This can be done by a least-squares fit if sufficient relevant data is available either directly from a fab or from measurements of test devices. Faced with a lack of such data, we developed the parameter search process depicted in Fig. 1.

The process is initialized by gathering data for use in a least squares fit to the degradation model (Fig. 1, step 1). We relied on two sources: the target technology's reliability rules which are a part of the technology's specifications, and public domain data sourced from peer-reviewed studies.

The reliability rules describe the device time to failure (TTF) statistical distribution under an operating condition selected to accentuate a given degradation mechanism. The specified operating condition and the TTF information are used to create a synthetic data point Λ which serves as the free search parameter. As will be explained shortly, Λ introduces an extra degree of freedom into the fitting process.

This synthetic point is intended to be a plausible degradation measurement of a target technology device. If the reliability rules provide the average TTF, Λ would represent a measurement from a typical device. If the average is not provided, other available TTF information such as a distribution quantile must be used. In such a case, Λ would represent a measurement from a realistic, though atypical device. Only one such point can be constructed because the reliability rules do not specify multiple operating conditions. Being a single data point, Λ cannot be used on its own to perform a least-squares fit.

Additional data which covers multiple operating conditions spanning the degradation model's dimensions is required to perform a least-squares fit. This was sourced from publicly available peer-reviewed studies. Unfortunately a single study is unlikely to provide sufficient data to span

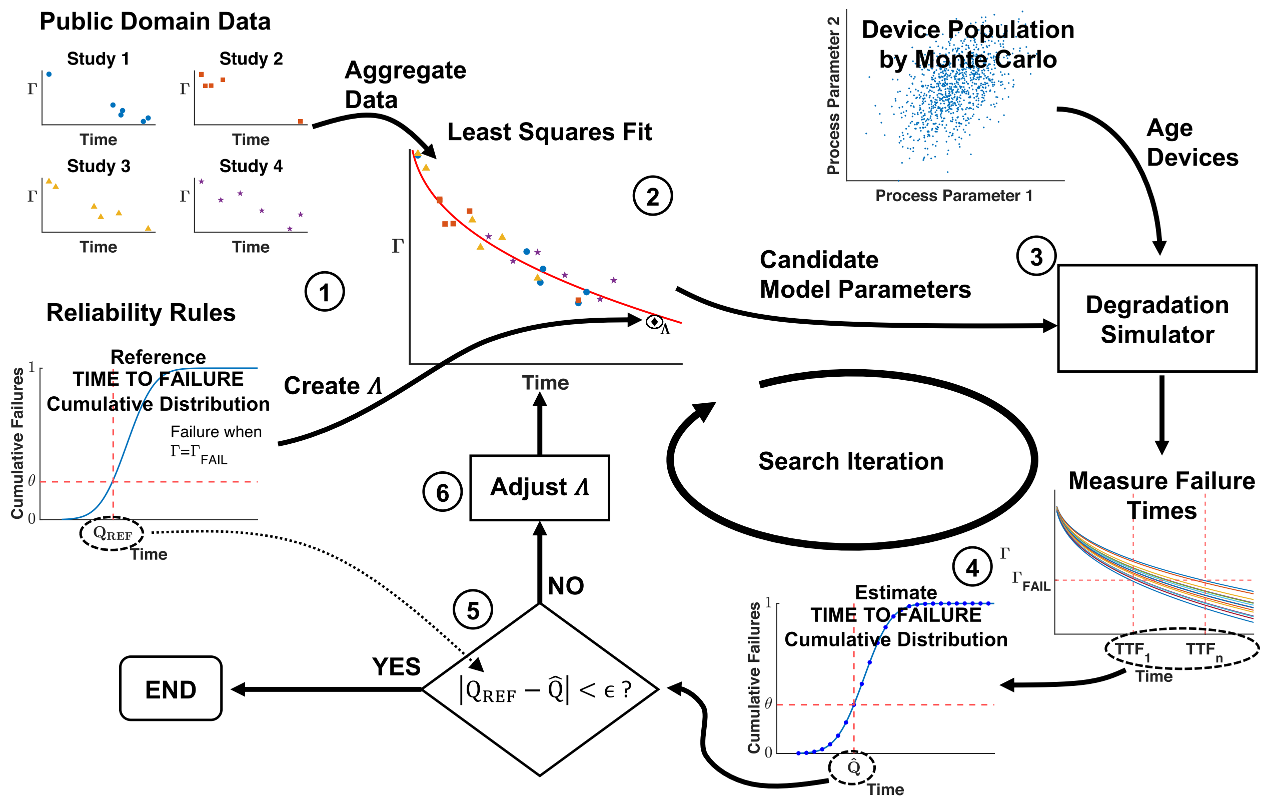

FIGURE 1. Illustration of the degradation model parameter search process. The degradation mechanism causes a reduction in the quantity Γ over time. 1. Data is aggregated from the public domain and Λ is constructed from the target technology reliability rules. In this illustration the reliability rules specify the TTF quantile Q_{REF}, the time by which a portion θ of devices fail. 2. A least squares fit is performed to determine candidate model parameters. 3. The candidate model parameters are used to simulate aging in a population of devices generated through a Monte Carlo process. 4. A time to failure distribution is computed from the simulation results and used to estimate $\hat{Q}$, the time by which θ of the population failed. 5. The validation checks the estimate $\hat{Q}$ against the reference Q_{REF}. 6. If the validation fails Λ is adjusted and a new iteration is performed.

all of a degradation model's dimensions. Thus we aggregated data from multiple studies. A complicating factor is that few studies explicitly identify the precise CMOS technology involved. In response we made the assumption that the effects of a degradation mechanism generalize across similar CMOS technologies. Since materials and device geometries are similar across such technologies, we surmised that degradation effects are also similar. Under this assumption, degradation model parameters for similar technologies fall into a near-neighborhood of the parameter space. Model parameters found through a least-squares fit to data aggregated from several similar technologies will also fall into this near-neighborhood. By iteratively adjusting Λ this near-neighborhood is searched until a solution for a specific target technology can be validated.

A least squares fit to the aggregated data is performed to determine a set of candidate degradation model parameters (Fig. 1, step 2). Because most or even all of the public domain data may not be from the target technology, the role of Λ is to bias the fit towards the target technology. The parameter near-neighborhood is searched by adjusting Λ. Different adjustments are possible depending on the information provided by the reliability rules. One possibility may be to change Λ's weight relative to the rest of the data. This strategy may be a good choice if the average TTF is used in constructing Λ. If only a TTF quantile is available, adjusting the time value of Λ may be an option. In this way, Λ may be moved towards a more typical measurement.

Validation of a candidate parameter set consists of generating estimated lifetime statistics for comparison against the reliability rules. A population of devices is first generated in a Monte Carlo simulation using a process, voltage, and temperature (PVT) variation device model provided by the target technology's design kit. This population is then aged according to the degradation model using the candidate parameter set (Fig. 1, step 3) and the same operating conditions as in the reliability rules. An estimate of the TTF distribution is then calculated from this simulation data (Fig. 1, step 4) and compared to the reference distribution from the reliability rules (Fig. 1, step 5). If the validation fails, a new search iteration begins with an adjustment to Λ (Fig. 1, step 6).

In summary, our model parameter search process is initialized with the construction of Λ from the target technology's reliability rules, and the collection of relevant public domain

data. The iterative search begins with the adjustment of the free search parameter. This may be the weight of Λ and/or Λ's degradation time. Next, a least-squares fit of the degradation model to the public domain data along with Λ is performed. Finally, the candidate model parameters are validated by their use in aging a simulated population of devices for comparison against the reliability rules. A new iteration is begun if the validation fails.

B. APPLICATION EXAMPLE

We now describe the application of our parameter search process to fitting an HCI model from Synopsys HSPICE [9] for use with TSMC's 65 nm technology. We first describe the HCI model as well as pertinent information from the reliability rules. We then describe the construction of Λ, including its initialization. Finally we describe the iterative search steps.

HSPICE is used to generate and age the simulated device population. Results are then pre-processed with a custom Python script and imported into MATLAB [10] where the rest of the steps are performed. These different tools are coordinated through a custom shell script.

1) HCI MODEL

Synopsys HSPICE includes the MOSFET Reliability Analysis (MOSRA) facility which provides the ability to perform circuit reliability analysis under the influence of HCI as well as another degradation mechanism, bias temperature instability (BTI). MOSRA allows the effects of BTI and HCI to be considered either in combination or in isolation of each other and provides three modeling approaches for each mechanism. The most straightforward to work with are the level 3 models which are parameterized compact models. For HCI, degradation is expressed as a percentage change in the drain current:

$$\Delta I_D(\%) = A_\mathrm{p} \cdot \mathrm{e}^{(G \cdot V_\mathrm{GS})} \cdot \mathrm{e}^{(D \cdot V_\mathrm{DS})} \cdot \mathrm{e}^{\left(\frac{-E_\mathrm{a}}{kT}\right)} \cdot \mathrm{e}^{(-m \cdot L)} \cdot t^n. \quad (1)$$

The stresses giving rise to this degradation are described by the variables listed in Table 1. It should be noted that the model depends on the polysilicon length (i.e. gate length) rather than the actual channel length. Table 2 lists the model's parameters, the values of which are target technology dependent. Synopsys suggests default values for several parameters which are claimed to be sufficient for many situations [9]. For brevity, (1) will be referred to as the MOSRA model in the rest of this work.

TABLE 1. MOSRA HCI Compact Model Variables [9].

Variable	Unit	Description
V_GS	V	Gate-source bias.
V_DS	V	Drain-source bias.
T	K	Channel temperature.
L	µm	Polysilicon length.
t	s	Total stress time.

TABLE 2. MOSRA HCI Compact Model Parameters [9].

Parameter	Unit	Default Value (Synopsys)	Description
A_p	-	0	Pre-factor.
G	V^{-1}	0	V_GS dependence.
D	V^{-1}	9.0	V_DS dependence.
E_a	eV	0.05	Temperature acceleration.
m	$\mathrm{\mu m}^{-1}$	2.0	Polysilicon length dependence.
n	-	0.5	Time dependence.

When describing a set of measurements, the MOSRA model can be logarithmically scaled and expressed in matrix form as

$$\Delta \mathbf{I}_\mathbf{D,log} = \mathbf{S} \cdot \mathbf{v}, \quad (2)$$

where the vectorized MOSRA model variables are grouped as the matrix

$$\mathbf{S} = \left[\mathbf{1}\ \mathbf{V}_\mathbf{GS}\ \mathbf{V}_\mathbf{DS}\ (k\mathbf{T})^{-1}\ \mathbf{L}\ \ln(\mathbf{t})\right]$$

and the MOSRA model parameters form the vector

$$\mathbf{v} = \left[\ln(A_\mathrm{p})\ G\ D\ -E_\mathrm{a}\ -m\ n\right]^\mathrm{T}.$$

For d data points, $\Delta \mathbf{I}_\mathbf{D,log} \in \mathbb{R}^d$, $\mathbf{S} \in \mathbb{R}^{d\times 6}$, and $\mathbf{v} \in \mathbb{R}^6$. This system has a unique least squares solution $\mathbf{v}$ while the matrix $\mathbf{S}$ is full column rank [11].

2) RELIABILITY RULES

The TSMC 65 nm reliability rules pertaining to HCI [6] define a failure as a 10% reduction in drain current in the saturation region ($I_\mathrm{D,sat}$) relative to initial conditions. For each device type (e.g. core and I/O), a constant voltage and temperature operating condition selected to accentuate HCI stress are prescribed and the resulting 10^{-3} TTF quantile, $Q^{0.001}_\mathrm{REF}$, is given. This is the time by which one out of a thousand devices is expected to have failed under to the prescribed operating conditions. Validation consists of comparing $Q^{0.001}_\mathrm{REF}$ to $\hat{Q}^{0.001}$, the estimated the 10^{-3} TTF quantile which results from a candidate set of model parameters $\mathbf{v}$.

3) FREE SEARCH PARAMETER INITIALIZATION

Λ, which corresponds to a row in $\left[\Delta \mathbf{I}_\mathbf{D,log} | \mathbf{S}\right]$, is constructed from the reliability rules. Its $\Delta I_\mathrm{D,log}$ is set to ln(10) since a failure is a 10% degradation. The variables V_GS, V_DS, T, and L are as specified in the reliability rules.

Because the reliability rules only provide $Q^{0.001}_\mathrm{REF}$, we use the degradation time t_Λ as the free search parameter. It is initialized to $Q^{0.001}_\mathrm{REF}$ and adjusted in each search iteration. Adjustments to t_Λ are informed by the mapping $t_\Lambda \to \hat{Q}^{0.001}$, the exact form of which is unknown. However, so long as the adjustments are kept small, the mapping can be approximated as linear and calculated iteratively.

Setting the weight of Λ relative to the rest of the data during fitting is done at this point. A desirable weight for Λ

should allow $\hat{Q}^{0.001}$ to quickly reach $Q^{0.001}_{\mathrm{REF}}$ with a few small adjustments to t_Λ. As its weight increases, Λ becomes more influential in the fitting step. This causes $\hat{Q}^{0.001}$ to be more sensitive to t_Λ. Too large a weight however risks causing Λ to completely overshadow the rest of the data. To determine an appropriate weight value, the dependence of $t_\Lambda \to \hat{Q}^{0.001}$ on Λ's weight was estimated for several weight values. To avoid performing the great number of Monte Carlo simulations which would be required to calculate $\hat{Q}^{0.001}$, $t_\Lambda \to \hat{Q}^{0.001}$ wass approximated as $t_\Lambda \to t_{\mathrm{FAIL}}$, where t_{FAIL} is the time at which the MOSRA model predicts a 10% degradation in a typical device under the reliability rules' operating conditions. Effectively, t_{FAIL} is the mean TTF resulting from a given $\mathbf{v}$. We assumed that the TTF distribution had a small variance, resulting in $\hat{Q}^{0.001}$ to be close to t_{FAIL}. Fig. 2 shows the result of sweeping t_Λ by $\pm 10\%$ from its initial value for various weights of Λ. The weight was adjusted by adding extra copies of Λ to the fitting data. A weight of 100% corresponds to as many copies as there are public domain data points. Here a weight of 50% is a good choice as this allows t_{FAIL} to reach $Q^{0.001}_{\mathrm{REF}}$ with only a small adjustment to t_Λ. Increasing the weight past this does not offer any significant advantage.

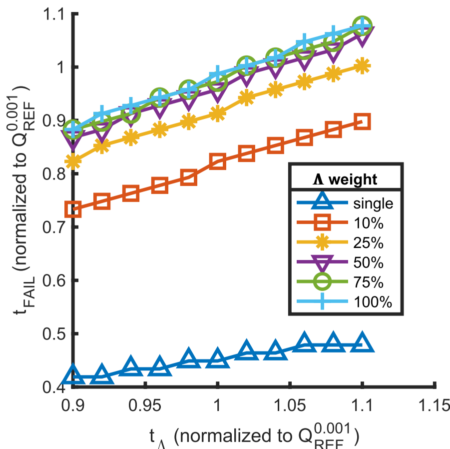

FIGURE 2. Dependence of t_{FAIL} on t_Λ for various weights of Λ relative to the number of public domain data points. A weight of 100% means Λ has as much weight as all public domain points combined. A weight of single means Λ has a weight equal to a single public domain point.

4) FREE SEARCH PARAMETER ADJUSTMENT

Adjusting t_Λ depends on the current search iteration. In the ith iteration t_Λ and $\hat{Q}^{0.001}$ are labelled as $t_{\Lambda,i}$ and $\hat{Q}^{0.001}_i$ respectively. We also introduce $\Delta\hat{Q}^{0.001}_{i-1} = Q^{0.001}_{\mathrm{REF}} - \hat{Q}^{0.001}_{i-1}$.

1) For $i = 1 : t_{\Lambda,i} = Q^{0.001}_{\mathrm{REF}}$.
2) For $i = 2$: $t_{\Lambda,i} = t_{\Lambda,i-1} + \frac{\partial t_\Lambda}{\partial t_{\mathrm{FAIL}}}\Delta\hat{Q}^{0.001}_{i-1}$.
3) For $i > 2$: $t_{\Lambda,i} = t_{\Lambda,i-1} + \frac{\partial t_\Lambda}{\partial \hat{Q}^{0.001}}\Delta\hat{Q}^{0.001}_{i-1}$.

$\frac{\partial t_\Lambda}{\partial t_{\mathrm{FAIL}}}$ was found when determining Λ's weight (see Fig. 2). $\frac{\partial t_\Lambda}{\partial \hat{Q}^{0.001}}$ is derived from a linear regression to the set of pairs $\left\{\left\langle t_{\Lambda,j}, \hat{Q}^{0.001}_j\right\rangle \mid j = 1\ldots i\right\}$. A new $\mathbf{v}$ is computed based on the updated value of t_Λ.

5) LEAST SQUARES FIT

$\mathbf{S}$, which is composed of public domain data and multiple copies of Λ, remains largely unchanged between search iterations. Only t_Λ is updated. Once this is done, a new least squares solution $\mathbf{v}$ to (2) is computed.

6) VALIDATION

If $\left|\hat{Q}^{0.001} - Q^{0.001}_{\mathrm{REF}}\right| > \epsilon$ the validation fails and a new search iteration begins. To compute $\hat{Q}^{0.001}$ we need a TTF sample population. The TSMC 65 nm design kit includes support for Monte Carlo simulations across process, voltage, and temperature (PVT) variations. This is used to generate a sample population of devices which are then individually aged using the MOSRA model with the current value of $\mathbf{v}$. When estimating a quantile Q^θ from a Monte Carlo simulation, the sample population should be larger than θ^{-1} [12], hence to estimate the 10^{-3} quantile we used a sample population of 10^4. The voltages and temperature are those specified by the reliability rules. This is all carried out in HSPICE. We then compute an estimate of the TTF cumulative distribution function (CDF) with the Kaplan-Meier estimator, a maximum likelihood estimator often used in failure analysis [13]. Once the CDF is estimated, $\hat{Q}^{0.001}$ is found by a simple lookup operation. We also calculate the confidence bounds on $\hat{Q}^{0.001}$ by estimating the confidence bounds on the TTF CDF using Greenwood's formula [13].

III. DATA SOURCES

The public domain data needed to satisfy three criteria:

1) express HCI degradation as a decrease in $I_{\mathrm{D,sat}}$;
2) have been measured from devices from a 65 nm technology;
3) fully span $\mathbf{S}$, meaning that the recorded HCI degradation was in response to variations in all of the dimensions of $\mathbf{S}$.

Identifying peer-reviewed studies which met these criteria was challenging. To increase the pool of data we assumed that the MOSRA model generalizes across technologies of comparable node size. This allowed us to combine data from different studies so long as they recorded HCI degradation as a shift in drain current in a 65 nm technology device. Even so, we were unable to identify enough data to entirely span $\mathbf{S}$. To resolve this we employed the default values suggested by Synopsys for the parameters E_a (temperature acceleration) and m (polysilicon length dependence) (see Table 2), reducing the dimensionality of the problem by two. We identified the 5 studies described below which met our needs. These studies are not all recent since 65 nm technologies are now several generations old, although still in common use. We used WebPlotDigitizer [14] to extract data from the plots reproduced below.

Fig. 3 is drawn from Fakhruddin et al., which examined the RF performance degradation of nMOSFETs from an unspecified 65 nm technology with test devices whose dimensions were $W/L = 1.2\,\mu\text{m}/0.06\,\mu\text{m}$ [15]. Fig. 3(a) and Fig. 3(c) reproduce the relevant HCI degradation measurements. All stress voltages were DC and are specified on the plots. Fig. 3(a) shows degradation in response to constant voltage

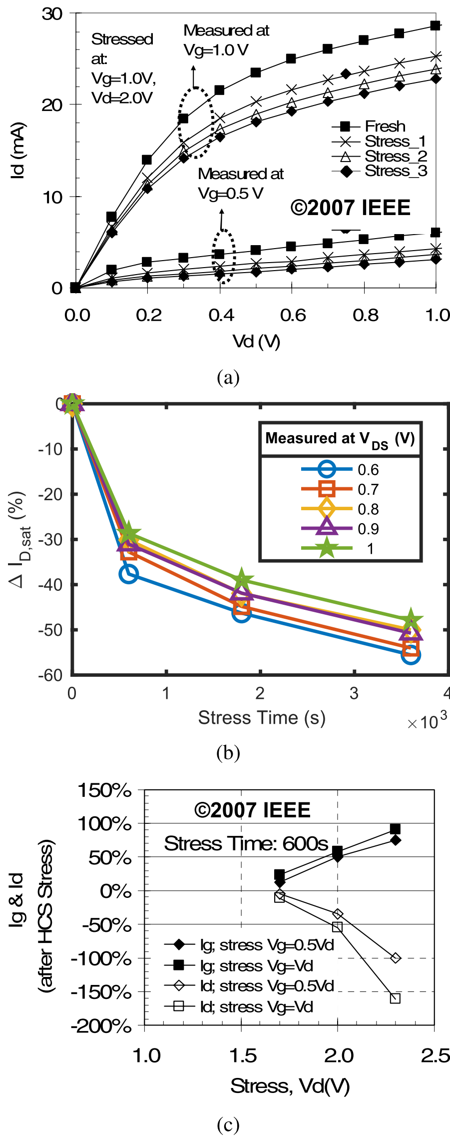

FIGURE 3. HCI measurements from Fakhruddin et al. [15]. (a) $I_D - V_{DS}$ scans performed after 0 s (Fresh), 600 s (Stress_1), 1800 s (Stress_2), and 3600 s (Stress_3) of constant $V_{GS} = 1$ V and $V_{DS} = 2$ V stress [15]. (b) Our conversion of (a) to relative $I_{D,sat}$ degradation over time. (c) Relative $I_{D,sat}$ degradation after 600 s of various DC voltage stresses (open symbols) [15].

stress as a series of $I_D - V_{DS}$ scans performed over time. We used a subset of the depicted measurements. We used data measured under $V_{GS} = 0.5$ V since these values are consistent with Fig. 3(c). Of these values, we only wanted $I_{D,sat}$ measurements so we limited the V_{DS} measurement range to ≥ 0.6 V. Fig. 3(b) shows our remapping of this data to relative $I_{D,sat}$ degradation. Fig. 3(c) shows the relative change in $I_{D,sat}$ after being subjected to various DC voltage stresses for 600 s. It should be noted that the degradation for a V_{DS} stress of 2.3 V was $\Delta I_{D,sat} \leq -100\%$, which is physically meaningless. These points were treated as outliers and excluded. The temperature was not reported and assumed to be 25°C.

Fig. 4 is drawn from Yuan et al., which reported on the performance degradation of a low noise amplifier when subjected to HCI stress [16]. This work was carried out using minimum size devices in TSMC's 65 nm technology. nMOSFET I_D degradation over time was measured as the six $I_D - V_{DS}$ scans reproduced in Fig. 4. The applied V_{DS}

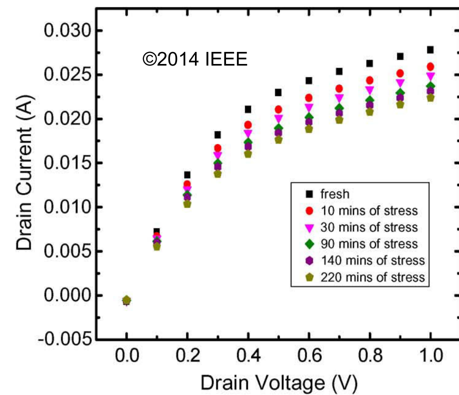

FIGURE 4. HCI measurements from Yuan et al. [16].

stress was 2 V and the over voltage (V_{OV}) stress was 0.35 V. We were able to calculate the stress V_{GS} from the provided V_{OV} by making use of the threshold voltage, which we knew from the design kit [6]. To limit the data to $I_{D,sat}$ we excluded points scanned at $V_{DS} < 0.6$ V. The temperature was not reported and assumed to be 25°C. We converted these measurements to relative $I_{D,sat}$ degradation over time using the same process which yielded Fig. 3(b).

Fig. 5 is drawn from Huard et al. [8]. This work describes a quantitative assessment methodology for HCI and NBTI degradation effects in an unspecified technology of a node size in the 90 nm to 65 nm range. Fig. 5(a) shows HCI dependence on stress V_{GS} for both core (empty triangles) and I/O nMOSFETs (filled triangles). The MOSRA model, which has an exponential dependence on V_{GS}, is a poor match for the I/O device data. Two workarounds are possible. First, we can assume that HCI degradation is independent of V_{GS} in I/O devices. This may be justified by observing that the data suggests HCI dependence on V_{GS} is far weaker in I/O devices than in core devices. Second, we can limit the V_{GS} range to values larger than $\frac{1}{2}V_{DS}$. The data suggests that HCI degradation peaks when $V_{GS} \approx \frac{1}{2}V_{DS}$, which is expected in longer channel devices [5]. This would limit the applicable voltage range for the MOSRA model to $V_{GS} \geq \frac{1}{2}V_{DS}$. Fig. 5(b) shows HCI degradation in an I/O nMOSFET with $W/L = 10\,\mu\text{m}/0.2\,\mu\text{m}$ as a change in $I_{D,sat}$ relative

magnitude over time when subjected to various voltage stresses. The temperature was assumed to be 25°C in all cases.

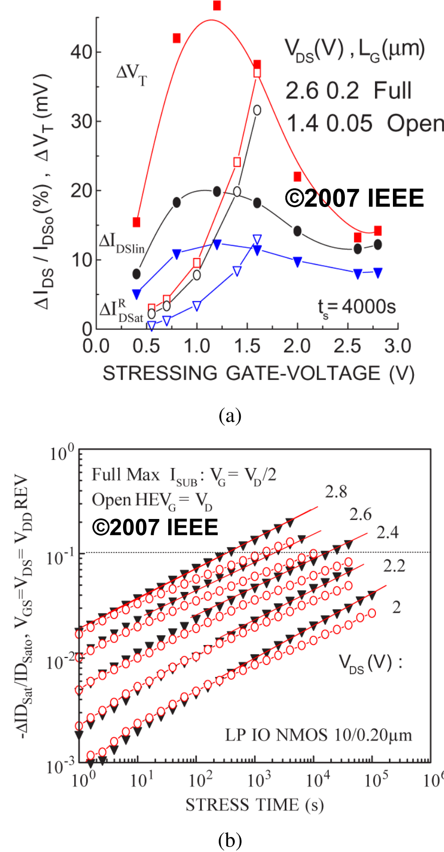

FIGURE 5. **HCI measurements from both core and I/O nMOSFETs [8]. (a) HCI dependence on stress V_{GS} for core (empty triangles) and I/O (filled triangles) nMOSFETs. (b) HCI degradation in an I/O nMOSFET when subjected to V_{DS} ranging from 2 V to 2.8 V and V_{GS} equal to either V_{DS} (circles) or $\frac{1}{2}V_{DS}$ (triangles).**

Fig. 6 is drawn from Xie et al., which examined HCI in annular gate devices intended for radiation hardened circuits [17]. Shown are relative $I_{D,sat}$ degradations over time under the three bias conditions listed in the figure for a conventional planar geometry nMOSFET with $W/L = 6.6\,\mu m/0.06\,\mu m$ fabricated in an unspecified 65 nm technology. The temperature was not reported and assumed to be 25°C.

Fig. 7 is drawn from Ren et al. and depicts HCI degradation in irradiated and unirradiated devices in response to the bias condition described on the figure [18]. The test devices had a $W/L = 0.2\,\mu m/0.06\,\mu m$ and were fabricated in an unspecified 65 nm technology. We only used measurements from unirradiated devices. The temperature was not reported and assumed to be 25°C.

IV. MODEL FITTING RESULTS

We obtained a total of five sets of MOSRA model parameters for TSMC 65 nm standard threshold voltage (STDVT) nMOSFETs: three for core devices and two for I/O devices.

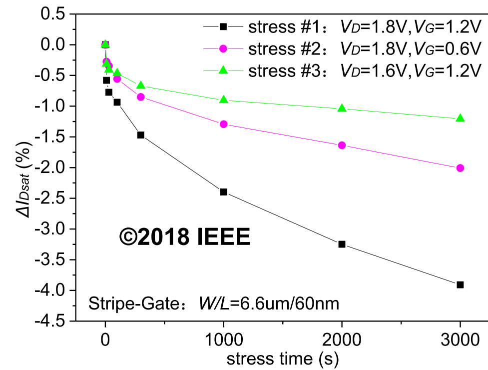

FIGURE 6. **HCI measurements from Xie et al. [17].**

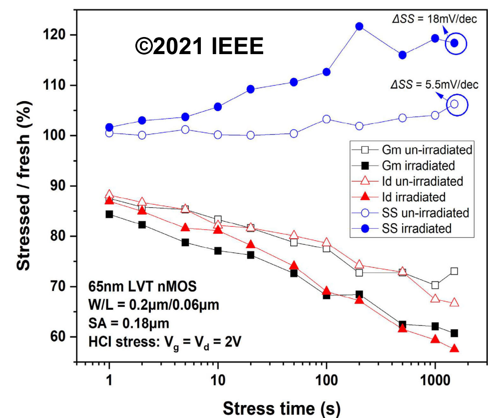

FIGURE 7. **HCI measurements from Ren et al. [18]. Only I_D measurements from the unirradiated device (open triangles) were used.**

The different parameter sets were obtained using different subsets of the public domain data as detailed in Table 3.

TABLE 3. **Public domain data used for determining the parameter sets. $\mathbf{v_{core}}$ are for core nMOSFETs and $\mathbf{v_{IO}}$ are for I/O nMOSFETs.**

	Parameter Set				
	$\mathbf{v_{core1}}$	$\mathbf{v_{core2}}$	$\mathbf{v_{core3}}$	$\mathbf{v_{IO1}}$	$\mathbf{v_{IO2}}$
Fig. 3	✓		✓		
Fig. 4	✓		✓		
Fig. 5(a)	✓		✓		✓
Fig. 5(b)				✓	✓
Fig. 6		✓	✓		
Fig. 7		✓	✓		

The parameters sets for I/O devices resulted from two approaches to using the I/O-relevant data in Fig. 5(a), which cannot be easily modelled by an exponential function. $\mathbf{v_{IO1}}$ resulted from assuming HCI degradation is independent of V_{GS}. It was obtained without the use of Fig. 5(a). $\mathbf{v_{IO2}}$, which assumes dependence on V_{GS}, was obtained by incorporating Fig. 5(a) data for which $V_{GS} \geq \frac{1}{2}V_{DS}$. Consequently $\mathbf{v_{IO2}}$ is only valid over this voltage range.

The parameter sets for core devices were obtained from three groupings of the public domain data. We split the data into two groups based on their geographic origins:

a Western group ($\mathbf{v_{core1}}$) and a Chinese group ($\mathbf{v_{core2}}$). These two groups were amalgamated into a third group ($\mathbf{v_{core3}}$). This was done to judge our underlying assumption that HCI effects are similar in similar technologies. Under the same conditions, devices from different but similar technologies should exhibit similar degradations. To examine this, we simulated the public domain data using a TSMC model and the different MOSRA model parameter sets. If all three $\mathbf{v_{core}}$ sets were to result in comparable simulation errors, then HCI effects would be virtually technology-independent. Otherwise process parameters other than node size would play a role.

Table 4 lists the values for our different parameter sets, and Table 5 summarizes the search settings. The number of data points is for the combined number of public domain points used. Λ weight is defined relative to this number. A weight of w relative to d data points means that wd copies of Λ were used. The search process was fast, reaching convergence in no more than three iterations.

TABLE 4. Derived MOSRA HCI parameter values. Parameters E_a and m assume their default values (see Table 2) in all cases.

Parameter Set	A_p	G	D	n
$\mathbf{v_{core1}}$	3.3191×10^{-4}	2.0473	4.8411	0.25063
$\mathbf{v_{core2}}$	1.1271×10^{-4}	2.2461	4.1104	0.33726
$\mathbf{v_{core3}}$	6.0821×10^{-6}	1.5335	6.3221	0.40415
$\mathbf{v_{IO1}}$	1.4171×10^{-3}	0	3.5089	0.25805
$\mathbf{v_{IO2}}$	1.3961×10^{-3}	-5.6519×10^{-2}	3.5624	0.25576

TABLE 5. MOSRA model parameter search process settings.

	Parameter Set				
	$\mathbf{v_{core1}}$	$\mathbf{v_{core2}}$	$\mathbf{v_{core3}}$	$\mathbf{v_{IO1}}$	$\mathbf{v_{IO2}}$
Data Points	49	32	81	225	229
Λ Weight	0.5	0.4	0.4	1.0	0.5
Monte Carlo Time Step (years)	5×10^{-3}	5×10^{-3}	5×10^{-3}	5×10^{-4}	5×10^{-4}
Search Iterations	2	2	3	3	3

All of our parameter sets passed the validation test with a high degree of confidence, as summarized in Table 6. $Q^{0.001}_{\mathrm{REF}}$ falls within the 99% confidence bounds on $\hat{Q}^{0.001}$ in all cases. From the sizes of the confidence bounds, we can conclude that $\hat{Q}^{0.001}$ differs from $Q^{0.001}_{\mathrm{REF}}$ by at most 0.2% (5.5 days) 99 times out of 100 for $\mathbf{v_{core}}$, and by at most 0.5% (1.2 days) 99 times out of 100 for $\mathbf{v_{IO}}$.

TABLE 6. MOSRA model parameter validation. All values have units of years.

Parameter Set	$Q^{0.001}_{\mathrm{REF}}$	$\hat{Q}^{0.001}$	99% Confidence Bounds	
			Lower	Upper
$\mathbf{v_{core1}}$	6.75	6.755	6.750	6.760
$\mathbf{v_{core2}}$	6.75	6.750	6.745	6.765
$\mathbf{v_{core3}}$	6.75	6.750	6.750	6.755
$\mathbf{v_{IO1}}$	0.6663	0.666	0.6635	0.6695
$\mathbf{v_{IO2}}$	0.6663	0.666	0.663	0.6695

Table 7 summarizes the root mean square (RMS) relative errors of the public domain data simulations using TSMC device models. The average error for $\mathbf{v_{core1}}$ taken over the data used in its derivation is 34%. The equivalent figure for $\mathbf{v_{core2}}$ is 40%. These results suggest that $\mathbf{v_{core1}}$ and $\mathbf{v_{core2}}$ represent technology groupings which are comparably related to the target technology. This seems to support our assumption that HCI effects depend on little more than the node size. However, the average error for $\mathbf{v_{core3}}$ is much larger, 63%. This apparent contradiction can be clarified by noticing that $\mathbf{v_{core1}}$ and $\mathbf{v_{core2}}$ both performed very poorly when simulating data used in each other's derivation. This suggests that $\mathbf{v_{core1}}$ and $\mathbf{v_{core2}}$ represent mutually exclusive technology groupings; consequently, HCI effects depend upon process parameters in addition to node size. Care must therefore be taken when selecting appropriate data. The average error results suggest that the $\mathbf{v_{core1}}$ parameters are more closely related to the target technology than the $\mathbf{v_{core2}}$ parameters. Hence we favor the $\mathbf{v_{core1}}$ parameter set. The $\mathbf{v_{IO}}$ parameter sets led to near identical simulation errors and cannot be clearly differentiated.

TABLE 7. RMS relative error for data set simulations using the MOSRA model and TSMC 65 nm device models.

	Parameter Set				
	$\mathbf{v_{core1}}$	$\mathbf{v_{core2}}$	$\mathbf{v_{core3}}$	$\mathbf{v_{IO1}}$	$\mathbf{v_{IO2}}$
Fig. 3	32%	82%	49%	N/A	N/A
Fig. 4	18%	80%	12%	N/A	N/A
Fig. 5(a)	50%	73%	72%	N/A	15%
Fig. 5(b)	N/A	N/A	N/A	19%	20%
Fig. 6	510%	38%	100%	N/A	N/A
Fig. 7	267%	42%	82%	N/A	N/A

V. CIRCUIT LEVEL VALIDATION

Ultimately, our interest lay in using the MOSRA model to predict circuit-level performance degradation. We therefore wanted to validate our derived parameter sets against circuit-level measurements. Ideally, we wanted to find a published report of HCI degradation in a simple circuit like an inverter. Fortunately, Huard et al. provided just such information [8]. They reported on a custom HCI model's ability to replicate the HCI degradation measured in an inverter's nMOSFET. They accelerated HCI degradation by operating their inverter at an elevated temperature of 125°C and driving it with specialized pulses. These pulses, specified in Table 8, had long rise and fall times in order to lengthen the time during which the nMOSFET conducted current. For each pulse type a single physical measurement and a single simulation result were reported without a corresponding age. These are reproduced in Table 9. For discussion clarity, the set of their simulation results will be referred as S_{H}, the set of their physical measurements as D_{H}, and their model as M_{H}.

We could not directly compare our own simulation results agains D_{H} since the degradation values were reported without the corresponding ages. However, through educated guessing

TABLE 8. Inverter stimuli [8].

Pulse Type	f (MHz)	t_r (μs)	t_f (μs)	Amplitude (V)
B	0.1	1.0	1.0	$V_{DD}/4$
C	0.1	1.0	1.0	$V_{DD}/2$
D	1.0	0.1	0.1	$V_{DD}/2$

TABLE 9. Reported inverter nMOSFET $I_{D,sat}$ percentage degradation from measurement (D_H) and simulation (S_H) [8].

Pulse Type	D_H	S_H
B	-1.4	-2.3
C	-0.8	-0.9
D	-1.6	-1.0

we were able to test whether we could match the accuracy of the M_H model.

We began by assuming that the different reported inverter degradations were all measured at the same age. We then ran our own simulations and tested whether our results all occurred within overlapping windows of uncertainty. The windows represent bounds on the accuracy of our model. The upper bound being perfect accuracy and the lower being equal to the accuracy of the M_H model. Fig. 8 illustrates the principle. Each curve corresponds to our own simulation results of the inverter driven by a different pulse. Onto each curve we map the physical measurement (D_H) for the same pulse type. Each point has vertical error bars equal to $|D_H - S_H|$ representing the accuracy of the M_H model. These vertical error bars are then mapped onto our curves to create a corresponding error in time. If the time error bars overlap, then the lower bound on the accuracy of our simulations is equal to the accuracy of the M_H model. The upper bound is perfect replication and coincides with the D_H points aligning in time.

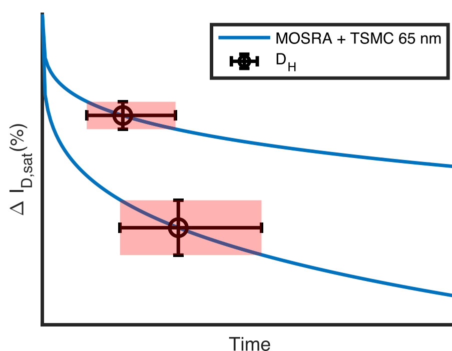

FIGURE 8. Demonstration of testing the bounds on the accuracy of our HCI model (blue curves). Measured data (D_H) is mapped onto our simulation curves and the horizontal error bars are checked for overlap. The D_H points are assumed to have occurred at the same age. If their time error bars overlap then the lower bound on the accuracy of our model is equal to the accuracy of the M_H model.

In addition to the aging time, the device dimensions, inverter load, and V_{DD} were unspecified. We assumed minimum channel length core devices were used and set $W/L = 1\,\mu m/0.06\,\mu m$ for our nMOSFET and $W/L = 2\,\mu m/0.06\,\mu m$ for our pMOSFET. We added two inverters in series to act as a load. These were each scaled 10× larger than the driving inverter. We considered three candidate values for V_{DD}: 1.0 V, the nominal voltage for TSMC 65 nm core devices; 1.1 V, their maximum rated voltage; and 1.5 V, which was used elsewhere by Huard et al. [8]. We used 1.5 V since it was the only V_{DD} value which would lead to the required degradation within one year for all input pulses.

Our simulations were carried out in HSPICE using typical corner device models from the TSMC 65 nm design kit. HCI degradation was simulated in all nMOSFETs using the MOSRA model with parameter set $\mathbf{v_{core1}}$. Fig. 9 shows the degradation of our driving inverter's nMOSFET along with the D_H points. The error bars in time all overlap, confirming that the accuracy of our HCI model is bounded by that of the previously-reported M_H model. Doubling the size of the load inverters did not change this result.

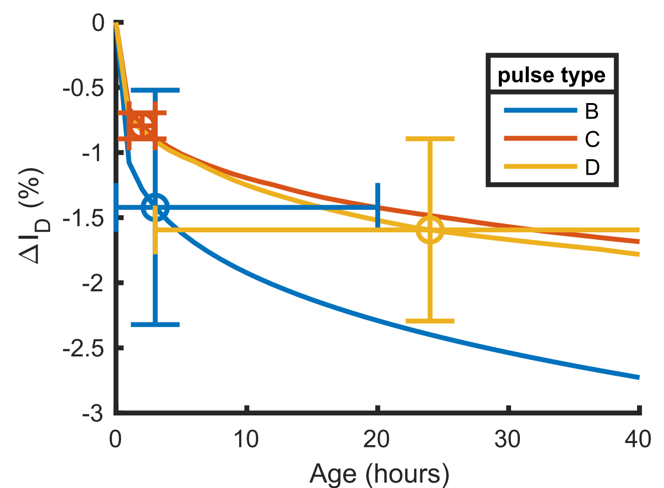

FIGURE 9. Inverter degradation according to MOSRA with $\mathbf{v_{core}}$. V_{DD} is 1.5 V. Also shown are the D_H points, each mapped onto its corresponding curve.

VI. CONCLUSION

In this work we have developed an iterative method to fit a compact MOSFET degradation model for use with a specific target technology. Data used to fit a model is aggregated from multiple public domain sources. This is made possible through an assumption that HCI degradation effects generalize across similar technologies. Results are validated against time to failure statistics from the target technology's reliability rules. We have demonstrated our method by fitting Synopsys' compact HCI model for use with both core and I/O nMOSFETs from TSMC's 65 nm technology with a high degree of confidence. We have also shown that our results can match the accuracy of a previously published model when simulating HCI degradation in an inverter. Our method for validating the fit to a deterministic model against a statistical specification is general and can easily be adapted for use with other EDA tools and CMOS technologies.

There are several limitations associated with our method. We have found that node size alone is an insufficient measure of similarity between technologies for our purposes. Some

care is therefore required when selecting the most appropriate data sources. Ultimately the accuracy of of any predictions born from our results is limited in two ways. First, the error in our model parameter values cannot be measured without access to a golden reference data set. This would have to be provided by a fab, or measured from a set of test devices. Second, the MOSRA model lacks the saturation mechanisms necessary to produce accurate long time or extreme operating condition degradation estimates. Regardless, we believe our results, listed in Table 4, to be adequate for generating circuit performance predictions particularly at initial design phases. This is of particular interest to anyone seeking to minimize the cost of exploratory design work, such as academics.

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