IEEE Access
Multidisciplinary : Rapid Review : Open Access Journal

Received 5 February 2023, accepted 20 February 2023, date of publication 1 March 2023, date of current version 8 March 2023.

Digital Object Identifier 10.1109/ACCESS.2023.3250940

RESEARCH ARTICLE

Ka-Band High-Linearity and Low-Noise Gallium Nitride MMIC Amplifiers for Spaceborne Telecommunications

PATRICK ETTORE LONGHI, (Member, IEEE), WALTER CICCOGNANI, SERGIO COLANGELI, AND ERNESTO LIMITI, (Senior Member, IEEE)
Department of Electronic Engineering, University of Rome "Tor Vergata," 00133 Rome, Italy

Corresponding author: Patrick Ettore Longhi (longhi@ing.uniroma2.it)

This work was supported in part by the European Space Agency (ESA) under Grant AO/1-9736/19/NL/CLP, and in part by the Associazione Società Italiana di Elettronica (S.I.E.).

ABSTRACT Gallium Nitride is becoming an interesting solution for low-noise applications in the lower part of the millimeter-wave spectrum and is gaining increasing attention in the space community for microwave receiver functionalities. Lately, its maturity level has increased and its performance in terms of noise figure and operating frequency is reaching other advanced III-V technologies such as Gallium Arsenide and Indium Phoshpide. Moreover, Gallium Nitride features higher power handling capability in comparison to the previously mentioned III-V technologies. In this context, we have designed and characterized two demonstrator circuits of critical microwave receiver functionalities: a Low-Noise Amplifier and a Low-Distortion Amplifier operating at Ka-band. It is shown that GaN circuits compare well in terms of noise figure, gain, and operating frequency with respect to other advanced III-V technologies, and most of all exhibit superior linearity in terms of intermodulation distortion. The designed Low-Noise Amplifier exhibits state-of-the-art 1.2 dB Noise Figure in the 27-31 GHz bandwidth thanks to a profitable combination of 60- and 100-nm gate length transistors on the same MMIC. On the other hand, the Low-Distortion Amplifier features state-of-the-art +30 dBm Output Third Order Intercept point in the same operating bandwidth while requiring only 216 mW dc power. The presented electrical performances are validated by comparing these designs to others available in open literature through figures of merit that normalize trade-offs by transistor length (therefore a fair comparison) aiming to highlight the merits of the proposed design methodologies.

INDEX TERMS Gallium nitride, intermodulation distortion, K-band, low-noise amplifiers, microwave amplifiers, millimeter wave integrated circuits, MMICs.

I. INTRODUCTION

SATCOM applications at Ka-band, particularly around 30 GHz, are gaining increasing attention from the satellite community due to the availability of large bandwidths. Satellite Ka-band communication is known for its high data rates, data traffic, and high throughput. The advantages of using Ka-band frequencies in satellite communication include wide spectrum availability, communication networks that support higher bit or data rates, feasibility of building multiple beam satellites, and incorporation of user terminals with small-size antennas. The Ka-band spectrum plays a key role in satellite communication and can improve global connectivity without deteriorating performance parameters.

Gallium Nitride (GaN) is gaining considerable interest in the space community due to some advantages over other low-noise and high-frequency technologies (mainly Gallium Arsenide and Indium Phosphide technologies [1], [2], [3]) for the reasons explained below. GaN is a wider band-gap material than GaAs; this results in a breakdown voltage field much higher by about one order of magnitude. Moreover, GaN supports smaller circuits for a given frequency and power levels, allowing for higher power densities and efficiencies. As a consequence of this feature, GaN is capable

The associate editor coordinating the review of this manuscript and approving it for publication was Chun-Hsing Li.

This work is licensed under a Creative Commons Attribution-NonCommercial-NoDerivatives 4.0 License.
For more information, see https://creativecommons.org/licenses/by-nc-nd/4.0/

of withstanding stronger signals without degradation or breakage [4]. Finally, the thermal conductivity of GaN is more than three times the thermal conductivity of the GaAs.

In this context we have developed a GaN chip-set for Ka-band SATCOM receivers, composed of a Low-Noise Amplifier (LNA) and Low-Distortion Amplifier (LDA) operating at Ka-band (27-31 GHz) targeting state-of-the art performance in terms of Noise Figure for the LNA and inter-modulation distortion for the LDA. Both circuits are designed also to minimize the dc power request (P_{dc}). The paper is organized as follows. A technology survey of advanced GaN technologies is given in Section II justifying the selection of OMMIC foundry GaN-on-Si process. Section III provides the details of the design solutions adopted for the two MMICs. Section IV contains the characterized data with the comparison to simulations and an assessment of the proposed requirements. Finally, Section V contains a state-of-the-art table that enables the reader to compare the proposed design with recently published material in the open literature. Some details of the research activity here described, in particular preliminary characterization results of the 60/100-nm Low-Noise Amplifier, were presented at the 53rd Annual Meeting of the Italian Electronics Society (Associazione SIE) [5].

II. TECHNOLOGY SURVEY

The most suitable MMIC technology for the demonstrator MMICs is selected considering the following parameters, which are not necessarily listed in order of importance. In order to produce an acceptable gain level in the Ka band, parameters such as gate length L_g, cut-off frequency f_T and maximum oscillation frequency f_{MAX} are evaluated. Also, noise performance, quantified by NF_{min} at operating frequency is also considered. Power handling requirements, evaluated by the breakdown voltage V_{BGD} has to be addressed since the LDA has to provide acceptable linearity performance. Finally, the maturity level of technology: possibly a space-level technology given the target application. A scouting of foundry processes that are capable of providing low-noise performance for Ka-band (27-31 GHz) operation, and capable of handling RF signals in the order of +20dBm are provided in the following. OMMIC'S D01GH, a 100nm GaN HEMT on Si process that is under evaluation for Space application [6]. UMS GH15 process is a 150nm GaN HEMT on SiC optimized to produce low noise, wide-band and medium power amplifier MMICs operating up to 30 GHz [7]. WIN foundry NP-15 GaN on SiC process leverages an advanced materials design with electron-beam defined 150 nm gates and a qualified 150 mm manufacturing infrastructure to obtain a high volume, ultra-high-performance technology platform. The process is targeted for Power amplifiers through 35 GHz as well as Switch and LNA functionalities [8]. Fraunhofer Institute for Applied Solid State Physics - IAF offers 100-nm GaN-on-silicon-carbide (SiC) HEMT process in grounded coplanar waveguide on 3-inch SiC substrates for operation up to W-band [9].

TABLE 1. Overview of MMIC GaN technologies for Ka-band Low-Noise and High-Linearity applications. NFmin is given at 30 GHz.

	OMMIC D01GH	UMS GH15	WIN NP15	IAF GAN10	QORVO QGaN15
f_T (GHz)	100	40	35	110	40
f_{MAX} (GHz)	180	100	120	270	160
NFmin (dB)	1.4	2.2	2.3	1.3	2.1
$g_{m,max}$ (mS/mm)	400	390	435	500	425
I_{DSS} (mA/mm)	1200	1200	990	1300	800
V_{BGD} (V)	40	40	60	40	75
Wafer (inches)	3	4	4	3	3
Substrate	Si	SiC	SiC	SiC	SiC
grade	Prod.	Prod.	Prod.	Research	Prod.

Finally, we consider Qorvo's 150 nm Gallium Nitride MMIC technology on 100 μ m thick and 100 mm diameter SiC substrates developed at TriQuint Texas for high volume Ku, Ka and Q-band applications [10].

A summary table of these technologies' key electrical performance is reported in Table 1. IAF's GaN technology is the most advanced in terms of electrical performance. However, it is a prototype level technology and consequently discarded considering the targeted spaceborne applications. Most listed technologies are realized on a Silicon Carbide (SiC) substrate. The latter is very useful when high-power and high-temperature applications are sought. This is not the case of this project and they are discarded in favour of OMMIC's GaN on Silicon process that demonstrates advanced electrical performance in an industrial level process. Moreover, OMMIC's GaN process, as explained in the following, is capable of processing two different gate length transistors, namely 100- and 60-nm, on the same MMIC. Consequently, NF can be improved when using the 60-nm version of the technology (D006GH).

III. CIRCUITS DESIGN

The two demonstrator circuits are designed to demonstrate the feasibility of the requirements expressed in the following. The design bandwidth is for SATCOM applications at Ka-band and in detail from 27 to 31 GHz [11]. For the Low-Noise Amplifier (LNA) the key objective is to fulfill the best possible Noise Figure obtainable from the technology. Analysis of recently published material [12] suggests that this value is around 1.2 dB at 30 GHz. The Low-Distortion Amplifier (LDA) is designed to demonstrate +30 dBm Output Third Order Intercept (OIP3) point. Both circuits are

designed to provide 20 dB gain specification and typically 13 dB return loss at I/O ports. Since dc power consumption is a critical requirement for space-borne applications, the value shall be minimized, while guaranteeing satisfactory nonlinear performance in terms of OP1dB and OIP3. The Low-noise amplifier shall also provide robustness to strong interfering signals. Here robustness is intended as the capability of a circuit to withstand a specific amount of input power in CW mode without altering its noise and gain performance. Robustness is different than survivability. The latter requires that the circuit maintains its functionality after a stress test accepting however some limited degradation of noise and gain performance. Consequently, the maximum input power to guarantee robustness capability is smaller than the corresponding value that fulfills survivability. The robustness level here considered is +20 dBm input power in CW mode.

Finally, we need to control the OIP3 of the LNA and NF of the LDA since the two circuits are cascaded in a microwave receiver and these parameters produce some effect at receiver level. Consequently, the LNA's OIP3 shall be greater than +26 dBm and the LDA's NF shall be less than 1.8 dB.

A. DEVICE MODELLING

Before commencing design activities we verified the accuracy of the models provided by the foundry in the PDK. The first check regarded the bias voltage. OMMIC initially recommended +12 V drain-to-source voltage for power amplifier operation and +7 V for high-gain / low-noise operation. However, we were interested in operating the devices at lower drain voltages to minimize dc power consumption. Therefore, we characterized the HEMT at +5 V drain voltage. No significant degradation in terms of noise and gain behaviour was observed and the reduction in the principal nonlinear figures of merit (OP1dB and P_{sat}) was compensated by the lower dc power request. Therefore, we extracted an ad hoc linear and noise model for operation at +5 V drain-to-source as an alternative capability to the model provided by the foundry.

The noise model was extracted by employing the standard noise-temperature approach to noise figure measurements implemented in two distinct frequency ranges: a lower band, where a typical Y-factor test bench is used, and an upper band, where a novel cold-source test bench is employed. At +5 V drain-source voltage, minimum noise figures as low as 1.5 dB and 1.1 dB at 40 GHz have been extracted for the considered 100 nm and 60 nm HEMTs, respectively: this testifies the validity of both processes and the usefulness of the gate length reduction. Additional details of the characterization and modeling activities are reported in [13]. Furthermore, previous research on D01GH LNAs had proven 1.05 W/mm saturated output power density at 36 GHz when operated at +5 V drain voltage and 150 mA/mm drain current density [14].

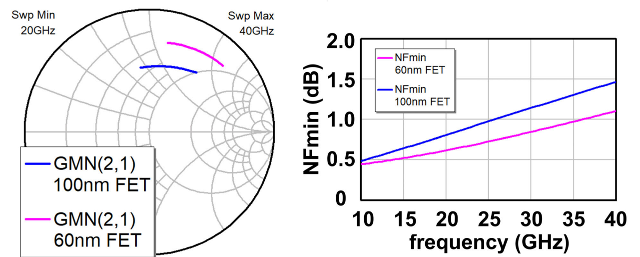

FIGURE 1. Minimum Noise Figure and Optimum Noise Termination of two representative transistors of D006GH and D01GH technologies.

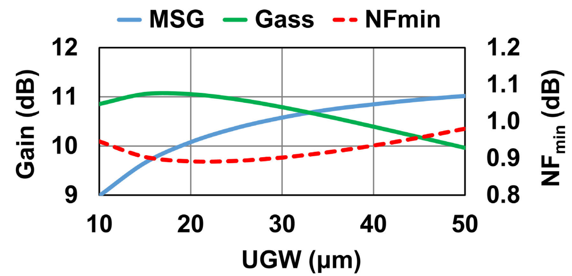

FIGURE 2. Figures of merit for the first stage transistor: associated gain, MSG and NF_{min} vs. Unit Gate Width (UGW) of a 4-finger device with the source grounded through a physical via-hole. Data are plotted at 31 GHz.

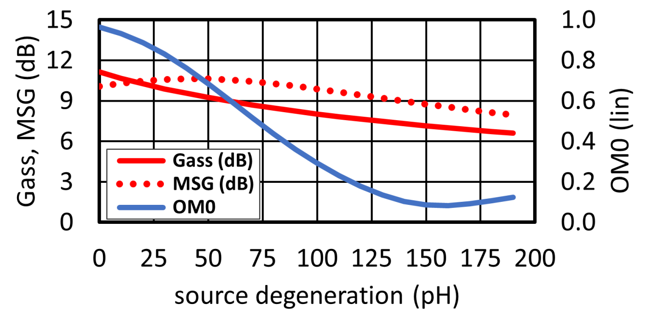

FIGURE 3. Figures of merit for the first stage transistor: associated gain, MSG and OM_0 vs source degeneration inductance for a 4f × 20 μ m device biased at low-noise operating condition. Data are plotted at 31 GHz.Source degeneration is inserted in series to the physical via-hole.

B. LOW-NOISE AMPLIFIER DESIGN

The main focus of LNA design is to obtain lowest possible Noise Figure, within the inherent limitations of the selected technologies, in conjunction with minimized dc power request and greater than 20 dB gain. As stated previously, OMMIC's GaN-on-Si process has the distinctive feature of providing two different gate length transistors on the same MMIC. Given the stringent Noise Figure goal we opted for the 60 nm (D006GH) technology on the first stage transistor, whose NF is critical for the overall LNA NF. This performance improvement is depicted in Fig. 1 , where we plot transistors' noise figures of merit at optimum noise bias point (+5 V drain voltage and 125 mA/mm normalized drain current) versus frequency. The Noise Figure improvement is quite clear, although it is obtained at the expense of

the optimum noise termination being further away from the centre of the Smith Chart. Subsequent analysis suggests that there is no significant NF degradation when using 100 nm HEMTs after the first stage, so we opted to use the 100 nm technology for the following stages, given the higher maturity of the process.

Having fixed technology and bias point, the next step of the LNA design consists in selecting the appropriate device geometry, in terms of the number of fingers and the unit gate width of the single finger (UGW). At Ka band, 4-finger devices exhibit adequate optimum terminations (i.e. having practical resistive value) and less drain current than larger 6- and 8-finger devices. The key parameters of a 4-finger HEMT, versus UGW at 31 GHz, are shown in Fig. 2.

A feasible device for the first stage, that is one having adequate associated gain and with practical optimum input and output terminations at the operating frequency, is chosen to be a $4f \times 20\ \mu$ m transistor. At the selected low-noise bias point, +5 V drain voltage and 125 mA/mm normalized drain current, the device exhibits 0.85 dB NF_{min} and 11 dB Associated Gain (G_{ass}) when the source is directly terminated in a physical via hole without additional degeneration. It is interesting to note that MSG increases with UGW; however, this gain increase is less exploitable in LNA design since G_{ass} diminishes due to optimum gain and noise terminations moving away from each other as UGW increases, and drain current increases too. At low UGW values the noise and gain behaviour becomes unpractical.

Consider that the device's G_{ass} will diminish after source degeneration is applied to fulfill the Simultaneous Signal and Noise Match (SSNM) condition at the input of the first stage transistor [15] and to improve transistor stability. Source degeneration consists of inserting an inductive element between the transistor's source terminal and ground, often referred to as series/series feedback. Source degeneration improves device stability and eases noise/signal matching over a moderate bandwidth. The drawback of this technique is that it reduces the device G_{ass} and therefore it must be used with caution otherwise the number of stages required to fulfil the gain requirement could increase above a feasible value. Three figures of merit for the first stage transistor are plotted in Fig. 3 as a function of the feedback element's inductance, evaluated at 31 GHz. In particular, the device's associated gain (i.e., the available gain when the input is matched for noise), the device's Maximum Stable Gain (MSG) and the output mismatch value (OM_0) when the input is matched for noise and the output termination is selected to fulfill the SSNM condition, ($\Gamma_L = \Gamma_{L,C,in}$). The equation for $\Gamma_{L,C,in}$ is:

$$\Gamma_{L,C,in} = \frac{s_{11} - \Gamma_S^*}{\Delta - s_{22}\Gamma_S^*} \tag{1}$$

We are assuming $\Gamma_S = \Gamma_{OPT}$, i.e., the input is terminated to fulfil an optimum noise condition, while the output termination will ensure the SSNM condition. Although the associated gain is rather high for low feedback values, it is inadvisable to operate such a choice, since associated gain is higher than MSG and this could lead to possible instability issues. The effect of feedback on the first stage transistor is also visible in Fig. 4 where we have plotted the transistor's optimum source termination for noise ($\Gamma_S = \Gamma_{OPT}$), $\Gamma_{L,C,in}$ as expressed in eq. 1, and the conjugate of the output reflection coefficient Γ_{out}^*. It is interesting to note that the effect of feedback is much more evident on $\Gamma_{L,C,in}$ and Γ_{out}^* rather than Γ_{OPT}. By analysing data in Fig. 3 and 4 we can infer that, for the first stage transistor, we will require at least 100 pH feedback to place $\Gamma_{L,C,in}$ in a position which helps the synthesis of the first inter-stage matching network. Consequently, the associated gain of the first stage will be less than 9 dB. This limitation yields the need for a 3-stage LNA, schematically depicted in Fig. 5, to satisfy the gain request in excess of 20 dB.

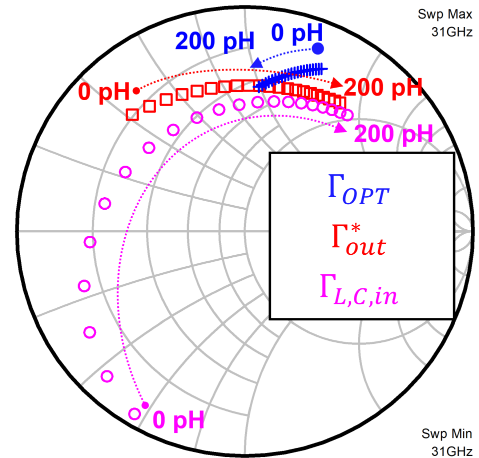

FIGURE 4. Optimum terminations of the first stage transistor: Γ_{OPT}, and $\Gamma_{L,C,in}$, and Γ_{out}^*. Source degeneration values are swept from 0 to 200 pH at 10 pH steps. Data are plotted at 31 GHz.

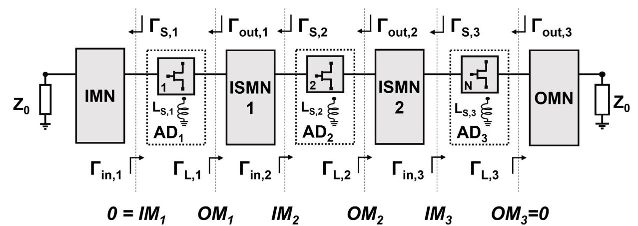

FIGURE 5. 3-stage LNA simplified block diagram. Reflection coefficients and mismatch levels are indicated at all sections.

In [16] we proposed a method that allows synthesizing a conjugately matched N-stage LNA with optimum noise performance, simultaneously controlling gain and in-band stability. This is accomplished by selecting appropriate mismatch levels at the intermediate sections. The mismatch levels at the input and output terminals of each transistor,

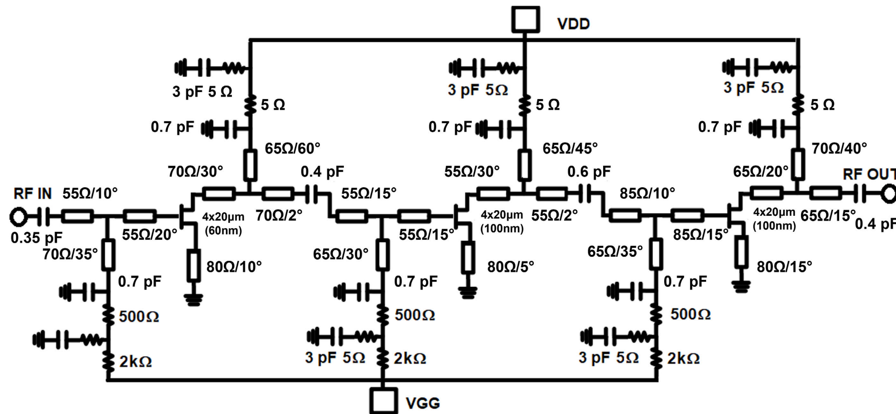

FIGURE 6. 3-stage 60/100-nm LNA electrical schematic. Transmission lines' electrical lengths, expressed in degrees, are given at 31 GHz.

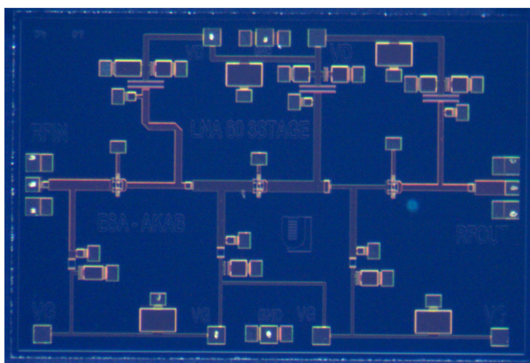

FIGURE 7. 3-stage 60/100-nm LNA MMIC.

depicted in Fig. 5, are defined as:

$$IM_k = \left| \frac{\Gamma_{S,k} - \Gamma^*_{in,k}}{1 - \Gamma_{S,k}\Gamma_{in,k}} \right| \tag{2}$$

$$OM_k = \left| \frac{\Gamma_{L,k} - \Gamma^*_{out,k}}{1 - \Gamma_{L,k}\Gamma_{out,k}} \right| \tag{3}$$

valid for all values of subscript k ranging from 1 to 3. In the hypothesis of matching networks synthesized through reciprocal and lossless elements, the following identity holds:

$$OM_k = IM_{k+1} \tag{4}$$

Finally, $IM_1 = 0$ and $OM_3 = 0$ must be imposed to obtain 50 Ω match at the 3-stage LNA I/O ports. A conjugately matched N-stage LNA has $N - 1$ degrees of freedom that correspond to $N - 1$ mismatch levels seen at the terminals of the $N - 1$ inter-stage matching networks of the LNA, as described [16]. Typically, a higher gain is obtained by increasing the intermediate mismatch levels. As often occurs in low-noise synthesis, the designer will have to perform a trade-off between the gain and intermediate mismatch levels. The latter are indicators of stability and the ability to obtain the desired electrical performance over a larger bandwidth. This method allows determining optimum source degeneration value on all transistors of the LNA by imposing a controlled mismatch at the intermediate sections of the LNA while simultaneously imposing 50 Ω match at the LNA's I/O ports, and optimum noise match at the input of every stage. The LNA gain is proportional to the mismatch at intermediate stages. The latter should be lowered to improve LNA stability and also to reduce gain ripple. However, lowering this value will reduce LNA transducer gain and therefore a compromise must be sought between a practical number of stages (higher gain per stage) and lowering the mismatch at the intermediate sections of the LNA (lower gain per stage). For this 3-stage LNA we need to determine the mismatch at the two intermediate sections, i.e. IM_2 and OM_2 in Fig. 5.

A first attempt is to fix both values at 0.2 (14 dB return loss at intermediate sections). For this design choice, and applying the algorithmic approach proposed in [16] we obtain the following available gain in dB per stage at 31 GHz (highest operating frequency): 7.8, 8.7, and 7.2 corresponding to 23.7 dB transducer gain of the 3-stage LNA. This value is acceptable, considering the unavoidable resistive losses of the physical matching network of the MMIC LNA, initially quantified in 2 dB. The three inductance values that meet the above-mentioned design condition are $L_{s,1} = 120$ pH, $L_{s,2} = 75$ pH, and $L_{s,3} = 145$ pH.

To evaluate the theoretical minimum noise figure, we applied a Noise Measure (M) analysis by identifying its minimum value, i.e. M_{min}, as suggested in [17]. $1 + M_{min}$, expressed in dB, corresponds to the Noise Figure of an infinite cascade of identical stages optimally noise matched under the hypothesis of lossless embedding (feedback and matching networks). Obviously, the latter hypothesis is unfeasible at microwave frequencies, and therefore $1 + M_{min}$ represents a lower boundary that is obtained only with lossless embedding. However, this figure of merit is useful to preliminary quantify the MMIC LNA's NF since the resistive losses of the Input Matching Network (IMN) can be added to $1 + M_{min}$ to obtain a more feasible target value for the MMIC

LNA's NF. Taking into account the restive losses of 0.2 dB in the IMN, we account for 1.2 dB NF for the MMIC LNA since the value of M_{min} is 0.26 at 31 GHz.

The LNA's final stage is also designed to meet the +26 dBm OIP3 request. Additional information on the methodology applied to meet the OIP3 requirement is given in the following section III-C on Low-Distortion Amplifier design.

A final aspect in LNA design consists in evaluating its robustness, intended as the capability of not altering its noise and linear performance after being subject to a strong interference signal. Design guidelines to improve robustness suggest inserting a large resistor between the transistor's gate terminal and the gate dc voltage supply to limit the flow of dc gate current as the input RF power increases due to the dc gate voltage drop across the gate biasing resistor [18]. Therefore, the device is pinched-off and the output power drops as the input power level increases. A total of 2kΩ resistance is inserted in the gate bias networks of each stage. An appropriately sized capacitor, 0.7 pF, is inserted in the gate bias network to conceal the resistor's effect (and noise) at operating frequency. Finally, we checked that the gate dc current, at +20 dBm input power, is lower than 2 mA/finger as specified by the foundry's PDK maximum rating section. In this sense, a transistor having a higher number of fingers is beneficial. The detailed electrical schematic of the LNA is given in Fig. 6 while Fig. 7 reports the micro-photograph of the realized MMIC. The chip size is 3mm × 2mm.

C. LOW-DISTORTION AMPLIFIER

The principal design goal of the Low-Distortion Amplifier (LDA) is to fulfill +30 dBm OIP3 requirement in conjunction with 20 dB gain, 13 dB typical return loss at I/O ports while minimizing the dc power request. LDA Noise Figure is not so critical since the gain of the preceding LNA is enough to conceal the noise contribution of the following stages. Consequently the LDA's NF is set to 1.8 dB and all transistors are designed with higher maturity the 100-nm gate length technology (D01GH). Some design solutions are shared with the LNA described in the previous section, while others are specific for LDA design. The LDA also adopts a 3-stage architecture applying reactively matched topology and source degeneration similar to that in Fig. 5. One main difference between the electrical schematics of LNA and LDA is the scaling of the transistor periphery from output to input , discussed later in this section, and the lower drain current bias point. The latter design choice is acceptable since the input reflection coefficients can be selected to lie upon higher constant available gain circles without requiring to optimally noise match the input of the transistor. Consequently, the penalty for having lower transistor maximum gain, due to lower drain current density, is compensated by placing the input reflection coefficients closer to the optimum gain value without needing to perform a noise vs. gain trade-off.

Input reflection coefficients are selected, on the three stages, to fulfill 7.5, 8.5 and 7.5 dB available gain at 31 GHz, respectively for the first, second and third stage transistors. This choice allows obtaining more than 20 dB cascade gain while accounting for some inevitable mismatch and resistive losses of the physical matching networks. The intermediate stage gain is higher than the first and last stage gain since a worse mismatch can be tolerated at the I/O ports of the intermediate stage. As described in [16], higher stage gain is obtained at the expense of poorer stage matching.

The first stage input reflection coefficient is a trade-off between the available gain and noise figure. In the LDA, source degeneration is applied to increase the bandwidth over which adequate return loss is obtained, rather than to ease noise/signal match at the amplifier's input. The inductor values are less than the LNA counterpart since here they are employed to obtain wide-band signal match, rather than performing a noise/signal match trade-off as in the LNA case.

Another interesting design difference is the use of a single positive power supply for FET biasing. Usually, in low-noise and gain amplifier design at microwave frequency in III-V technology depletion mode FETs, the negative gate-to-source voltage is obtained by grounding the source and applying a negative voltage to the gate terminal. This technique allows versatile biasing, but requires two separate biasing voltages. A way to overcome the latter constraint is to apply a single positive biasing strategy. In the latter case, the gate terminal is dc-grounded through a choke inductor L_g as shown in Fig. 8. In order to obtain the required V_{GS} a resistor R_S is inserted between the source terminal and ground in series to an inductive element L_s whose role has already been discussed. Capacitor C is added to shunt the lossy effect of the resistor at the operating frequency. A drawback of this biasing technique is the reduction of the drain-to-source voltage, since the source terminal is placed at a potential higher than 0 V. Consequently, to maintain +5 V drain-to-source voltage operation, we applied +6 V drain bias voltage (V_D). As stated previously, we opted to select a normalized drain current of the LDA transistors at 100 mA/mm, rather than 125 mA/mm as in the LNA, to minimize dc power consumption.

A collateral effect of the biasing scheme shown in Fig. 8 is the worsening of the geometrical stability factor (μ) at lower frequencies with respect to the grounded-source (dual bias) case. This effect can be seen in Fig. 9 where the I/O geometrical stability factors μ_1 and μ_2 are plotted as a function of frequency with and without the source resistor R_S. To generate the plot in Fig. 9, the resistor value was initially set to 100 Ω, reasonably close to the value actually determined in the final schematic. The resistor value, on all stages is calculated using the approximation:

$$I_D \approx I_{DSS}\left[1 - \frac{V_{GS}}{V_t}\right]^2 \quad (5)$$

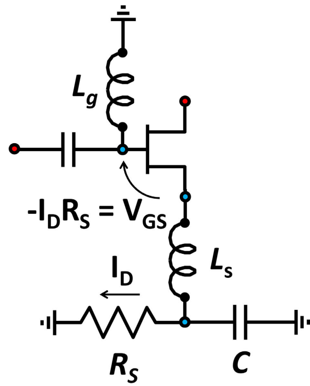

FIGURE 8. Single bias FET schematic.

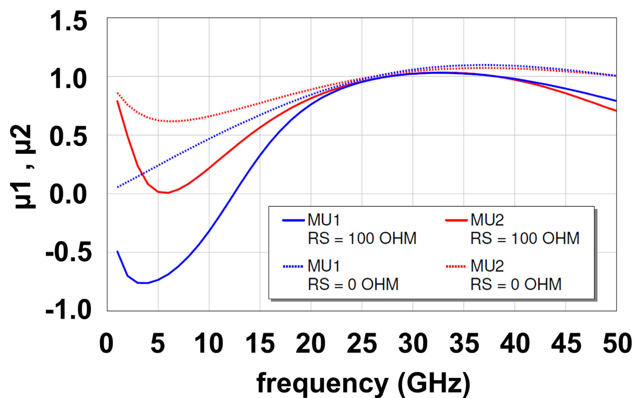

FIGURE 9. I/O geometrical stability factors μ_1 and (blue lines) μ_2 (red curves) vs. frequency for $R_S = 100\Omega$ (solid curves) and $R_S = 0\Omega$ (dotted curves).

In particular, to obtain 100 mA/mm drain current we require -1 V gate-to-source voltage considering 1 A/mm I_{DSS} and -1.45 V threshold voltage, V_t.

Honestly, the biasing scheme shown in Fig. 8 is sensible to process variations and in particular R_S yield. Moreover, the drain voltage has to be increased to compensate the higher than zero source terminal voltage. An analytic approach to quantify such dependence consists in differentiating I_D in (5) with respect to variable R_S while imposing $V_{GS} = -I_D R_S$. An experimental approach shows that, for small variations around the nominal resistor values (i.e. 20 %) the current of the final stage transistor is reduced by 1 mA for a 5 % increase in resistor value, and vice-versa. Surely, other more robust biasing schemes are described in the open literature, such as current mirrors. However, the scheme proposed here is fairly simple and allows obtaining adequate performance.

Fig. 9 reports a stability deterioration for the single bias FET below 20 GHz. Below 12.5 GHz, μ_1 of the single bias FET is even negative, meaning that the FET is potentially unstable when terminated on 50 Ω. Consequently, a thorough stability analysis is performed to evaluate such effect at amplifier level. On the other hand, the geometrical stability factors are practically identical around 30 GHz implying there is no gain penalty to pay when applying the single bias strategy, since the resistor is shunted by the capacitor in the operating bandwidth.

Nonlinear design evaluations to appropriately select the geometry of the final stage transistors are reported in Fig. 10. Here we have plotted constant OIP3 contours in the output plane at 31 GHz of the $4f \times 40\ \mu$ m final stage FET. Drain bias point is +6 V and 100 mA/mm. The input reflection coefficient is selected to provide 7.5 dB available gain, and inductive source degeneration is applied to obtain 13 dB output return loss over the operating bandwidth. The output termination is selected near a +30 dBm constant OIP3 contour close to the conjugate of the third/final stage output reflection coefficient ($\Gamma^*_{out,3}$), as shown in Fig. 10. In this way, we obtain an optimal signal match to 50 Ω in conjunction with the selected OIP3 level, +30 dBm. The maximum OIP3 is around +32 dBm, however in a position far away from $\Gamma^*_{out,3}$ consequently not being able to satisfy the conjugate output match condition.

The first and second stage transistor geometries are selected targeting linearity (OIP3), and most of all LDA dc power request. Data reported in Fig. 11 is used for this scope. Eleven LDA configurations are analyzed. The gain per stage is set at, 7.5, 8.5 and 7.5 dB available gain per stage from input to output at 31 GHz, as justified previously in this section. The final stage OIP3 is set at +30 dBm (grey line, top plot), which is a bottleneck for the cascade OIP3. The first stage OIP3 is reduced by 1 dB steps from +30 to +20 dBm (blue line, top plot). The intermediate stage OIP3 (orange curve, top plot) is varied from +30 to +26.4 dBm, reducing it by 1.2 dB every 3 steps. Cascade OIP3, (green curve, bottom plot), is calculated for each configuration as described in engineering handbook texts, as, for example, [19]. Table 2 reports the total gate width per stage (w_{gN}) and the corresponding expected OIP3 for the three stages when considering the eleven analyzed LDA configurations shown in Fig. 11. Finally, we estimated LDA dc power (red dashed curve, bottom plot) on the assumption there is a direct relationship between FET OIP3 and FET dc power request.

For LDA design we select configuration 3, where a plateau of dc power appears in Fig. 11. The dc power is slightly above 200 mW and the LDA OIP3 is +29 dBm. Selecting higher configuration indexes implies reducing dc power, however, at the expense of lower LDA OIP3. On the contrary, selecting lower configuration indexes would produce an increase in LDA dc power, while benefiting of only additional +0.3 dB in LDA OIP3.

Configuration 3 corresponds to the following OIP3 levels from input to output: 27.0, 28.8, 30.0 dBm. In a linear scale, the relationship between these three values is proportional to 1.0:1.5:2.0, so the size of the devices is scaled accordingly from input to output.

Finally, Ohtomo test [20] is performed from dc to 50 GHz to verify any internal instability by evaluating the open-loop transfer functions. No encirclement of $1 + j \cdot 0$ occurs, and consequently the test does not highlight any instability issues,

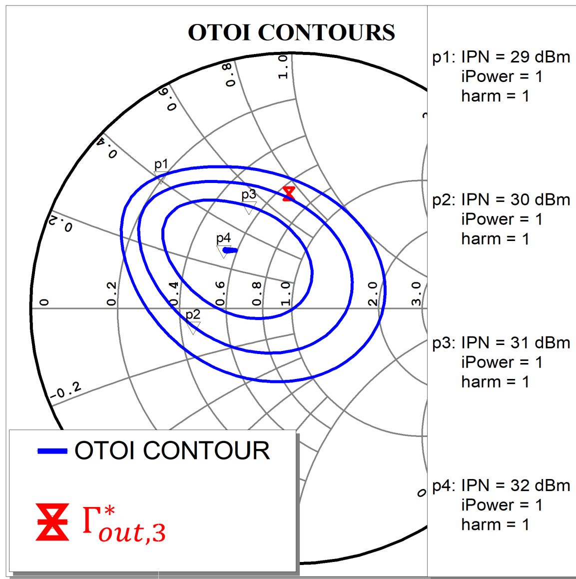

FIGURE 10. Constant OIP3 curves of the $4f \times 40\ \mu$ m final stage FET. Drain bias point is +6 V and 100 mA/mm. Data are provided at 31 GHz. The conjugate of the third/final stage output reflection coefficient ($\Gamma^*_{out,3}$) is also shown.

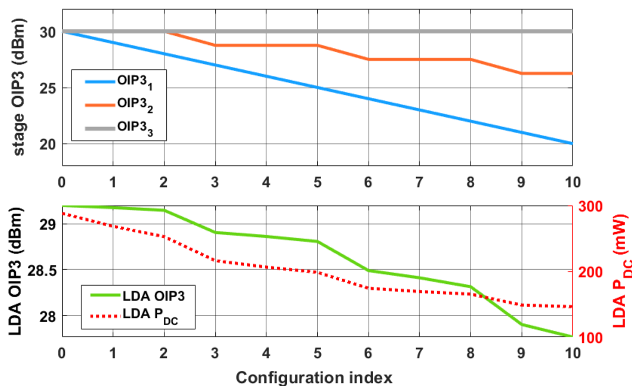

FIGURE 11. LDA OIP3 and approximate LDA dc power as a function of the three stages OIP3.

as seen in Fig. 12. For this test, we have treated the three transistors as 3-terminal active networks. Consequently, the R-L-C source degeneration is part of the passive networks in Ohtomo's test. Fig. 13 shows the detailed electrical schematic of the LDA, while Fig. 14 reports the micro-photograph of the realized MMIC. Chip size is 3mm × 2mm.

IV. MMIC CHARACTERIZATION

The two MMICs are characterized at the design bias condition to verify their performance with respect to requirements and simulated data. On wafer scattering parameters were acquired through an HP8510C Vector Network Analyzer from 0.1 up to 40.1 GHz at 100 MHz steps. Calibration was performed by means of a short open load through (SOLT)

TABLE 2. total gate width (W_{gN}) and OIP3$_N$ of the three stages for the eleven considered LDA configurations.

CNFG.	W_{g1} (µm)	OIP3$_1$ (dBm)	W_{g2} (µm)	OIP3$_2$ (dBm)	W_{g3} (µm)	OIP3$_3$ (dBm)
0	160	30	160	30	160	30
1	124	29	160	30	160	30
2	100	28	160	30	160	30
3	80	27	120	28.8	160	30
4	64	26	120	28.8	160	30
5	50	25	120	28.8	160	30
6	40	24	90	27.6	160	30
7	32	23	90	27.6	160	30
8	24	22	90	27.6	160	30
9	20	21	70	26.4	160	30
10	16	20	70	26.4	160	30

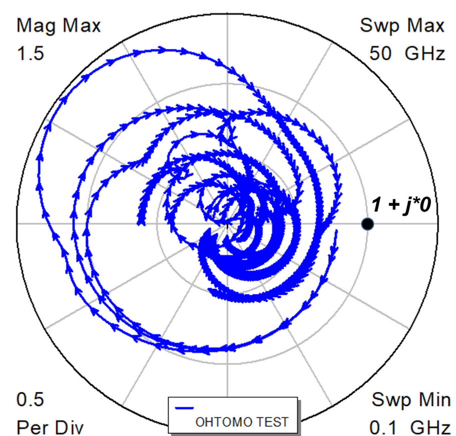

FIGURE 12. LDA Ohtomo test plot in dc-50 GHz.

standard substrate. Noise characterization was performed measuring noise power with an Agilent E4448A Power Spectrum Analyzer pre-amplified by two LNAs, a MACOM MAAM-011109 and an HP83051A. A standard hot-cold test-bench was adopted. The latter is based on a Noise Com NC346KA diode noise source with a matched 6 dB attenuator. Nonlinear measurements were performed by an Agilent E4448A Power Spectrum Analyzer, coupled with an absolute power reference provided by a Keysight USB power sensor. The two tone signals were realized by a pair of Agilent N5183A Synthesizers.

A. LOW-NOISE AMPLIFIER

The 3-stage 60/100-nm LNA MMIC is characterized in the nominal bias condition, that is +5 V drain voltage and 30 mA total drain current (10 mA per stage). The latter figure is equivalent to 125 mA/mm drain current density. Nominal drain current is obtained by adjusting the gate voltage at −0.9 V. Fig. 15 reports the LNA's linear characterization from dc to 40 GHz. Solid lines are measured data while dotted lines represent simulations. The MMIC respects the linear requirements and compares well with simulated data thanks to active device modelling. Linear gain is greater than

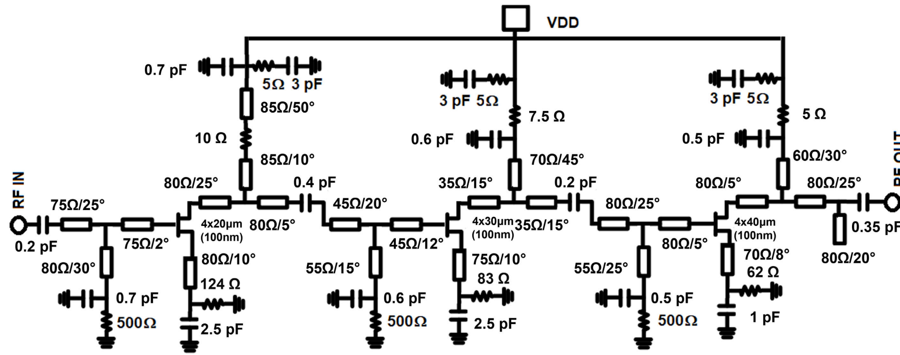

FIGURE 13. 3-stage single bias (SB) Low-Distortion Amplifier electrical schematic. Transmission lines' electrical lengths, expressed in degrees, are given at 31 GHz.

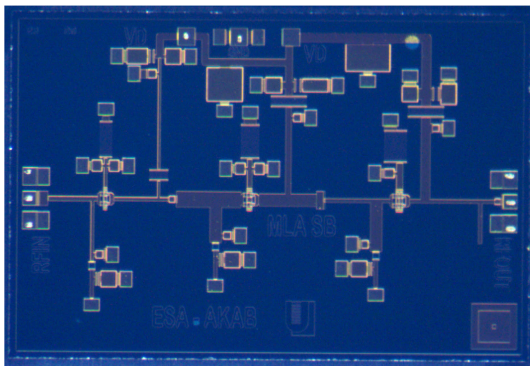

FIGURE 14. 3-stage single bias (SB) Low-Distortion Amplifier MMIC.

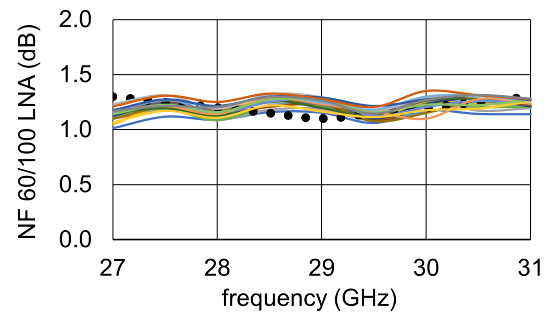

FIGURE 16. 3-stage 60/100-nm LNA MMIC measured 20 samples (coloured traces) and simulated (dotted black trace) noise performance.

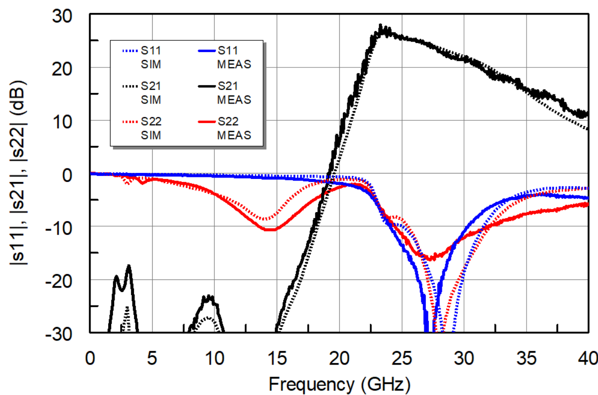

FIGURE 15. 3-stage 60/100-nm LNA MMIC measured (solid traces) and simulated (dotted traces) linear performance.

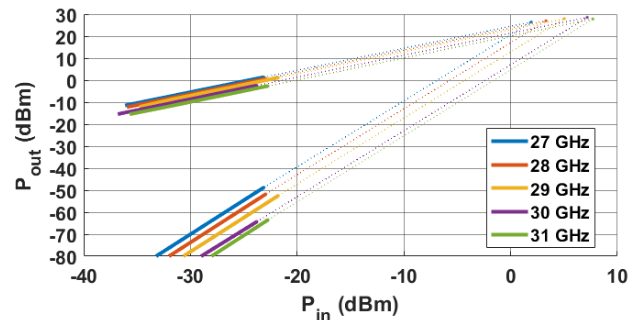

FIGURE 17. 3-stage 60/100-nm LNA MMIC measured OIP3.

20 dB in the operating bandwidth and return loss is better than +10 dB. A frequency shift is observed on $s11$ due to the preliminary electrical model of the 60-nm transistor.

LNA noise performance is depicted in Fig. 16. Simulations agree well with measured data and typically show 1.2 dB NF over the operating bandwidth for 20 verified MMICs. The standard deviation observed in 20 verified MMICs is 0.07 dB. The LNA's measured OIP3 is shown in Fig. 21. The target +26 dBm level is obtained over the operating bandwidth.

Finally, the LNA is subject to a 10 cycle swept RF input power in CW mode stress test. The input power is swept from −8 to +22 dBm at 1 dB steps. Each input power level is held for 5 seconds in CW mode. No degradation in terms of linear gain and NF is observed after the stress test. The output power to input power curves for the stress test are given in Fig. 18.

B. LOW-DISTORTION AMPLIFIER

The 3-stage LDA MMIC is characterized in the nominal bias condition, that is +6 V drain voltage and 36 mA drain current. The latter figure is equivalent to 100 mA/mm drain current density. In this case, it is not possible to tune the drain current

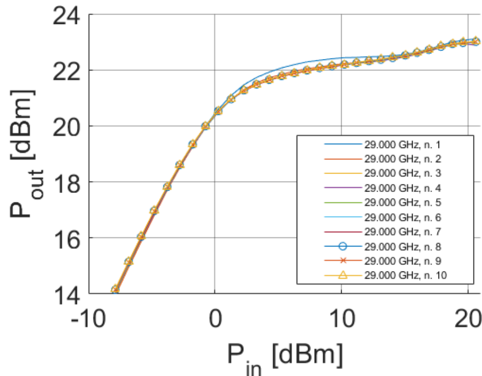

FIGURE 18. 3-stage 60/100-nm LNA MMIC CW stress test, 10 sweeps at 29 GHz.

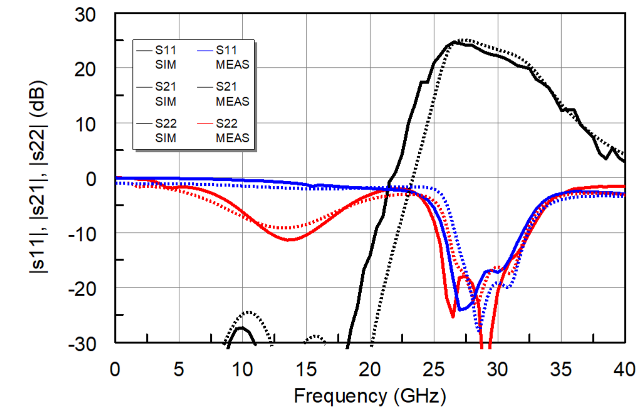

FIGURE 19. 3-stage Low-Distortion Amplifier MMIC measured (solid traces) and simulated (dotted traces) linear performance.

through the gate bias. The only way to modify the drain current is by acting on the drain voltage.

Fig. 19 reports the Low-Distortion Amplifier s-parameters vs. frequency. Solid lines are measured data while dotted lines represents simulations. The MMIC respects the linear requirements and compares well with simulated data. Linear gain is +20 dB in the operating bandwidth and return loss is better than +14 dB in 27-31 GHz. LDA noise performance is depicted in Fig. 20. Simulations agree well with measured data and shows typically 1.2 dB NF over the operating bandwidth for 20 verified MMICs. The standard deviation observed over 20 verified MMICs is 0.08 dB.

Finally, we present the LDA's nonlinear characterization in terms of OIP3 in Fig. 21 Average measured OIP3 is +30 dBm in the 27-31 GHz bandwidth in good agreement with the expected simulation value.

V. BENCHMARKING AND DISCUSSION

The two GaN-on-Si MMICs described here are compared in table 3 to other recently published GaN circuits operating at K-band.

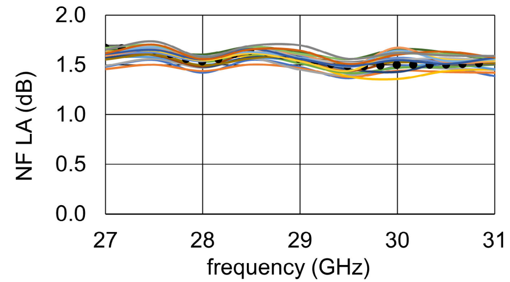

FIGURE 20. 3-stage Low-Distortion Amplifier MMIC measured 20 samples (coloured traces) and simulated (dotted black trace) noise performance.

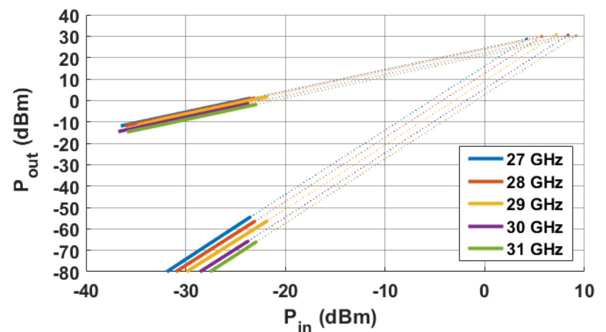

FIGURE 21. 3-stage Low-Distortion Amplifier MMIC measured OIP3 at +6 V drain bias and 36 mA drain current.

The MMICs proposed here compare well with those reported in the open literature. In particular, the LNA exhibits superior noise performance, thanks to the combined use of 60- and 100-nm gate length technology. The Low-Distortion Amplifier exhibits +30 dBm OIP3 requiring a power consumption of only 216 mW. A figure-of-merit (F.O.M.) proposed in [24] oriented to concurrently evaluating amplifier noise, dynamic-range and dc power consumption performance is provided in the Table to help the reader compare the proposed references. Higher F.O.M. values correspond to higher technical merit. The FoM normalizes trade-offs by transistor length and operating frequency, aiming to highlight the merits of LNA design methodologies. In practice, designs using shorter gate length technologies - as in the presented LNA - are penalized when calculating the FOM. The LDA has the highest FOM considering its high linearity and relatively low noise behavior obtained with 100-nm technology and low dc power consumption. The 60-nm LNA has a very good FOM, but the use of 60-nm worsens the FOM with respect to LDA making it comparable to [4]. In truth, the latter reference is advantaged by its lower gain increasing the input-referred 1 dB compression point (IP1dB). The comparison would be more favourable for the presented 60-nm LNA if the FOM had considered OP1dB rather than IP1dB.

Finally, the FOM of the 60-nm LNA is compared with that of a wide bandwidth low-noise amplifier (LNA) fabricated in a 0.15 μ m e-mode GaAs pHEMT process reported in [3].

TABLE 3. Comparison of GaN Ka-band MMIC amplifiers with the literature.

REF	TECH	L_g (nm)	BW (GHz)	Gain (dB)	NF (dB)	OP1dB (dBm)	OIP3 (dBm)	P_{dc} (mW)	V_D - I_D (V – mA)	$F.O.M._D$
[21]	GaN-on-Si	100	33 - 38	26	2.0	20	28.4	540	6 - 90	6
[18]	GaN-on-SiC	150	27 - 29	20	4.0	12.5	N/R	800	10 - 80	2.2
[22]	GaN-on-SiC	40	30 - 40	25	1.5	11	20	100	2 – 50	5.6
[4]	GaN-on-Si	100	22 - 30	16	1.5	21	N/R	720	8 - 90	14.4
[23]	GaN-on-Si	100	18 - 31	22	1.9	16	28	280	3.5 - 80	8.7
OMMIC CGY2250U	GaN-on-Si	100	26 - 34	20	1.6	17	N/R	720	8 – 90	7.7
t.w. LNA D006GH	GaN-on-Si	60/100	27 - 31	23	1.2	16	26	150	5 – 30	13.4
t.w. LDA D01GH	GaN-on-Si	100	27 - 31	20	1.7	21	30	216	6 - 36	18.3

The FOM of the latter LNA is 12.1, in line with the one of the proposed LNA. Similar results for GaAs LNAs operating at Ka-band are reported in [25] and [26]. In [26] the comparison is more favourable for the referenced GaAs LNA due to its lower gain (higher IP1dB) and its relatively low P_{dc}, being biased at +2 V drain bias.

VI. CONCLUSION

Design solutions and characterization of two critical amplifier functionalities for low-noise SATCOM Ka-band receivers are highlighted and discussed. The selection of a dual gate length industrial grade GaN-on-Si process is justified. The designed Low-Noise Amplifier MMIC exhibits state-of-the-art for GaN 1.2 dB Noise Figure in the 27-31 GHz bandwidth thanks to a profitable combination of 60- and 100-nm gate length transistors on the same MMIC. The Low-Distortion Amplifier features +30 dBm OIP3 in the same frequency range. Both MMICs are operated at a relatively low, considering GaN technology, +5 V drain-to-source voltage. The LNA is also stressed with a CW input power up to +22 dBm without showing any degradation. The usefulness of the proposed design approaches for LNA and LDA are validated through a figure-of-merit that takes into account technology gate length, thus making the FOM an indicator of the applied design methodology. This research activity demonstrates that GaN technology can be used profitably in the lower part of the millimetre-wave spectrum in SATCOM receivers simultaneously requiring low-noise and high-linearity performance while minimizing dc power request.

REFERENCES

[1] A. Leuther, A. Tessmann, M. Dammann, H. Massler, M. Schlechtweg, and O. Ambacher, "35 nm mHEMT technology for THz and ultra low noise applications," in *Proc. Int. Conf. Indium Phosph. Rel. Mater. (IPRM)*, May 2013, pp. 1–2.

[2] Y.-L. Tang, N. Wadefalk, M. A. Morgan, and S. Weinreb, "Full Ka-band high performance InP MMIC LNA module," in *IEEE MTT-S Int. Microw. Symp. Dig.*, Jun. 2006, pp. 81–84.

[3] D. P. Nguyen, B. L. Pham, T. Pham, and A.-V. Pham, "A 14–31 GHz 1.25 dB NF enhancement mode GaAs pHEMT low noise amplifier," in *IEEE MTT-S Int. Microw. Symp. Dig.*, Jun. 2017, pp. 1961–1964. [Online]. Available: http://ieeexplore.ieee.org/document/8059048/

[4] X. Tong, R. Wang, S. Zhang, J. Xu, P. Zheng, and F.-X. Chen, "Degradation of Ka-band GaN LNA under high-input power stress: Experimental and theoretical insights," *IEEE Trans. Electron Devices*, vol. 66, no. 12, pp. 5091–5096, Dec. 2019. [Online]. Available: https://ieeexplore.ieee.org/document/8894418/

[5] P. E. Longhi, L. Pace, W. Ciccognani, S. Colangeli, and E. Limiti, "Low-noise amplifiers in gallium nitride for robust and highly linear Ka-band SATCOM," in *Proc. 53rd Annu. Meeting Italian Electron. Soc.* (Lecture Notes in Electrical Engineering). Cham, Switzerland: Springer, 2023, pp. 1–6. [Online]. Available: https://link.springer.com/book/9783031260650

[6] R. Leblanc, N. S. Ibeas, A. Gasmi, F. Auvray, J. Poulain, F. Lecourt, G. Dagher, and P. Frijlink, "6W Ka band power amplifier and 1.2 dB NF X-band amplifier using a 100 nm GaN/Si process," in *Proc. IEEE Compound Semiconductor Integr. Circuit Symp. (CSICS)*, Oct. 2016, pp. 1–4.

[7] V. Di Giacomo-Brunel, E. Byk, C. Chang, J. Grunenputt, B. Lambert, G. Mouginot, D. Sommer, H. Jung, M. Camiade, P. Fellon, D. Floriot, H. Blanck, and J.-P. Viaud, "Industrial 0.15-μm AlGaN/GaN on SiC technology for applications up to Ka band," in *Proc. 13th Eur. Microw. Integr. Circuits Conf.*, Sep. 2018, pp. 1–4. [Online]. Available: https://ieeexplore.ieee.org/document/8539905/

[8] "Win semiconductors offering sample kit for 0.15 microns GAN on sic process," *Microw. J.*, 2019. [Online]. Available: https://www.microwavejournal.com/articles/32939-win-semiconductors-offering-sample-kit-for-015-m-gan-on-sic-process

[9] E. Ture, F. Thome, D. Schwantuschke, M. Mikulla, and R. Quay, "E-band ultra-low-noise (4.5 dB) and high-power (27 dBm) GaN T/R front-end MMIC," in *Proc. 52nd Eur. Microw. Conf. (EuMC)*, Sep. 2022, pp. 756–759. [Online]. Available: https://ieeexplore.ieee.org/document/9924317/

[10] Y. Cao, V. Kumar, S. Chen, Y. Cui, S. Yoon, E. Beam, A. Xie, J. Jimenez, A. Ketterson, C. Lee, D. Linkhart, and A. Geiler, "Qorvo's emerging GaN technologies for mmWave applications," in *IEEE MTT-S Int. Microw. Symp. Dig.*, Aug. 2020, pp. 570–572. [Online]. Available: https://ieeexplore.ieee.org/document/9223913/

[11] X. Luo, J. Ouyang, Z. H. Chen, Y. Yan, L. Han, Z. Wu, T. Yu, and K. Zheng, "A scalable Ka-band 1024-element transmit dual-circularly-polarized planar phased array for SATCOM application," *IEEE Access*, vol. 8, pp. 156084–156095, 2020. [Online]. Available: https://ieeexplore.ieee.org/document/9174984/

[12] W. Ciccognani, S. Colangeli, A. Serino, L. Pace, S. Fenu, P. E. Longhi, E. Limiti, J. Poulain, and R. Leblanc, "Comparative noise investigation of high-performance GaAs and GaN millimeter-wave monolithic technologies," in *Proc. 14th Eur. Microw. Integr. Circuits Conf. (EuMIC)*, Sep. 2019, pp. 192–195.

[13] S. Colangeli, W. Ciccognani, P. E. Longhi, L. Pace, J. Poulain, R. Leblanc, and E. Limiti, "Linear characterization and modeling of GaN-on-Si HEMT technologies with 100 nm and 60 nm gate lengths," *Electronics*, vol. 10, no. 2, pp. 1–16, 2021. [Online]. Available: https://www.mdpi.com/2079-9292/10/2/134

[14] L. Pace, S. Colangeli, W. Ciccognani, P. E. Longhi, E. Limiti, R. Leblanc, M. Feudale, and F. Vitobello, "Design and validation of 100 nm GaN-on-Si Ka-band LNA based on custom noise and small signal models," *Electronics*, vol. 9, no. 1, p. 150, Jan. 2020.

[15] R. E. Lehmann and D. D. Heston, "X-band monolithic series feedback LNA," *IEEE Trans. Microw. Theory Techn.*, vol. MTT-33, no. 12, pp. 1560–1566, Dec. 1985.

[16] P. E. Longhi, L. Pace, S. Colangeli, W. Ciccognani, and E. Limiti, "Novel design charts for optimum source degeneration tradeoff in conjugately matched multistage low-noise amplifiers," *IEEE Trans. Microw. Theory Techn.*, vol. 69, no. 5, pp. 2531–2540, May 2021.

[17] C. Poole and R. Grammenos, "Correct equations for minimum noise measure of a microwave transistor amplifier," *IEEE Trans. Microw. Theory Techn.*, vol. 70, no. 2, pp. 1361–1366, Feb. 2022. [Online]. Available: https://ieeexplore.ieee.org/document/9633124/

[18] E. M. Suijker, M. Rodenburg, J. A. Hoogland, M. van Heijningen, M. Seelmann-Eggebert, R. Quay, P. Bruckner, and F. E. Van Vliet, "Robust AlGaN/GaN low noise amplifier MMICs for C-, Ku- and Ka-band space applications," in *Proc. Annu. IEEE Compound Semiconductor Integr. Circuit Symp.*, Oct. 2009, pp. 1–4.

[19] D. M. Pozar, *Microwave Engineering*, 4th ed. Hoboken, NJ, USA: Wiley, 2011.

[20] M. Ohtomo, "Stability analysis and numerical simulation of multidevice amplifiers," *IEEE Trans. Microw. Theory Techn.*, vol. 41, no. 6, pp. 983–991, Jun. 1993. [Online]. Available: http://ieeexplore.ieee.org/document/238513/

[21] C. Florian, P. A. Traverso, and A. Santarelli, "A Ka-band MMIC LNA in GaN-on-Si 100-nm technology for high dynamic range radar receivers," *IEEE Microw. Wireless Compon. Lett.*, vol. 31, no. 2, pp. 161–164, Jan. 2021. [Online]. Available: https://ieeexplore.ieee.org/document/9318994/

[22] M. Micovic, D. Brown, D. Regan, J. Wong, J. Tai, A. Kurdoghlian, F. Herrault, Y. Tang, S. D. Burnham, H. Fung, A. Schmitz, I. Khalaf, D. Santos, E. Prophet, H. Bracamontes, C. McGuire, and R. Grabar, "Ka-band LNA MMIC's realized in Fmax >580 GHz GaN HEMT technology," in *Proc. IEEE Compound Semiconductor Integr. Circuit Symp. (CSICS)*, Oct. 2016, pp. 1–4. [Online]. Available: http://ieeexplore.ieee.org/document/7751051/

[23] X. Tong, S. Zhang, P. Zheng, J. Xu, and X. Shi, "18–31 GHz GaN MMIC LNA using a 0.1 um T-gate HEMT process," in *Proc. 22nd Int. Microw. Radar Conf.*, May 2018, pp. 500–503. [Online]. Available: https://ieeexplore.ieee.org/document/8405269/

[24] L. Belostotski and E. A. M. Klumperink, "Figures of merit for CMOS low-noise amplifiers and estimates for their theoretical limits," *IEEE Trans. Circuits Syst. II, Exp. Briefs*, vol. 69, no. 3, pp. 734–738, Mar. 2022. [Online]. Available: https://ieeexplore.ieee.org/document/9540773/

[25] D. D. Vu, S. Chakraborty, Q. T. Chau, A. Jones, and M. Gorman, "A Ka-band low noise amplifier in 0.1 μm Gallium Arsenide pHEMT process," in *Proc. 17th Eur. Microw. Integr. Circuits Conf.*, Sep. 2022, pp. 72–75. [Online]. Available: https://ieeexplore.ieee.org/document/9923506/

[26] Z. Wang, D. Hou, Z. Li, P. Zhou, Z. Chen, J. Chen, and W. Hong, "A linearity-enhanced 18.7–36.5-GHz LNA with 1.5–2.1-dB NF for radar applications," *IEEE Microw. Wireless Compon. Lett.*, vol. 32, no. 8, pp. 972–975, Aug. 2022. [Online]. Available: https://ieeexplore.ieee.org/document/9756842/

PATRICK ETTORE LONGHI (Member, IEEE) received the M.S. degree in electronic engineering and the Ph.D. degree in microelectronics from the University of Rome "Tor Vergata," Italy, in 2004 and 2009, respectively. From 2009 to 2018, he was with ELT-Elettronica Group, Rome, Italy, holding several managerial and technical positions in engineering, manufacturing, and sales. Since August 2018, he has been an Assistant Professor with the Department of Electronic Engineering, University of Rome "Tor Vergata." He also acts as a Project Manager of research and innovation projects funded by European (EC, ESA, and EDA) and national agencies (MIUR, ASI, and Lazio Innova). His main research interests include analysis and synthesis methodologies for linear and noisy active networks at microwave and millimeter-wave frequencies, the design of signal conditioning circuits, and the design of multi-functional circuits for AESAs.

WALTER CICCOGNANI was born in Rome, Italy, in 1977. He received the M.S. degree in electronic engineering and the Ph.D. degree in telecommunications and microelectronics from the University of Rome "Tor Vergata," Rome, in 2002 and 2007, respectively. Since 2012, he has been an Assistant Professor with the University of Rome "Tor Vergata," where he has been teaching a course in microwave measurements, since 2013. He has coauthored more than 60 papers in international scientific journals and conferences and has been involved in several national and international research projects, and in those contexts, he had the opportunity to collaborate with major European semiconductor foundries. His main research interests include linear microwave circuit-design methodologies, linear and noise analysis/measurement techniques, and small-signal and noise modeling of microwave active devices.

SERGIO COLANGELI was born in Rome, Italy, in 1984. He received the Ph.D. degree in telecommunications and microelectronics from the University of Rome "Tor Vergata," Rome, in 2013. He has been with the Department of Electronics, University of Rome "Tor Vergata," ever since, where he is currently a Researcher. His research interests include low-noise design methodologies for microwave applications, with particular reference to low-noise amplification, and small-signal and noise characterization and modeling of microwave active devices. He was a recipient of the EuMIC Young Engineer Prize, in 2012.

ERNESTO LIMITI (Senior Member, IEEE) was a Research and Teaching Assistant, in 1991 and 1997, and an Associate Professor, from 1998 to 2001, with the Department of Electronic Engineering, University of Rome "Tor Vergata," Rome, Italy, where he has been a Full Professor of electronics, since 2001. He is currently the Head of the Department of Electronic Engineering and the Director of Microwave Engineering Center for Space Applications (MECSA). He is also the President of the Laurea and Laurea Magistrale degrees in electronic engineering with the University of Rome "Tor Vergata." He has authored or coauthored more than 500 publications in refereed international journals and presentations within proceedings of international conferences. His research activity is focused on three main lines, all of them belonging to the microwave and millimeter-wave electronics area. The first one is related to the characterization and modeling of active and passive microwave and millimeter-wave devices. Regarding active devices, the research line is oriented to small-signal, noise, and large-signal modeling. For active devices, novel methodologies are developed for the noise characterization and the subsequent modeling, and equivalent-circuit modeling strategies are implemented both for small- and large-signal operating regimes for GaAs, GaN, SiC, Si, and InP MESFET/HEMT devices. The second line is related to design methodologies and characterization methods for low-noise devices and circuits. The main focus is on cryogenic amplifiers and devices. Finally, the third line is in the analysis and design methodologies for linear and nonlinear microwave circuits. He is a member of the steering committee of international conferences and workshops and the Committee of the Ph.D. Program in telecommunications and microelectronics, tutoring an average of four Ph.D. candidates per year. He is also a referee of international journals in the microwave and millimeter-wave electronics sector.

Open Access funding provided by 'Universitá degli Studi di Roma "Tor Vergata"' within the CRUI CARE Agreement