IEEE Access
Multidisciplinary | Rapid Review | Open Access Journal

Received 16 January 2023, accepted 14 February 2023, date of publication 27 February 2023, date of current version 2 March 2023.

Digital Object Identifier 10.1109/ACCESS.2023.3249479

RESEARCH ARTICLE

Short- and Long-Term Memory Based on a Floating-Gate IGZO Synaptic Transistor

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This work was supported in part by the National Research Foundation of Korea (NRF) through the Korean Government [Ministry of Science and ICT (MSIT)] under Grant 2016R1A5A1012966 and Grant 2020R1A2B5B01001979. The work of Yoon Kim was supported by the 2022 Research Fund of the University of Seoul. The work of Dae Hwan Kim was supported by the Institute of Information and Communications Technology Planning and Evaluation (IITP) through the Korea Government (MSIT) under Grant 2021-0-01764.

ABSTRACT Short- and long-term neuroplasticity behaviors are key mechanisms for various activities. In this paper, we propose a synaptic transistor with a floating-gate (FG) node and an amorphous InGaZnO (IGZO) channel layer. The proposed device emulates the neuroplasticity functions of both short-term memory (STM) and long-term memory (LTM) through the control of the amplitude and the number of input pulses. The STM operated by ion movement in the gate dielectrics occurs when the input amplitude is relatively small (<9 V). The LTM operated through the storage of electrons in the FG occurs when the input amplitude is relatively large (>10 V). In addition, as the number of input pulses increases, information is stored for a longer time. Our FG IGZO synaptic transistor could be a promising device solution for brain-inspired computing systems.

INDEX TERMS Synapse device, neuromorphic system, IGZO, short-term memory, long-term memory, synaptic transistor.

I. INTRODUCTION

Conventional computing systems are based on the von Neumann architecture, in which the processing and memory units are physically separated. These systems are well-suited for high-precision data processing and accurate boolean logic operations. However, they suffer from an inherent drawback referred to as the von Neumann bottle-neck. Shuttling data between the processing and memory units consumes a significant amount of power and latency. Owing to this shortcoming, von Neumann systems are usually inefficient in performing big data-based artificial intelligence tasks, such as learning, reasoning, recognition, and decision making. Brain-inspired computing systems that emulate the structure and working principles of the biological nervous system present promising solutions for next-generation computing systems [1], [2], [3], [4], [5].

The memory unit in the biological neural system is composed of synapses that serve as electrical connections between neurons. The connection strength of synapses and their overall connection structure are key mechanisms for various brain activities. Two types of neuroplasticities have been reported, wherein changes in the connection strength (synaptic weight) are caused by learning events. Short-term plasticity can be achieved through a temporal change in the synaptic weight based on a less frequent input stimulus, which rapidly decays to its initial state [6]. However, more frequent input stimuli cause a semi-permanent change in the synaptic weight, which is known as long-term plasticity.

The associate editor coordinating the review of this manuscript and approving it for publication was Cristian Zambelli.

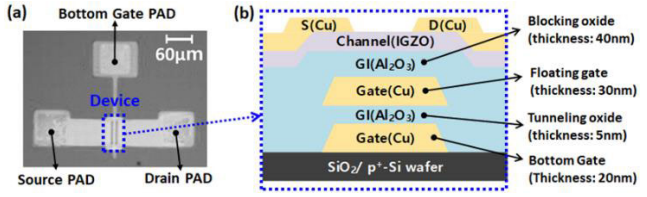

FIGURE 1. Floating-gate IGZO synaptic transistor sample. Blue dotted line indicates the device active region. (a) Top view of the layout image. (b) Schematic structure of device active region.

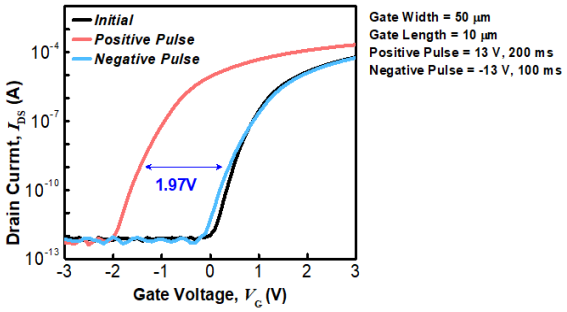

FIGURE 2. I_D-V_G characteristics of the fabricated devices.

Several memory devices have been demonstrated to exhibit both short- and long-term plasticity behaviors [7], [8], [9], [10], [11], [12], [13], [14], [15]. The synaptic weight is represented by the conductance of a memory device. In this paper, we propose a synaptic transistor with a floating-gate (FG) node and an amorphous InGaZnO (IGZO) channel layer. Most previous devices have implemented a short-term memory (STM) and long-term memory (LTM) as a single operation mechanism. For example, memristor-based devices implement both short- and long-term memory operations using an ion migration mechanism. In this case, the boundary of the input operation condition that distinguishes the short- and long- term operations become ambiguous and is more vulnerable to device-to-device variation. The proposed device is based on different operation mechanisms for each memory operation, and to the best of our knowledge, it is the first of its kind. Notably, short- and long-term memory operations are based on ion migration and charge storage, respectively.

II. FLOATING-GATE IGZO SYNAPTIC TRANSISTOR

Amorphous IGZO (a-IGZO) is an attractive channel material for thin-film transistors owing to its high on/off ratio, low-temperature processing capability, and good compati-bility with the silicon complementary metal–oxide–semiconductor process [16], [17], [18]. In this study, we fabricated a floating-gate synaptic transistor with an IGZO channel layer, as depicted in Figure 1.

Key fabrication steps of the device are as follows:

The Cu layer was deposited by an electron-beam(E-beam) evaporator with a thickness of 20nm and patterned to form the bottom gate on the SiO_2/Si substrate. The Al_2O_3 layer with a thickness of 5 nm was deposited by atomic layer deposition (ALD) for constructing tunneling oxide. Then,

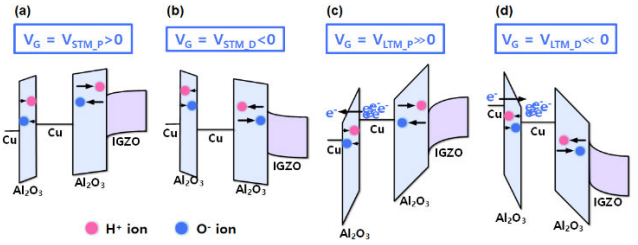

FIGURE 3. STM and LTM operation mechanisms in the floating-gate IGZO synaptic transistor. (a) STM potentiation operation. (b) STM depression operation. (c) LTM potentiation operation. (d) LTM de-pression operation.

the floating-gate Cu layer with a thickness of 30 nm was deposited by an E-beam evaporator. Next, the Al_2O_3 blocking oxide layer with a thickness of 40 nm and the a-IGZO layer with a thickness of 35 nm are deposited by ALD and sputtering, respectively. Finally, source and drain electrode were patterned with Cu.

The electrical properties of the fabricated devices were measured in the dark at room temperature using an Agilent B1500A semiconductor parameter analyzer (Agilent Technologies, Santa Clara, California, United States).

The fabricated FG IGZO synaptic transistor showed sound transfer characteristics (drain current-gate voltage) and conventional long-term memory characteristics as shown in Figure 2.

Figure 3(a) presents a schematic of the STM mechanism in the proposed device. When the ALD process is performed for the Al_2O_3 deposition, residual hydrogen can be produced due to incomplete chemical reaction between $Al(CH_3)_3$ and H2O [19], [20]. In our previous studies, it was confirmed that the hydrogen ion can migrate inside Al_2O_3 layer [21], [22]. In addition, Al_2O_3 is widely used as a switching material in the resistive random access memory (RRAM) field based on the movement of oxygen ions inside [23], [24], [25]. Therefore, the movement of these ions inside Al_2O_3 layer can cause the STM operation.

When a positive STM potentiation voltage (V_{STM_P}) was applied to the gate, H^+ ions inside the Al_2O_3 layer moved towards the IGZO channel, whereas the O^{2-} ions moved away from the channel. Consequently, the threshold voltage (V_{th}) was negatively modulated; hence, the conductance (drain current) increased, as depicted in Figure 3(a). In contrast, when a negative STM depression voltage (V_{STM_D}) was applied to the gate, the ions moved in the direction of increasing threshold voltage, and the conductance (drain current) decreased, as depicted in Figure 3(b).

Because the proposed device has a FG node surrounded by insulating layers (tunneling oxide and blocking oxide), the LTM operation is possible like conventional nonvolatile FG memories [26], [27]. Electrons injected by tunneling according to the application of a high depression voltage are stored in an electrically insulated FG node until they are removed by another application of high potentiation voltage. The threshold voltage of a memory cell and hence the drain

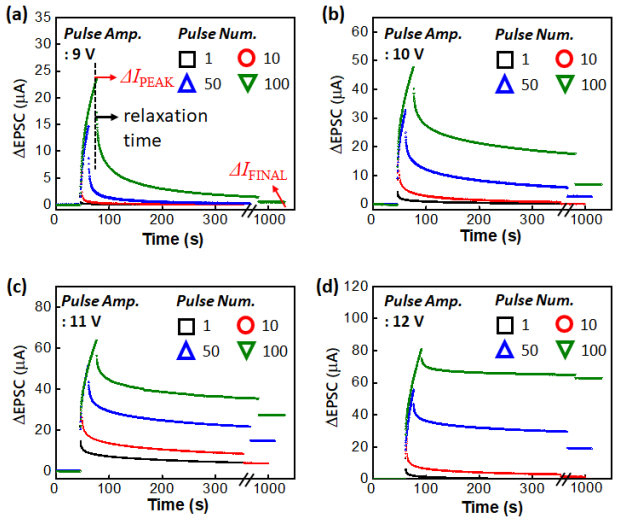

FIGURE 4. Memory characteristics of the FG IGZO synaptic transistors with pulse amplitudes of (a) 9 V, (b) 10 V, (c) 11 V, and (d) 12 V. The frequency of pulse trains is 3.27 Hz, and each pulse duration is 300 ms. The drain current is measured at $V_G = 2$ V and $V_D = 2$ V. The gate width and length of the device are 10 μm and 5 μm, respectively.

current (conductance) is determined by the total amount of charge stored in the FG. The LTM mechanism of the proposed device is illustrated in Figure 3(c) and (d). It should be noted that the locations of the blocking and tunneling oxides are different from those in conventional FG memories. In the case of conventional n-channel FG memory, when a gate voltage high enough to cause tunneling is applied, the threshold voltage increases as the electrons are tunneled from the channel toward the FG. However, because the tunneling oxide is located between the FG node and gate in the proposed device, electrons are extracted from the FG while an positive LTM potentiation voltage (V_{LTM_P}) is applied, as depicted in Figure 3(c). Consequently, the threshold voltage (V_{th}) is negatively modulated; hence, the conductance (drain current) increases.

The conductance reduction during the LTM depression operation is illustrated in Figure 3(d). Through this device configuration, the polarity of the gate bias that induces potentiation or depression can be unified for both the STM and LTM. The electrons (information) stored in the FG node can be retained for a long duration, similar to that in typical flash memories, because the FG node is surrounded by gate dielectrics. The potentiation memory characteristics of FG IGZO synaptic transistors are illustrated in Figure 4. The excitatory postsynaptic current (EPSC) represents the drain current of synaptic transistors when $V_G = V_D = 2$ V. The EPSC gradually increases with a train of potentiation voltages and then decays gradually during the relaxation time. This decay phenomenon is attributed to the return of ions (H^+ and O^{2-}) toward their initial positions. When the potentiation pulse amplitude is lower than 9 V, the STM operation occurs, as illustrated in Figure 4(a), where the EPSC eventually returns to its initial value. As the number of pulses increases

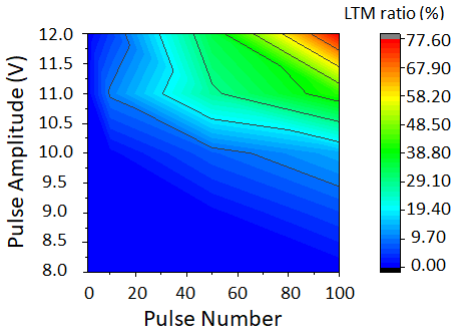

FIGURE 5. Contour map of the LTM ratio as a function of the pulse amplitude and number.

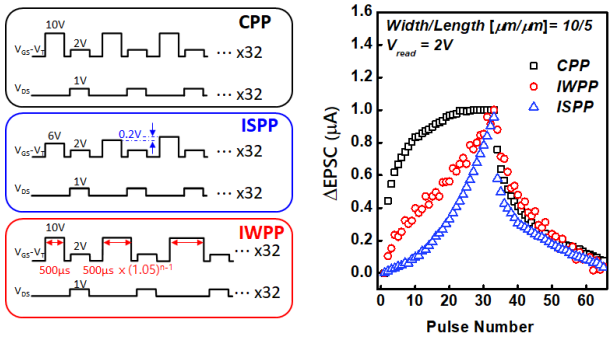

FIGURE 6. Conductance modulation characteristics of the proposed synaptic transistor with CPP, ISPP, and IWPP methods.

from 1 to 100, the decay time, which is defined as the relaxation time after which the change in the EPSC completely disappears, increases from 5 to 800 s. This characteristic is similar to human STM, which is known to obey the Hermann Ebbinghaus forgetting curve [28]. The information stored by more frequently performed learning events (input pulses) is remembered for a longer period, which implies that the most effective learning approach for the human brain is repetitive learning.

When the potentiation pulse amplitude is larger than 10 V, the proposed synaptic transistors exhibit not only STM but also LTM characteristics, as depicted in Figure 4(b)-(d). In the LTM operation, the EPSC did not return to its initial value, even after a relaxation time of 1000 s. We separated the total stored information into the STM and LTM components according to the following equations:

$$\text{STM ratio}\,(\%) = \frac{\Delta I_{PEAK} - \Delta I_{FINAL}}{\Delta I_{PEAK}} \quad (1)$$

$$\text{LTM ratio}\,(\%) = \frac{\Delta I_{FINAL}}{\Delta I_{PEAK}} \quad (2)$$

where ΔI_{FINAL} is defined as ΔESPC at a relaxation time of 1000 s, as depicted in Figure 4(a). A contour map of the LTM ratio under various pulse conditions is depicted in Figure 5. We can observe that the LTM operation cannot be implemented with a small amplitude of less than approximately 10 V, even though the number of pulses increases.

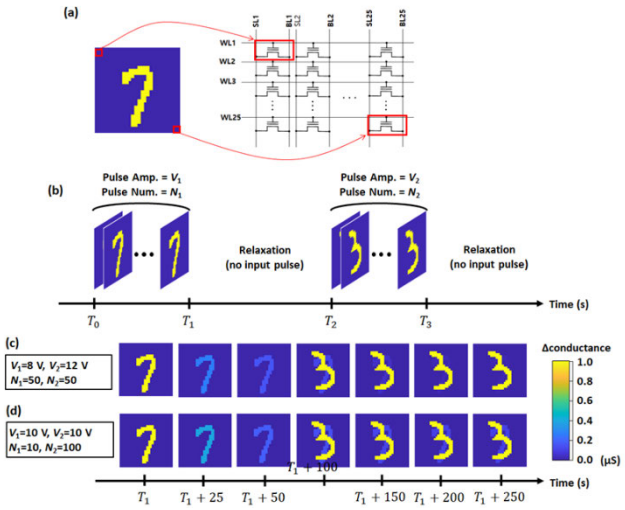

FIGURE 7. Memorization of images on a 25 × 25 crossbar array of the FG IGZO synaptic transistor. (a) Image of digits were memorized into the array. (b) Image "7" was stored in the STM mode (pulse amplitude = V_1, pulse number = N_1). After a relaxation time, image "3" was stored in the LTM mode (pulse amplitude = V_2, pulse number = N). (c) Snapshots of the conductance changes for $V_1 = 8$ V, $V_2 = 12$ V, and $N_1 = N_2 = 50$. (d) Snapshots of the conductance changes for $N_1 = 10$, $N_2 = 100$, and $V_1 = V_2 = 10$.

These results present that the most important factor for the selective operation of an STM or LTM is the pulse amplitude.

In order to implement accurate learning process in neuromorphic applications, gradual potentiation and depression characteristics of synaptic devices is crucial. Especially, linearity and symmetry of the synaptic device is needed for precise conductance modulation. Figure 6 shows the measured potentiation-depression conductance modulation as a function of the number of pulses through the following three dynamic methods: constant pulse programming (CPP) that was used in the previous experimental results (Figure 4 and 5), incremental width pulse programming (IWPP), and incremental step pulse programming (ISPP). Because the charges stored in the floating gate reduce the effective electric field required for tunneling, the amount of tunneling charge during each pulse step gradually decreases as the number of applied pulse increases in the CPP method. However, if IWPP or ISPP is used to make the tunneling charge constant for each pulse step, highly linear and symmetric conductance modulation can be obtained.

III. APPLICATION SIMULATION

To demonstrate the STM and LTM in the proposed FG IGZO synaptic transistor, we simulated an image memorization application with binary 25 pixel × 25 pixel images. As illustrated in Figure 7(a), image memorization operation can be performed by matching each pixel of the image one-to-one to each synaptic transistor cell on the 25 × 25 crossbar array. By applying potentiation pulses only to the device cell corresponding to the yellow pixel, the array stores the digit image. We performed array simulation by reflecting the measured device characteristics. Figure 7(b) shows the image input that is fed into the array. Initially, image of the number "7" were fed into the array by applying voltage pulses. After the relaxation time, image of the number "3" were input into to array. Snapshots of the conductance changes at various instances are presented in Figure 7(c) and (d). The image corresponding to "7" stored in the STM mode through a smaller input amplitude (Figure 7(c)) or a smaller number of pulses (Figure 7(d)) was eventually forgotten. During the pulsing of the "3" pattern into the array, notice that there is some period in which the previous STM image information and the new LTM image information coexist at the same time. Eventually, the synaptic transistor array will "forget" the "7" pattern leaving behind the "3" pattern. Finally, the array "remember" the "3" pattern stored in the LTM mode for a long time. These simulation results clearly indicate that the STM and LTM can be implemented simultaneously in the proposed device.

IV. CONCLUSION

A synaptic transistor was designed and fabricated; subsequently, Cu and IGZO were employed as the FG node and active channel, respectively. We successfully demonstrated STM and LTM operations with variations in the input pulse conditions. When the input amplitude was small (<9 V), the STM operation occurred, with plasticity (conductance) changes according to the movement of ions in the gate dielectrics. When the input amplitude was large enough to cause tunneling of electrons (>10 V), the LTM operation occurred with modulated plasticity (conductance) according to the amount of semi-permanently stored electrons in the FG node. The proposed FG IGZO synaptic transistor is a promising candidate for next-generation brain-inspired computing systems.

ACKNOWLEDGMENT

(Dongyeon Kang and Wonjung Kim contributed equally to this work.)

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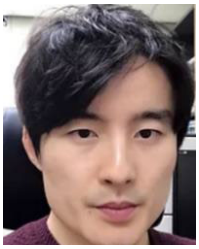

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