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RESEARCH ARTICLE

Design, Simulation and Optimization of an Enhanced Vertical GaN Nanowire Transistor on Silicon Substrate for Power Electronic Applications

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ABSTRACT A new vertical transistor structure based on GaN nanowire is designed and optimized using the TCAD-Santaurus tool with an electrothermal model. The studied structure with quasi-1D drift region is adapted to GaN nanowires synthesized with the bottom-up approach on a highly n-doped silicon substrate. The electrical performance is studied as a function of various epi-structure parameters, including region lengths and doping levels, nanowire diameter, and the impact of the surface states. The results reveal that the optimized structure has a Normally-OFF mode with a threshold voltage higher than 0.8 V and exhibits minimized leakage current, low on-state resistance, and maximized breakdown voltage. To the best of our knowledge, this is the first exhaustive study of GaN-based nanowire transistors, providing valuable insights for the scientific community and contributing to a deeper understanding of the impact of GaN nanowire parameters on device performance.

INDEX TERMS Normally-off, vertical transistor, GaN, nanowire, gate-all-around, sentaurus TCAD, breakdown voltage, on-state resistance, surface states, threshold voltage.

I. INTRODUCTION

The most widely used semiconductor for the fabrication of electronic devices is silicon due to its low cost. However, its physical properties do not allow it to meet the needs of today's and tomorrow's mass-market power electronics [1], [2].

Gallium nitride (GaN) technology is one of the most promising alternatives to overcome Silicon limitations, thanks to their excellent physical parameters [3]. GaN on silicon-based technology is recognized as mature enough for fabricating power electronic devices able to withstand harsh temperatures and environments. Its price-performance ratio in the 100 V – 650V [4] range makes it the best candidate to satisfy the demand for high-power applications requiring Normally-OFF transistors [5]. The electric vehicle market is the fastest-growing market for these devices [6].

Currently, the most mature technologies to fabricate GaN-based power transistors on silicon substrate are MOS-HEMT [7], [8] and Junction-HEMT [9], which are based on the p-GaN layer. However, these lateral devices suffer from several limitations [3]: i) leakage currents through traps (surface, gate, and buffer layer) [10], [11]; ii) High self-heating at the channel leads to the degradation of the transport properties [12]; iii) The vertical breakdown [13].

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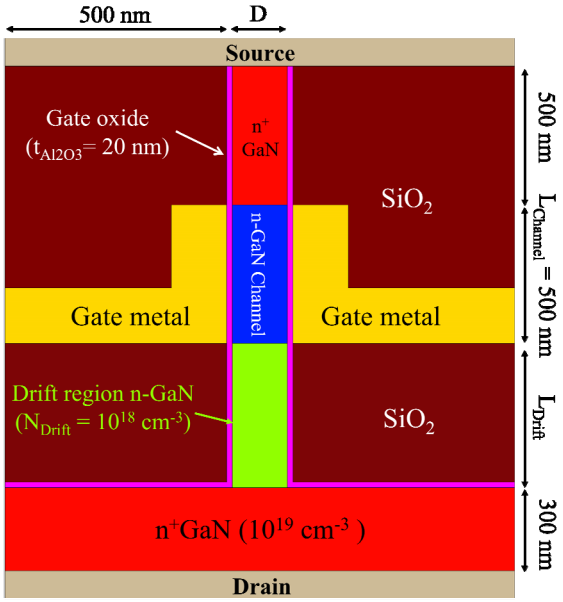

FIGURE 1. Schematic cross-section of the initial nanowire transistor structure.

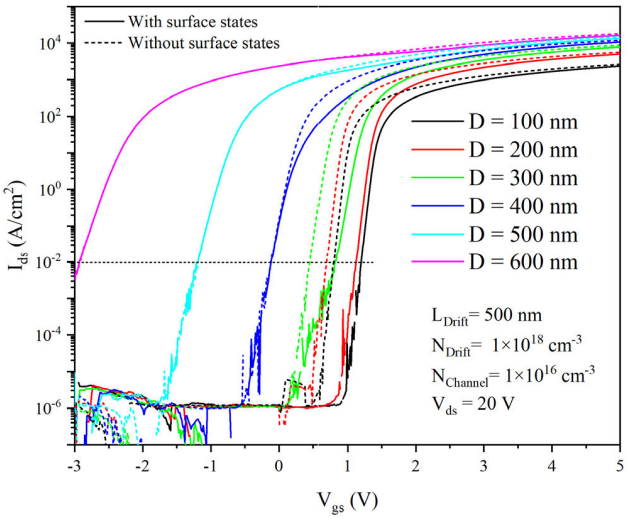

FIGURE 2. Transfer characteristics I_{ds}-V_{gs} of the simulated transistor for different diameters.

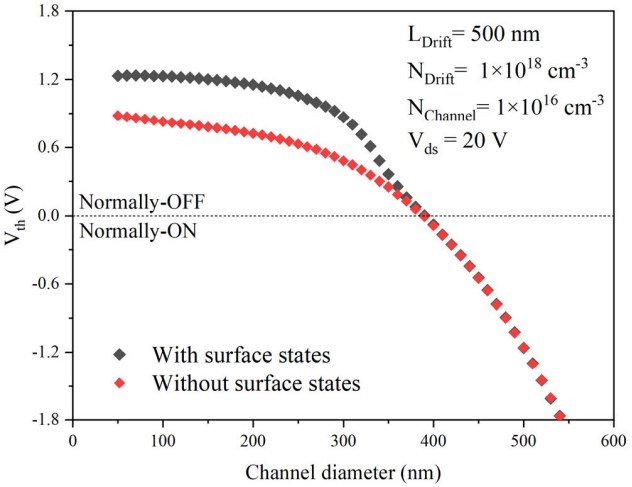

FIGURE 3. Threshold voltage values versus channel diameter are obtained for a channel doping level of 1 × 10^{16} cm^3.

In order to overcome these problems, a new GaN vertical device architecture has emerged as an alternative solution to this planar technology [9]. This new device architecture allows for better electric field distribution, keeping it confined to the volume of the GaN far from the device surface, thanks to the guard-ring approach [14]. Additionally, the vertical structure is more suitable for efficiently dissipating heat generated during device operation [15]. In this context, several works have been reported in the literature, such as VHFET [16], CAVET [17], and FinFET [18], which use a GaN substrate to reduce dislocations in the GaN epi-layer, improve the device's breakdown voltage, and enhance thermal dissipation [19]. However, these technologies are costly due to the small size of available GaN wafers, making it challenging to introduce them into the semiconductor market in the near future.

To reduce the cost of GaN vertical devices, another technology based on a nanowire approach is a promising alternative [20]. Indeed, nanowires without dislocations [21], [22] can be obtained using a bottom-up approach on the silicon substrate, depending on their density and diameter. This new approach offers the same advantages as the standard GaN vertical device. In addition, the insulated Gate-All-Around (GAA) surrounding the channel region allows for more efficient electrostatic control of the drain current [23]. Several devices based on GaN nanowires have been published in the literature [23], [24], [25]. However, their performance needs to meet the potentialities of GaN for several reasons: the device architecture, the doping levels, and the dimensions of the epi-structure need to be optimized.

This study aims to find a set of optimized parameters for the fabrication of vertical GaN nanowire transistors using the TCAD Sentaurus simulator. The objectives are to achieve a positive threshold voltage to ensure a Normally-OFF operation mode with a trade-off between the on-state resistance R_{ON} and the breakdown voltage V_{BR} of the device.

II. SIMULATION SETUP

A. DEVICE STRUCTURE

The starting nanowire-based device structure used as a reference in this TCAD simulation work is shown in figure 1. The total epi-structure is 1.8 μm of GaN, starting with a 300 nm highly doped n^+GaN layer (1 × 10^{19} cm^{-3}) connecting the drain metal on the device's backside. The bottom region of the nanowire is the drift region n-doped to 1 × 10^{18} cm^{-3} (N_{Drift}) with a length of 500 nm (L_{Drift}). These two parameters are modified in this work to maximize the transistor breakdown voltage. The conductive channel is made of a

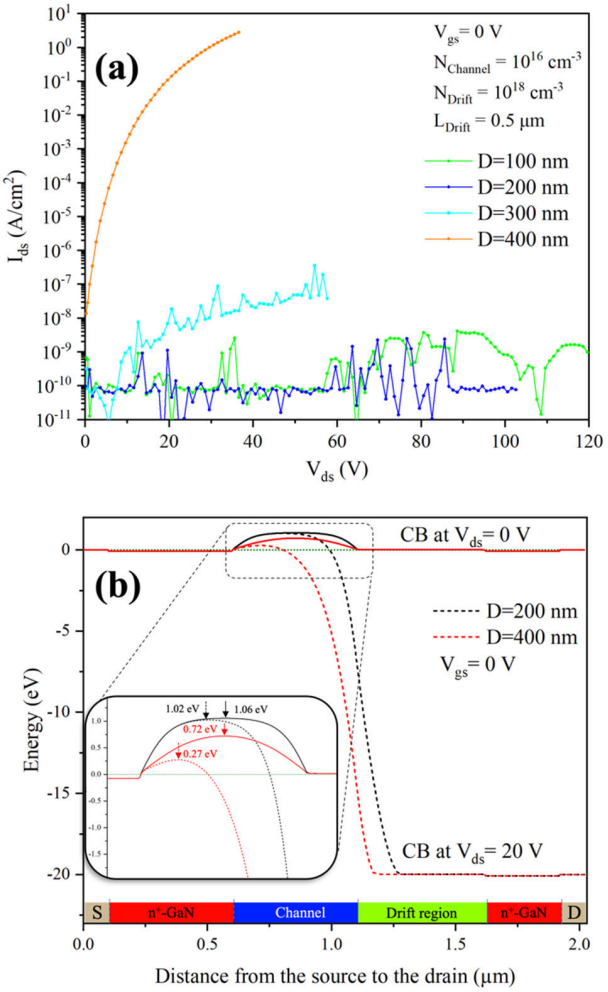

FIGURE 4. (a) Leakage current versus V_{ds} for different nanowire diameters. (b) Band diagrams from source to drain along the center of the nanowire, at V_{gs} = 0 V, for different diameters and drain voltages (V_{ds} = 0 V and V_{ds} = 20 V).

n-GaN ($N_{channel} = 1 \times 10^{16}$ cm^{-3}). The top region of the nanowire is highly doped (1×10^{19} cm^{-3}) to reduce the source ohmic contact resistance. In addition, the nanowire sidewall surface and the top of the drain n$^+$GaN layer are passivated with a 20 nm thick layer of Al_2O_3. The gate metal is deposited on a SiO_2 isolation layer and surrounds the channel. Finally, another isolation layer of SiO_2 is used to support the source contact and to ensure electrical insulation with the gate.

The current densities were normalized with respect to the total device active area in all the simulations performed in this work. Indeed, the distance between the edges of two adjacent nanowires is 1 μm, so the active area is composed of the nanowire surface plus a doughnut-shaped surface of 0.5 μm radius of flat gate metallization surrounding the nanowire. Vertical gate metallization is a critical process that must be reproducible and robust. For that purpose, we choose to

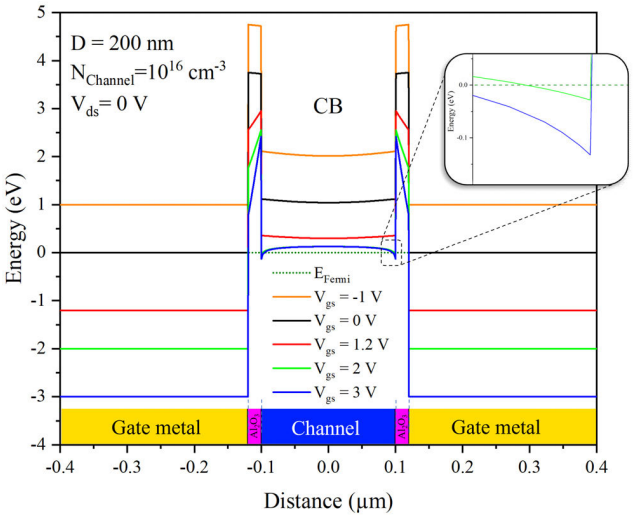

FIGURE 5. Conduction band diagrams of a horizontal cross-section's diameter nanowire of 200 nm for different gate bias voltages.

maintain a 1 μm gap between two nanowires regardless of their surface area.

B. SIMULATION MODELS

The design and simulation of the vertical GaN nanowire transistor are made using the Sentaurus TCAD tool based on the finite element method. The structure is first designed as a 2D cross-section and then rotated using the cylindrical coordinates to simulate the Gate-All-Around nanowire device. The physical models are based on the Drift-Diffusion (D-D) transport model and Fermi-Dirac statistics. The thermodynamic model has also been considered to include the thermal effect on the device's electrical transport. Moreover, the Auger, radiative, avalanche and Shockley-Read-Hall generation-recombination mechanisms are also activated. To consider the impact of the surface states at the Al_2O_3/GaN interface, the surface states are added as acceptor types uniformly distributed at 0.8 eV from the conduction band with a surface states density of 1×10^{13} eV^{-1}.cm^{-2} [26], [27]. The relative permittivity values of $\varepsilon_r = 3.9$ [28] and $\varepsilon_r = 9.1$ [29] are used for SiO_2 and Al_2O_3 dielectrics materials, respectively.

III. PERFORMANCE ANALYSIS AND SIMULATION RESULTS

In this section, the optimization and the performance analysis of the reference structure are presented. The first step of this work is the study of the impact of the channel parameters (diameter D and doping level) on the control of the drain current by the voltage applied to the gate. The optimal parameters extracted from this first investigation will further improve the device's on-state resistance R_{ON} and breakdown voltage V_{BR} by optimizing the quasi-1D drift region parameters.

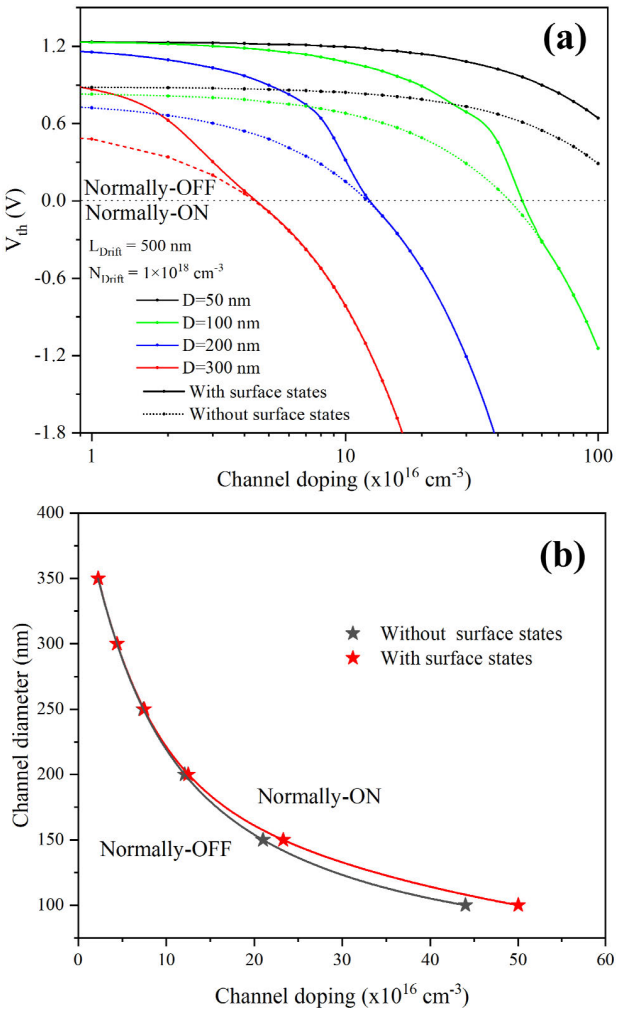

FIGURE 6. (a) Extracted threshold voltage at I_{ds} = 10 mA/cm^2 versus channel doping for different diameters, with and without surface states. (b) Evolution of the critical channel doping level (where the device switches from Normally-ON to Normally-OFF mode) versus the nanowire diameter with and without surface states.

A. CHANNEL REGION: EFFECT OF DIAMETER, DOPING LEVEL, AND SURFACE STATES

The effect of channel diameter (D varying from 100 nm to 600 nm) on the I_{ds}-V_{gs} electrical characteristics, with and without surface states, is shown in figure 2. The drift region length is set at 500 nm, and its doping level is set at 1×10^{18} cm^{-3}. The drain voltage V_{ds} is fixed at 20 V.

It is clearly observed that the diameter D significantly affects the threshold voltage (defined at I_{ds} = 10 mA/cm^2), and for small diameters (below 400 nm), the pinch-off voltage shifts towards positive values, leading to Normally-OFF operation mode devices. The presence of surface states accentuates this phenomenon for nanowire diameters less than 300 nm. Figure 3 shows the evolution of the threshold voltage versus the channel diameter, with and without surface states. These last lead, for small diameters, to a shift of around +0.4 V in the threshold voltage compared to the nanowire

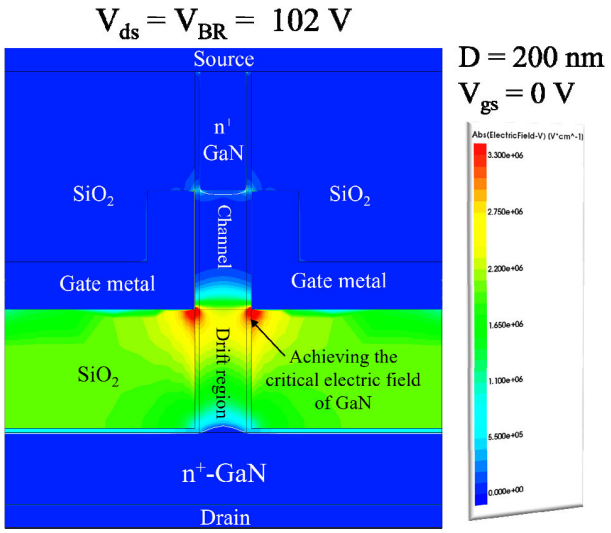

FIGURE 7. Electric field mapping at V_{gs} = 0 V and V_{ds} = 102 V by setting the channel diameter to 200 nm and the length of the drift region to 0.5 μm.

without surface states. This is due to the surface depletion depth that becomes comparable to the nanowire radius.

In figures 2 and 3, the pinch-off voltage is extracted at V_{ds} = 20 V. The reason for that is because we observed on I_{ds}-V_{ds} characteristics that when the diameter of the nanowire increases, the transistor that seems to be pinched-off at low drain voltage becomes non-pinched-off at 20 V. Figure 4(a) shows the evolution of the leakage current at V_{gs} = 0 V for different nanowire diameters at high drain voltage. For a nanowire diameter of 400 nm, the leakage current increases at high V_{ds}, resulting in a device that is not in the Normally-OFF mode. To explain the origin of this behavior, the conduction band from source to drain along the center of the nanowire is plotted for two nanowire diameters (D = 200 nm, D = 400 nm) while considering the presence of surface states at V_{gs} = 0 V, and for two different drain-source voltages: V_{ds} = 0 V and V_{ds} = 20 V, as shown in figure 4(b).

Figure 4(b) shows that the electrons cannot flow from the source to the drain at low drain voltage due to the conduction band barrier at the channel region, regardless of the nanowire diameter. For a 200 nm diameter, this barrier is equal to 1 eV and remains constant even at V_{ds} = 20 V. This means that the transistor is pinched-off even at high drain voltage. However, in the case of a 400 nm diameter, the conduction band barrier is equal to 0,72 eV at V_{ds} = 0 V, which drops to 0,27 eV at V_{ds} = 20 V. So, the device pinch-off is not sharp enough because of the phenomenon called Drain-induced barrier lowering (DIBL). As a result, the leakage current increased and passed through the center of the channel at high V_{ds}. This effect becomes increasingly significant as the diameter of the nanowire increases.

Figure 5 shows the conduction band diagrams of a horizontal cross-section of the Metal/Al_2O_3/GaN/Al_2O_3/Metal structure. These curves are plotted at the mid-channel for a

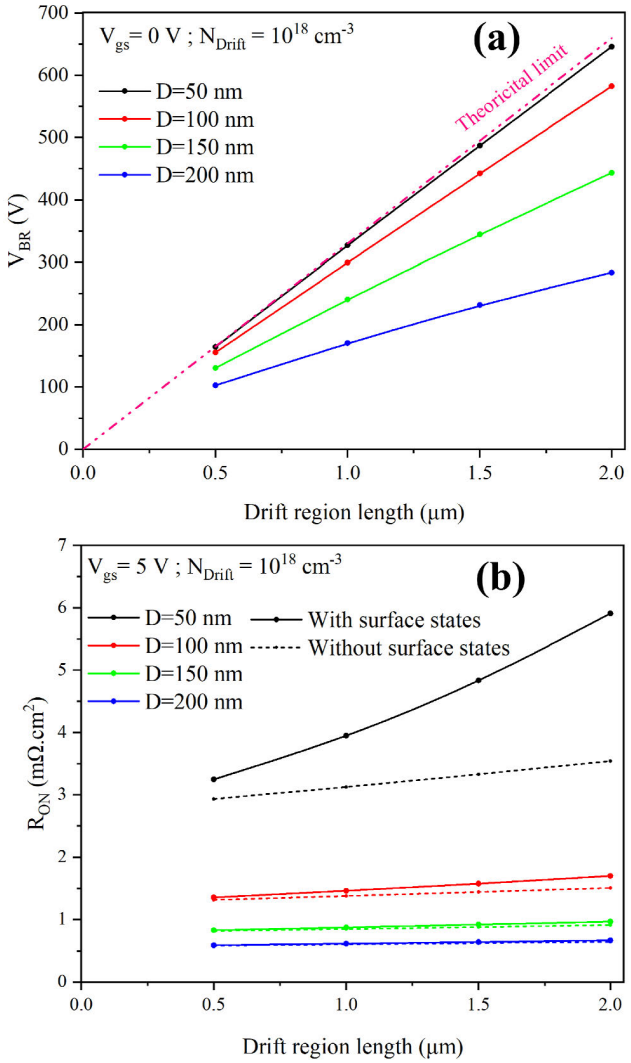

FIGURE 8. Evolution of breakdown voltage V_{BR} (a) and on-state resistance R_{ON} (b) as a function of drift region length doped at 1 × 10^{18} cm^{-3} for several nanowire diameters, with and without surface states.

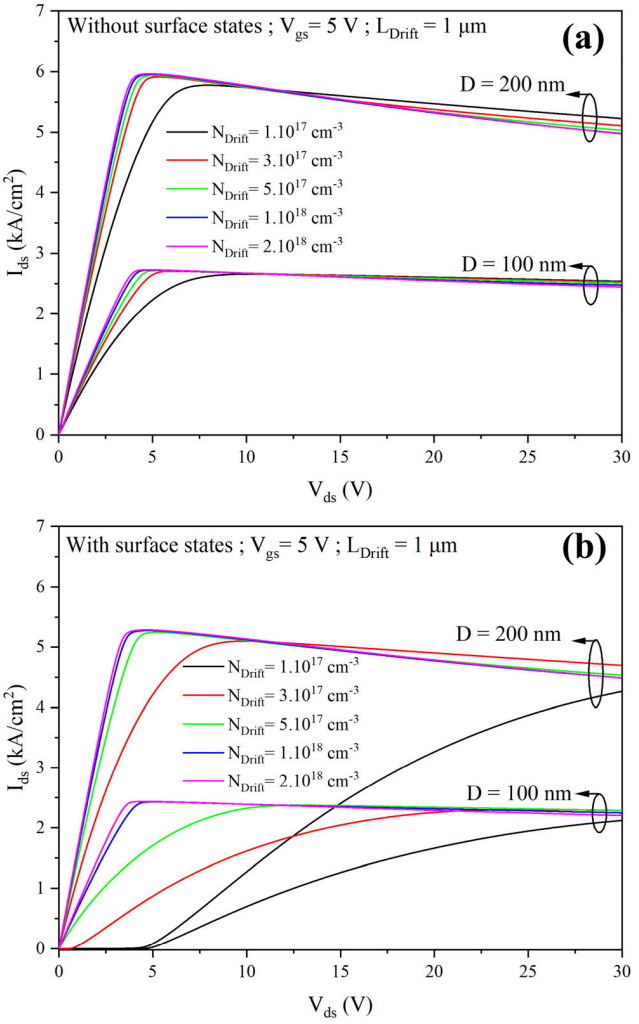

FIGURE 9. I_{ds}-V_{ds} characteristics as a function of drift region doping level, without (a) and with (b) surface states and for nanowire diameters of 100 nm and 200 nm.

nanowire diameter of 200 nm, considering the presence of the surface states for different gate bias voltages and with $V_{ds} = 0$ V.

Figure 5 shows the three behaviors of the conduction band at $V_{ds} = 0$ V: i) When $V_{gs} < V_{th}$, the conduction band is always above the Fermi level, resulting in a depleted channel region; ii) When $V_{gs} = V_{th}$, the conduction band is close to the Fermi level, meaning that the conductive channel starts to be formed; iii) At $V_{gs} > V_{th}$, the conduction band drops deeper below the Fermi level, resulting in an accumulation of electrons in the well at the Al_2O_3/GaN interface. In this latter case, a two-dimensional conductive channel is formed, and electrons start flowing from the source to the drain by applying a small positive voltage at the drain.

In the previous study, the n-type channel doping was set to 1 × 10^{16} cm^{-3}, a reference value we used as a starting point. Here, the impact of channel doping on the threshold voltage is investigated for different nanowire diameters. These results are shown in figure 6(a). The curves show that the Normally-OFF mode persists over a more extensive doping range when the nanowire diameter is reduced.

Figure 6(b) presents the nanowire diameter versus the critical doping level at which the transistor switches from the Normally-OFF mode to the Normally-ON mode. Using these curves, the maximum appropriate channel doping levels that result in the Normally-OFF operation mode for a wide range of nanowire diameters up to 350 nm can be determined. Based on these findings, we choose the nanowire with diameters less than 200 nm for the remaining part of this paper.

B. IMPACT OF THE QUASI-1D DRIFT REGION

In order to identify the region where the electrical breakdown occurs at high V_{ds} in the Normally-OFF transistor, the reference structure with a channel diameter of 200 nm and a drift region length (L_{Drift}) of 0.5 μm doped at 1 × 10^{18} cm^{-3}

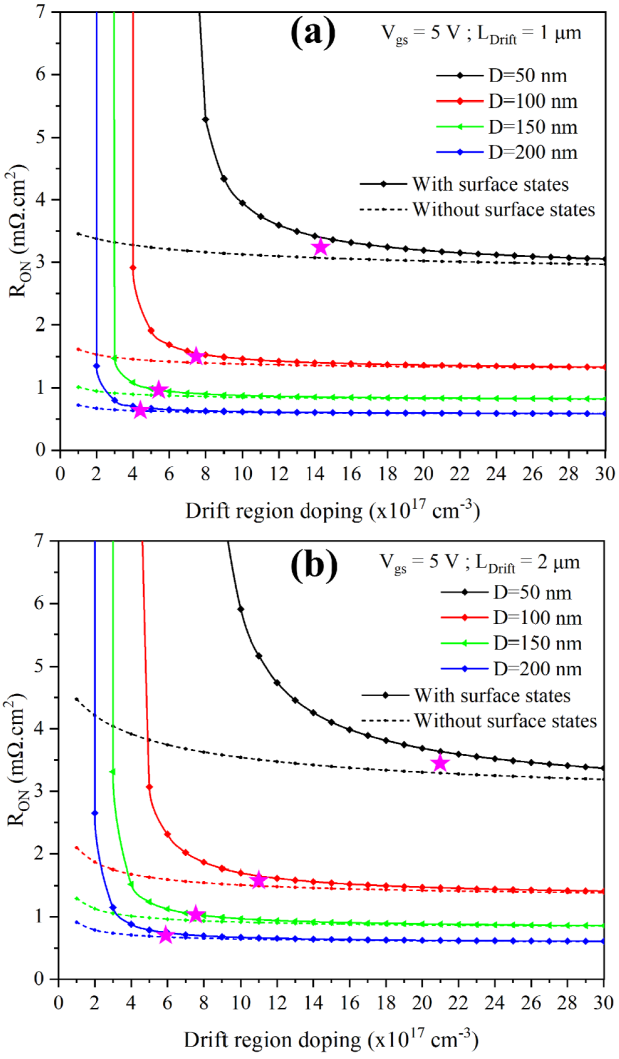

FIGURE 10. Evolution of the on-state resistance R_{ON} as a function of the doping level of the drift region, for a length L_{Drift} = 1 μm (a) and L_{Drift} = 2 μm (b).

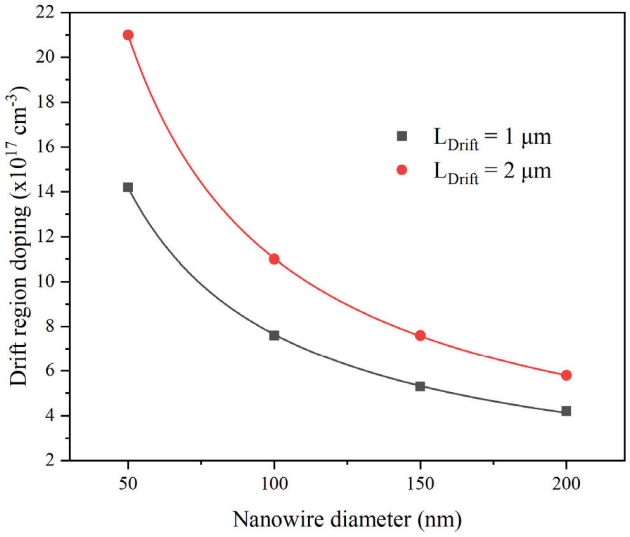

FIGURE 11. Best doping level to achieve a good R_{ON} as a function of the nanowire diameter for two different lengths of the drift region.

is simulated. The GaN breakdown electrical field is set to 3.3 MV/cm [30]. Figure 7 shows the electric field map at V_{gs} = 0 V for V_{ds} = 102 V (breakdown voltage). In this configuration, the conduction band barrier height along the channel remains at 1 eV, as seen in figure 4, regardless of the applied drain voltage. The electric field reaches its maximum at the channel/drift region interface near the gate metal corner. This local field's amplitude decreases as the drift region length increases.

Figure 8(a) shows that increasing the drift region length while maintaining its doping level constant (at 1 × 10^{18} cm^{-3}) results in a quasi-linear increase in breakdown voltage, and the slope decreases as the nanowire diameter increases. However, the doping level of the drift region can be adjusted to maximize the breakdown voltage for specific nanowire diameter devices.

Figure 8(b) shows that the on-state resistance R_{ON} increases with the length of the drift region and decreases with increasing nanowire diameter, in agreement with the microscopic Ohm's law. Furthermore, this resistance is more significant in the presence of surface states, and this phenomenon is even more noticeable when the nanowire diameter is small. Indeed, these surface states along the nanowire surface deplete the drift region, thus reducing the conductive section of the nanowire. This explains why this phenomenon is more sensitive in the case of small nanowire diameters, where the surface depletion depth is comparable to the nanowire radius. To optimize the device performance and find a trade-off between the V_{BR} and R_{ON}, the doping level of the drift region must be defined according to the diameter D of the chosen nanowire, the L_{Drift}, and the density of surface states D_{it} (chosen constant in this study). However, considering the constraints of the fabrication process and the synthesis of the nanowires in our ongoing experimental work, we decided to set the maximum length of the drift region to 2 μm.

The I_{ds}-V_{ds} characteristics of the transistor are plotted in figure 9 (with D = 100 nm, D = 200 nm, and L_{Drift} = 1 μm), for different doping levels in the drift region, with and without surface states. As seen in figure 9(b), when surface states are present, the transistor does not exhibit linear behavior at low V_{ds}, regardless of the nanowire diameter (D ≤ 200 nm), when the drift region doping level is below 1 × 10^{17} cm^{-3}. This can be easily explained by the depletion of the drift region by the surface states. For high drift region doping levels (N_{Drift} ≥ 5 × 10^{17} cm^{-3}), the impact of surface states on the I_{ds}-V_{ds} characteristics is negligible for a transistor with D = 200 nm. However, the surface states highly impact the transistor with D = 100 nm, as the surface depletion region becomes comparable to the nanowire radius.

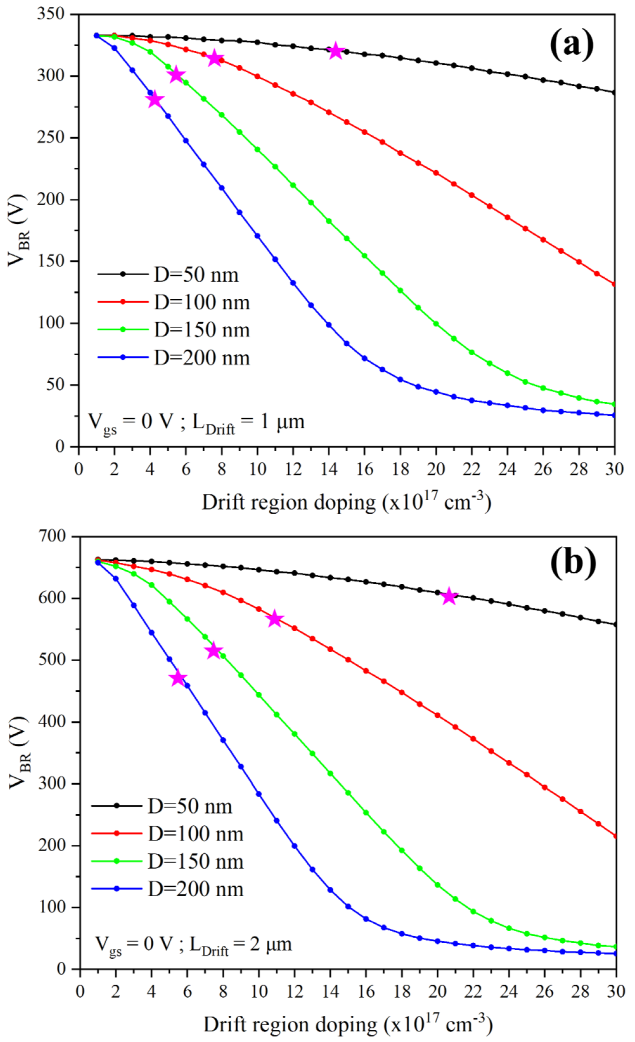

FIGURE 12. Evolution of breakdown voltage V_{BR} as a function of drift region doping for a length L_{Drift} = 1 μm (a) and L_{Drift} = 2 μm (b) with surface states.

Additionally, we can observe (in figure 9) a negative differential resistance beyond the saturation voltage (V_{ds-sat}), which can be attributed to the self-heating effect of the device. Indeed, the electron mobility is degraded when the channel temperature increases, decreasing the I_{ds} current at high V_{ds}. Figure 10(a) and figure 10(b) show the on-state resistance R_{ON}, extracted from the I_{ds}-V_{ds} curves, as a function of the drift region doping level, with and without surface states, for two drift region lengths: L_{Drift} = 1 μm and L_{Drift} = 2 μm respectively. It can be observed that the R_{ON} resistance is higher with a smaller nanowire diameter, lower doping, and a long drift region. This phenomenon is accentuated in the presence of surface states, especially at low doping levels in the drift region.

For all nanowire diameters, regardless of surface states, the R_{ON} resistance decreases by increasing the doping level of the drift region, eventually reaching a constant value at high doping levels. At such high doping levels, the surface states have less effect on the transistor R_{ON}.

For each nanowire diameter, we have identified (by a star symbol) the minimum doping level corresponding to the point where the R_{ON} is less dependent on the doping level and quite similar with and without surface states. These minimum doping level values are plotted as a function of the nanowire diameter in figure 11 for two lengths of the drift region. These simulations allow us to estimate the best compromise to maximize the performance of the Normally-OFF transistor.

Figure 12 shows the evolution of the breakdown voltage as a function of the drift region doping level for different nanowire diameters (Figure 12(a) for L_{Drift} = 1 μm and figure 12(b) for L_{Drift} = 2 μm). It is found that the breakdown voltage decreases as the doping level of the drift region increases, with this behavior being more pronounced for larger nanowire diameters. The "star" symbols in figure 12 correspond to the V_{BR} breakdown voltages associated with the optimal parameter couples (D and L_{Drift}) previously identified in figures 10 and 11. It is important to note that the values of the doping level where R_{ON} is minimum do not correspond to those where V_{BR} is maximum. Thus, a compromise must be made to optimize the device's overall performance.

The results presented in this paper allow researchers to design epi-structure devices with specific nanowire diameters to meet pre-determined specifications, providing valuable insight for the scientific community.

IV. CONCLUSION

GaN nanowire-based Normally-OFF transistor is simulated using TCAD-Santaurus simulator. The device performances are extracted and analyzed as a function of geometrical parameters such as nanowire diameter, drift region length, doping levels in the channel and the drift region, and surface states. The simulation results indicate that a robust Normally-OFF mode with minimum leakage current, even at high drain voltage, is obtained when the nanowire diameter is less than 200 nm. The study also examines the impact of acceptor-type surface states on the device's performance and designs the device to minimize this impact. Indeed, the doping of the drift region is optimized as a function of the nanowire diameter to minimize the on-state resistance and maximize the breakdown voltage. To the best of our knowledge, this study provides new insights into the design of GaN nanowire-based Normally-OFF transistors and will be very helpful for the scientific community.

REFERENCES

[1] M. D. Vecchia, S. Ravyts, G. Van den Broeck, and J. Driesen, "Gallium-nitride semiconductor technology and its practical design challenges in power electronics applications: An overview," *Energies*, vol. 12, no. 14, p. 2663, Jul. 2019, doi: 10.3390/en12142663.

[2] X. Ding, Y. Zhou, and J. Cheng, "A review of gallium nitride power device and its applications in motor drive," *CES Trans. Electr. Mach. Syst.*, vol. 3, no. 1, pp. 54–64, Apr. 2019, doi: 10.30941/cestems.2019.00008.

[3] H. Amano et al., "The 2018 GaN power electronics roadmap," *J. Phys. D, Appl. Phys.*, vol. 51, no. 16, Mar. 2018, Art. no. 163001, doi: 10.1088/1361-6463/aaaf9d.

[4] K. J. Chen, O. Häberlen, A. Lidow, C. L. Tsai, T. Ueda, Y. Uemoto, and Y. Wu, "GaN-on-Si power technology: Devices and applications," *IEEE Trans. Electron Devices*, vol. 64, no. 3, pp. 779–795, Mar. 2017, doi: 10.1109/TED.2017.2657579.
[5] M. S. Shur, "GaN based transistors for high power applications," *Solid State Electron.*, vol. 42, no. 12, pp. 2131–2138, 1998, doi: 10.1016/S0038-1101(98)00208-1.
[6] M. Su, C. Chen, and S. Rajan, "Prospects for the application of GaN power devices in hybrid electric vehicle drive systems," *Semicond. Sci. Technol.*, vol. 28, no. 7, Jul. 2013, Art. no. 074012, doi: 10.1088/0268-1242/28/7/074012.
[7] T. Hashizume, K. Nishiguchi, S. Kaneki, J. Kuzmik, and Z. Yatabe, "State of the art on gate insulation and surface passivation for GaN-based power HEMTs," *Mater. Sci. Semicond. Process.*, vol. 78, pp. 85–95, May 2018, doi: 10.1016/j.mssp.2017.09.028.
[8] J. Millán, "A review of WBG power semiconductor devices," in *Proc. Int. Semiconductor Conf. (CAS)*, vol. 1, 2012, pp. 57–66, doi: 10.1109/SMICND.2012.6400696.
[9] E. A. Jones, F. F. Wang, and D. Costinett, "Review of commercial GaN power devices and GaN-based converter design challenges," *IEEE J. Emerg. Sel. Topics Power Electron.*, vol. 4, no. 3, pp. 707–719, Sep. 2016, doi: 10.1109/JESTPE.2016.2582685.
[10] M. Ma, Y. Cao, H. Lv, Z. Wang, X. Zhang, C. Chen, L. Wu, L. Lv, X. Zheng, W. Tian, X. Ma, and Y. Hao, "Effect of acceptor traps in GaN buffer layer on breakdown performance of AlGaN/GaN HEMTs," *Micromachines*, vol. 14, no. 1, p. 79, Dec. 2022, doi: 10.3390/mi14010079.
[11] J. Mukherjee, R. K. Chaubey, D. S. Rawal, and R. S. Dhaka, "Analysis of the post-stress recovery of reverse leakage current in GaN HEMTs," *Mater. Sci. Semicond. Process.*, vol. 137, Jan. 2022, Art. no. 106222, doi: 10.1016/j.mssp.2021.106222.
[12] M. Haziq, S. Falina, A. A. Manaf, H. Kawarada, and M. Syamsul, "Challenges and opportunities for high-power and high-frequency AlGaN/GaN high-electron-mobility transistor (HEMT) applications: A review," *Micromachines*, vol. 13, no. 12, p. 2133, Dec. 2022, doi: 10.3390/mi13122133.
[13] A. E. H. Khediri, B. Benbakhti, J.-C. Gerbedoen, H. Maher, A. Jaouad, N. E. Bourzgui, and A. Soltani, "Dual role of 3C-SiC interlayer on DC and RF isolation of GaN/Si-based devices," *Appl. Phys. Lett.*, vol. 121, no. 12, Sep. 2022, Art. no. 122103, doi: 10.1063/5.0102644.
[14] D. V. Krishna, A. Panchal, E. Sharma, and S. Dalal, "Trench edge termination in a GaN-based power device," *Mater. Today, Proc.*, vol. 79, pp. 219–222, Jan. 2023, doi: 10.1016/j.matpr.2022.10.076.
[15] Y. Zhang, M. Sun, Z. Liu, D. Piedra, H.-S. Lee, F. Gao, T. Fujishima, and T. Palacios, "Electrothermal simulation and thermal performance study of GaN vertical and lateral power transistors," *IEEE Trans. Electron Devices*, vol. 60, no. 7, pp. 2224–2230, Jul. 2013, doi: 10.1109/TED.2013.2261072.
[16] M. Okada, Y. Saitoh, M. Yokoyama, K. Nakata, S. Yaegassi, K. Katayama, M. Ueno, M. Kiyama, T. Katsuyama, and T. Nakamura, "Novel vertical heterojunction field-effect transistors with re-grown AlGaN/GaN two-dimensional electron gas channels on GaN substrates," *Appl. Phys. Exp.*, vol. 3, no. 5, May 2010, Art. no. 054201, doi: 10.1143/APEX.3.054201.
[17] S. Chowdhury, B. L. Swenson, and U. K. Mishra, "Enhancement and depletion mode AlGaN/GaN CAVET with Mg-ion-implanted GaN as current blocking layer," *IEEE Electron Device Lett.*, vol. 29, no. 6, pp. 543–545, Jun. 2008, doi: 10.1109/LED.2008.922982.
[18] Y. Zhang, M. Sun, J. Perozek, Z. Liu, A. Zubair, D. Piedra, N. Chowdhury, X. Gao, K. Shepard, and T. Palacios, "Large-area 1.2-kV GaN vertical power FinFETs with a record switching figure of merit," *IEEE Electron Device Lett.*, vol. 40, no. 1, pp. 75–78, Jan. 2019, doi: 10.1109/LED.2018.2880306.
[19] S. You, K. Geens, M. Borga, H. Liang, H. Hahn, D. Fahle, M. Heuken, K. Mukherjee, C. De Santi, M. Meneghini, E. Zanoni, M. Berg, P. Ramvall, A. Kumar, M. T. Björk, B. J. Ohlsson, and S. Decoutere, "Vertical GaN devices: Process and reliability," *Microelectron. Rel.*, vol. 126, Nov. 2021, Art. no. 114218, doi: 10.1016/j.microrel.2021.114218.
[20] M. F. Fatahilah, K. Strempel, F. Yu, S. Vodapally, A. Waag, and H. S. Wasisto, "3D GaN nanoarchitecture for field-effect transistors," *Micro Nano Eng.*, vol. 3, pp. 59–81, May 2019, doi: 10.1016/j.mne.2019.04.001.
[21] O. Saket, J. Wang, N. Amador-Mendez, M. Morassi, A. Kunti, F. Bayle, S. Collin, A. Jollivet, A. Babichev, T. Sodhi, J.-C. Harmand, F. H. Julien, N. Gogneau, and M. Tchernycheva, "Investigation of the effect of the doping order in GaN nanowire p–n junctions grown by molecular-beam epitaxy," *Nanotechnology*, vol. 32, no. 8, Feb. 2021, Art. no. 085705, doi: 10.1088/1361-6528/abc91a.
[22] M. Tchernycheva, C. Sartel, G. Cirlin, L. Travers, G. Patriarche, J.-C. Harmand, L. S. Dang, J. Renard, B. Gayral, L. Nevou, and F. Julien, "Growth of GaN free-standing nanowires by plasma-assisted molecular beam epitaxy: Structural and optical characterization," *Nanotechnology*, vol. 18, no. 38, Sep. 2007, Art. no. 385306, doi: 10.1088/0957-4484/18/38/385306.
[23] D.-H. Son, Y.-W. Jo, J. H. Seo, C.-H. Won, K.-S. Im, Y. S. Lee, H. S. Jang, D.-H. Kim, I. M. Kang, and J.-H. Lee, "Low voltage operation of GaN vertical nanowire MOSFET," *Solid-State Electron.*, vol. 145, pp. 1–7, Jul. 2018, doi: 10.1016/j.sse.2018.03.001.
[24] F. Yu, K. Strempel, M. F. Fatahilah, H. Zhou, F. Römer, A. Bakin, B. Witzigmann, H. W. Schumacher, H. S. Wasisto, and A. Waag, "Normally off vertical 3-D GaN nanowire MOSFETs with inverted *p*-GaN channel," *IEEE Trans. Electron Devices*, vol. 65, no. 6, pp. 2439–2445, Jun. 2018, doi: 10.1109/TED.2018.2824985.
[25] S. Keller, S. Yao, F. Römer, B. Witzigmann, T. Schimpke, M. Strassburg, A. Bakin, H. W. Schumacher, E. Peiner, H. S. Wasisto, and A. Waag, "GaN nanowire arrays with nonpolar sidewalls for vertically integrated field-effect transistors," *Nanotechnology*, vol. 28, no. 9, pp. 1–9, 2017, doi: 10.1088/1361-6528/aa57b6.
[26] M. Ťapajna, "Current understanding of bias-temperature instabilities in GaN MIS transistors for power switching applications," *Crystals*, vol. 10, no. 12, pp. 1–28, Dec. 2020, doi: 10.3390/cryst10121153.
[27] M. Ťapajna and J. Kuzmík, "A comprehensive analytical model for threshold voltage calculation in GaN based metal-oxide-semiconductor high-electron-mobility transistors," *Appl. Phys. Lett.*, vol. 100, no. 11, Mar. 2012, Art. no. 113509, doi: 10.1063/1.3694768.
[28] M. D. Janezic, D. F. Williams, V. Blaschke, A. Karamcheti, and C. S. Chang, "Permittivity characterization of low-*k* thin films from transmission-line measurements," *IEEE Trans. Microw. Theory Techn.*, vol. 51, no. 1, pp. 132–136, Jan. 2003, doi: 10.1109/TMTT.2002.806925.
[29] J. Kumar, S. Birla, and G. Agarwal, "A review on effect of various high-*k* dielectric materials on the performance of FinFET device," *Mater. Today, Proc.*, vol. 79, pp. 297–302, Jan. 2023, doi: 10.1016/j.matpr.2022.11.204.
[30] H. Wu, X. Fu, Y. Wang, J. Guo, J. Shen, and S. Hu, "Breakdown voltage improvement of enhancement mode AlGaN/GaN HEMT by a novel step-etched GaN buffer structure," *Results Phys.*, vol. 29, Oct. 2021, Art. no. 104768, doi: 10.1016/j.rinp.2021.104768.

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