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RESEARCH ARTICLE

New Random PWM Method at Constant Switching Frequency and Maximum Harmonic Reduction Created With a Flexible FPGA-Based Test Bench

TOMÁS MORALES-LEAL[1], ANTONIO MORENO-MUNOZ[2], (Senior Member, IEEE), MANUEL AGUSTÍN ORTIZ-LÓPEZ[2], SERGIO R. GENINATTI[3], AND FRANCISCO JAVIER QUILES-LATORRE[2]

[1]Department of Electrical Engineering and Automation, University of Córdoba, 14071 Córdoba, Spain
[2]Department of Electronics and Computer Engineering, University of Córdoba, 14071 Córdoba, Spain
[3]Electronic Department, Universidad Nacional de Rosario, Rosario CP 2000, Argentina

Corresponding author: Tomás Morales Leal (el1molet@uco.es)

ABSTRACT It has been shown that the converters that integrate random PWM produce a spread spectrum in their harmonic emission, shortening the emission peaks. On the converter's input side, the reduction minimizes electromagnetic interference EMI. On the output side of the converter, the reduction manages to smooth the voltage and current ripple in the load. We have built a flexible test bench (FTB) developed with FPGA to generate most of the proposed random PWM modes for converters. The conducted harmonic voltage emission of these modes, both on the input side of the converter and on the load side, has been measured and compared in a DC-DC Buck converter. FTB also has the ability to create new random PWM modes. Of the random modes, the ones that produce the greatest peak reductions are those with variable switching frequency. However, variable frequency modes lead to load feedback problems. A new random PWM method has been developed that significantly reduces the amplitude of the emission peaks but keeps the switching frequency constant.

INDEX TERMS FPGA, flexible test bench (FTB), random PWM at the constant switching frequency, random PWM at a variable switching frequency.

I. INTRODUCTION

Pulse width modulation, PWM, is the most widely used method in power converters to vary and control voltages and currents in loads. It is used in switched-mode power supplies, in their initial input stage, and in the load supply stage, it is used in DC-DC converters, inverters, and class B amplifiers. Its widespread use is logical, given its simple operating principle and its ability to transform and transmit power with low losses. However, since it works at a fixed repetitive frequency, it produces sharp harmonic peaks at the switching frequency and its multiples.

The harmonic emission is transmitted both by the input side of the converter and by the output side of the converter. On the input side, it produces conducted and radiated EMI that can affect relatively nearby devices, fed from the mains where the converter is connected. On the output side, it produces a ripple with peaks in the voltage and current that feed the load, which affect it negatively. On the load side, in addition to ripple, peaks cause an increase in acoustic noise in converters for electric drives.

The study of harmonic emission is extensive on both sides of the converter, however, there are considerably more articles that study the impact of emission on the load side than on the source side. This may be because the emission can be attenuated on the source side by including a filter. The presence of the filter becomes necessary since without it the

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electromagnetic emission would be too high to comply with the electromagnetic compatibility standards (EMC). However, the filter reduces the efficiency of the converter [1].

An alternative to the filter, which also solves the load ripple problem, is reducing the peaks in the switching operation by widening the harmonic emission band, called the spread spectrum (SS). By broadening the spectrum, the emitted harmonic energy does not vary, but the amplitudes of the peaks are greatly reduced, which produces most of the undesired effects. Pulse width modulation with the inclusion of some mechanism capable of creating a spread spectrum will be called SS-Based PWM, proposed in [2].

The concern for harmonic emission parallels the development of switching techniques. In 1962, a switching scheme for harmonic neutralization was already proposed in [3]. Suppression techniques were shaped by the technology of the time in which they were developed. The first used harmonic suppression technique was developed in the 1960s and 1970s. It is called programmed PWM. The idea is the selective elimination of harmonics [4], The technique is still used today and is described in recent editions of power electronics textbooks.

In the second half of the 1980s, the switching frequency randomization technique was introduced to produce a spread spectrum, which is generally called Random Pulse With Modulation (RPWM); however, in this paper, it is called Random PWM, so as not to confuse it with the acronym for a specific random PWM mode. In 1989, [5] used this technique for switching noise-smoothing. The technique of randomizing the frequency was previously used in [6].

In 1992 the authors in [7] proposed a new method of creating a spread spectrum for EMI reduction. They called it Switching Frequency Modulation. Now generally called Spread Spectrum Clock Generation (SSCG), it is also called Frequency Dithering. With the SSCG, in which a periodic variation of the switching frequency from a central frequency is made, a reduction of harmonic peaks at the cost of broadening the spectrum is achieved.

The most recent technique for creating a spread spectrum is called chaotic. In 1999, Deane [8] uses chaos to reduce EMI in a current-controlled boost converter. More recent techniques using chaos focus on producing a spread spectrum by chaotically varying the switching frequency, chaotic PWM [9].

A broad classification of methods that produce a spread spectrum is collected in [2].

This paper describes the implementation of what we call Flexible Test Bed (FTB). Field Programmable Gate Array (FPGA) technology is employed to design the flexible test bench. Its purpose is to generate SS-Based PWM in a variety of methods. In addition, it allows the creation of new modes without having to program them previously. The structure of the FTB, detailing its functional blocks and internal signals is described. The FTB is implemented on an FPGA board whose output drives the MOSFET of a Buck converter. Random PWM modes developed for DC-DC converters have been generated; we visualize the harmonic voltage emission at the dc input of the converter and the harmonic voltage noise at the output of the converter, whose load, in this work, is COB-led lighting. A new randomization mode is proposed while keeping the switching frequency constant. This is intended to significantly reduce harmonic peaks on both the source and load sides.

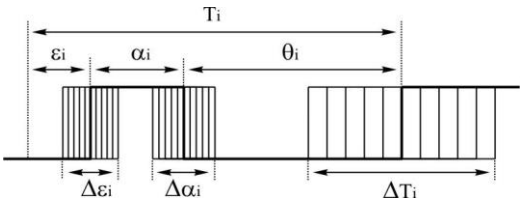

FIGURE 1. PWM signal parameters with values that can vary.

TABLE 1. Random PWM Modes.

Mode	Submode	T_i	α_i	ε_i	d_i
Fixed	PWM	C	C	C	C
Random	RPPM	C	C	R	C
Random	RPWM	C	R	C	R
Random	RCFMFD	R	R	C	C
Random	RCFMVD	R	R	C	R
Random	RDRPPMFCF	C	R	R	R
Random	RCFRPPMFD	R	R	R	C
Random	RRRM	R	R	R	R

R: Random, C: Constant
RPPM Random Pulse Position Modulation
RPWM Random Pulse Width Modulation
RCFMFD Random Carrier Frequency Modulation Fixed Duty
RCFMVD Random Carrier Frequency Modulation Variable Duty
RDRPPMFCF Random duty ratio RPPM Fixed carrier frequency
RCFRPPMFD Random carrier frequency RPPM Fixed duty ratio
RRRM Random carrier frequency RPPM Random duty ratio

II. DIFFERENT WAYS TO ACHIEVE SPREAD SPECTRUM

Figure 1 shows the parameters whose variations define the different SS-Based PWM methods.

T_i: PWM full cycle time
α_i: Power connection time.
ε_i: Waiting time before α_i
θ_i: Remaining cycle time after α_i.
Being $f_i = 1/T_i$

The prefix Δ in each parameter represents the time increment or decrement that produces the variation.

To the above parameters must be added the duty cycle d_i, which is defined as $d_i = \alpha_i / T_i$.

Of the 4 ways to create SS-Based PWM, in this paper we focus on Random PWM modes, although the FTB has the capability to generate SSCG and Chaotic.

The classification of the different randomness creation modes to produce SS-Based PWM and implemented in the proposed FTB is shown in Table 1.

Since it was discovered that a random PWM generates a spread spectrum, new approaches have been developed. In 1999 K.K. Tse [10] presented a table with the classification of the techniques developed up to that date. The number

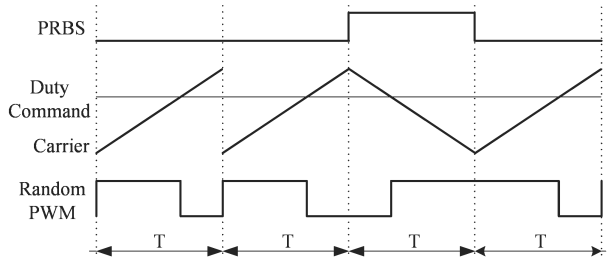

FIGURE 2. The timing diagram of RPPM S mode.

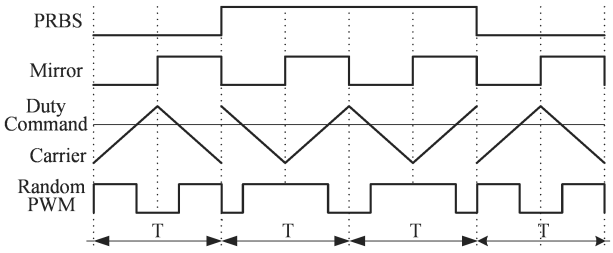

FIGURE 3. The timing diagram of RPPM T mode.

of methods was increasing until the classification embodied in [11] in 2011.

From each of the 7 PWM randomization modes shown in Table 1, multiple variations have been developed depending on the converter class. For example, the random distribution of the zero voltage vector (RZD) mode is a variant of the RPWM mode [12]. A comparison of the harmonic emission of various randomization modes in DC-AC inverters for adjustable speed drives (ASD) is made in [13]. In the FTB, in addition to the 7 modes in Table 1, two variations of the RPPM mode have been programmed by generating a random bit. The bit sequence is not purely random, being called Pseudo Random Binary Sequence, PRBS. The reason for labeling it as pseudo is because with microprogrammed technologies, such as the one used in this paper - i.e., with FPGA - a completely random sequence is not achieved, but an operation that simulates full randomization can be generated. The logic level of the pseudorandom bit determines whether the slope of the sawtooth carrier is positive or negative. This ensures that the position of the pulse in the period is aligned at the beginning, or at the end of the period. This way of creating randomness is called random lead lag, RLL. [12], [14], [15]. RLL is of the RPPM type, randomly changing the position of the pulse in two arrangements. We have called this mode of creating randomness, RPPM S. Figure 2 shows the timing diagram of the RPPM S mode.

A second way to use the random bit in the FTB is with a triangle carrier. Starting from a sawtooth carrier to obtain the triangular carrier. A so-called mirror bit produces a triangular carrier from the sawtooth carrier. A level change in the mirror bit reverses the slope of the sawtooth. Thus, the mirror bit produces a triangular carrier, and the random bit produces the random change of the triangle vertex. Like the previous mode, this mode is RPPM. We have called it RPPM T. Figure 3 shows the timing diagram of all the signals involved.

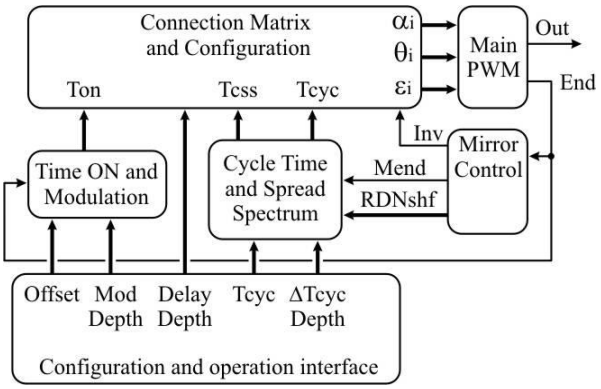

FIGURE 4. Block diagram of the FTB.

III. FLEXIBLE TEST BENCH

An FPGA prototyping board, described with VHDL, has been used as a tool for the flexible test bench. A Xilinx Spartan 3 board was used. Apparently, it might seem like an outdated card, but for our purposes, the power of the used card is more than enough.

The strength of the FTB design lies in the definition of basic building blocks that define the functions common to all Random PWM strategies. The diagram in Figure 4 shows the organization of the blocks, which move from one behavior to another instantaneously by changing connections and configurations.

The entire system is synchronized with a fixed frequency clock of 50 MHz (Fclk), which can be changed to suit the resolution and frequency of a specific application.

The *Main PWM* block uses Fclk to compute the times ε_i, α_i y θ defined by the rest of the blocks, thus obtaining the PWM output signal, as shown in Figure 4. *Main PWM* also supplies the *End* signal that indicates to the rest of the blocks when a PWM cycle ends.

A detail to highlight in the different blocks is the importance of the numerical representation in the FPGA calculation. We use a fixed point, adapting the width of each bus to the numerical range of the operations to ensure there is no overflow, and control truncation. With these design details, we think that the proposed architecture is suitable for low-cost implementations, such as LED lighting or switched sources. Each of the FTB blocks is described below.

A. CONFIGURATION AND OPERATION INTERFACE (COI)

In the Configuration and Operation Interface block (COI) all the options programmed in the FTB are configured. This facilitates the creation and comparison of different strategies for creating a spread spectrum.

The COI allows the operator to define, manually, with the pushbuttons and switches of the FPGA board, the following parameters:

Tcyc: Duration time of a cycle, which defines the center carrier frequency over which variations are applied to create spread spectrum. Can be set from 2 kHz to 100 kHz.

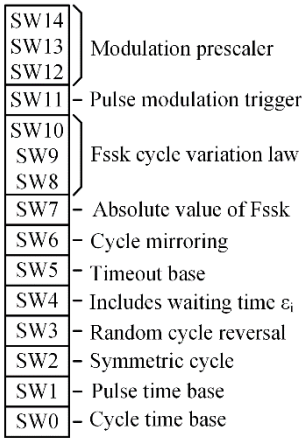

FIGURE 5. Configuration register.

ΔTcyc Depth: Time variation over Tcyc, which represents in % the random variation over the central frequency. It can vary from 0% (constant switching frequency) to 90%.

Offset: It is the pulse duration time, α, which defines the desired duty cycle. It is expressed as a percentage and can be set from 0% (0 V voltage at load) to 100% (maximum voltage at load).

Mod Depth: Time variation over pulse duration, $\Delta\alpha$, which defines in percent the random variation of the pulse duration.

Delay Depth: Defines the pulse delay at PWM cycle start, ε. It is expressed as a percentage, as a proportion of its selected time base.

The versatility of the FTB is based on the configuration register, shown in Figure 5. The configuration register allows you to select and connect the FTB options to implement each SS-Based PWM mode. Sixteen copies of this configuration register have been installed, allowing quick switching from one mode to another for easy comparison.

B. CYCLE AND SPREAD SPECTRUM BLOCK (CTSSB)

This block defines the PWM cycle time using Fclk as the time base, the internal diagram of the block is shown in Fig. 6.

CTSSB is characterized by 2 parameters (Tcyc y ΔTcyc) that affect the duration of each SS-Based PWM cycle.

CTSSB generates the PWM cycle variation functions (Fssk) using Direct Digital Synthesis (DDS). By means of 3 bits of the configuration register (SW8, SW9, and SW10) it is possible to select one of the eight waveforms stored in ROM.

The values of the selected $Fssk_{(i)}$ variation function are read consecutively thanks to an address counter (*ADDR CMT 2*) which is incremented by the *Mend* signal at the end of each PWM cycle or alternated, depending on the Mirror Control Block configuration.

Each value of the selected *Fssk* function is multiplied by the depth factor ΔTcyc (MUL1) and then by the average cycle time Tcyc (MUL2). In this way the percentage variation ΔTcyc is expressed in clock cycles. The result is added to Tcyc to obtain the Tcss value.

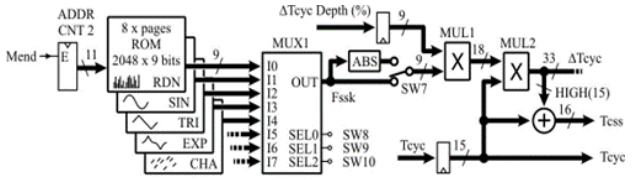

FIGURE 6. Cycle time and spread spectrum block.

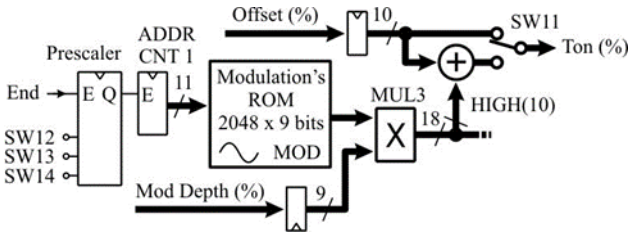

FIGURE 7. Time on and modulation block.

Equation 1 shows the modified cycle time expression for SS-Based PWM:

$$Tcss_{(i)} = Tcyc \times (1 + Fssk_{(i)} \times \Delta Tcyc \times 2^{-18}) \quad (1)$$

CTSSB provides two numerical values to the next stage *Tcyc* and *Tcss*, expressed in cycles of Fclk.

Bit SW7 of the configuration register applies absolute value to the variation *Fssk* function.

Furthermore, assuming that the modulation signal introduces its own spectrum spread, a memory for storing the modulation waveform is incorporated in CTSSB, as solved by [16] and [17], which store sine signals in lookup tables. DDS is used to extend the lookup tables by adding other modulation shapes.

C. TIME ON AND MODULATION BLOCK (TOMB)

This block defines the duration of the active PWM pulse as a percentage of the total PWM cycle, the internal diagram of the block is shown in Figure 7.

In the configuration register, SW11 defines the *Ton* output of the block, which can come from a constant *Offset* value or a variable modulation value.

The modulation function is obtained by SSD from a table stored in a block RAM. As with the CTSSB block, data is extracted cycle by cycle using an address counter (*ADDR CMT 1*) that is updated with the *End* signal.

Under the assumption that the PWM modulation can evolve slower than the spread spectrum variation, a Prescaler has been added in order to adjust the change of the modulation signal.

TOMB also incorporates a parameter to adjust the modulation depth (*Depth Mod*) using the MUL3 multiplier.

D. MIRROR CONTROL BLOCK (MCB)

As already discussed, the inversion of the PWM pulse from the beginning to the end of the cycle is a resource used by some random PWM strategies (Figure 2); thus, MCB generates the *Inv* signal that controls the inversion.

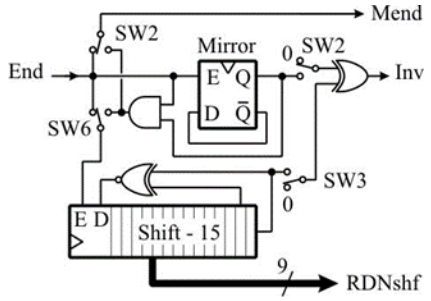

FIGURE 8. Mirror control block.

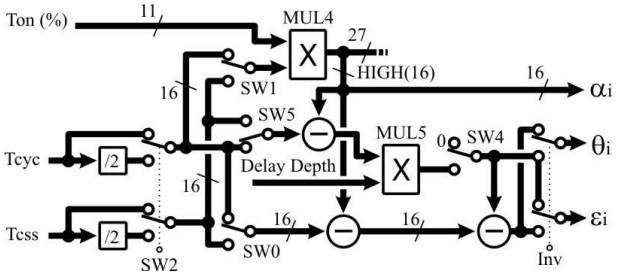

FIGURE 9. Connection matrix and configuration.

Figure 8 shows the internal diagram of MCB, which is a circuit synchronized by Fclk and evolving under the control of the *End* signal. A pseudo-random sequence with a shift register has been implemented for the ramp RPPM modes, as in Figure 2. The symmetry control, which we call *Mirror*, allows us to implement the triangular reference RPPM modes like the one shown in Figure 3.

E. CONNECTION MATRIX AND CONFIGURATION BLOCK (CM&CB)

It has been seen that the CTSSB block defines the time base of SS-Based PWM, and the TOMB block defines the pulse width proportionally. CM&CB allows all possible combinations of the parameters defined by CTSSB and TOMB, resulting in different SS-Based PWM modes. Fig. 9 shows the internal organization of CM&CB.

The *Tcyc* and *Tcss* inputs are the PWM time references, both divided by two to give the option of symmetrical modes like the one in Figure 3.

SW0, *SW1,* and *SW5* are used to individually define the time base for α_i, θ_i y ε_i respectively, selecting between the two options *Tcyc* and *Tcss*.

The MUL4 multiplier uses the time base selected by SW1 to calculate the cycles of Fclk corresponding to α_i. Similarly, ε_i is calculated using the time base selected by SW5, from which α_i is subtracted, the result is the total PWM OFF time (Toff). The MUL5 multiplier affects Toff by a proportionality coefficient, which we call Delay Depth, to obtain ε_i.

Finally, from the time base selected by SW0, α_i and ε_i are subtracted to obtain θ_i, which is the remaining PWM cycle time.

The *Inv* signal can drive a two-way output selector to decide whether ε_i and θ_i go to the beginning or end of the PWM cycle.

TABLE 2. Configuration Register for Random PWM.

Configuration Register															PWM
14	13	12	11	10	9	8	7	6	5	4	3	2	1	0	
-	-	-	0	-	-	-	0	0	0	0	0	0	0	0	Constant PWM
-	-	-	0	0	0	0	0	0	1	1	0	0	0	0	RPPM
-	-	-	0	0	0	0	0	0	0	0	0	0	1	0	RPWM
-	-	-	0	0	0	0	0	0	0	0	0	0	1	1	RCFMFD
-	-	-	0	0	0	0	0	0	0	0	0	0	0	1	RCFMVD
-	-	-	0	0	0	0	0	0	1	1	0	0	1	0	RDRPPMFCF
-	-	-	0	0	0	0	0	0	1	1	0	0	0	1	RCFRPPMFD
-	-	-	0	0	0	0	0	0	1	1	0	0	1	1	RRRM

TABLE 3. Alternative Configuration Register for Random PWM.

Configuration Register															Random PWM
14	13	12	11	10	9	8	7	6	5	4	3	2	1	0	
-	-	-	0	0	0	0	0	0	0	0	1	0	0	0	RPPM S
-	-	-	0	0	0	0	0	1	0	0	1	1	0	0	RPPM T

F. FTB CONFIGURATION

The behavior of the FTB is defined by the Configuration Register which is located in the COI. Figure 5 shows the contents of the Configuration Register

Table 2 shows the Configuration Register fields that implement the 7 randomization modes (in addition to constant PWM) described in Table 1. The bits indicated with "-" do not affect the SS-Based PWM mode.

Table 3 shows two configurations with different symmetries. In these cases, T_i and ε_i remain constant, α_i only depends on the modulation and a random inversion is incorporated by means of the random bit. Thus, the RPPM S random mode is implemented, whose timing scheme is shown in Figure 2, and the RPPM T mode, whose timing scheme is shown in Figure 3.

The configuration register allows combining several randomization modes. Each bit of the register defines a parameter. Pushbuttons and switches on the FPGA board are used to fill in the different parameters, thus achieving new randomization modes. Although the possibilities of combinations are high, in this paper we propose a new mode, such that it offers the greatest peak reduction with constant switching frequency.

IV. BUCK DC–DC CONVERTER HARMONIC EMISSION MEASUREMENTS AND IMPLEMENTATION

FTB is used to create random PWM in a DC-DC Buck converter that powers a LED lighting load, type COB. We visualize the harmonic emission of voltage at the input of the converter, and we visualize the harmonic emission of voltage in the load itself. The input to the converter is 10 V dc, and the output to the load varies from 0 to 10 V dc. The points at which the measurements were taken, and the converter schematic, are shown in Figure 10.

The results obtained with this converter can be extrapolated to other types of converters that use PWM as the basis of the conversion. In [18] random space-vector pulse-width modulation is generated in a motor inverter. In [19] uses RPPM

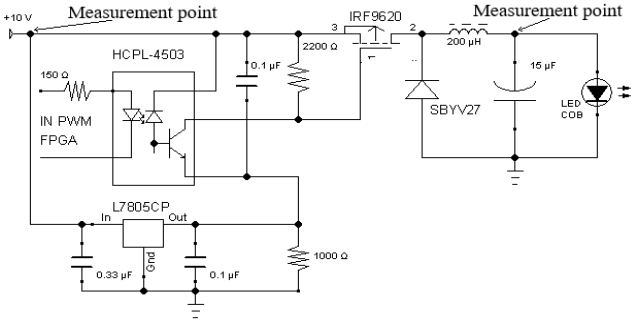

FIGURE 10. Buck converter diagram and measurement points.

in an induction motor inverter. In [20] uses a DC-DC Boost converter to generate random PWM to feed lighting led.

Both input and load side harmonic voltage emission spectra of all the random PWM modes listed in Tables 2 and 3 were measured on the buck converter. Spectrum measurements were obtained in decibels, and in amplitude. Although in most of the papers, the measurements are shown in decibels, those obtained in amplitude give a good insight into the emission comparison between the different random modes.

A center switching frequency of 50 kHz and a duty cycle of 50% was used for the measurements. A duty cycle of 50% was chosen in the tests and measurements presented because we observed that it is at this duty cycle that the highest emission peaks occur, both on the source side and on the load side. The bandwidth of emission frequencies represented ranges from 0 to 400 kHz. It is a range up to 8 times the center switching frequency. Frequencies above 400 kHz are not represented because harmonic emissions are small.

Figures 11 to 20 show the source-side emissions of the random PWM modes presented in Tables 2 and 3.

The measurements of the graphs shown in figures 11 to 20 correspond, as already mentioned, to the input of the converter, fed with a stabilized power supply at 10 V dc. In the unrandomized constant PWM signal, the peak with the highest amplitude corresponds to the center switching frequency, with a value of –38.3 dB (12.2 mV). Some random modes reduced the peaks to almost eliminate them. The mode with the largest reduction is RRRM mode, whose maximum value is –51.1 dB (2.8 mV), i.e., there was a reduction of 12.8 dB, 9.4 mV, over constant PWM. Random bit modes offer good reduction but retain harmonic peaks.

On the load side, measurements were taken at the node shown in Figure 10. The duty cycle was 50%, and the voltage magnitude was 7.2 V.

The harmonic voltage ripple on the load side was approximately the same as the harmonic emission on the source side, but with higher magnitude peaks. For this reason, not all modes are represented, only the most significant ones. Figures 21, 22, 23, and 24 show respectively the constant PWM, RPWM, RRRM, and RPPM T modes.

The load voltage spectrum with constant PWM has a maximum peak at 50 kHz with a value of –31.7 dB (25.93 mV). For RPWM mode the maximum peak is –33.7 dB (20.46 mV).

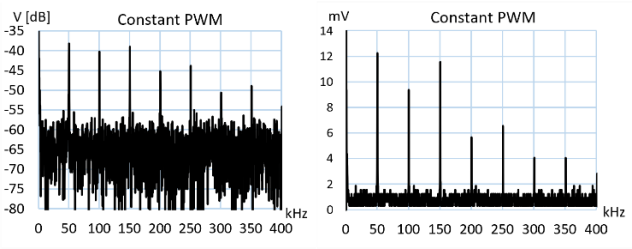

FIGURE 11. Input voltage spectrum with constant PWM.

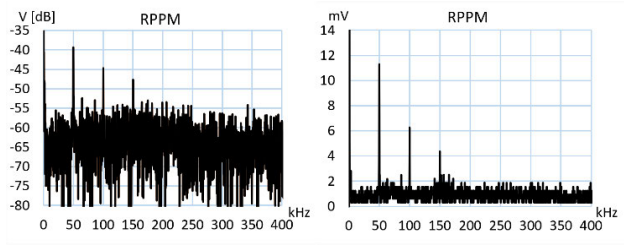

FIGURE 12. Input voltage spectrum with RPPM.

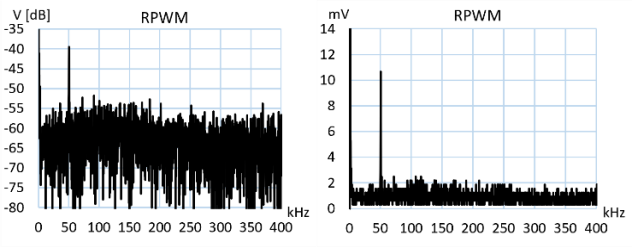

FIGURE 13. Input voltage spectrum with RPWM.

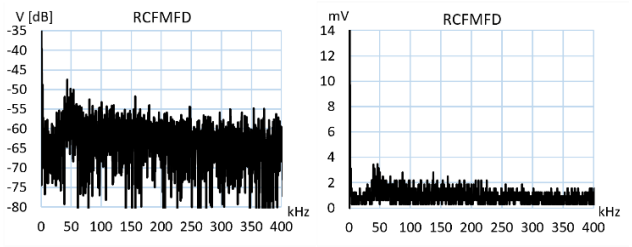

FIGURE 14. Input voltage spectrum with RCFMFD.

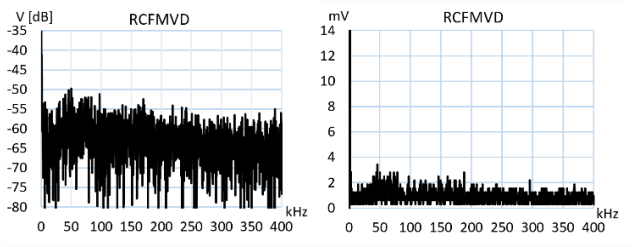

FIGURE 15. Input voltage spectrum with RCFMVD.

In RRRM mode the highest amplitude is –42.8 dB (7.18 mV). And for the RPPM T mode, there are peaks around 50 kHz and a peak at 100 kHz that almost equals the maximum peak,

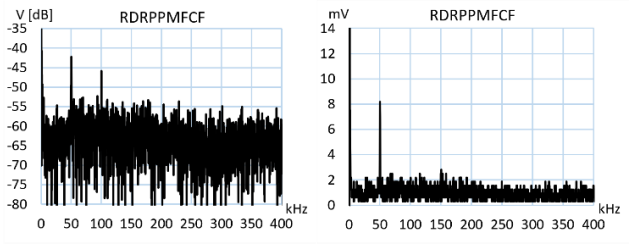

FIGURE 16. Input voltage spectrum with RDRPPMFCF.

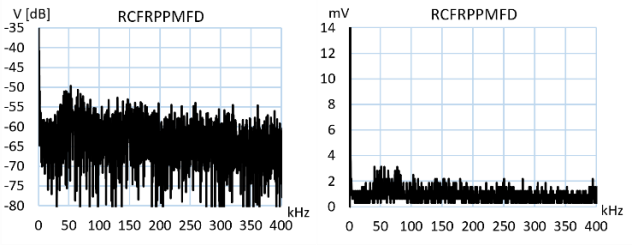

FIGURE 17. Input voltage spectrum with RCFRPPMFD.

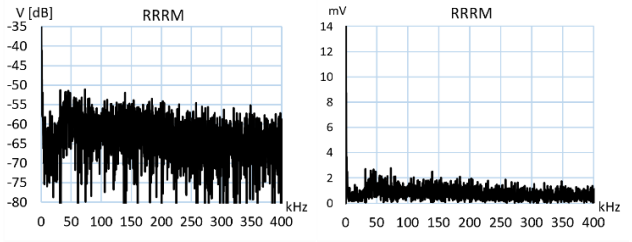

FIGURE 18. Input voltage spectrum with RRRM.

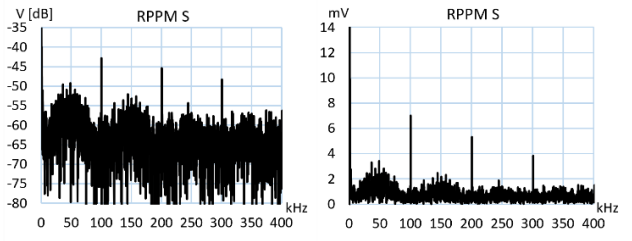

FIGURE 19. Input voltage spectrum with RPPM S.

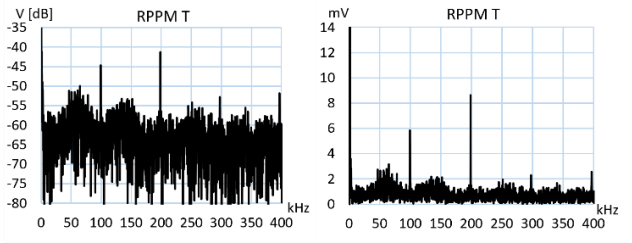

FIGURE 20. Input voltage spectrum with rppm T.

the highest value is –44.0 dB (6.33 mV). As can be seen, the largest reduction occurs for the RPPM-T method, with a decrease of 12.3 dB, 19.6 mV, with respect to the constant PWM mode.

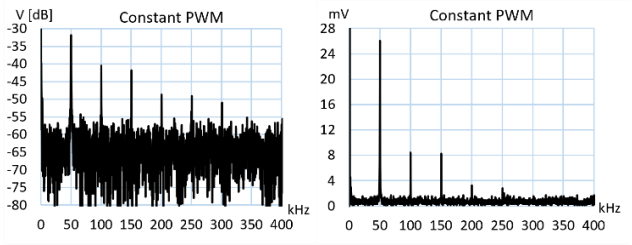

FIGURE 21. Voltage spectrum on load with constant PWM.

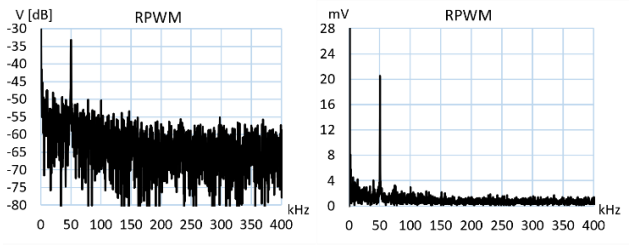

FIGURE 22. Voltage spectrum on load with RPWM.

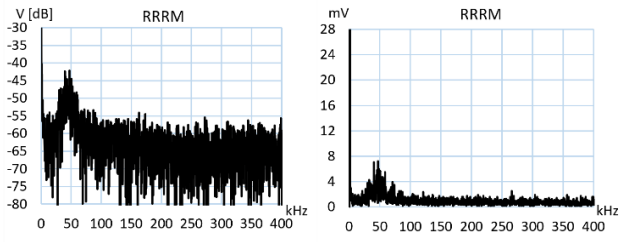

FIGURE 23. Voltage spectrum on load with RRRM.

V. NEW PROPOSED RANDOM PWM MODE AT CONSTANT SWITCHING FREQUENCY

The harmonic emission graphs of figures 11 to 20 on the source side, and of figures 21 to 24 on the load side, show that the modes with random variation of the switching frequency are the ones that offer a greater harmonic reduction. However, a non-constant frequency may produce additional harmful effects on the load side. In converters with a load feedback loop, a variable switching frequency causes stability problems in the closed loop. In digital control systems with sampling frequency taken from the system switching frequency, the current controller updates the reference voltage once per switching cycle. A non-constant cycle produces an unpredictable effect. The problem was raised in 1998 [21] and is studied in [15], [22], [23], and [24].

Random bit PWM methods have been proposed that reduce the ripple in the load [25], spreading the emission spectrum; however, they do not cancel out the emission peaks.

In this research, we have created a new method that reduces the harmonic emission to the same level as the modes with the random switching frequency, but with a constant switching frequency. In this way, maximum harmonic emission

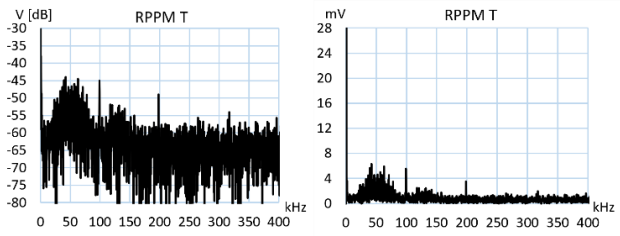

FIGURE 24. Voltage spectrum on load with RPPM T.

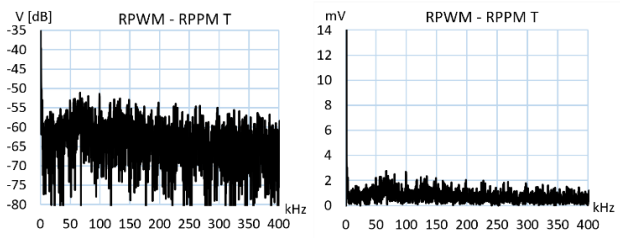

FIGURE 25. Input voltage spectrum with RPWM - RPPM T.

reduction is achieved without having to vary the switching frequency.

In order to achieve maximum reduction at a fixed frequency, the fixed frequency modes have been taken as a basis, which are: RPPM, RPWM, and RDRPPMFCF. As seen in Figures 12, 13, and 16, these modes produce much higher peaks than the random frequency modes. Of these three modes, the RPPM and RPWM modes can be merged, but the result is the RDRPPMFCF mode. The random bit modes RPPM S and RPPM T, at a fixed frequency, also produce large peaks, as can be seen in Figs. 19 and 20. The first three modes have been combined with the second two. With the FTB it can be easily achieved by filling in the corresponding bits of the configuration register, shown in Tables 2 and 3. This results in 6 possibilities, all of which have been programmed and studied. The combinations RPPM - RPPM S and RPPM - RPPM T still create large peaks. The combinations RDRPPMFCF - RPPM S and RDRPPMFCF - RPPM T also produce large peaks. The two combinations RPWM - RPPM S and RPWM - RPPM T offer comparable results to the random frequency mode with higher peak reduction, i.e. RRRM. Of these last two modes, there is slightly more peaks reduction in the RPWM - RPPM T mode. So, of the new modes, the one with the highest reduction is chosen, and we have named it after the combination that has produced it: RPWM - RPPM T.

Figure 25 shows the harmonic emission at the source side, and Figure 26 shows the harmonic noise at the load of the proposed new mode.

Figures 24 and 26 show that at load the emission reductions in RPPM T and RPWM - RPPM T mode are comparable, and there is even a slightly higher reduction in RPPM T mode. The maximum peak emission in RPWM - RPPM T mode is –40.8 dB (9.10 mV). Compared to the maximum peak emission of the constant PWM, a reduction of 9.1 dB,

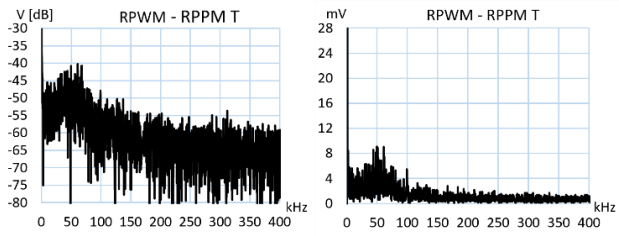

FIGURE 26. Voltage spectrum on load with RPWM - RPPM T.

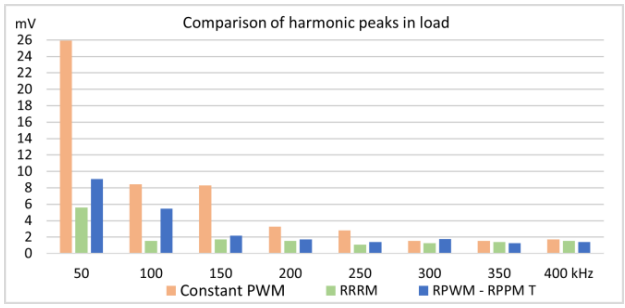

FIGURE 27. Comparison of harmonic frequency peaks on load, from 0 to 400 kHz, between constant PWM, RRRM, AND RPWM - RPPMT modes.

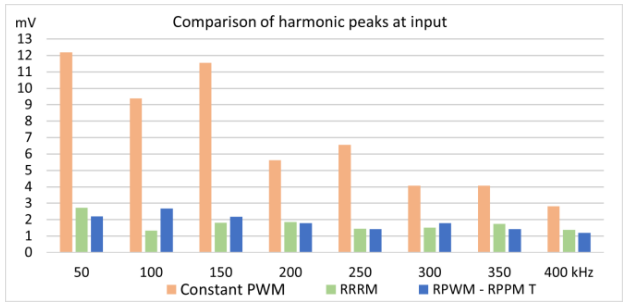

FIGURE 28. Comparison of input harmonic frequency peaks, from 0 to 400 kHz, between constant PWM, RRRM and RPWM - RPPMT modes.

16.83 mV, is achieved. Figure 27 shows a comparison of the harmonic peaks in the load, in millivolts, at the harmonic frequencies shown, between the constant PWM, RRRM, and RPWM - RPPM T modes.

On the source side, the harmonic emission achieved in the RPWM - RPPM T mode has a maximum value of –51.2 dB (2.76 mV). The reduction achieved with respect to constant PWM is 12.9 dB, 9.44 mV, a value that increases even the best of modes with random frequency. Figure 28 shows a comparison of the harmonic peaks at the input of the converter, in millivolts, at the harmonic frequencies shown, between the constant PWM, RRRM (the one with the highest reduction, although at a variable frequency), and RPWM - RPPM T modes.

It can be stated that we have succeeded in generating a new PWM randomization mode with a remarkable harmonic emission reduction on the source side, EMI reduction, and a remarkable noise reduction in the load, without having to vary the switching frequency, thus avoiding that a random PWM affects the stability of the load control loop.

VI. CONCLUSION

It is feasible to design an FPGA-based system, without a microprocessor, capable of generating a multitude of PWM generation modes with spread spectrum creation.

It is possible to significantly reduce EMI peaks on the source side and noise peaks on the load side with a constant switching frequency by joining two constant frequency randomization methods, whose harmonic responses are individually mediocre, but when added together offer a large reduction in harmonic emission peaks.

The peaks on the load side reach a higher magnitude than the peaks on the source side. However, the order of magnitude of peak reduction achieved with the proposed new method is similar on both sides.

The RPPM S and RPPM T random bit modes, which are constant frequency, almost completely reduce peaks on the load side but produce large peaks on the source side. Thus, on the load side, random bit modes may be acceptable enough, without having to resort to composite modes, i.e., random bit combined with RPPM, RPWM, or RDRPPMFCF, to achieve constant frequency and spread spectrum. However, simple random bit modes on the source side would not be acceptable, due to the broad peaks they cause.

With the implementation of the new method, it has been possible to verify the flexibility of the FTB and its usefulness as a rapid prototyping board. Thus, the FTB makes it possible to design new randomization methods easily, and to verify them quickly.

On the other hand, if an RPWM method needs to be implemented in a low-cost application, such as LED lighting, an FPGA can be used, since it would not need to have a large number of logic resources. In this sense, one could use, for example, an FPGA of the Ice40 family from Lattice semiconductor, which have a low cost and very low power consumption.

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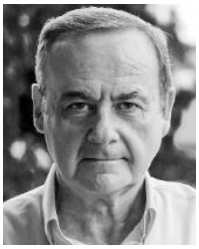
TOMÁS MORALES-LEAL received the degree in electrical engineering and the degree in engineering in automation and industrial electronics from the University of Córdoba, Spain, in 1990 and 2006, respectively. From 1992 to 1997, he was a Researcher with the EATCO Research Group, University of Córdoba, designing computer peripherals for disabled people, including some patents for this type of device, where he has been a Professor in electrical engineering, since 1997. He has carried out research work related to university teaching, which has been published in books for conferences. He is currently working on the study of PWM with spread spectrum creation implemented with FPGA.

ANTONIO MORENO-MUNOZ (Senior Member, IEEE) received the B.Eng. degree in industrial electronics from the University of Córdoba, Córdoba, Spain, in 1988, and the M.Sc. and Ph.D. degrees in physics (with a speciality in automatic control) from the Universidad Nacional de Educación a Distancia, Madrid, Spain, in 1992 and 1998, respectively. From 1981 to 1992, he was with RENFE Maintenance Service, Spanish National Railways Company, where he received a scholarship for his university studies. Since 1992, he has been with the University of Córdoba, where he has been the Director of its Department and the Academic Director of the Master in Distributed Renewable Energies. He is currently a Professor with the Department of Electronics and Computer Engineering, Universidad de Córdoba, where he is also the Chair of the Industrial Electronics and Instrumentation Research and Development Group. His research interests include smart cities, smart grids, power quality, and the Internet of Energy. He has participated in 22 research and development projects and/or contracts and has more than 200 publications on these topics. He is also a member of European Technology & Innovation Platforms (ETIP) Smart Networks for Energy Transition (SNET) WG-4, a WG Member of the Spanish Railways Technological Platform (PTFE), a WG Member of the IEEE P3001.9 Recommended Practice for the Lighting of Industrial and Commercial Facilities, and a member of the Technical Committee on *Smart Grids* of the IEEE Industrial Electronics Society. He has also been a member of the CIGRÉ/CIRED JWG-C4.24 Committee "Power Quality and EMC Issues associated with future electricity networks," the IEC/CENELEC TC-77/SC-77A/WG-9 Committee, and the ISO International Organization for Standardization AEN/CTN-208/SC-77-210. He is an Evaluator of R&D&I Projects for the Estonian Research Council, the Fund for Scientific and Technological Research (FONCYT) of the National Agency for the Promotion of Science and Technology in Argentina, and the Directorate General of Research, Development, and Innovation of the Ministry of Science, Innovation, and the University of Spain, and academic promotion with Qatar University. He is also an Evaluator of European Quality Assurance (EQA) and DNV-GL. He is also a Section Board Member of *Electronics* journal (MDPI). He is also an Associate Editor of *e-Prime Journal* (Elsevier), the Section Editor-in-Chief of *Smart Cities* journal (MDPI), an Associate Editor of *Electronics* journal (MDPI), and an Editor of *Intelligent Industrial Systems Journal* (Springer Nature Science), *Frontiers in Energy Research Sustainable Energy Systems*, and *Journal of Policies*, and also a guest editor and a reviewer of numerous journals of IEEE, IET, MDPI, and Elsevier.

MANUEL AGUSTÍN ORTIZ-LÓPEZ received the M.Sc. degree in physics electronics from the University of Granada, Spain, in 1987, and the Ph.D. degree from the University of Córdoba, Spain, in 2013. From 1987 to 1988, he worked with the Research and Development Department, TECOSA (a Siemens Group Company). From 1988 to 1993, he worked with the Research and Development Department, Fujitsu. From 1993 to 1996, he worked with the Department of Computer Communications and Networks, Telefonica. He has been an Associate Professor with the Department of Electronic and Computer Engineering, University of Córdoba, since 1996, where he has also been the Head of the Department of Electronic and Computer Engineering, since June 2017. He has authored or coauthored several monographs, technical papers, and articles covering topics on embedded systems and wired and wireless networks applied to communications for energy management systems and applications. His research work is related to the development of low-power embedded systems for use in sensor networks and the implementation of redundant arithmetic in FPGAs and HW/SWcodesign. He has been the General Chair of 26th International Annual Seminar on Automation, Industrial Electronics and Instrumentation (Seminario Anual de Automática, Electrónica Industrial e Instrumentación—SAAEI 2019).

SERGIO R. GENINATTI received the degree in electronic engineering from the Universidad Nacional de Rosario (UNR), in 1988, the M.Sc. degree in local economic development from the University Autónoma de Madrid (UAM), in 2003, and the M.Sc. degree in analysis, simulation, and control systems from the Universidad de Córdoba (UCO), Spain, in 2007. He was the Director of the Electronics Engineering School, UNR, from 1996 to 2009, where he is currently an Associate Professor in advanced digital design. He was a visiting Professor in industrial computing with UCO, from 2009 to 2012. In 2016, he was an academic Vice Rector with the Universidad Nacional de Rafaela (UNRA). In 1987, he founded Teknotrol Engineering, a company specialized in tailored solutions related to CNC units for machine tools, non-destructive eddy current sensors for automotive testing, railway information, and embedded systems for a wide range of industries, such as metallurgy, food, or consumer electronics. In 2007, he was a recipient of the Celoxica Designer Forum Best Paper Award with the III Southern Conference on Programmable Logic.



FRANCISCO JAVIER QUILES-LATORRE received the degree in industrial electronic engineering from the University of Jaen, Spain, in 1984. He worked for a period of more than seven years as a Senior Design Engineer with the Research and Development Laboratory, Fujitsu, Spain. He has been an Associate Professor in architecture and computer technology with the University of Córdoba, Spain, since 1994. He has taken part in several research projects, including the design and development of the S1400 and S1500 series of minicomputers and several modems. He has authored or coauthored several monographs, technical papers, and articles covering topics on low power embedded systems and networks applied to communications for energy management applications in the framework of the IoT, smart grids, HEMs, and BEMs. His research interests include the development of embedded systems with low power consumption, both hardware and software to implement wired and wireless sensor networks, the implementation of redundant arithmetic in FPGAs, research hardware/software co-design, and the design and development of systems within the scope of the IoT.