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RESEARCH ARTICLE

A 29.5 dBm OOB IIP3 TIA Based on a Two-Stage Pseudo-Differential OTA With R-C Compensation and Cascode Negative Resistance

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ABSTRACT This paper presents a highly linear and wideband transimpedance amplifier (TIA) suitable for 5G Sub-6 GHz surface acoustic wave (SAW) filter-less receivers (RX). It is known that for the baseband TIA in a SAW-less RX, the high out-of-band (OOB) linearity is necessary to cope with huge OOB blockers. In other words, the input impedance (Z_{in}) of the TIAs should be as low as possible, which in turn necessitates high-gain, large-bandwidth (BW) operational transconductance amplifiers (OTA). In this work, a pseudo-differential two-stage OTA with 46 dB open-loop gain and 1 GHz unity-gain loop bandwidth (UGLB) is designed at low supply voltage (Vdd). To stabilize the differential mode (DM) loop, the phase margin (PM) is compensated with the zeros generated by the series of resistors and capacitors (R-C), and the gain margin is improved by the feed-forward technique. To stabilize the common mode (CM) loop without the degradation of the DM gain, a wideband common mode rejection (CMR) technique named cascode negative resistance (CNR) is proposed. This TIA prototype is implemented in a 40 nm low-power (LP) CMOS technology. The measured results show that the TIA achieves 56 MHz BW and 29.5 dBm OOB IIP3. The input impedance is below 29 Ω in the concerned frequency range and the in-band (IB) input referred noise (IRN) is 120 uV_{RMS}. The total chip power consumption is around 8.5 mW at 1.2 V supply voltage and the core area is as small as 0.015 mm^2.

INDEX TERMS Transimpedance amplifier, SAW-less receiver, cascode negative resistance, R-C compensation, pseudo-differential, feed-forward, linearity, common mode rejection, wideband.

I. INTRODUCTION

Transimpedance amplifiers are widely used not only for optical communication RXs [1], [2] but also increasingly for wireless communication RXs [3], such as the low-noise transconductance amplifier (LNTA)-first RXs [4], [5], [6], [7], [8]. TIAs in the former are more like low-noise amplifiers (LNA), requiring low noise and large bandwidth. By contrast, TIAs in the latter work as the current-driven low-pass filters mostly, requiring low input impedance and high linearity.

The block diagram of a SAW-less LNTA-first wide-band RX is shown in Fig. 1. As illustrated, the large OOB blocker is mingled with the desired signal current and is transferred to the input of TIA because of the lack of the SAW before

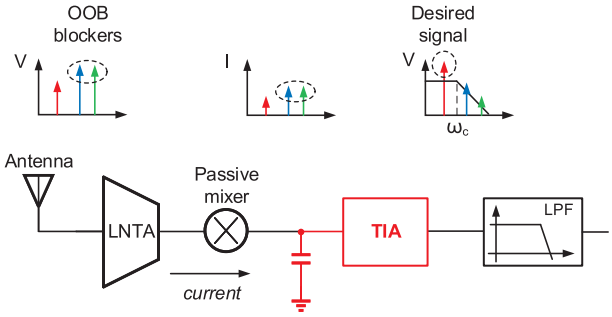

FIGURE 1. Block diagram of the SAW-less LNTA-first receiver.

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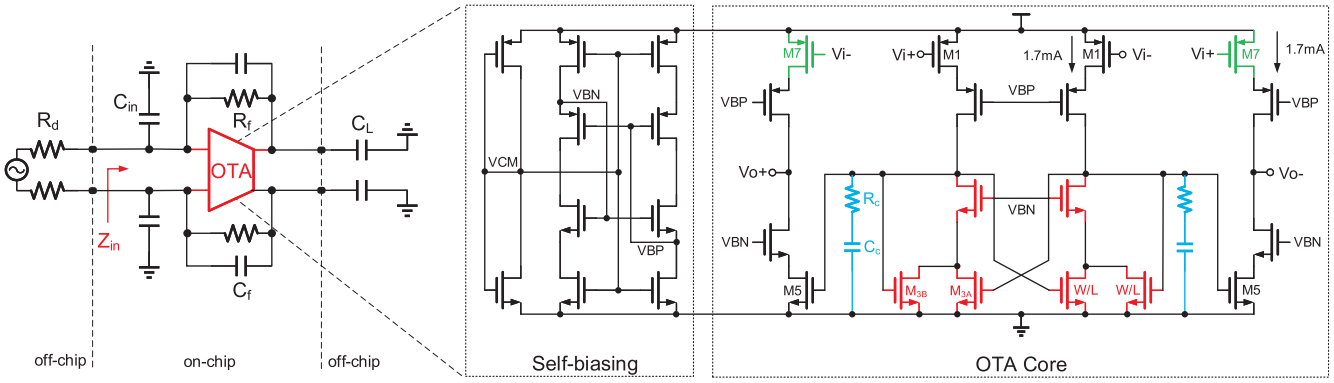

FIGURE 2. Schematic of the proposed TIA.

the LNTA. Therefore, the TIA input impedance at the blocker frequency must be low enough to ensure the receiver is unsaturated. So, the input impedance is an important characteristic of TIAs' linearity.

There are typically two dominant TIA structures, the common gate one and the OTA-based feedback one [9], to get low Z_{in}. But the common gate TIA [10], [11] operates in an open loop mode and its linearity is not so good that some techniques such as derivative superposition [11] are required to improve linearity. On the other hand, an OTA-based feedback TIA [4], [5], [6], [7], [8] operating in the closed loop is of inborn good linearity, and its classical structure is shown on the left side of Fig. 2. The feedback capacitor C_f and resistor R_f form a first-order filter. C_{in} is connected in parallel with the input to filter out the high-frequency interference and LO leakage. R_d denotes the LNTA output impedance (R_{LNTA}) seen by the passive mixer. If the mixer is driven by a 25% duty cycle LO, R_d is equal to $4R_{LNTA}$ [12]. Assuming the OTA is two-stage and the voltage gain is $A_{v,DC}/(1 + as + bs^2)$, the input impedance of the TIA is expressed as:

$$Z_{in} = \frac{1}{C_{in}s} \| \frac{R_f}{\left(1 + R_f C_f s\right)\left(1 + \frac{A_{v,DC}}{1+as+bs^2}\right)} \tag{1}$$

$$Z_{in,DC} = \frac{R_f}{\left(1 + A_{v,DC}\right)} \tag{2}$$

where $Z_{in,DC}$ is the DC input impedance, and $A_{v,DC}$ is the DC gain of the OTA. It's clear that Z_{in} is low at both low and high frequencies, thanks to high $A_{v,DC}$ and large C_{in}, respectively. But at the medium frequency which is concerned in this design, because of the finite value of C_{in} and the gain degradation of the traditional Miller-compensated OTA due to the limited BW, Z_{in} tends to have a large peak. This peak transforms the blocker current to a large voltage swing, degrading TIA's OOB linearity. Increasing C_{in} can reduce the peaking, which is a common approach in traditional design [3], [13]. However, it comes with the disadvantage of increased in-band input referred noise (IRN) [6], [7]. As illustrated in Fig. 3, considering the IRN voltage ($V_{in,n,OTA}$) of

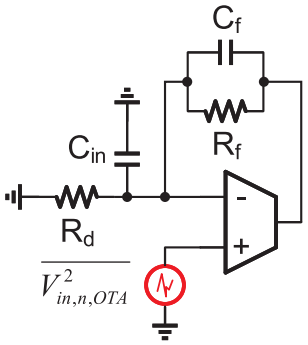

FIGURE 3. Single-ended TIA representation for NTF calculation.

the OTA, the noise transfer function (NTF) of the TIA is:

$$NTF = \frac{\overline{v^2_{o,n,O\ TA}}}{\overline{v^2_{in,n,O\ TA}}} = \left|\frac{R_d + R_f}{R_d}\right|^2 \frac{\left|1 + \frac{sR_dR_fC_{in}}{R_d+R_f}\right|^2}{\left|1 + sR_fC_f\right|^2} \tag{3}$$

The NTF shows a zero at frequency $\omega_z = -\frac{1}{C_{in}(R_f||R_d)}$. The larger the C_{in}, the higher the IB noise, also the larger the chip area. So, there is a compromise among area, noise, and OOB linearity.

At present, there are two main approaches to break the trade-off and solve the peaking problem. One is filtering [4], [5]. Notch filters [4] and low-pass filters [5] are employed in parallel with the TIA input to eliminate the peak, but this method is power-intensive. The other is to adopt three-stage OTAs [6], [7], [8] with high gain and large BW, which is more popular now. Instead of Miller compensation, the OTAs in [6] and [7] use zeros generated by the series of resistor and capacitor (R-C) and feedforward compensation, respectively, to achieve over 1 GHz BW within 15 mW of power. These two are very efficient compensation techniques for broadband OTA designs. However, the three-stage design is complicated, especially the frequency compensation. Actually, comparable performance is achieved by combining the two techniques in a two-stage OTA [14]. Additionally, a broadband common mode rejection technique

TABLE 1. Design parameters of the TIA.

R_d	C_{in}	R_f	C_f	C_L	R_c	C_c	W_p	W_n	L	$f_{in,1,5,7}$	$f_{in,3}$
$1k\Omega$	$20pF$	$1k\Omega$	$3pF$	$100fF$	$4k\Omega$	$0.6pF$	$1.8um$	$1um$	$45nm$	40	20

called cascode negative resistance is proposed to stabilize the CM without reducing the differential-mode gain. The TIA in [14] only gives the post-layout simulation results, while this paper will exhibit the test results and more design details and findings.

The paper is structured as follows, Section II presents the circuit design ideas, Section III gives the measurement settings and results, and Section IV concludes.

II. TIA DESIGN

The overall structure of the TIA is shown in Fig. 2, and the design parameters are listed in Table 1. R_d is set to be 1 kΩ, a large but reasonable value when the LNTA adopts cascode inverters as the output stage like that in [15]. C_{in} is chosen to be 20 pF, the same as in [6]. R_f is 1 kΩ, providing a transimpedance gain of 60 dBΩ. C_f is 3 pF, allowing a BW greater than 50 MHz since the TIA cut-off frequency ω_c is defined by $1/(R_f C_f)$. C_L represents the input capacitance of the next stage such as an LPF or buffer. It's assumed to be 100 fF for on-chip LPFs and may be several pF for off-chip test buffers. $W_{p(n)}$ is the finger width of each P(N)MOS, L is the channel length and $f_{in,x}$ is the number of fingers of M_x.

For the OTA design, a pseudo-differential structure without the tail current source is utilized to increase each MOSFET's voltage headroom at the low power supply. A very short channel length of 45 nm is used to make the unity-gain loop bandwidth of the OTA exceed 1 GHz. The purpose of the telescopic cascode typology in the first stage is to provide high voltage gain. As will be explained later, the first stage contributes a non-dominant pole, and its frequency should be as high as possible, so, a big current is required to increase the bandwidth as well as to reduce the thermal noise of the first stage. The PMOS input pair is chosen for its larger area compared with the NMOS counterpart, that is beneficial to low 1/f noise and mismatch.

Our goal is to achieve a 46 dB DC open-loop gain. Therefore, in the second stage, cascode is also adopted to increase the gain further, while decreasing the size of the MOSFETs, lowering the first stage's load capacitance, and raising the non-dominant pole frequency. The second stage also requires a big current to provide a large value of G_m (transconductance). Since the gain is set by $G_m R_{out}$, where R_{out} is the equivalent output resistance, which is very small due to the loading effect of R_f, G_m should be large to maintain the gain. The cascode MOSFETs are biased through a 10:1 replicated self-biasing network. Each branch draws 1.7 mA of current, for a total of 8.5 mW of power given the supply of 1.2 V.

The phase margin of the differential mode is improved by R-C compensation as shown in the blue part of Fig. 2, and the common mode is stabilized by the cascode negative resistance proposed in the red part. In addition, the feedforward path made up of $M7$ plays an important role in both modes. These stabilization techniques will be developed in detail in the following.

A. DIFFERENTIAL MODE STABILITY

The single-ended closed-loop model of the TIA is shown in Fig. 4(a). The loop gain is calculated using the open-loop circuit by breaking the loop at the input as shown in Fig. 4(b). g_m is the transconductance of the MOSFET, and r_o and c_o are the output resistance and capacitance, respectively. R_c and C_c form the R-C compensation. Ignoring g_{m7} first, the TIA loop transfer function is given in equation (4), as shown at the bottom of the page.

When $C_{in} \gg C_L$ *and* $C_f, Cc \gg c_{o1}$, the poles and zeros are located at:

$$\omega_{Z_1} = -1/(R_f C_f) \tag{5}$$
$$\omega_{Z_2} = -1/(R_c C_c) \tag{6}$$
$$\omega_{P_1} \approx -1/\{[R_d // (R_f + r_{o2})]C_{in}\} \tag{7}$$
$$\omega_{P_2} \approx -1/[(R_f // r_{o2})(C_f + C_L)] \tag{8}$$
$$\omega_{P_3} \approx -1/(r_{o1} C_c) \tag{9}$$
$$\omega_{P_4} \approx -1/(R_c c_{o1}) \tag{10}$$

The relative positions of the poles and zeros are illustrated in Fig. 5. As can be observed from formula (7), the dominant pole P_1 of this OTA is produced by C_{in}, unlike the conventional two-stage OTA. Usually, the output resistance r_{o2} is much larger than R_f, and $C_f \gg C_L$, then ω_{P_2} can be further simplified to $-1/(R_f C_f)$. So P_2 and Z_1 form a pole-zero doublet, and P_3 and Z_2 (created by R-C) form another doublet. Thus, the sole element that determines the PM is P_4, which is outside the unity-gain bandwidth (UGB), guaranteeing a PM of at least 45^o. As a result, the OTA can be regarded as a very stable single-pole system. The basic idea behind R-C compensation is that, it splits the poles and produces a zero to cancel the low-frequency pole, and pushes the non-dominant

$$\frac{V_r}{V_t} = \frac{g_{m1} g_{m5} R_d r_{o1} r_{o2} (1 + C_c R_c s)(1 + C_f R_f s)}{\left\{ \begin{array}{c} [1 + (C_c R_c + c_{o1} r_{o1} + C_c r_{o1}) s + C_c c_{o1} R_c r_{o1} s^2]\{R_d + R_f + r_{o2} + \\ [(C_{in} + C_f) R_d R_f + (C_{in} + C_L) R_d r_{o2} + (C_f + C_L) R_f r_{o2}] s + (C_f C_{in} + C_f C_L + C_{in} C_L) R_d R_f r_{o2} s^2 \} \end{array} \right\}} \tag{4}$$

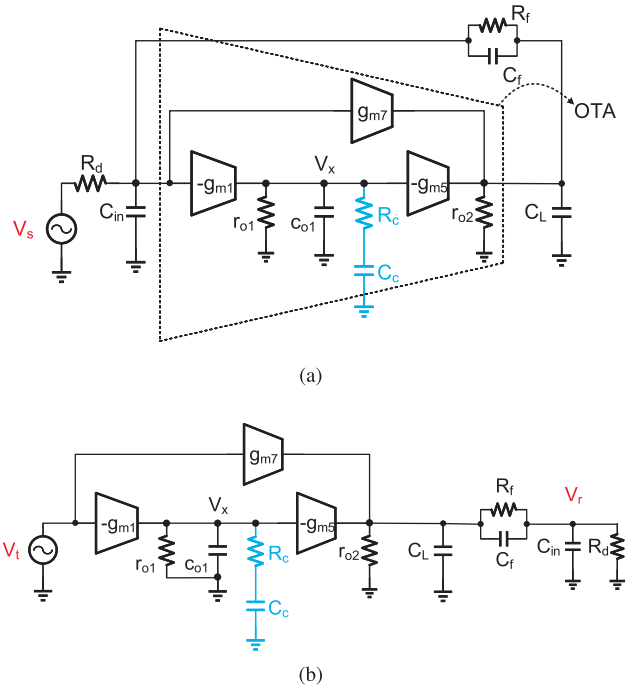

FIGURE 4. (a) Simplified single-ended representation of the proposed TIA. (b) The open-loop circuit used to compute the loop gain.

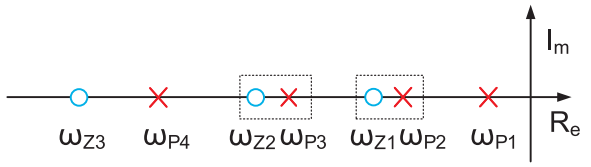

FIGURE 5. Pole-zero map of the proposed TIA.

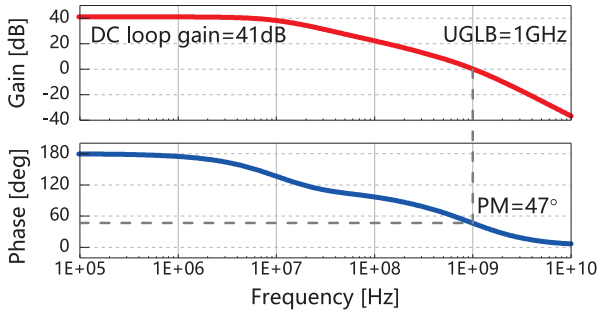

FIGURE 6. Simulated magnitude and phase response of differential loop gain.

pole to the high frequency, thereby increasing the PM. It is considerably different as compared to Miller compensation.

The zero generated by g_{m7} is approximately located at $\omega_{Z_3} = -(\frac{1}{R_c c_{o1}} + \frac{g_{m1}g_{m5}}{g_{m7}c_{o1}})$, a very high frequency and does not affect PM, but significantly improves the gain margin, which is also beneficial to stability. Fig. 6 exhibits the post-layout simulation results for the DM loop frequency response, where the PM is 47^o and the gain margin is almost 40 dB.

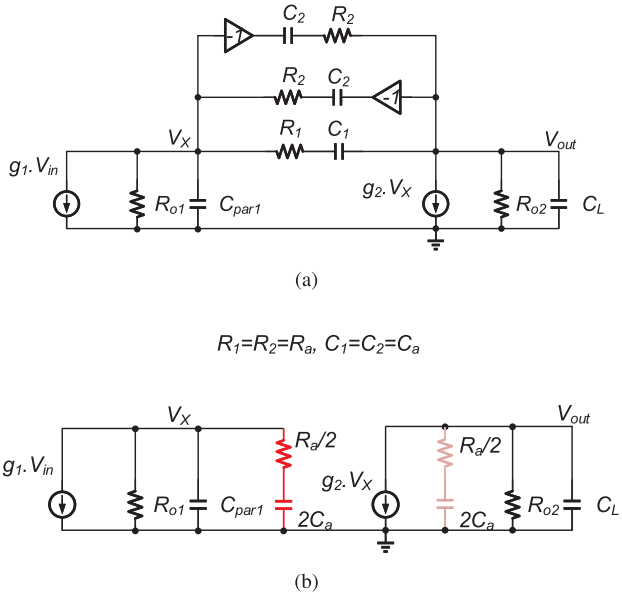

FIGURE 7. Half circuit small signal model of the OTA with (a) enhanced phase compensation, (b) R-C compensation.

The series of R-C has been frequently exploited for frequency compensation in previous literature but with different names, including local impedance attenuation (LIA) [16], [17], impedance adapting compensation (IAC) [18], and capacitors with equivalent series resistance (ESR) [19]. Despite having the same circuit form, they differ slightly in terms of philosophy or implementation. In the LIA, the R-C is used to control the complex poles [16]. The IAC and capacitor with ESR work on the same principle as R-C compensation, but they require big resistors or capacitors, respectively, both of which take up a lot of areas. However, only very small resistors and capacitors are needed in high-frequency circuits. So, R-C compensation is particularly appropriate in this design, occupying negligible area and consuming no power.

B. CONVERSION OF R-C COMPENSATION

There is an intrinsic connection between the R-C compensation and the enhanced phase compensation proposed in [20], which is frequently used in wideband RXs [4], [21], [22], and its principle is shown in Fig. 7(a). It combines the traditional Miller compensation (with a nulling resistor) and positive feedback. The positive feedback capacitor has an "anti-pole-splitting" effect [23], while the Miller capacitor has a pole-splitting effect. When they are combined, this type of compensation essentially no longer takes advantage of the Miller effect. In the original design, the values of R_1 and R_2 are close enough, and $C_1 = C_2$. Here, assuming R_1 is also equal to R_2, that is:

$$R_1 = R_2 = R_a, C_1 = C_2 = C_a \tag{11}$$

Thus, the transfer function of the model is displayed in equation (12), as shown at the bottom of the next page, which is just the same as that of the model in Fig. 7(b). When $C_a \gg C_L$

is not satisfied, the zero and pole generated by R-C cancel each other and don't contribute to the PM, so, the R-C at the output can be removed.

TABLE 2. Parameters of the circuit in fig. 7.

g_1	g_2	R_{o1}	R_{o2}	C_{par1}	C_L	R_a	C_a
$12mS$	$12mS$	$4k\Omega$	$0.5k\Omega$	$50fF$	$26pF$	$8k\Omega$	$0.3pF$

In practice, as the process fluctuates, condition (11) is not fully satisfied and the two circuits are not equivalent. However, their compensation effects are nearly indistinguishable. To verify this theory, Monte Carlo simulation over 1000 samples is performed with the parameters in Table 2. Only the process and mismatch of R_a and C_a are considered, R_a is poly resistor, and C_a is MOM capacitor. The results show that both two compensation techniques can increase the PM from 28^o to 50^o. The standard deviation of PM of R-C-compensated OTA is 0.9, and 0.904 for the enhanced phase compensation, almost the same. So, the two techniques are equivalent to some extent, and R-C compensation is easier to understand and simpler to design.

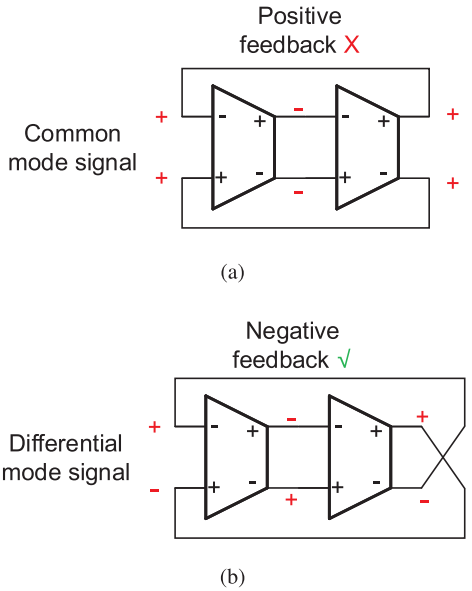

FIGURE 8. (a) Common mode loop of a two-stage differential OTA. (b) Differential mode loop.

C. COMMON MODE STABILITY

The common-mode feedback loop of the two-stage OTA is positive, unlike the differential-mode feedback loop, which becomes negative through cross-connections, as illustrated in Fig. 8. So, lowering the CM loop gain below 0 dB by

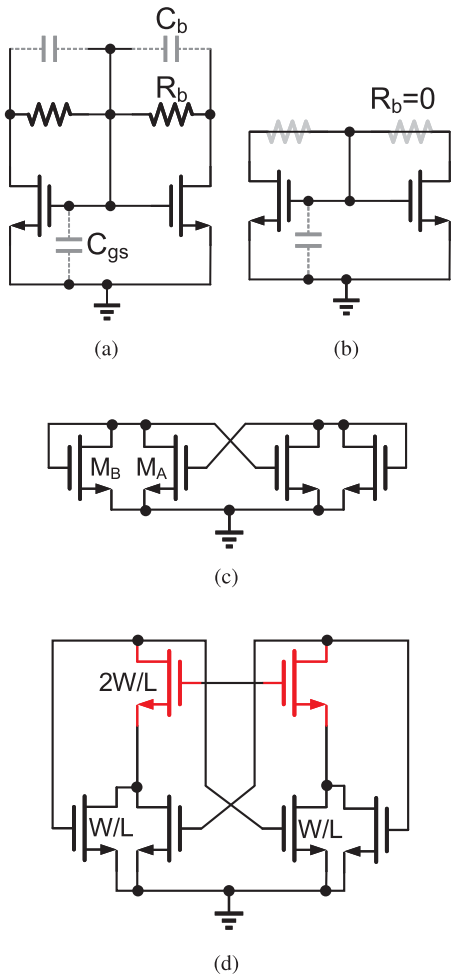

FIGURE 9. Evolution of the idea of cascode negative resistance.

common mode rejection techniques is necessary to avoid oscillation. The traditional local common-mode feedback (CMFB) uses resistors to sense the CM voltage. However, in high-frequency circuits, as shown in Fig. 9 (a), the capacitor C_{gs} of the MOSFET will form a low-pass network with R_b, reducing the high-frequency CMR capability. Adding a capacitor C_b can alleviate this phenomenon by introducing a zero [24], but when the OTA bandwidth is high, C_b should be very large, degrading the DM bandwidth and PM. In an ideal case where R_b is 0, the low-pass concern is eradicated, but at the cost of no DM gain. The negative resistance structure as shown in Fig. 9(c) can be used to improve the gain, but in short channel devices, the gain is still low due to the big value of output transconductance (g_{ds}). The work in [25] makes the size of M_A larger than M_B, allowing certain $-g_m$ to cancel g_{ds}, but this approach is unstable and PVT sensitive,

$$A_v(s)=\frac{V_{\text{out}}}{V_{\text{in}}}=\frac{g_1g_2R_{o1}R_{o2}\left(1+R_aC_as\right)^2}{\left(1+C_aR_as+2C_aR_{o2}s+C_LR_{o2}s+C_aC_LR_aR_{o2}s^2\right)\left(1+C_aR_as+2C_aR_{o1}s+C_{par1}R_{o1}s+C_aC_{par1}R_aR_{o1}s^2\right)} \tag{12}$$

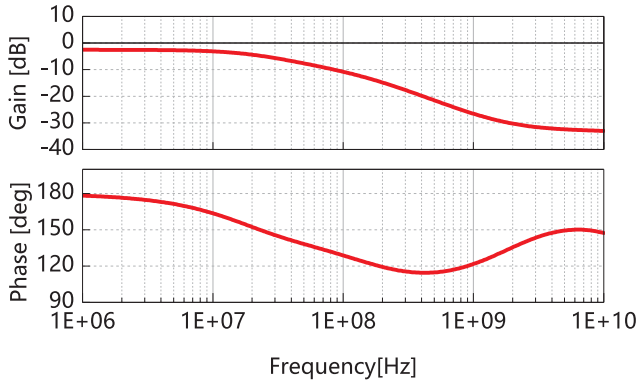

FIGURE 10. Simulated magnitude and phase response of common mode loop gain.

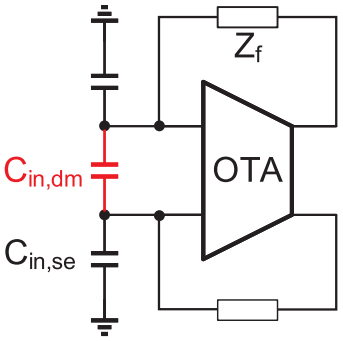

FIGURE 11. The implementation of C_{in}.

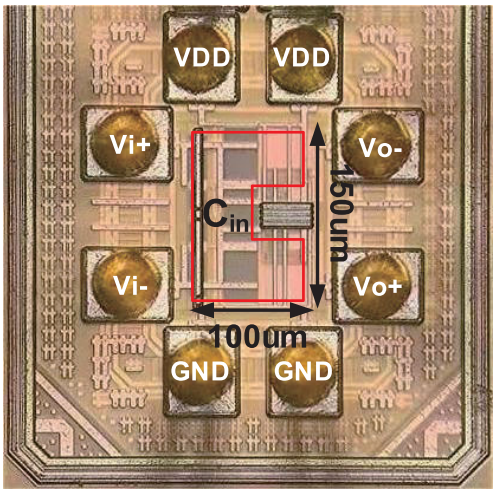

FIGURE 12. The chip photograph.

because g_m and g_{ds} are uncorrelated, and their values can be hardly controlled. In this work, M_A and M_B are set to the same size and matched in layout, and the DM gain is improved by cascode. Fig. 9(d) displays the final structure which we called cascode negative resistance.

The DM output impedance of CNR is A/g_{ds}, while the CM output impedance is $1/(g_m + g_{ds}/A)$, where A is the self-gain of the cascode MOSFET. Common-mode rejection of the second stage is achieved by feedforward [26]. Assuming that the g_m/i_d of the PMOS and NMOS is the same, the CM loop DC gain of the OTA is:

$$G_{ain,DC,CM} = \beta\left(\frac{1}{1+\frac{g_{ds1}+g_{ds3}}{Ag_{m3}}}-1\right)g_{m7}r_{o2} < 0 \quad (13)$$

where β is the feedback coefficient. It can be seen that the feedback of the CM loop has changed from positive to negative and the gain is very small, which greatly enhances the CM stability. The simulated CM loop response of the TIA is demonstrated in Fig. 10, where the gain is always below 0 dB and the phase is always negative.

Since, CNR and feedforward are broadband CMR techniques, which means that the rejection doesn't get worse as the frequency increases, this has the added benefit of allowing for a significant reduction in the area of C_{in}. As shown in Fig. 11, C_{in} can be implemented single-ended or differentially, with an equivalent C_{in} equal to $(2C_{in,dm}+C_{in,se})$. However, for the common-mode loop, $C_{in,dm}$ is open-circuited and doesn't serve as a load, which results in a common-mode loop BW much larger than the differential-mode loop BW. At high frequencies, the common-mode gain may exceed 0 dB, threatening stability. The TIA proposed in this study, however, takes advantage of the broadband properties of both CMR techniques, and C_{in} can be obtained differentially in a large amount. The single-ended implementation of C_{in} requires 40 pF. However, in this design, $C_{in,dm}$ is 9 pF, $C_{in,se}$ is 2 pF, and equivalent C_{in} is 20 pF, but only 13 pF is used, thus, greatly reducing the chip area.

The chip is taped out alone, and no other circuits are connected to the latter stage, so, the output CM voltage is not controlled by the comparator-type CMFB circuit. When working in a link, a global CMFB like the one in [6] should be added to precisely control the CM voltage around Vdd/2 and further improve the CMR.

III. MEASUREMENT RESULTS

The circuit is fabricated in a 40 nm LP 1P6M CMOS technology and the chip photograph is shown in Fig. 12. Thanks to the small C_{in}, which dominates the area as shown in the red block, the chip core only occupies 0.015 mm^2.

The chip is bonded directly to the printed circuit board (PCB) and the measurement setup is shown in Fig. 13. The TIA is powered by an ultra-low noise adjustable low dropout voltage (LDO) regulator (LT3042). A wideband differential op-amp (AD8351), AC-coupled to the TIA output, serves as the voltage buffer to drive test instruments, and its output impedance is 150 Ω. Therefore, a balun (ADT3-1T+) with an impedance ratio of 3:1 is adopted for the output impedance matching. The gain of the buffer can be adjusted by a single resistor. Low insertion loss baluns (TC1.5-52TG2+) operating at 0.5-550 MHz are used for input single-ended to differential conversion. A 75 Ω resistor R_m is added for

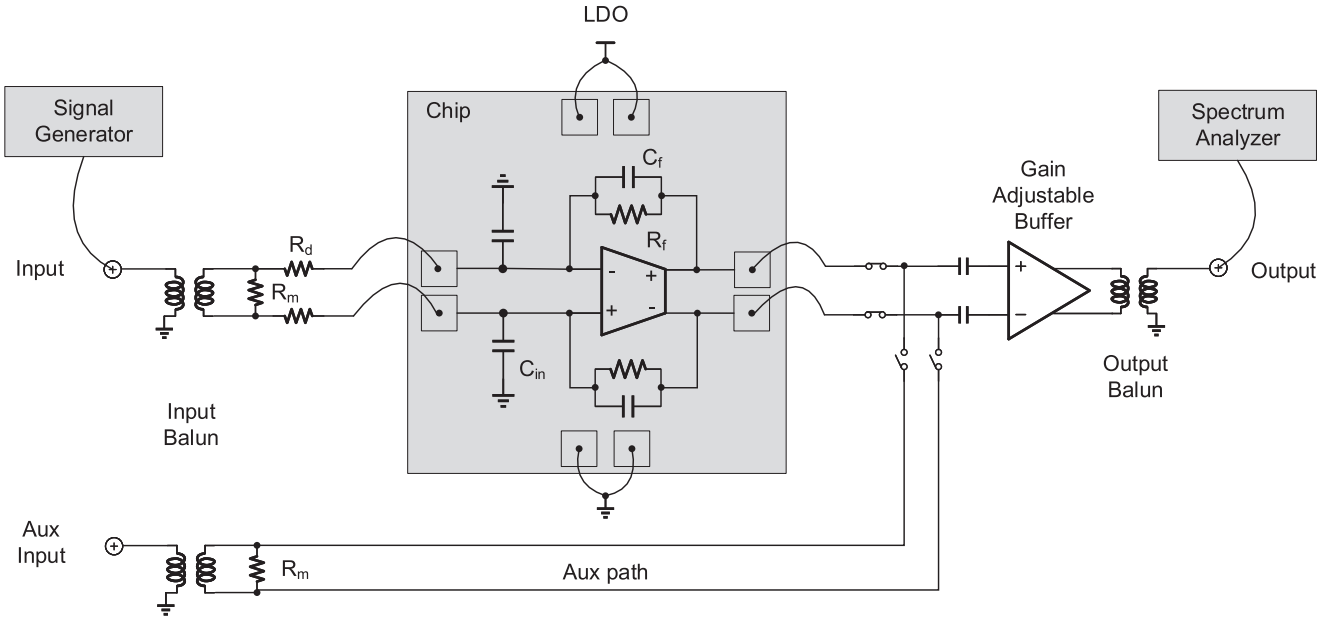

FIGURE 13. Measurement setup.

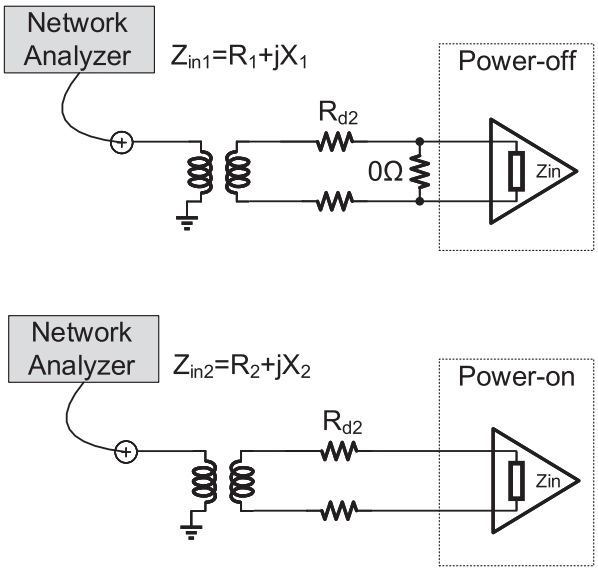

FIGURE 14. The method to measure the TIA input impedance.

input impedance matching. Buffer's performance is measured through the auxiliary path and de-embedded from the final results.

The input impedance is crucial because it reflects the gain and bandwidth of the OTA. The test principle is shown in Fig. 14. Replace R_d with a small resistor of close value to Z_{in} to reduce the error, and disconnect TIA and buffer. First, the input impedance parameter $(R_1 + jX_1)$ of the balun in series with R_{d2} is measured with a network analyzer (NA). Second, measure the impedance $(R_2 + jX_2)$ of the balun, R_{d2}, and TIA in series. Thus, the differential input impedance of the TIA is $[(R_2 - R_1) + j(X_2 - X_1)]$ and the results are shown in Fig. 16. Compared with the simulation results, Z_{in} peaks earlier, indicating that the bandwidth of the OTA is reduced. This is caused mainly by the PVT variation of the chip. However, Z_{in} is always below 29 Ω, and around 10 Ω at low frequency, representing a DC open-loop gain of the OTA of 46 dB according to formula (2), which closely matches the simulation and meets the design target.

Since, the input and output impedance of the test circuit is matched, the voltage gain is equal to the power gain, obtained through the S21 parameter from the NA. The TIA closed-loop DC gain is defined by R_f/R_d, but due to the process variation of R_f, it shifts to 0.24 dB as illustrated in Fig. 17. The -3 dB bandwidth is 56 MHz, and the filtering slope is slightly larger than 20 dB/Dec mainly due to the parasitic poles created by C_{in} and C_L. These errors can be calibrated by adjusting the values of R_f and C_f but require more pads.

The noise was measured using a spectrum analyzer (N9040B) with the input shorted and the buffer gain adjusted to 14 dB. Fig. 18 depicts the measured total output noise of the TIA and buffer, which is in good agreement with the simulation results. The noise integrated from 1 MHz to 50 MHz is -51.4 dBm, and the buffer's output noise is negligible, so, the equivalent input noise of the TIA is 120 uV_{RMS}, mainly contributed by R_d, R_f, and input PMOS of the OTA.

Linearity is tested with two-tone signals generated by the arbitrary waveform generator (M8190A). The buffer gain is set to -5 dB, and the IB IIP3 test results are shown in Fig. 15 (a). The IIP3 of the TIA is calculated by the cascade linearity formula:

$$\frac{1}{IIP3_{tot}} = \frac{1}{IIP3_{TIA}} + \frac{a_1}{IIP3_{buff}} \tag{14}$$

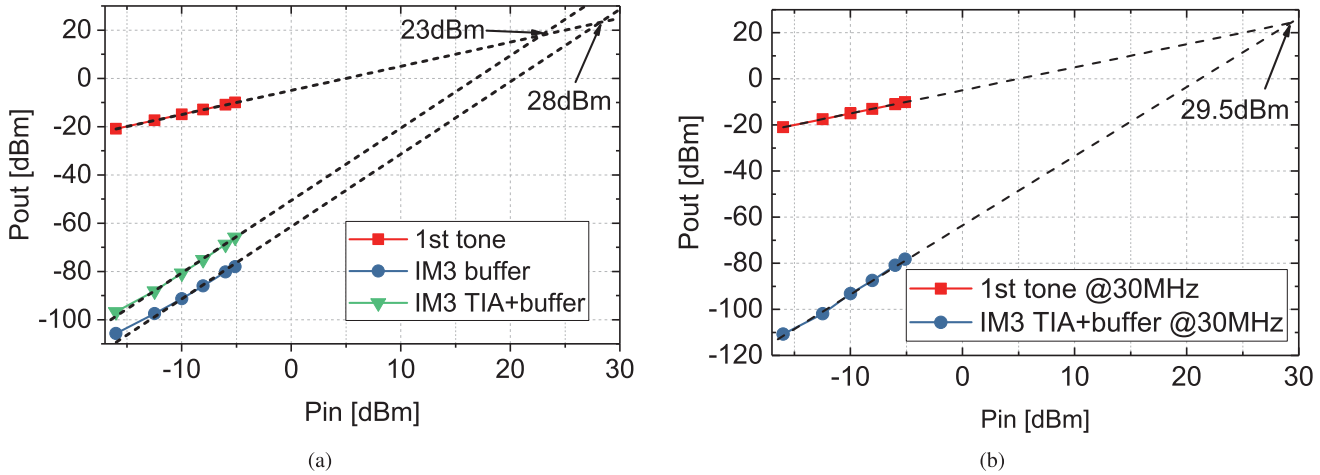

FIGURE 15. (a) Measured in-band IIP3 with two tones at 30-31 MHz. (b) Measured out-of-band IIP3 with two tones at 250-470 MHz.

TABLE 3. Performance summary and comparison.

Ref.	Tech. [nm]	Filter order [N]	Vdd [V]	$Z_{in,peak}$ [Ω]	BW [MHz]	IRN^a [uV_{RMS}]	OOB IIP3 [dBm]	f_{IM3} [MHz]	Power [mW]	Core area [mm^2]	$SFDR^b$ [dB]	FoM^c [dB]
[6] JSSC'18	28	1	1.8	32	20	13	50.5	10	5.4	0.026	90	182.8
[7] TCAS-I'20	65	2	1.8	90	80	6.2	26.8	10	14.2	0.037	78.6	170.1
[27] JSSC'17	180	4	1.8	NA	22.5	38.7	21.5	4	12.6	0.35	64.5	155.5
[28] JSSC'15	180	4	1.8	NA	33	9	18	1	1.38	0.14	70.6	155.9
This Work	**40**	**1**	**1.2**	**29**	**56**	**24.5**	**29.5**	**30**	**8.5**	**0.015**	**72.5**	**168**

[a] IRN is normalized to 10 MHz, assuming thermal noise is dominant
[b] $SFDR = 10\lg(\frac{OOB\ IIP3}{IRN})^{2/3}$
[c] $FoM = SFDR + 10\lg(\frac{BW \cdot N}{Power} \cdot \frac{f_{IM3}}{BW})$ [7]

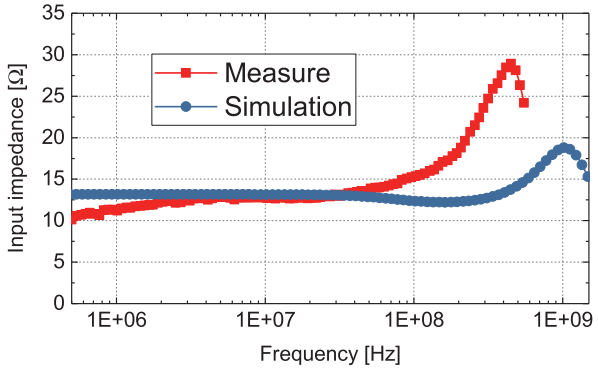

FIGURE 16. Measured differential input impedance of the TIA.

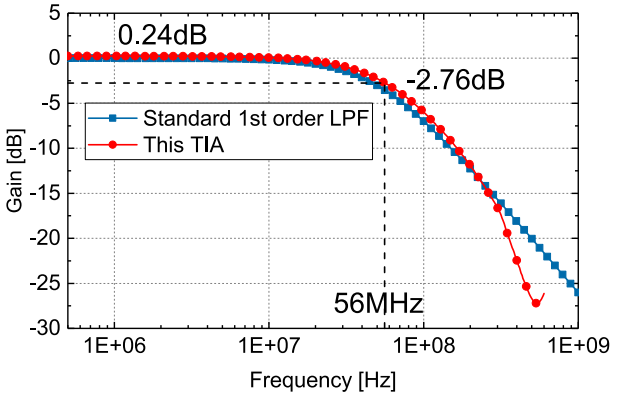

FIGURE 17. Measured voltage gain of the TIA.

where a_1 is the power gain of the TIA. The calculated TIA IB IIP3 is 24.7 dBm. The OOB IIP3 is 29.5 dBm, approximately equal to that of the TIA cascading buffer because a_1 is very small out-of-band, and the impact of the buffer can be ignored. The measured IB IIP3 and OOB IIP3 are about 10 dB and 15 dB smaller than the simulation, respectively, partly due to the low input resistance (5 kΩ) and the large input capacitance (0.8 pF) of the buffer that reduce the gain and bandwidth of the OTA. In the previous simulation, C_L is taken as 100 fF. If considering the non-ideality of the buffer,

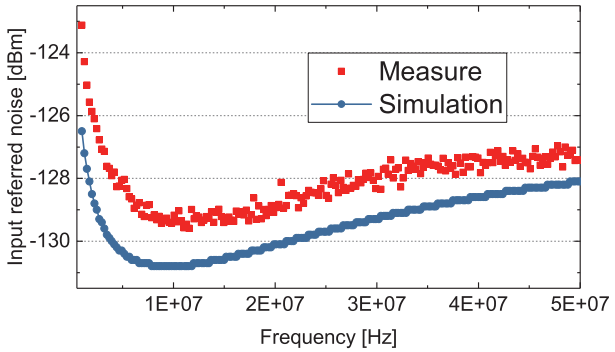

FIGURE 18. Measured output noise power spectral density of the TIA and buffer.

the simulated IIP3 of the TIA reduces by about 5 dB. Moreover, the nonlinearity of the feedback resistor R_f will further deteriorate the linearity as mentioned in [6].

The overall performances are compared in Table 3. This work achieves the lowest $Z_{in,peak}$ at the lowest supply voltage and occupies the smallest chip area, and the figure of merit (FoM) is comparable to similar products.

IV. CONCLUSION

In this paper, a 56 MHz bandwidth TIA for wideband LNTA-first receivers is designed. An input impedance of less than 29 Ω is achieved at a 1.2 V supply voltage. The out-of-band IIP3 is as high as 29.5 dBm. The power consumption of the entire chip is only 8.5 mW, occupying 0.015 mm^2 of area. This work attempts to achieve a performance comparable to that of a three-stage OTA using a two-stage one, so, advanced R-C and feedforward compensation are employed. The zero created by the series R-C improves the differential mode phase margin, and the gain margin is increased by feedforward. A high-frequency and robust common-mode rejection technology called cascode negative resistance is proposed for CM stability. The article also proves that the traditional enhanced phase compensation can be converted into R-C compensation, with no difference in compensation effectiveness or robustness, and that the R-C compensation is much easier.

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