IEEE Access
Multidisciplinary ⋮ Rapid Review ⋮ Open Access Journal

Received 13 January 2023, accepted 3 February 2023, date of publication 10 February 2023, date of current version 15 February 2023.

Digital Object Identifier 10.1109/ACCESS.2023.3244127

RESEARCH ARTICLE

Stacked Common-Base vs Common-Emitter mmWave PA Cells and 68-105 GHz Broadband Asymmetrical PA in 250nm InP HBT

ZHENG LIU[1], (Graduate Student Member, IEEE), TUSHAR SHARMA[2], (Member, IEEE), AND KAUSHIK SENGUPTA[1], (Senior Member, IEEE)

[1]Electrical and Computer Engineering, Princeton University, Princeton, NJ 08544, USA
[2]Renesas Electronics, San Diego, CA 92121, USA

Corresponding author: Zheng Liu (zhengl@princeton.edu)

This work was supported in part by the Defense Advanced Research Projects Agency (DARPA) Young Faculty Award.

ABSTRACT In this paper, we perform a comparative analysis between stacked common-emitter (SCE) and stacked common-base topologies (SCB) for high efficiency and broadband millimeter-Wave (mmWave) power amplifiers (PAs) in 250 nm InP-based heterojunction bipolar transistor (HBT) technology. We propose an analytical approach to design stacked PA cells accounting for complex load impedance and intra-matching between stacked transistors to allow optimal loadpull operation of both the devices in the stack. We demonstrate how SCB cell can allow higher gain, mitigated power and efficiency trade-off and linearity, when compared to more well-established SCE cells at higher mmWave frequencies. The designed SCB and SCE cells achieve a measured gain of 11.8 dB/6dB gain, 33%/34% peak PAE, 16.8%/14.5% PAE at 6-dB back-off, and P_{sat} of 18.7 dBm/19.6 dBm at 90 GHz. The SCB PA demonstrates superior linearity, and achieves an EVM of 2.38% at 11.8-dBm average power supporting 3 Gbps 64-QAM. The SCB PA achieves 17.9-18.9-dBm P_{sat} across 80-110 GHz and is one of the highest efficiency, broadband and linear PAs in W-band using InP technology. Utilizing the PA cells, we demonstrate an asymmetrical broadband power combining circuit for high efficiency combining across a large relatively bandwidth. The PA operates across a 68-105 GHz $P_{sat,3dB}$ bandwidth with 21.5 dBm peak saturation power and 24% peak PAE.

INDEX TERMS Asymmetrical combiner, broadband, common-base, InP HBT, millimeter-Wave (mmWave), power amplifiers (PAs), stacked PA.

I. INTRODUCTION

InP heterojunction bipolar transistors (HBTs) with f_{max} approaching 700 GHz enable high-power, high-efficiency amplification at mmWave frequencies for communication and sensing. Courtesy of both the vertical and horizontal scalings, InP HBT balances the speed-breakdown trade-off and is a strong candidate for mmWave power amplifier operating at high mmWave frequencies above 40 GHz [1], [2]. As more mmWave bands have been allocated, the future spectrum sharing and intelligent spectrum management require the PA to be operable across a larger relative bandwidth. Among various mmWave InP PA topologies, common emitter (CE) device with Wilkinson type or corporate power combiner is the most popular [3], [4], [5], [6]. However, the low output impedance of a single CE PA cell suffers a larger output matching impedance transformation ratio as more PA cells are parallel combined, which limits the bandwidth. On the other hand, the conventional Wilkinson or muti-stage corporate power combiner typically trades matching efficiency for bandwidth. Therefore, the bandwidth of mmWave PA should be strategically addressed in both PA cell level and power combining architecture level.

For mmWave PA cells, transistor stacking allows a simultaneous higher power and higher gain and more importantly, a larger bandwidth due to higher output impedance [7], [8],

The associate editor coordinating the review of this manuscript and approving it for publication was Dušan Grujić.

[9], [10], [11], [12], [13], [14], [15], [16]. Most of the prior works utilize a CE transistor as the input device with an output transistor connected in series to form a stacked common emitter (SCE) PA cell. Besides CE based topologies, common base (CB) topology, due to the greater breakdown voltage and higher available gain compared to CE-based PA cells, may also be exploited in power amplifier applications. Furthermore, combining the advantage of CB device and transistor stacking architecture leads to a new type of high gain, broadband PA cell: stacked common base (SCB) cell which will be discussed in this paper.

For broadband power combining architecture, the in-phase multi-way power combining presents the classical trade-off between bandwidth, matching efficiency and output power in PA design space [17]. Introduction of active matching networks or equivalent negative reactance components to direct cancel the reactive part can overcome this limitation [18], but this often comes with the limitations of instability and poor power handing [19], [20], [21]. Techniques such as frequency reconfigurable networks [22], [23], or external power injection with reconfigurable amplitude and phase [24], [25] have been proposed to loosen the trade-offs, but such architecture increases the control complexity, introduces switch losses and non-linearity, and are particularly more complex in InP-based technologies. Distributed amplifier architecture enhances the bandwidth, but typically struggles with efficiency due to non-optimum load across each stage [8].

In this paper, we address both the PA cell and combiner networks to create efficient and broadband mmWave PAs. First, we study and compare the various PA cells in mmWave with a focus on the SCE and SCB topologies, presenting an analytical method to design stacked PA cells, and demonstrating the importance of taking the load reactance into analysis for operation at mmWave. Secondly, using the SCE PA cells, we utilize an asymmetrical power combining architecture for bandwidth enhancement over conventional symmetrical power combiner [26]. The remainder of the paper is organized as follows. Section II discusses our proposed analytical method and design flow of the optimum stacked HBT PA cell (SCB and SCE) to enable simultaneous higher power and gain compared to single transistor PA cell at mmWave. Section III presents a comparison between CE, CB, SCE and SCB cells in terms of large signal performance, linearity and stability. The PA cell performance is also verified experimentally, emphasizing the consideration of stacked PA cell selection. With the selected PA cell, Section IV introduces the PA architecture with asymmetrical power combining to maintain high combining efficiency across a wide bandwidth. Section V presents the design and measurement result of the 68-105 GHz asymmetrical power combined PA using SCE cell in 250nm InP technology.

II. ANALYSIS AND DESIGN OF STACKED HBT PA CELL

A. PRINCIPLE AND DESIGN METHODOLOGY

Transistor stacking is a series power combining technique based on the series interconnection of a bottom transistor

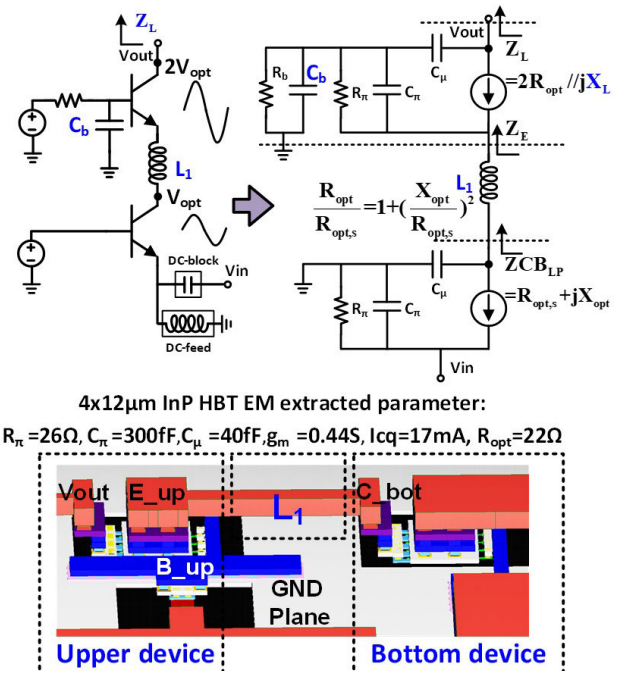


FIGURE 1. Proposed stacked common base (SCB) PA cell and its layout.

cascaded with a common-base-like upper transistor. Compared to single transistor, this enables higher output impedance for higher intrinsic gain, higher optimum impedance for better output matching bandwidth and efficiency, and higher saturation power. Conventional stack topology utilizes a common-emitter transistor at the bottom as the input transistor [7], [8], [9], [10], [11], [12], [13], [14], [15], [27]. As will be seen in Section III, the common-base (CB) InP HBT leads to superior performance than CE in terms of gain, gain compression and back-off efficiency at mmWave frequency range (>70 GHz), which motivates the investigation of utilizing the advantages of CB device by replacing the bottom CE device with a CB counterpart in a stacked PA cell, namely, forming a stacked common-base (SCB) topology (Fig. 1). Here, the base of the bottom device is ac grounded and the input signal is fed into its emitter, the top transistor has a shunt capacitor C_b at its base while an inductor L_1 is inserted between the two transistors (Fig. 1). Intuitively, the SCB topology is a voltage amplifier since the input current ideally flows direct to the output node. The SCB topology was first proposed in [28] and the following section extends the analysis and design of an optimum SCB PA cell. There are three key considerations governing the proper operation of the SCB PA cell. They are

- *Output voltage doubling:* Assume the optimum collector voltage swing of bottom CB transistor is V_{opt} and its corresponding optimum load-pull impedance is $ZCB_{LP}=R_{opt,s}+jX_{opt}$, which has an equivalent shunt resistance of R_{opt} ($R_{opt}=R_{opt,s} \times (1+(X_{opt}/R_{opt,s})^2)$. The stacked PA is expected to have a doubled voltage swing ($2V_{opt}$) at the output node which is in-phase with

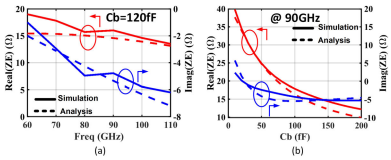


FIGURE 2. Variation of input impedance Z_E. (a) Variation against frequency for a fixed C_b (120 fF); (b) Variation against C_b for a fixed frequency (90 GHz).

bottom transistor collector swing. To achieve this, the desired optimum load impedance (Z_L) of the stacked PA should have a shunt resistance of $2R_{opt}$ in parallel with a shunt reactance of X_L (Fig.1).

- *Broadband inter node impedance matching:* If we directly connect the emitter of top transistor to the collector of bottom transistor like a cascode, the interface is typically strongly mismatched because the input impedance of the top transistor is typically different from the optimum load impedance of bottom transistor. As we will show later, the top transistor input impedance is a function of Cb and X_L, so one can choose these two parameters such that the required inter node impedance transformer ratio is minimized, which leads to a simple low loss matching network typically a single series inductor, and a wide matching bandwidth.
- *In-phase voltage addition at intrinsic current generator plane:* The imaginary part X_L in Z_L cannot be ignored because it should resonate out the stack device output capacitance. Only if this cancellation happens, the output current can flow to a pure resistive load ($2R_{opt}$) to produce a voltage at intrinsic current generator plane that is in-phase with V_{opt}. Therefore, the Z_L=$2R_{opt}$//jX_L serves the optimum impedance at the "load-pull" plane.

Therefore, the design task is to properly choose these parameters: C_b, X_L and L_1 such that the above three constraints are fulfilled simultaneously. Our analysis and design method extends the methods in prior stacked PA analysis, taking into account the complexities of the reactive parts, and coupling capacitance and its effect on bandwidth. The stacked mmWave amplifier analysis presented in [7] is based on the assumption that the load impedance of stacked PA is a pure real value. A follow-up analysis in [10] accounts for the reactive part, but does not account for the gate-drain capacitance (C_μ in our HBT case). In addition, the added intra-matching component on the stacked PA output impedance also needs to be taken into account [10]. In our analysis, the effect of the matching circuit on stack output capacitance is properly addressed.

Fig. 1 shows the equivalent model for the SCB PA cell analysis. An external Rb is added for base DC biasing. To address the inter-node matching, we firstly calculate the input impedance of the top transistor (Z_E) as a function of Cb and X_L:

$$Z_E = \frac{\frac{1}{Z_\pi} + \frac{1}{Z_{tune}} + (\frac{1}{Z_L} + \frac{1}{Z_\pi} + \frac{1}{Z_{tune}} + g_m)(SZ_L C_\mu)}{(g_m + \frac{1}{Z_\pi})(SC_\mu + \frac{1}{Z_{tune}}(1 + SZ_L C_\mu))} \quad (1)$$

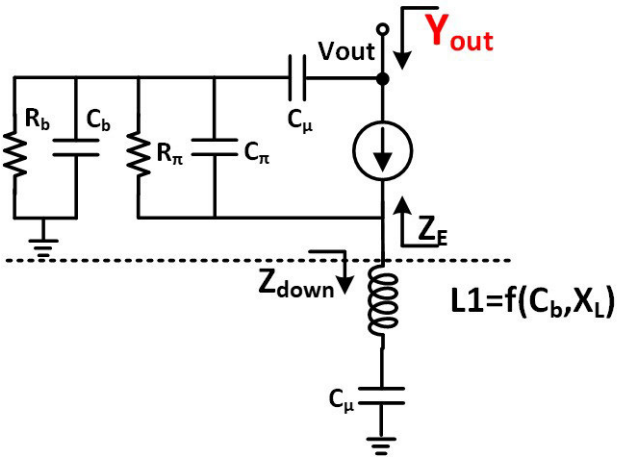


FIGURE 3. Second design constraint determined by stack output capacitance to ensure optimal resonant matching.

where

$$Z_\pi = \frac{R_\pi}{1 + SR_\pi C_\pi}, Z_{tune} = \frac{R_b}{1 + SR_b C_b} \approx \frac{1}{SC_b} \quad (2)$$

and

$$Z_L = \frac{2jR_{opt}X_L}{2R_{opt} + jX_L} \quad (3)$$

The external shunt cap (C_b) at the base of top device plays an important role in adjusting Z_E, because C_b influences the base voltage swing of top transistor, and through C_π coupling, the emitter node of top transistor also gets influenced. Note that for 250nm InP technology, the moderate current gain ($\beta \approx 20$) results in a relatively small R_π, which presents the similar impedance as C_π, so R_π should not be ignored in Z_π. However, the biasing resistor R_b should be large as a few hundred ohms to avoid the bypass effect on C_b, so C_b dominates the Z_{tune}.

Fig. 2 shows the good correlation between the simulation and analysis represented in (1) for both real part and imaginary part of Z_E, as 1. A function of frequency under fixed C_b and 2. A function of C_b at fixed frequency. All the analysis in this section is based on the extracted circuit parameters ($C\pi$, $C\mu$, $R\pi$, gm and R_{opt}) for a 4×12 μ m transistor with 17 mA quiescent bias current, which is shown in Fig. 1. For the purpose of this figure, we assume the output load impedance of the stack is resistive (X_L=∞). Fig. 2(b) shows that the externally added C_b can significantly modulate the real part of the top device input impedance while a weaker effect on imaginary part is observed once C_b is large enough.

First, we concentrate on the intra-node impedance matching such that the bottom CB transistor sees the loadpull impedance (ZCB_{LP}) for optimal power generation. A perfect complex impedance matching condition of Z_E=ZCB_{LP} maybe achieved by simultaneously selecting C_b and X_L from (1). However, such solution may not exist especially at high frequency. Therefore to achieve intra-node matching, new passive component should be added. For broad

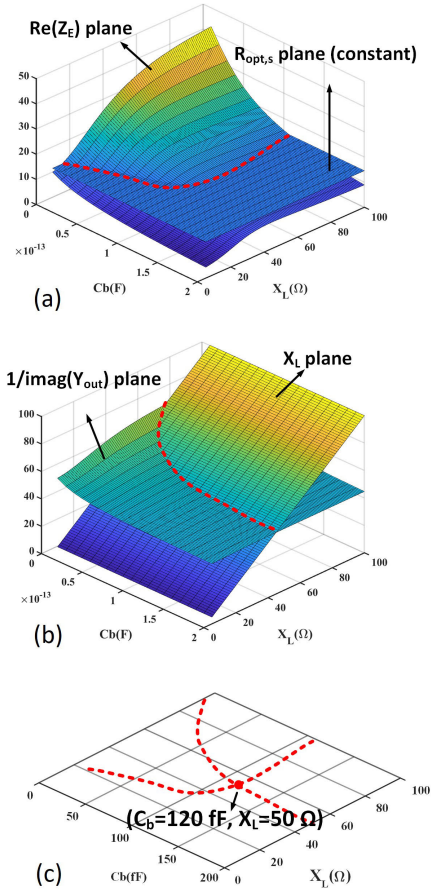


FIGURE 4. Variation of $\Re(Z_E)$ and $1/\Im(Y_{out})$ as functions of C_b and X_L. The intersection of the two lines gives the unique values of C_b and X_L for optimal stack operation.

matching bandwidth, we can select the two design parameters (C_b and X_L) such that the impedance transformation ratio is minimized by ensuring the following:

$$\Re(Z_E) = R_{opt,s} \tag{4}$$

where $R_{opt,s}$ is the real part of the load-pull optimum load impedance of the bottom CB transistor. By doing so, only a series reactance tuning inductor L_1 is needed to compensate the imaginary part. Since Z_E is a function of C_b and X_L according to (1), Fig. 4 (a) shows the plane of $\Re(Z_E)$ and the curved intersection line illustrating the range of values of C_b and X_L that ensure (4).

For a certain combination of C_b and X_L, the imaginary part of Z_E ($\Im(Z_E)$) is also determined. Therefore, the broadband reactance tuning inductor L_1 can be calculated from (5) which is also a function of C_b and X_L. This inductor can be implemented by a high impedance transmission line (Layout in Fig. 1).

$$L_1 = \frac{X_{opt} - \Im(Z_E)}{\omega_0} = f(C_b, X_L) \tag{5}$$

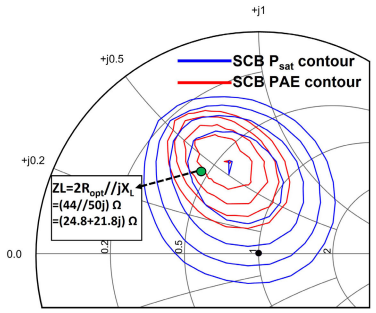


FIGURE 5. Calculated optimum load impedance against simulated results.

In addition to the constraint in (4), ideally the loadline impedance of the stack at intrinsic current generator plane should be real ($2R_{opt}$), which requires the reactance X_L to cancel the device output capacitance. This naturally leads to the second design equation of the stacked PA. As shown in Fig. 3, the output admittance Y_{out} can be analyzed, also as a function of Cb and and X_L in (6). The Y_{out} dependence on X_L is due to that Y_{out} is a function of L_1 while L_1 is a function of X_L (from (5)). Note that for the common-base transistor at the bottom, the output network is equivalent to a capacitor C_μ assuming a large output resistance.

$$Y_{out} = \frac{SC\mu(1+g_mZ\pi+SC_b(Z_{down}+Z_\pi+g_mZ_{down}Z_\pi))}{1+S(C_bC_u)(Z_{down}+Z_\pi+g_mZ_{down}Z_\pi)} \tag{6}$$

where

$$Z_{down} = SL_1 + \frac{1}{SC_\mu}, \tag{7}$$

Therefore, to optimally resonate out the output capacitance captured in the imaginary part of Y_{out}, the second design equation is

$$\frac{1}{\Im(Y_{out})} = \frac{1}{\omega_0 C_{out}} = X_L \tag{8}$$

At $f_0 = 90$ GHz, equation (8) leads to another constraint curve governing C_b and X_L, as shown in Fig. 4(b). The intersections of the two lines in C_b and X_L plane gives the unique solutions to these parameters (Fig. 4(c)).

At 90 GHz, the SCB PA cell with extracted device parameters shown in Fig.1 results in C_b=120 fF, X_L=50 Ω and L_1=30 pH. Therefore, the solution of the optimum load impedance for stacked PA cell can be calculated according to equation (3). The calculated impedance ($2R_{opt}||jX_L \approx$ 24.8+j21.8 Ω) is compared with the circuit load-pull simulation in Fig. 5. The good correlation validates the proposed analytical design method. The small discrepancy may due to the neglect of the device C_{ce} and output resistance. Note that this generalized design method for optimum stack PA operation achieving voltage scaling and ease of intra-matching can also apply to SCE PA cell.

B. DESIGN FLOW SUMMARY

Following the analysis in Section II, the design flow of a stacked HBT PA cell can be summarized as below:

1. Given stacked PA supply VDD, center operating frequency f_0 and desired P_{sat}, choose bottom device (CB or CE) size to deliver 1dB compression output power equal to at least half of the P_{sat}, under supply of VDD/2. Then extract the device parameters (R_π,C_π,C_μ,gm) according to [29], and optimum load pull impedance ZCB_{LP}.

2. Set the top device base bias point such that the collector bias voltage of bottom device is VDD/2. Based on the analysis presented in (1) - (8), find the intersections of the two design constraints described by (4) and (8) to evaluate C_b and X_L. Evaluate L_1 according to (5). Verify the calculated optimum load impedance Z_L is close to the load-pull simulation result of the stacked PA (Fig. 5).

3. Fine tune the first pass design parameters, followed by a load-pull analysis for performance optimization.

III. COMPARISON OF CE,CB,SCE AND SCB TOPOLOGIES

In this Section, we focus on the trade-offs CB device for mmWave power amplification and comparison of different PA cells selection, especially between SCE and SCB.

A. CB PA CELLS FOR HIGH GAIN, HIGH LINEARITY, AND HIGH EFFICIENCY WITH InP HBTs

CB topology, generally due to the reduced input-output feedback capacitance C_{ce} compared to the C_{bc} in the regular common-emitter (CE) topology, provides higher available gain at mmWave. Based on BJT transistor T model shown in Fig. 6, the maximum stable gain (MSG) and K factor of CB and CE device can be compared [30]:

$$\frac{MSG_{CB}}{MSG_{CE}} \approx \frac{r_{ex}+r_e}{r_b} \tag{9}$$

$$K_{CE} \approx ((r_b+2r_{ex})C_\mu + r_e C_\pi(1+\frac{2r_b}{r_{ex}}))\omega$$

$$K_{CB} \approx ((r_b+2r_{ex})C_\mu + r_e C_\pi)\omega$$

$$\omega_{(k=1,CB)} > \omega_{(k=1,CE)} \tag{10}$$

From (9), for a HBT device with high base doping such that r_b is relatively smaller than the numerator, MSG_{CB} can be larger than MSG_{CE}. From (10), starting from low frequency, we can see the K factor increases as frequency with a lower rate for CB topology compared to CE topology, which means the knee frequency where K=1 is higher for CB compared to CE. With a simultaneous higher knee frequency and potential higher MSG for CB, the maximum available gain (MAG), therefore, is also higher for CB. The simulation of a $4 \times 12\ \mu$m InP device for CB and CE topology also shows the similar behavior where the G_{max} of CB is higher than CE by up to 6 dB across 70-300 GHz (Fig. 6).

Secondly, due to higher breakdown voltage VB_{CBO} for CB topology, CB can also be attractive for power amplifications under high supply voltage [16], [31]. From the DC-IV simulation of the InP transistor, we can see CB cell has a sharper transition from off state to active state which indicates a preferable V_{knee}. In addition, in practice due to the thermal-electric feedback behavior [32], the CE configuration suffers from a larger signal-dependent Ic slope compared to CB. This results in a superior gain compression and larger achievable swing for CB (Fig. 7). For a regular class B CE or Common-source (CS) transistor, its optimum load impedances for power ($Z_{opt,pwr}$) and efficiency ($Z_{opt,eff}$) are notoriously distinct which typically needs a compromised choice of load impedance between these two conflicting requirements (Fig. 7(b)). The difference between $Z_{opt,pwr}$ and $Z_{opt,eff}$ can be explained by soft-turn on and

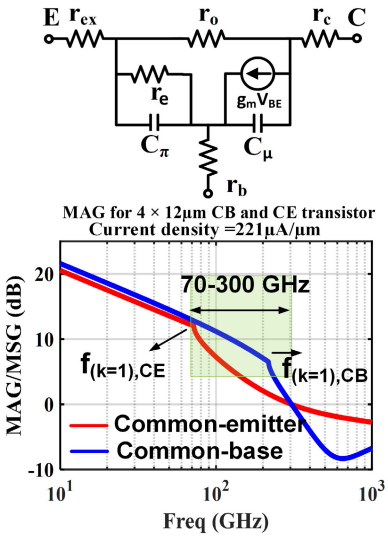


FIGURE 6. Simulation result showing higher available gain for CB cell.

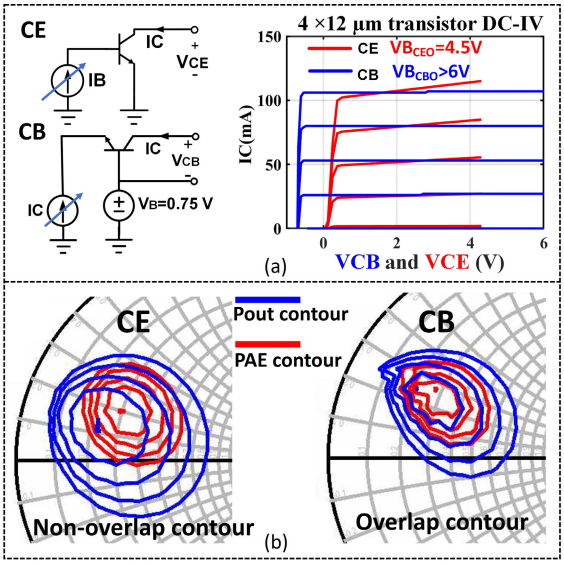


FIGURE 7. (a) DC-IV Simulation results showing superior gain compression and larger achievable swing for CB allowing higher linearity. (b) The 'close to ideal' DC-IV response leads to an overlapping of power and efficiency optimum loadpull impedance for CB.

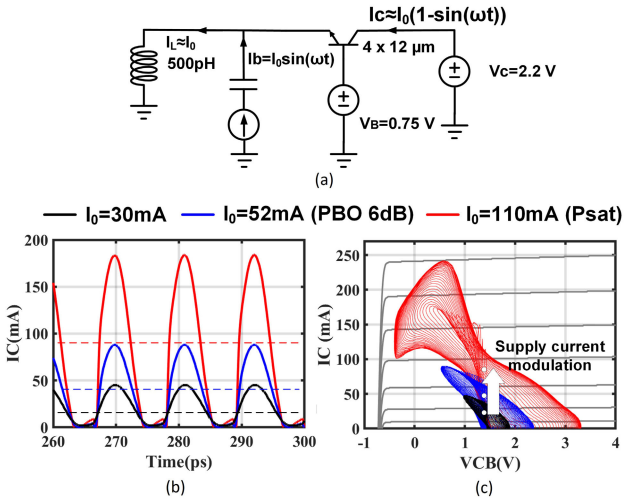


FIGURE 8. Current clamping effect for better back-off efficiency for CB.

current-dependent knee voltage [33]. On the contrary, due to the sharper turn on and relatively low knee voltage of CB transistor, the close to ideal DC-IV curve leads to almost overlapping of power and efficiency loadpull impedances (Fig. 7(b)). Such a property allows the simultaneous maximization of power and efficiency performance of a CB transistor.

Thirdly, the unique bias and signal feed mechanism for CB topology enables the current clamping effect [34] for linear and back-off efficiency enhancement operation. As shown in Fig. 8 (a), an inductor is used to bias the emitter to ground potential and a sinusoidal current with magnitude of I_0 stimulates the amplifier. When the input current magnitude I_0 is larger than the quiescent bias current, in the first several periods, the transistor is forced to be off and after several charging cycles, the inductor will be charged with a DC current of I_0. The charging cycles can be illustrated in the continuous load-line trajectory in Fig. 8 (c). Once the steady state is achieved, the shorted circuit output current of the amplifier will be $Ic=I_0(1-\sin(\omega_0 t))$. This collector current is a level shifted sinusoidal waveform with class A conduction angle, but more importantly, the average current is proportional to the input current magnitude. The reduced bias current at lower input power results in the back-off efficiency enhancement as class B. Fig. 8 (b) and (c) show the shorted circuit time domain current and load-line under three different input power levels, which demonstrate the supply current modulation effect. It can be noted that the current modulation in Fig. 8 (b) does not correspond to a truncated current waveform like in class B operation. The simulated waveform shows full conduction angle for CB operation, thereby allowing high linearity.

B. LARGE SIGNAL PERFORMANCE COMPARISON BETWEEN FOUR OPTIMALLY DESIGNED TOPOLOGIES

Utilizing the benefit of CB device, a SCB PA cell is properly designed according to the flow in Section II. As a systematic comparison, four PA cell topologies namely, CE, CB, SCE and SCB are simulated with optimum load termination. The large signal performance in terms of gain, efficiency and linearity at 90 GHz are shown in Fig. 9 and summarized in Fig. 12. Under same quiescent current, in the SCE and SCB amplifier R_{opt} expectedly increases, in this design, to approximately 50 Ω. The increase in the output impedance increases the gain, and allows good bandwidth and low loss output matching. Due to the high gain property of CB device, under almost same load impedance, SCB demonstrates 3.6 dB higher gain than SCE, while the single CB device achieves almost same gain as SCE.

In addition, almost close to ideal 3dB saturation power enhancement is achieved from stacked PA cells (2.6 dB for SCE over CE and 2.2 dB for SCB over CB). For the CB cell, a smaller difference between P_{1dB} and P_{sat} demonstrates sharper gain compression behavior. Even though the collector efficiency from the stacked PA cells are lower, due to higher gain, the peak PAE achieved from the four candidates are in the similar range. It should be noted that the PAE simulation accounts for the output matching network loss, assuming quality factors of capacitors and inductors as 20. To compare linearity and ACLR across different average power levels, envelope simulation is done using a 500MHz bandwidth 256QAM signal. As can be seen from the figure, SCE delivers the highest linear power with −35 dBc ACLR. As an example, the spectrum and constellation of the SCE PA cell at 7 dB back off is shown in Fig. 10.

C. STABILITY COMPARISON BETWEEN FOUR TOPOLOGIES

The benefit of CB device can come at the cost of stability risks. To compare the stability for the four topologies, we show the knee frequency (where K factor equals 1) of the four PA cells ($4 \times 12\ \mu$ m transistor) as a function of bias current in Fig. 11(a). The higher knee frequency indicates that the device is not unconditionally stable across a large range of frequencies, and care needs to be taken into account to ensure that the PA does not enter the instability region. As can be seen, for CB based PA cells, the frequency beyond which the device is unconditionally stable is at a much higher frequency when compared to CE based cells across all bias levels. The stability properties of a CB device can be improved by using SCB device to enhance device reverse isolation. At 100 GHz for example, the CE, SCE and SCB based PAs are unconditionally stable at 15mA quiescent bias current, while CB PAs are only conditionally stable. The source and load stability circles are plotted for CB and SCB PA cells (Fig. 11 (b)) as the design guideline.

D. MEASUREMENT RESULTS WITH SCE AND SCB PA CELLS

Single stage SCE and SCB PA cells are fabricated and compared experimentally (Fig. 13). To ensure high gain and good stability of SCB PA cell, the base resistance and inductance of the bottom device should be minimized. Therefore, an

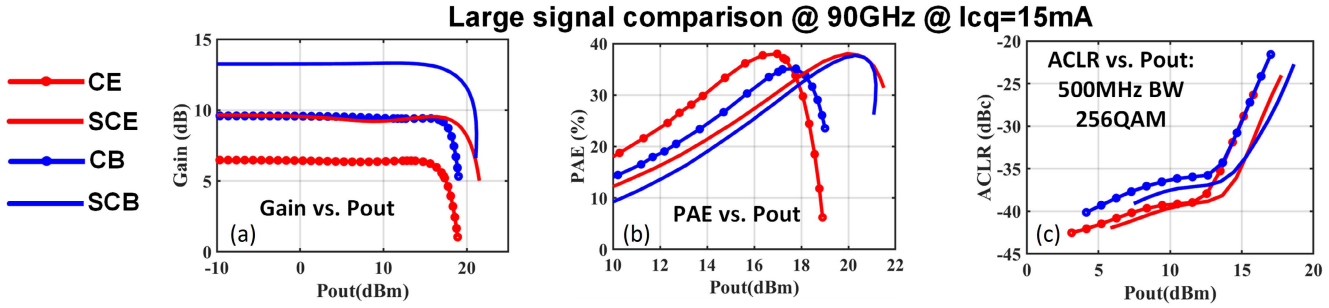


FIGURE 9. Large signal performance comparison between CE, CB, SCE and SCB at 90GHz.(a) Gain vs. power, (b) PAE, (c) Linearity (ACLR).

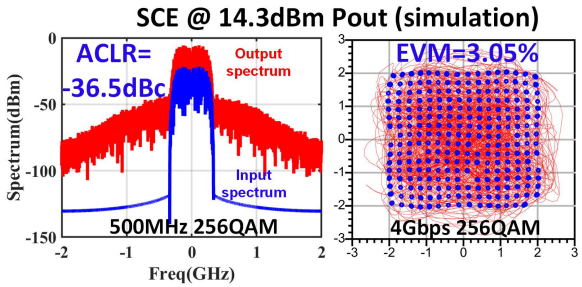


FIGURE 10. Simulated spectrum and 256 QAM constellation for SCE cell.

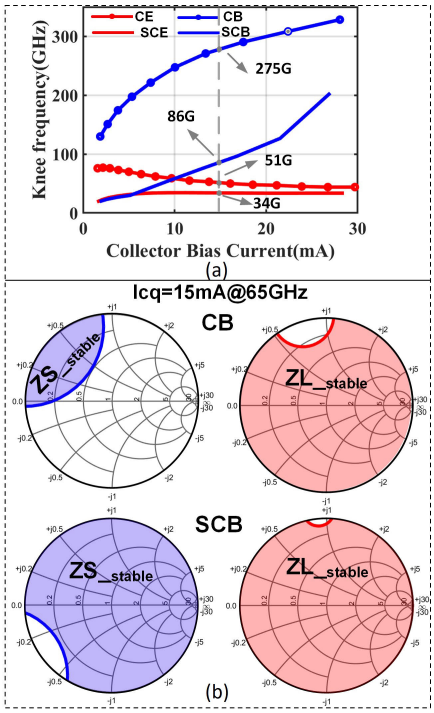


FIGURE 11. (a) Stability knee frequencies as a function of bias current. (b) Stability circles for CB and SCB at 65GHz.

on-chip bypass network is added very close to the base node (Fig. 1). The matching network loss and the voltage waveform are plotted in Fig. 13 indicating VCE of top device

Topology /Performance	CE (4x12µm)	CB (4x12µm)	SCE (2x4x12µm)	SCB (2x4x12µm)
Bias point	2.2V, 15mA	2.2V, 15mA	4.3V, 15mA	4.3V, 15mA
Optimum Z_{load} (Ω)	14.5+10j (R_{opt}=22)	14.5+10j (R_{opt}=22)	24+25j (R_{opt}=50)	24+27j (R_{opt}=54)
Gain (dB)	6.5	9.6	9.7	13.3
Psat (dBm)	18.9	18.9	21.5	21.1
P1dB (dBm)	17.2	18	19.3	19.2
Linear power (dBm) @ -35dBc ACLR w/500MHz BW 256 QAM	13.55	13.15	14.9	14.6
Peak CE (%)	54.8	41.1	46	42
Peak PAE (%)	38	36	38	37.8
Freq range for unconditional stability @ 15mA Ibias	> 51 GHz	>275 GHz	>34GHz	>86GHz

FIGURE 12. Large signal performance at 90 GHz and stability summary between four topologies.

is in-phase combined with VCB of bottom device, boosting the power of stacked CB stage over single CB stage, similar behavior as the traditional SCE device.

Fig.14 shows the measurement results of the test cells. Across 60-110 GHz, the SCB and SCE PA have a peak small signal peak S21 of 12.6 and 6.5 dB, respectively, demonstrating high gain capability for the SCB candidate. For CW measurement, at 98 GHz, the stacked CB/CE PA achieves 9.2 dB/5.3 dB gain, 31.6%/33% peak PAE, 16.3%/13.4% PAE at 6-dB back-off and P_{sat} of 18.75 dBm/20 dBm. The back-off efficiency enhancement with high gain and flat AM-AM of SCB PA validates the advantage of power-dependent supply current modulation due to current clamping effect of CB PA. The SCB PA cell delivers broadband P_{sat} of 17.9–19 dBm across 82–110 GHz and SCE delivers P_{sat} of 19–20.1 dBm across 85–105 GHz, both exhibiting good bandwidth due to the proposed intra-matching and low impedance transformation ratio at the output. High-speed modulation test is performed as shown in Fig. 14 (c). At 90 GHz LO frequency, SCB design exhibits an EVM of 2.38% at average power of 11.8 dBm with average PAE of 15.9% supporting 3 Gbps 64-QAM signal while SCE design supports 2 Gbps 16-QAM signal with EVM of 3.88% at average power of 12.9 dBm and average PAE of 14%.

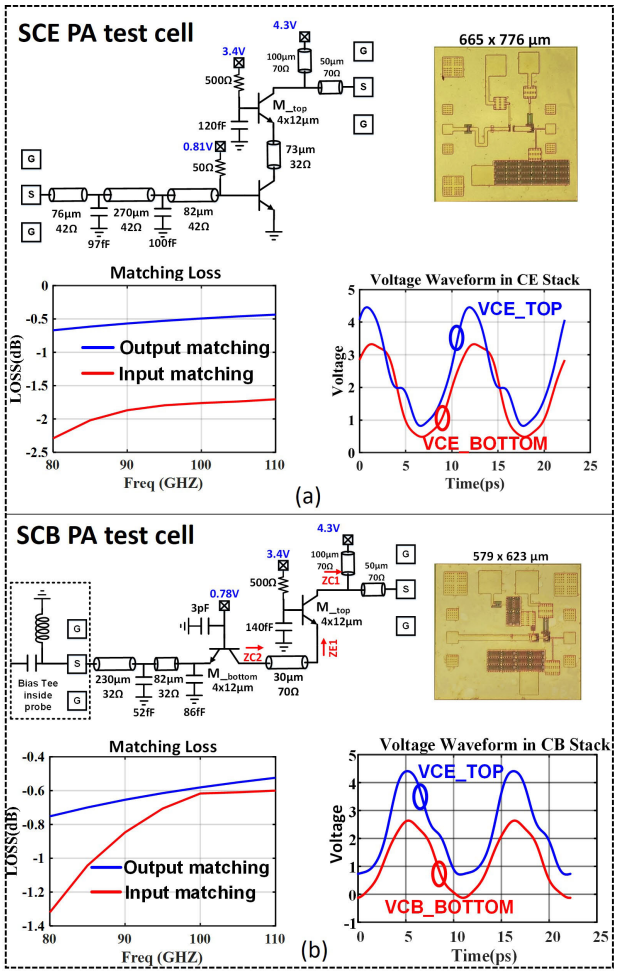


FIGURE 13. Test cell implementation (a) SCE cell. (b) SCB cell.

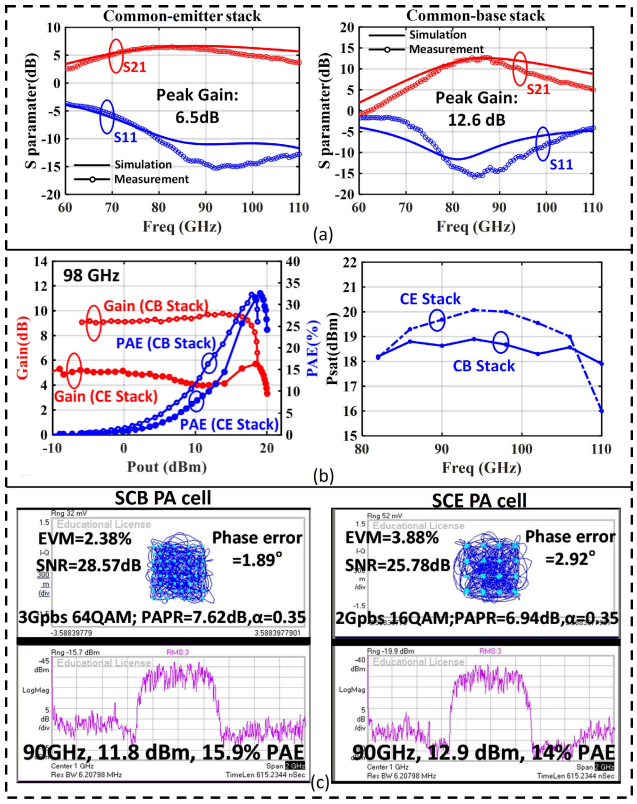


FIGURE 14. SCE and SCB test cell measurement comparison. (a) S-parameters. (b) CW performance and P_{sat} across frequency. (c) Modulation performance.

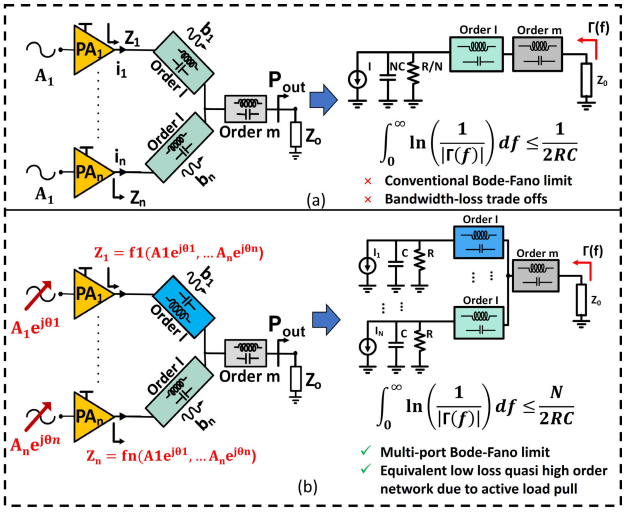


FIGURE 15. Symmetrical and asymmetrical networks for high efficiency and broadband combining. (a) Conventional in-phase power combining technique suffering from bandwidth and matching loss trade-off. (b) Asymmetrical power combining with excitations in each path for high efficiency matching across a wide bandwidth creating a quasi higher order network due to active loadpulling.

IV. BROADBAND ASYMMETRICAL POWER COMBINING BASED ON STACKED PA CELL

In this Section, we utilize the stacked PA cells and design broadband mmWave PAs with an asymmetrical power combining architecture.

A. PRINCIPLE OF BROADBAND ASYMMETRICAL POWER COMBINING

In [35] and [36], multi-port asymmetrical networks were proposed to overcome the strict bandwidth and efficiency trade-offs. The fundamental principle is captured in Fig. 15. In a symmetrical combiner, all the combining PA cells combine in phase with symmetry, resulting in the network collapsing to a two port network limited by the classical Bode-Fano limit. Higher power necessitates higher number of combining stages, requiring a larger impedance transformation ratio and higher losses [37], [38], [39], [40]. In comparison, consider the case where we break the symmetry with an array of PA cells operating with phase offsets that combining in a specially designed asymmetrical combiner, such that they combine in phase only at the output load. In such a case, due to the asymmetrical nature of the topology with amplitude and phase offsets, the network does not collapse to

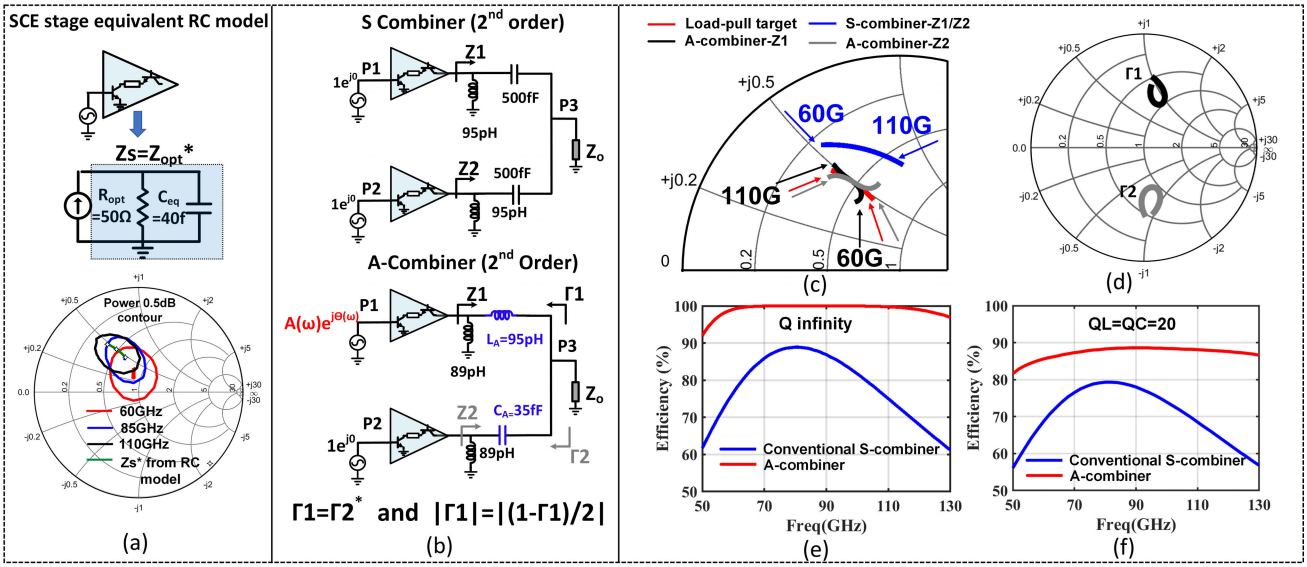


FIGURE 16. Comparison of symmetrical and asymmetrically combined broadband mmWave PAs in InP. (a) SCE stage modeling using RC network for network analysis. (b) S-combiner and A-combiner design. (c) Load impedance seen by the two PAs for S-combiner and A-combiner, exhibiting the broader bandwidth for A-combiner. (d) Simulation of $\Gamma 1(\omega)$ and $\Gamma 2(\omega)$. (e) Power combining efficiency η for lossless component. (f) Power combining efficiency η with QC=QL=20 for passive component.

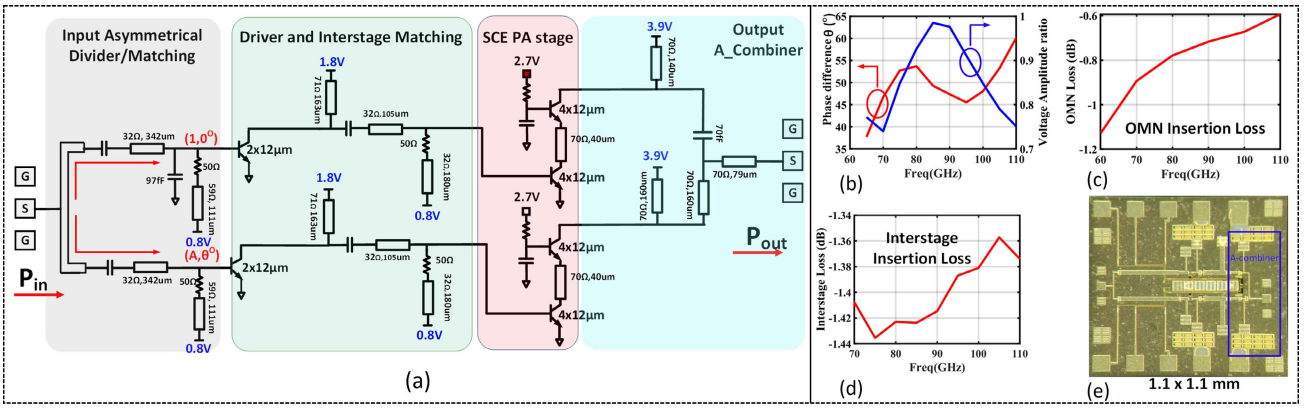


FIGURE 17. PA with an asymmetrical 2port combiner and SCE cells. (a) 2-stage SCE PA cell based asymmetrical power combining PA schematic. (b) Input amplitude ratio and phase difference response versus frequency. (c) Output combiner insertion loss across 60-110 GHz. (d) Inter-stage insertion loss across 60-110 GHz. (e) Chip micrograph.

a two-port network. Instead, the bandwidth limitations of a N way A-combiner are related to the bound of a multi-port system and the bound is improved compared to the conventional two-port bound of S-combiner [41]. In reality, a N-port asymmetrical network behaves like a quasi-Nth order filter, allowing simultaneously high power and high bandwidth typologies [36]. The PAs synthesize their broadband optimal load-pull impedance across the frequency range through controlled mutual active load-pulling by the non-isolated asymmetrical combiner.

As an example, a two-way symmetrical combiner (S-combiner) and an asymmetrical combiner (A-combiner) for a two-way combined PA is designed at 85 GHz with the SCE PA cells, as shown in Fig. 16 (b). The port 1 and 2 of the 3 port combiner are driven by the proper designed stacked PA cell from Section III, where each stacked PA can be modeled as a RC network (R=50 Ω, C=40 fF) whose impedance Zs is the conjugate of its load-pull impedance at center frequency (Fig. 16 (a)). As shown in the smith chart, this linear RC modeling of the PA cell tracks the real non-linear load-pull contours well across the 60-110 GHz frequency and therefore, can be used to perform linear network analysis. While there are many possible solutions to the asymmetrical combiner, in this example, we follow the conjugate nature of the combiner as presented in [36], where

$$\Gamma 1(\omega_0) = \Gamma 2^*(\omega_0)$$
$$|\Gamma 1(\omega_0)| = |(1 - \Gamma 1(\omega_0))/2| \quad (11)$$

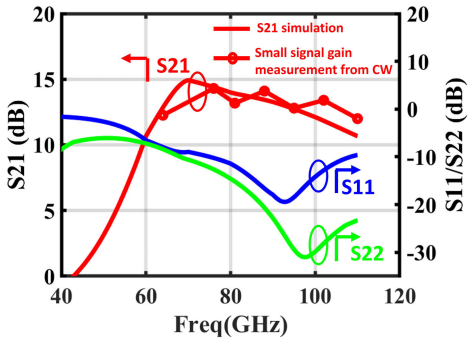


FIGURE 18. S-parameters performance.

where Γ_1 and Γ_2 are the reflection coefficient looking back to P1 and P2 path from the combining load (Fig. 16 (b)), and ω_0 is the center frequency. To start the asymmetrical combiner design with second order matching network on each path, we first choose the shunt inductance value (89 pH) to resonate out the output capacitance at center frequency 85 GHz. Then following (11), a series inductor and capacitor are added to the two paths, such that L and C resonate at center frequency (95 pH and 35 fF) guaranteeing (11). When properly excited at the optimal phases (generated in the asymmetrical input network), the A-network achieves a much wider and higher efficiency operation due to their nature of actively synthesizing optimal impedance across frequency. The simulation results of this asymmetrical combiner under optimum excitation are shown in Fig.16 (c)-(f). For lossless matching component, the load impedance Z1 and Z2 seen by the two stacked PAs are very close to each other (exactly equal at center frequency and slightly separate apart at band edge) and also align with the desired load-pull contours across 60-100 GHz, indicating a wideband matching, compared to a narrow band and inaccurately matched contour from S-combiner (Fig. 16 (c)). Plot of $\Gamma 1$ and $\Gamma 2$ in smith chart (Fig. 16 (d)) shows a conjugate location at center frequency and holds roughly true across 60-100 GHz, as expected from equation (11). As can be seen in Fig.16(e)-(f), the A-combiner achieves much wider bandwidth at higher efficiency for both lossless and lossy passive components due to their ability to synthesize quasi-higher order networks (as a result of the lack of symmetry) that allows it to synthesize optimal impedances across frequency through mutual loadpulling through the combiner network. Fig.16(g) shows the desired phase ($\theta(\omega)$) and amplitude (A(ω)) response for the A-combiner.

B. DESIGN OF BROADBAND ASYMMETRICAL POWER COMBINING PA IN InP

Following the design principles laid out, we design a broadband two stage asymmetrical power combining PA using SCE PA cell as the output stage in 250 nm InP HBT technology. The lumped inductor components are implemented using high impedance transmission lines. The complete schematic is shown in Fig. 17 (a). The driver is CE topology sized $2 \times 12\ \mu$m in upper and lower branches. Inter-stage matching is achieved using transmission lines and capacitors optimized for broadband operation. The input power dividing network needs to ensure broadband input matching while synthesizing the desired driving phases difference across frequency as shown in Fig. 17 (b). The output A-combiner achieves an insertion loss of 0.6-1.1 dB across 60-110 GHz (Fig. 17 (c)). The insertion loss of the transmission line based inter-stage matching is better than 1.5 dB over 64-110 GHz. The simulated S-parameters are shown in Fig. 18, where both input and output matching matching is broadband with reflection coefficient below -10 dB across the 60-110 GHz.

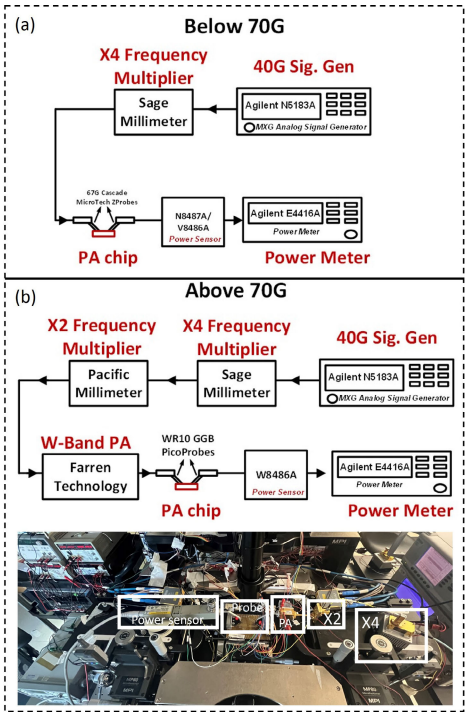


FIGURE 19. Setup for the CW large signal measurement (a) Below 70 GHz. (b) Above 70 GHz.

C. MEASUREMENT RESULTS

The PA micrograph is shown in Fig.17 (e) which occupies 1.1mm $\times$ 1.1mm chip area. The main stage PA cells operate from 3.9 V supply, while the driver cells operate from 1.8 V supply. The measured small signal gain across frequency is plotted in Fig. 18 showing broadband output matching. The PA is characterized for large signal measurement across 60–110 GHz using the measurement setup shown in Fig. 19. For CW measurements, the input chain includes signal generator and frequency quadrupler. For frequency above 70 GHz, a frequency doubler and a W band commercial PA are also added to drive the DUT.

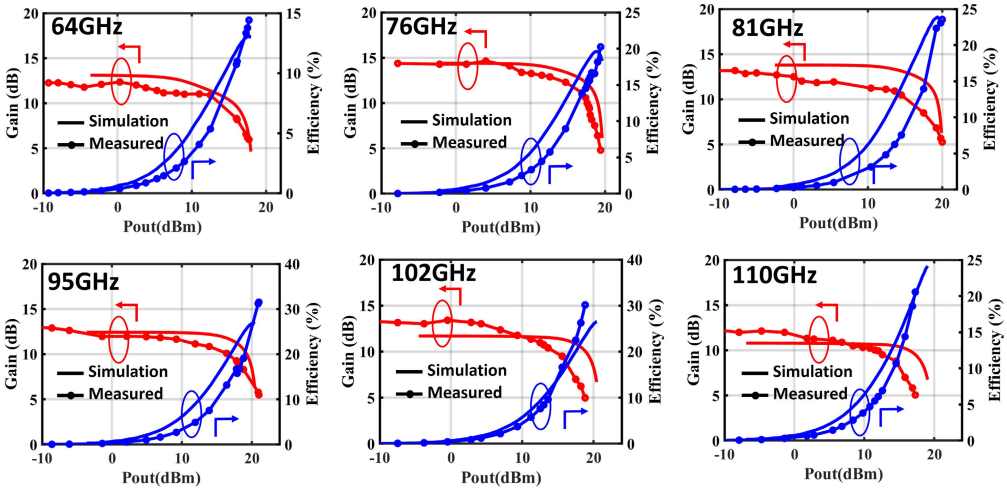


FIGURE 20. CW large-signal measurement across 64-110 GHz.

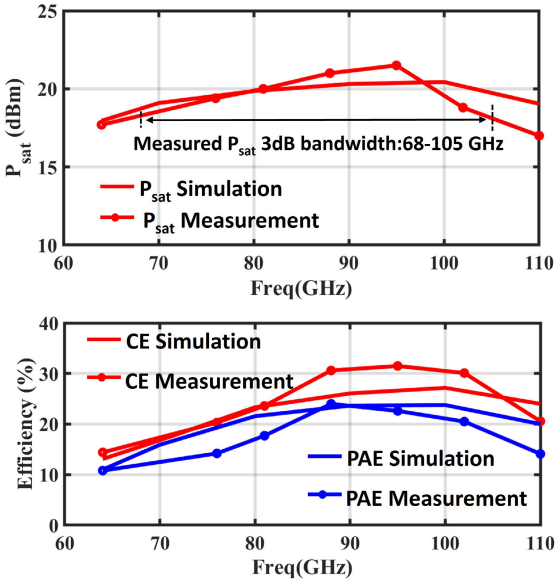


FIGURE 21. Measurement and simulated large signal performance across frequency. (a) Saturation power. (b) Total collector efficiency and PAE.

Ref	Technology	PA Topology	Freq (GHz)	Fractional BW (%)	Psat (dBm)	Peak PAE (%)	Peak S21 (dB)
Huang IMS 21'	250nm InP	Coupler differential	35-100	96.3	18.9-22.6	14.7-29.3	16.5@ 60GHz
Griffith MWCL 20'	250nm InP	T-line combining	88-104	16.7	20-20.8	14-24.7	28@ 88GHz
Liu MWCL 21'	250nm InP	Stack single ended	85-110	21.1	19-20.1	15-34	6.5 @ 82GHz
Griffith IMS 19'	250nm InP	T-line combining	55-135	84.2	19.6-21.4	6.2-8.8	27.3@ 90GHz
Nguyen TMTT 20'	InP HBT	Distributed amplifier	DC-90	NA	18-22	20@ 20GHz	10.5@ 15GHz
Griffith IMS 16'	250nm InP	Single ended CE	96-120	22.2	19.3-20.2	19-22	18@ 110GHz
Maurer CSICS 16'	130nm InP	Series combining	50-100	66	17-22	7-14.7	15.5@ 60GHz
Griffith CSICS 14'	250nm InP	Wilkinson combining	76-94	21.2	22.3-23.7	21-29	15 @ 70GHz
This work	**250nm InP**	**SCB PA cell**	**82-110**	**29.2**	**17.9-19**	**20-33**	**12.6@ 87GHz**
This work	**250nm InP**	**SCE PA cell**	**82-105**	**24.6**	**18-20**	**16-35**	**6.5@ 82GHz**
This work	**250nm InP**	**Asymmetry combining**	**68-105**	**43**	**18.5-21.5**	**13-24**	**14 @ 76GHz**

FIGURE 22. Comparison with state of the art broadband mmWave PA in InP.

The measured gain and total collector efficiency (Accounting both PA stage and driver stage) are plotted against output power across 64-110 GHz, as shown in Fig. 20. At 95 GHz, the PA delivers an output power of 21.4 dBm with peak total collector efficiency of 32%, and 13 dB small signal gain. The PA achieves 18.5-21.5 dBm P_{sat} over 64-108 GHz (3dB P_{sat} bandwidth of 43%). Across the above bandwidth, the PA demonstrates a total collector efficiency between 16-32% with a peak efficiency achieved at 95 GHz and a PAE between 11-24% with peak at 88 GHz. Fig. 21 summarizes the measurement CW performance across frequency, overlap with simulation results. Fig. 22 presents the comparison with state of the art broadband mmWave PA in InP covering W band.

V. CONCLUSION

This paper presents a comparative approach toward high efficiency mmWave PAs using stacked common emitter and stacked common base PAs. We present an analytical approach to guaranteeing optimal stack operation at high mmWave frequencies with SCB cells taking into consideration intra-stack matching and optimal loadpull operation of the bottom transistor and the top transistor. The analytical approach is valid for SCE cells as well. We present a systematic comparison between conventional single device PA cells and optimally designed stacked PA cells: SCE and proposed SCB PA cell, showing that SCB cell allows high gain, sharp gain compression but needs careful analysis

of stability. At 90 GHz, the designed stacked CB/CE PA achieves 11.8 dB/6dB gain, 33%/34% peak PAE, 16.8%/14.5% PAE at 6-dB back-off, and P_{sat} of 18.7 dBm/ 19.6 dBm. The SCB PA achieves an EVM of 2.38% at 11.8-dBm average power supporting 3 Gbps 64-QAM. The SCB PA with 17.9-19 dBm P_{sat} across 82-110 GHz demonstrates one of the highest efficiency, broadband and linear PAs in W-band using InP technology. We utilize an asymmetrical power combining circuit topology for high combining efficiency across large relatively bandwidth. A 68-105 GHz asymmetrical power combined PA using SCE cell in 250nm InP technology is demonstrated showing 21.5 dBm peak saturation power and 24% peak PAE.

ACKNOWLEDGMENT

The authors would like to acknowledge fabrication support from Teledyne, and thanks to Dr. Tim Hancock, DARPA, and IMRL's Laboratory members for technical discussions and support.

REFERENCES

[1] M. Urteaga, Z. Griffith, M. Seo, J. Hacker, and M. J. W. Rodwell, "InP HBT technologies for THz integrated circuits," *Proc. IEEE*, vol. 105, no. 6, pp. 1051–1067, Jun. 2017.

[2] T.-Y. Huang, S. Li, N. S. Mannem, and H. Wang, "A 35–100 GHz continuous mode coupler balun Doherty power amplifier with differential complex neutralization in 250 nm InP," in *IEEE MTT-S Int. Microw. Symp. Dig.*, Jun. 2021, pp. 374–377.

[3] Z. Griffith, M. Urteaga, and P. Rowell, "A W-band SSPA with 100–140-mW P_{out}, >20% PAE, and 26–30-dB S_{21} gain across 88–104 GHz," *IEEE Microw. Wireless Compon. Lett.*, vol. 30, no. 2, pp. 189–192, Feb. 2020.

[4] Z. Griffith, M. Urteaga, P. Rowell, and R. Pierson, "71–95 GHz (23–40% PAE) and 96–120 GHz (19–22% PAE) high efficiency 100–130 mW power amplifiers in InP HBT," in *IEEE MTT-S Int. Microw. Symp. Dig.*, May 2016, pp. 1–4.

[5] Z. Griffith, M. Urteaga, and P. Rowell, "A 140-GHz 0.25-W PA and a 55–135 GHz 115–135 mW PA, high-gain, broadband power amplifier MMICs in 250-nm InP HBT," in *IEEE MTT-S Int. Microw. Symp. Dig.*, Jun. 2019, pp. 1245–1248.

[6] A. S. Ahmed, M. Seo, A. A. Farid, M. Urteaga, J. F. Buckwalter, and M. J. Rodwell, "A 200 mw D-band power amplifier with 17.8% PAE in 250-nm InP HBT technology," in *Proc. 15th Eur. Microw. Integr. Circuits Conf. (EuMIC)*, 2021, pp. 1–4.

[7] H.-T. Dabag, B. Hanafi, F. Golcuk, A. Agah, J. F. Buckwalter, and P. M. Asbeck, "Analysis and design of stacked-FET millimeter-wave power amplifiers," *IEEE Trans. Microw. Theory Techn.*, vol. 61, no. 4, pp. 1543–1556, Apr. 2013.

[8] D. P. Nguyen, N. L. K. Nguyen, A. N. Stameroff, V. Camarchia, M. Pirola, and A.-V. Pham, "A wideband highly linear distributed amplifier using intermodulation cancellation technique for stacked-HBT cell," *IEEE Trans. Microw. Theory Techn.*, vol. 68, no. 7, pp. 2984–2997, Jul. 2020.

[9] D. Fritsche, R. Wolf, and F. Ellinger, "Analysis and design of a stacked power amplifier with very high bandwidth," *IEEE Trans. Microw. Theory Techn.*, vol. 60, no. 10, pp. 3223–3231, Oct. 2012.

[10] Y. Kim and Y. Kwon, "Analysis and design of millimeter-wave power amplifier using stacked-FET structure," *IEEE Trans. Microw. Theory Techn.*, vol. 63, no. 2, pp. 691–702, Feb. 2015.

[11] S. M. A. Ali and S. M. R. Hasan, "A 38-GHz millimeter-wave double-stacked HBT class-F^{-1} high-gain power amplifier in 130-nm SiGe-BiCMOS," *IEEE Trans. Microw. Theory Techn.*, vol. 68, no. 7, pp. 3039–3044, Jul. 2020.

[12] K. Datta and H. Hashemi, "Performance limits, design and implementation of mm-wave SiGe HBT class-E and stacked class-E power amplifiers," *IEEE J. Solid-State Circuits*, vol. 49, no. 10, pp. 2150–2171, Oct. 2014.

[13] A. Chakrabarti and H. Krishnaswamy, "High-power high-efficiency class-E-like stacked mmWave PAs in SOI and bulk CMOS: Theory and implementation," *IEEE Trans. Microw. Theory Techn.*, vol. 62, no. 8, pp. 1686–1704, Aug. 2014.

[14] T. Sharma, Z. Liu, C. R. Chappidi, H. Saeidi, S. Venkatesh, and K. Sengupta, "Broadband PA architectures with asymmetrical combining and stacked PA cells across 50–70 GHz and 64–110 GHz in 250 nm InP," in *IEEE MTT-S Int. Microw. Symp. Dig.*, Aug. 2020, pp. 405–408.

[15] Z. Liu and K. Sengupta, "A 44–64-GHz mmWave broadband linear Doherty PA in silicon with quadrature hybrid combiner and non-foster impedance tuner," *IEEE J. Solid-State Circuits*, vol. 57, no. 8, pp. 2320–2335, Aug. 2022.

[16] Z. Liu, E. A. Karahan, and K. Sengupta, "A compact SiGe stacked common-base dual-band PA with 20/18.8 dBm P_{sat} at 36/64 GHz supporting concurrent modulation," *IEEE Microw. Wireless Compon. Lett.*, vol. 32, no. 6, pp. 720–723, Jun. 2022.

[17] C. R. Chappidi and K. Sengupta, "Globally optimal matching networks with lossy passives and efficiency bounds," *IEEE Trans. Circuits Syst. I, Reg. Papers*, vol. 65, no. 1, pp. 257–269, Jan. 2018.

[18] S. E. Sussman-Fort and R. M. Rudish, "Non-foster impedance matching of electrically-small antennas," *IEEE Trans. Antennas Propag.*, vol. 57, no. 8, pp. 2230–2241, Aug. 2009.

[19] S. Lee, H. Park, K. Choi, and Y. Kwon, "A broadband GaN pHEMT power amplifier using non-foster matching," *IEEE Trans. Microw. Theory Techn.*, vol. 63, no. 12, pp. 4406–4414, Dec. 2015.

[20] Z. Liu, Y. Yu, and K. Sengupta, "A 44 to 64 GHz broadband 90° hybrid Doherty PA with quasi non-foster tuner in 0.13 μm SiGe," *IEEE Microw. Wireless Compon. Lett.*, vol. 31, no. 6, pp. 760–763, Jun. 2021.

[21] S. D. Stearns, "Circuit stability theory for non-foster circuits," in *IEEE MTT-S Int. Microw. Symp. Dig.*, Jun. 2013, pp. 1–3.

[22] S. N. Ali, P. Agarwal, L. Renaud, R. Molavi, S. Mirabbasi, P. P. Pande, and D. Heo, "A 40% PAE frequency-reconfigurable CMOS power amplifier with tunable gate–drain neutralization for 28-GHz 5G radios," *IEEE Trans. Microw. Theory Techn.*, vol. 66, no. 5, pp. 2231–2245, May 2018.

[23] U. Kim, S. Kang, J. Woo, Y. Kwon, and J. Kim, "A multiband reconfigurable power amplifier for UMTS handset applications," *IEEE Trans. Microw. Theory Techn.*, vol. 60, no. 8, pp. 2532–2542, Aug. 2012.

[24] D. J. Shepphard, J. Powell, and S. C. Cripps, "A broadband reconfigurable load modulated balanced amplifier (LMBA)," in *IEEE MTT-S Int. Microw. Symp. Dig.*, Jun. 2017, pp. 947–949.

[25] C. R. Chappidi, T. Sharma, Z. Liu, and K. Sengupta, "Load modulated balanced mm-wave CMOS PA with integrated linearity enhancement for 5G applications," in *IEEE MTT-S Int. Microw. Symp. Dig.*, Aug. 2020, pp. 1101–1104.

[26] C. R. Chappidi and K. Sengupta, "Frequency reconfigurable mm-wave power amplifier with active impedance synthesis in an asymmetrical non-isolated combiner: Analysis and design," *IEEE J. Solid-State Circuits*, vol. 52, no. 8, pp. 1990–2008, Aug. 2017.

[27] T. Yao, M. Q. Gordon, K. K. W. Tang, K. H. K. Yau, M.-T. Yang, P. Schvan, and S. P. Voinigescu, "Algorithmic design of CMOS LNAs and PAs for 60-GHz radio," *IEEE J. Solid-State Circuits*, vol. 42, no. 5, pp. 1044–1057, May 2007.

[28] Z. Liu, T. Sharma, and K. Sengupta, "80–110-GHz broadband linear PA with 33% peak PAE and comparison of stacked common base and common emitter PA in InP," *IEEE Microw. Wireless Compon. Lett.*, vol. 31, no. 6, pp. 756–759, Jun. 2021.

[29] Z. Liu, "A 42–62 GHz transformer-based broadband mm-wave InP PA with second-harmonic waveform engineering and enhanced linearity," *IEEE Trans. Microw. Theory Techn.*, vol. 69, no. 1, pp. 756–773, Jan. 2021.

[30] Z. Ma and N. Jiang, "On the operation configuration of SiGe HBTs based on power gain analysis," *IEEE Trans. Electron Devices*, vol. 52, no. 2, pp. 248–255, Feb. 2005.

[31] I. Petricli, D. Riccardi, and A. Mazzanti, "D-band SiGe BiCMOS power amplifier with 16.8 dBm P_1 dB and 17.1% PAE enhanced by current-clamping in multiple common-base stages," *IEEE Microw. Wireless Compon. Lett.*, vol. 31, no. 3, pp. 288–291, Mar. 2021.

[32] N. Rinaldi and V. d'Alessandro, "Theory of electrothermal behavior of bipolar transistors: Part I -single-finger devices," *IEEE Trans. Electron Devices*, vol. 52, no. 9, pp. 2009–2021, Sep. 2005.

[33] J. C. Pedro, L. C. Nunes, and P. M. Cabral, "A simple method to estimate the output power and efficiency load–pull contours of class-B power amplifiers," *IEEE Trans. Microw. Theory Techn.*, vol. 63, no. 4, pp. 1239–1249, Apr. 2015.

[34] E. Rahimi, J. Zhao, F. Svelto, and A. Mazzanti, "High-efficiency SiGe-BiCMOS *E*-band power amplifiers exploiting current clamping in the common-base stage," *IEEE J. Solid-State Circuits*, vol. 54, no. 8, pp. 2175–2185, Aug. 2019.

[35] C. R. Chappidi, X. Wu, and K. Sengupta, "Simultaneously broadband and back-off efficient mm-wave PAs: A multi-port network synthesis approach," *IEEE J. Solid-State Circuits*, vol. 53, no. 9, pp. 2543–2559, Jun. 2018.

[36] C. R. Chappidi, T. Sharma, and K. Sengupta, "Multi-port active load pulling for mm-wave 5G power amplifiers: Bandwidth, back-off efficiency, and VSWR tolerance," *IEEE Trans. Microw. Theory Techn.*, vol. 68, no. 7, pp. 2998–3016, Jul. 2020.

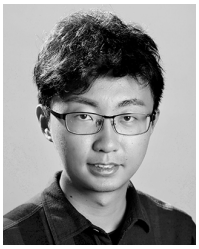
[37] K. Chen and D. Peroulis, "Design of highly efficient broadband class-E power amplifier using synthesized low-pass matching networks," *IEEE Trans. Microw. Theory Techn.*, vol. 59, no. 12, pp. 3162–3173, Dec. 2011.

[38] X.-L. Huang, L. Zhou, Y. Yuan, L.-F. Qiu, and J.-F. Mao, "Quintuple-mode W-band packaged filter based on a modified quarter-mode substrate-integrated waveguide cavity," *IEEE Trans. Compon., Packag., Manuf. Technol.*, vol. 9, no. 11, pp. 2237–2247, Nov. 2019.

[39] M. Vigilante and P. Reynaert, "On the design of wideband transformer-based fourth order matching networks for *E*-band receivers in 28-nm CMOS," *IEEE J. Solid-State Circuits*, vol. 52, no. 8, pp. 2071–2082, Aug. 2017.

[40] X.-L. Huang, L. Zhou, M. Völkel, A. Hagelauer, J.-F. Mao, and R. Weigel, "Design of a novel quarter-mode substrate-integrated waveguide filter with multiple transmission zeros and higher mode suppressions," *IEEE Trans. Microw. Theory Techn.*, vol. 66, no. 12, pp. 5573–5584, Dec. 2018.

[41] D. Nie and B. M. Hochwald, "Broadband matching bounds for coupled loads," *IEEE Trans. Circuits Syst. I, Reg. Papers*, vol. 62, no. 4, pp. 995–1004, Apr. 2015.



ZHENG LIU (Graduate Student Member, IEEE) received the B.S. degree in electronics from Peking University, Beijing, China. He is currently pursuing the Ph.D. degree with Princeton University, NJ, USA. From 2015 to 2018, he was a Design Engineer at Skyworks Solutions Inc., Newbury Park, CA, USA, where he worked on RF front-end module. His research interests include mm-wave broadband power amplifiers and transmitter architectures, mm-wave phased array systems, and sub-THz/THz power generation and detection. He was a recipient of the Advanced Practice Paper Award in IEEE International Microwave Symposium (IMS) 2022, the MTT-s Graduate Fellowship Award in 2021, the Analog Devices Outstanding Student Designer Award in 2021, and the Yan Huo'94 Fellowship from Princeton University in 2020. He was a co-recipient of the IEEE IMS Best Student Paper Award (second place in 2020 and third place in 2021).

TUSHAR SHARMA (Member, IEEE) received the Ph.D. degree in electrical engineering from the University of Calgary, Canada, in 2018. He has completed a Postdoctoral Research at the Integrated Micro-Systems Research Laboratory, Princeton University, NJ, USA. He is currently a Country Head of the Renesas-TCS Joint Innovation Center and a Visiting Professor at the Indian Institute of Technology, Bombay, India. He joined as an Institute Adjunct Faculty at the Indian Institute of Sciences (IISc), Bengaluru, in 2021. He has more than 50 publications in international journals and conferences along with four granted patents. His research interests include high frequency novel reconfigurable techniques in RF and mm-wave transmitters, broadband high-power gallium nitride (GaN) power amplifiers, large signal device modeling, technology characterization, digital signal processing, mm-Wave amplifiers, and waveform engineering. He was a Youngest Elected Member on IEEE Microwave Theory and Techniques Society (MTTS) adcom. He was a recipient of the IMS 2020 Best Industry Paper Award, the 2019/2020 IMS Best Student paper Award, the Izaak Walton Killam Pre-doctoral Scholarship, the Alberta Science and Innovation under 30 Future Leader Award, the Alberta Innovates Technology Future Doctoral Scholarship, the Alberta Transformative Talent Scholarship, the IEEE Education Activity Board Pre-Educator Award, the IEEE MGA Young Professionals Achievement Award, and the University of Calgary 2018 Early Achievement Alumni Award.

KAUSHIK SENGUPTA (Senior Member, IEEE) received the B.Tech. and M.Tech. degrees in electronics and electrical communication engineering from the Indian Institute of Technology Kharagpur, Kharagpur, India, in 2007, and the M.S. and Ph.D. degrees in electrical engineering from the California Institute of Technology (Caltech), Pasadena, CA, USA, in 2008 and 2012, respectively. He performed research with the University of Southern California, Los Angeles, CA, and the Massachusetts Institute of Technology, Cambridge, MA, USA, in 2005 and 2006, respectively, where he was involved in nonlinear integrated systems for high-purity signal generation and low-power RF identification tags. He joined the Department of Electrical Engineering, Princeton University, Princeton, NJ, USA, as a Faculty Member, in 2013, where he is currently an Associate Professor and the Director of Graduate Studies. His current research interests include high-frequency ICs, electromagnetics, optics for various applications in sensing, imaging, and high-speed communication.

He is a member of the MTT-4 Committee on Terahertz Technology. He received the DARPA Young Faculty Award in 2018, the Bell Labs Prize in 2017, the Young Investigator Program Award from the Office of Naval Research in 2017, the E. Lawrence Keys, Jr. Emerson Electric Co. Junior Faculty Award from the Princeton School of Engineering and Applied Science in 2018, and the Excellence in Teaching Award in 2018 nominated by the Undergraduate and Graduate Student Council in the Princeton School of Engineering and Applied Science. He was a recipient of the Charles Wilts Prize in 2013 from Electrical Engineering, Caltech, for the best Ph.D. thesis, the Caltech Institute Fellowship, the Prime Minister Gold Medal Award of IIT in 2007, and the Inaugural Young Alumni Achievement Award from IIT Kharagpur. He was a co-recipient of the IEEE RFIC Symposium Best Student Paper Award in 2012, the multiple Best Student Paper Awards in IEEE IMS, and the 2015 Microwave Prize from the IEEE Microwave Theory and Techniques Society. He was a recipient of the Outstanding Young Engineer Award from IEEE Microwave Theory and Techniques in 2021. He serves as the Chair for Emerging Technologies for IEEE Custom Integrated Circuits Conference (CICC) and in the Steering Committee of the IEEE International Microwave Symposium. He served as a Distinguished Lecturer for the IEEE Solid-State Circuits Society, from 2019 to 2020. He is currently serving as a Distinguished Lecturer for the IEEE Microwave Theory and Techniques.