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TOPICAL REVIEW

Recent Developments in Negative Capacitance Gate-All-Around Field Effect Transistors: A Review

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ABSTRACT With transistors scaling down to 3 nm node and beyond, short channel effect (SCE) as well as power consumption dissipation present immense challenges for further scaling down of the transistor. Hence the Gate all around field effect transistor (GAA-FET) is proposed to replace the Fin field effect transistor (FinFET) in 3 nm technology node and beyond due to its better gate control over the channel with surrounding gate structure, thus providing improved SCE constraint ability. Traditional transistors suffer from the problems of ''Boltzmann Tyranny'' and cannot overcome the subthreshold swing (SS) limit of 60 mV/dec at room temperature. To maintain high I_{on} and avoid I_{off} from increasing too much, supply voltage (V_{DD}) of the conventional transistor cannot scale down proportionally with the dimension of the transistor. The concept of negative capacitance (NC) has been demonstrated to be able to obtain sub-60 mV/dec SS with the ability of amplifying the potential of the channel region without V_{DD} increment. The novel device structure of negative capacitance gate all around field effect transistor(NC GAA-FET) can combine both the advantages of GAA-FET and NC-FET, and is the most promising ultra-low power consumption device and promises to sustain the Moore's law further beyond what is predicted now. Whereas, according to our knowledge, there have been few review papers about NC GAA-FET till now. Herein, we summarize the recent developments of the NC GAA-FET both in simulation and experimental aspects, which we believe will bring about profound changes to the further development of NC GAA-FET devices.

INDEX TERMS Negative capacitance effect, short channel effect, subthreshold swing, power consumption dissipation, negative capacitance gate all around field effect transistor.

I. INTRODUCTION

Since Moore's law was proposed in 1965, the number of transistors on a chip doubles every two years [1]. The speed increase, power consumption and cost reduction are main motivations for transistor's further scaling down, which also bring about tremendous conveniences and a life full of varieties [2]. However, Moore's law meets challenges nowadays, which come from SCE degradation and power consumption increment. SCE is always a big obstacle when transistors scale down beyond 100 nm node. Specifically, drain induced barrier lower (DIBL) [3] and subthreshold swing (SS) [4] are two main SCE factors that degrade device performance seriously. The voltage applied on the drain side (V_d) affects the barrier height between source and drain, thus stealing the privilege of gate control over the channel region, this effect is termed as DIBL. DIBL effect affects the controlling ability of the gate over the channel, leading to threshold voltage (V_{th}) reduction and off state current (I_{off}) increment. SS signifies the switch down ability of the transistor, and it is defined

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as the minimum gate voltage (V_g) needed to increase drain current (I_d) by one order. SS degradation caused by channel length decreasing leads to I_{off} increasing. Besides, punch through caused by source and drain junction connecting with each other contributes to leakage current increase; hot carrier injection effect causes irreversible damage to the dielectric layer; surface scattering degrades carrier mobility; velocity saturation affects I_{on} increase. Fortunately, according to the published work [5], SCE of a transistor can be inhibited if the channel length is 3 to 5 times larger than the screening length, λ. λ is defined as,

$$\lambda = \sqrt{\frac{\varepsilon_s}{N\varepsilon_{ox}} \cdot t_s \cdot t_{ox}} \tag{1}$$

ε_s and ε_{ox} are permittivities of channel material and dielectric oxide respectively, t_s and t_{ox} are channel and oxide thickness, N is the number of gates. The screening length, λ, describes the distance over which the potential drops at the interfaces between the source and channel and from the channel to drain. To decrease λ, high k dielectric such as HfO_2 or Al_2O_3 [6], [7] is chosen instead of SiO_2 to increase ε_{ox}. On the other hand, oxide and channel thickness (t_{ox} and t_s) also decrease proportionally with channel length scaling down, which both increases the gate control over the channel and degrades the carrier mobility due to surface scattering. Increasing gate numbers can also decrease λ according to (1), and that is why FinFET with three sides of the channel surrounded by the gates performs better than planar FET in regards to suppressing SCE [8]. Recently, GAA-FET has been predicted to replace FinFET and dominate the semiconductor market for 3 nm technology node and beyond, since GAA-FET has better gate control and stronger SCE suppression ability than FinFET attributing to its surrounding gate structure [9].

Although GAA-FET has verified its superiority as a promising alternative in suppressing SCE, the power consumption increase still cannot be neglected, especially as static power consumption increases exponentially with transistor length scaling down, exceeding dynamic power consumption nowadays [10]. As is known, the power consumption of a transistor consists of two parts, static power consumption and dynamic power consumption, which is expressed as below,

$$P = P_{static} + P_{dynamic} = I_{off} \cdot V_{DD} + C \cdot f \cdot V_{DD}^2 \tag{2}$$

P_{static} and $P_{dynamic}$ refer to static and dynamic power consumption respectively, I_{off} denotes off state current and can be obtained by measuring I_d at V_g =0 and $V_d = V_{DD}$. C is the total capacitance of the transistor and f is the frequency. According to (2), to decrease static and dynamic power consumption simultaneously, the most effective method is reducing V_{DD}. However, from 10 nm technology node and beyond, conventional transistors suffer from the problem that V_{DD} is not able to scale down proportionally with dimension due to ''Boltzmann tyranny'' (SS cannot be smaller than 60 mV/dec at room temperature). At room temperature, SS is expressed as,

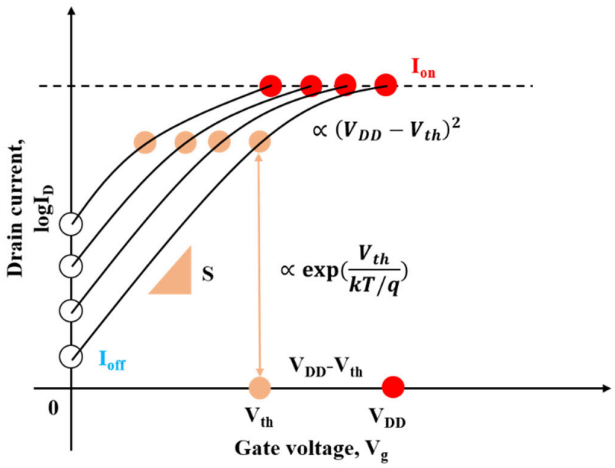

FIGURE 1. The I_d-V_g curves for conventional transistor with gate length scaling down. To remain I_{on} constant as the gate length scales down, I_{off} increases exponentially if V_{DD} and V_{th} scale down proportionally with gate length due to that SS of conventional transistor is no smaller than 60 mV/dec, produced with permission from [10].

$$SS = \frac{\partial V_g}{\partial \log_{10} I_D} = \frac{\partial V_g}{\partial \psi_S} \cdot \frac{\partial \psi_S}{\partial \log_{10} I_D} = m \cdot n \tag{3}$$

ψ_s is the potential of the channel. m is defined as body factor, representing the control ability of gate over channel potential; n is the transport factor, describing the control ability of channel potential over drain current. Generally, in a conventional transistor at room temperature, m and n are expressed as,

$$m = \left(1 + \frac{C_S}{C_{OX}}\right) \tag{4}$$

$$\mathrm{n} = \frac{kt}{q} \ln 10 \approx 60mV/dec \tag{5}$$

$$SS = 60mV/dec \times \left(1 + \frac{C_S}{C_{OX}}\right) \tag{6}$$

In a conventional transistor, C_S (the equivalent capacitance of MOS) and C_{OX} (the capacitance of oxide dielectric layer) are all positive, so the minimum value of SS is 60 mV/dec at room temperature according to (6). As the transistor gate length is reduced, improved performance requires V_{DD}, and simultaneously V_{th}, to be lowered proportionally to keep I_{on} high. Thus, I_{off} increases exponentially because SS cannot be lower than 60 mV/dec caused by ''Boltzmann tyranny'', as shown in Fig. 1.

To make sure that V_{DD} and V_{th} scale proportionally with transistor dimension without causing serious I_{off} increment, steep SS devices are needed. Nowadays, tunneling field effect transistors (TFET), impact ionization transistors (I-FET), nano-electromechanical FETs (NEMFET), Dirac source FETs (DSFET) and negative capacitance FETs (NC-FET) [11], [12], [13], [14], [15] are proposed steep SS devices. They all have their merits but also face limitations. TFET can achieve sub-60 mV/dec SS due to carriers transporting

by band to band (BTBT) mechanism. However, TFET suffers from low I_{on}. Besides, the opposite doped source and drain regions not only cause asymmetric problems, but also complicate the manufacturing process; I-FET needs a high breakdown voltage, which causes stability issues. On the other hand, high breakdown voltage also collides with the purpose of scaling down V_{DD}; NEMFET needs a complicated manufacturing process, which limits its mass production. As for DSFET, it can achieve both sub-60 mV/dec SS and high I_{on} at the same time, however, the Dirac materials needed are two-dimensional (2D) materials like graphene and its counterparts. Their mass production is impractical at the moment, besides, more studies are needed to clarify the working mechanism of DSFET, so there is still a long way to go before DSFET can be produced massively. NC-FET can achieve steep SS, and at the same time, maintain the carrier transport mechanism as in conventional FET. As a result, a high I_{on} can be sustained. On the other hand, NC-FET is obtained by simply adding an additional ferroelectric layer in the gate stack, which doesn't change much of the manufacturing process of the NC-FET and makes it compatible with the modern semiconductor manufacturing process. The advantages mentioned above make NC-FET stand out as a most promising steep switch ultra-low power consumption device.

GAA-FET promises to substitute FinFET and dominate the semiconductor industry in 3 nm and beyond technology nodes due to better gate control ability provided by the surrounding gate structure. The NC GAA-FET fabricated by integrating NC effect with GAA FET structure can combine both the advantages of NC-FET and GAA-FET, and is the best-potential ultra-low power consumption device and promises to sustain the Moore's law further.

The main purpose of this article is to introduce the working mechanism and to elaborate on the current status of NC GAA-FET, which will be helpful for researchers to get the gist quickly and decide what to focus on next. The essay is organized as follows. **Part I** is the introduction part, emphasizing on the background of NC GAA-FET; **Part II** thoroughly describes the historical developments and working mechanism of the NC-FET; **Part III** detailedly covers the recent developments of NC GAA-FET both theoretically and experimentally; **Part IV** describes the opportunities and challenges faced by NC GAA-FET and gives a future outlook based on recent findings.

II. HISTORICAL DEVELOPMENT

It was S. Salahuddin and S. Datta who first proposed that by integrating NC effect in a transistor, steep switch and a SS smaller than Boltzmann limit of 60 mV/dec could be obtained [16]. Later in the same year, Giovanni A. Salvatore et al first demonstrated a NC-FET experimentally, the NC-FET achieved a minimum SS of 13 mV/dec by using a 40 nm P(VDF-TrFE)/SiO_2 gate stack [17]. From then on, NC-FET has drawn much attention from all over the world. And what is more, the emerging NC GAA-FET is promising in further scaling transistors to 3 nm and beyond technology nodes. Whereas, the early ferroelectric materials used were conventional perovskite ferroelectric materials, like $Pb(Zr_{0.2}Ti_{0.8})O_3$ (PZT), $SrBi_2TaO_9$ (SBT), and so forth [18], [19], [20]. They need to be very thick to maintain the ferroelectricity needed, and the ferroelectric behavior is weak when the thickness of the material is small, which is incompatible with modern IC industry manufacturing processes. In 2011, T. S. Böscke et al discovered ferroelectric properties in crystalline hafnium silicon oxide film [21]. Later, HfO_2 films doped with Si, Zr, Al and so on were also found to show ferroelectricity [22], [23], [24], [25]. What is more, Zr doped HfO_2 can maintain its ferroelectricity strong enough with a thickness down to 1.8 nm [26] or even 1 nm [27], which makes it possible for the thickness of the gate stack of NC-FET to scale with transistor dimension, thus making NC-FET promising as an ultra-low power consumption device. Just by means of inserting a ferroelectric material layer in the gate stack of a transistor, SS and I_{on} can be significantly improved via internal voltage amplification induced by NC effect: the facility and compatibility make it possible for NC effect to be widely used in all kinds of transistor structures, including the most promisingly commercial ultra-low power consumption NC GAA-FET, and impressive results have been obtained both theoretically and experimentally [19], [28], [29], [30], [31], [32].

A. NEGATIVE CAPACITANCE EFFECT

Ferroelectric materials have been discovered for a long time, but only recently have they been used in MOSFET. Ferroelectric materials are unique in sustaining polarization after the electric field is removed. The polarization left is called remnant polarization, P_r. Another important parameter of ferroelectric materials is the reverse electric field applied to make the P_r return to zero. This electric field is called the conceive electric field, E_c. A typical P-E curve of ferroelectric materials is a S curve, as shown in Fig. 2 [33]. The relation of polarization and electric field E of FE materials is described by the famous Landau-Khalatnikov equation, which is expressed as,

$$E = 2\alpha P + 4\beta P^3 + 6\gamma P^5 - 2g\Delta P + \rho\frac{\mathrm{d}P}{\mathrm{d}t} \tag{7}$$

In (7), α, β, γ are Laudau coefficients, $\alpha = -3\sqrt{3}/4 \times E_C/P_r$, and $\beta = 3\sqrt{3}/8 \times E_C/P_r$, ρ and g refer to coefficients of the viscosity and polarization gradients, respectively [22]. The capacitance is defined as $C = dQ/dV \approx dP/dV$. In Fig. 2, the region where the slope of P versus electric field E is negative corresponds to the NC region. In the energy landscape of ferroelectric materials in Fig. 3, the capacitance is obtained by taking the reciprocal of the second order derivatives of potential energy U with respect to charge Q, as expressed below,

$$C = \left(\frac{\mathrm{d}^2U}{\mathrm{d}Q^2}\right)^{-1} \tag{8}$$

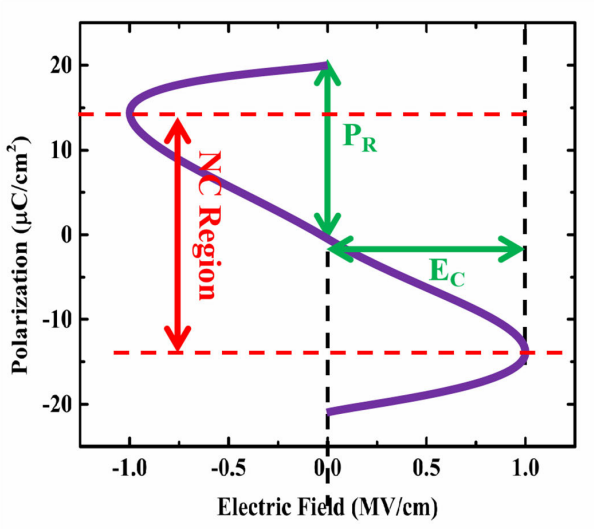

FIGURE 2. The *P-E* S curve of a ferroelectric material, the negative capacitance region is marked by red dotted lines in the picture, reproduced with permission [33].

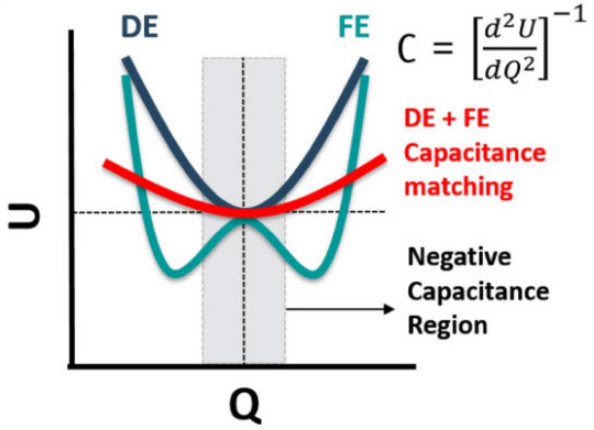

FIGURE 3. Energy (*U*) vs. charge (*Q*) curve of ferroelectric capacitor. The navy, green, and red-colored curves represents the *U* vs. *Q* curves of a dielectric capacitor, a ferroelectric capacitor, and a capacitance-matched capacitor respectively, reproduced with permission from [34].

From the energy landscape of ferroelectric materials shown in Fig. 3, we can see that the region where the capacitance is negative has relatively higher energy, thus NC region is a quasi-stable state. The carrier moves from one stable state to another under a V_g higher than the critical voltage, V_c, and during this process, NC state is passed by. Thus the NC effect is a transient process, which is hard to be detected directly. It is found that by connecting a dielectric material with a ferroelectric material in series, the ferroelectric material can stay in the NC region stably by appropriately adjusting the capacitance proportion of dielectric and ferroelectric materials, as shown in Fig. 3 [34].

B. NC-FET

1) MECHANISM

The NC effect helps the transistor to achieve steep switch by amplifying the internal voltage in vicinity to the channel

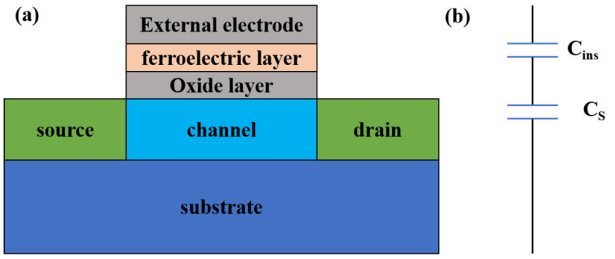

FIGURE 4. (a) Simplified NC-FET device structure schematic, and (b) the corresponding equivalent capacitance circuit of NC-FET.

region. A common NC-FET structure and its equivalent circuit are shown in Fig. 4 (a) and (b) respectively. According to the definition equation of SS, the SS of a NC-FET at room temperature can be expressed as,

$$SS = 60mV/dec \times (1 + \frac{C_S}{C_{ins}}) = 60\text{m}V/dec \times m \quad (9)$$

C_{ins} is the equivalent capacitance of ferroelectric (FE) and dielectric (DE) materials, and it can be obtained by $C_{\text{ins}} = \left(C_{OX}^{-1} + C_{FE}^{-1}\right)^{-1}$. C_S is the capacitance of the transistor; C_S is always positive, and to obtain a SS<60 mV/dec result, m should be smaller than 1, that is to say, C_{ins} should be negative. On the other hand, m should be positive to make the NC-FET stable, thus $|C_{ins}|$ should be larger than C_S. If t_{FE} is small, and $|C_{ins}|$ is much larger than C_S, the second term in the bracket, that is $C_S/C_{ins} \approx 0$, m is closer to 1, the internal voltage amplification effect is weak, SS will not be improved obviously. When t_{FE} increases further, $|C_{ins}|$ decreases gradually, $|C_{ins}|$ is closer to C_S, C_S/C_{ins} is closer to -1, m is closer to 0, SS is steeper. But t_{FE} should not be larger than a critical value at which point hysteresis will happen, thus there exists a tradeoff between SS and hysteresis behavior. By properly adjusting the capacitance matching between C_{ins} and C_S, a steeper SS NC-FET with hysteresis behavior being inhibited can be achieved. Thus far, much research has been done in this field [19], [35], [36], [37]. On the other hand, the FE material parameters also have significant influence on NC-FET performance. Generally, a smaller P_r is beneficial for charge matching between the ferroelectric material and the FET channel, while E_c should be properly chosen to avoid hysteresis.

Previously reported NC-FET mostly discussed the device behavior with single domain L-K model, which hypothesized that the polarization of ferroelectric layer was uniformly distributed. Whereas, polycrystalline mixed phases result in the multi-domain switching issues, including polarization incoherency and NC instability. What is more, with channel length further shrinking, trap-related leakage and domain-wall pinning lead to the influence of gate stack traps with thickness scaling down non-negligible. Under such conditions, multi-domain L-K model, which considers that the polarization intensity direction of each position in ferroelectric material layer is not in consistence, set in to simulate the NC effect of

ferroelectric materials in NC-FET devices recently [38], [39], [40], [41].

2) FRROELECTRIC MATERIALS

Ferroelectric materials have been discovered for a long time. At first, conventional FE materials like perovskite $P(Zr_{1-x}Ti_x)O_3$ (PZT), $SrBi_2Ta_2O_9$ (SBT) and $Bi_4Ti_3O_{12}$ (BTO) attracted immense attentions due to their merits like larger E_c and P_r, favorable thermal stabilities and higher dielectric constants [42]. They have long been proposed to be used in ferroelectric memory devices. And recently, NC-FETs based on PZT have also shown promising results. In 2016, Ali Saeidi and coworkers used PZT in a double-gate NC MOSFET and simulated the 14 nm node ultrathin body and box fully depleted silicon-on-insulator (SOI) FET, and found that SOI-FETs could operate at 0.26 V instead of 0.9 V gate voltage using the NC effect, with an average SS of 55 mV/decade at room temperature, and double gate NC-FETs could operate at 0.24 V with an average SS of 54.5 mV/decade at room temperature [43]. In 2022, Sarabdeep Singh et al simulated a junctionless NWFET with PZT ferroelectric material (NC JLNWFET), and they found that compared with junctionless NWFET without ferroelectric materials (JL NWFET), the NC JLNWFET showed I_{on} and I_{on}/I_{off} ratio improvement factors of 12.5 and 6.8 respectively [44]. Although promising results have been achieved with conventional ferroelectric materials, the disadvantages of higher deposition temperature, inability to keep polarization intensity large enough with film thickness reduction and incompatibility with CMOS fabrication process limit their further usage in NC-FET devices.

Organic ferroelectric materials, such as P(VDF-TrFE), have existed for more than 50 years [45], and as mentioned above, in 2008, Giovanni A. Salvatore and coworkers first demonstrated a NC-FET in experiment by inserting a 40 nm P(VDF-TrFE)/SiO_2 gate stack in the NC-FET and achieved a minimum SS of 13 mV/dec, certifying for the first time that the NC effect could be used in a transistor to induce steep switch behavior [17]. Later, organic ferroelectric materials were widely used in flexible electronics, 2D NC-FET and carbon nanotube FETs due to their excellent scalability and compatibility with different device structures and promising results were obtained [46], [47], [48]. Organic ferroelectric materials possess the merits of low processing temperatures, superb scalability and compatibility with different device structures, which make them promising candidates in future flexible, wearable and bioelectric devices. Unfortunately, organic ferroelectric materials suffer from the main limitations of smaller polarization coefficients and lower cubic temperature, which influence their further application in electronics.

2D ferroelectrics are recently emerging 2D materials. Until recently, cumulative research works have been focused on theory prediction and simulation, while experiment demonstrations of NC-FETs based on 2D ferroelectric materials have been rare. $CuInP_2S_6$ is a commonly used 2D ferroelectric material in NC-FETs. In 2018, Peide D. Ye et al of Purdue University fabricated a NC-FET based on ferroelectric $CuInP_2S_6$ and MoS_2 channels, exhibiting a clear counterclockwise hysteresis loop in transfer characteristics and enhanced on/off current ratio [49]. In 2022, Liming Xie et al demonstrated a NC-FET from all 2D materials with a metal ferroelectric semiconductor (MFS) vertical heterostructure: Graphene/$CuInP_2S_6$/MoS_2, and achieved a sub-60 mV/dec SS for 3 orders of I_{ds} and a lowest SS<10 mV/dec [50]. 2D ferroelectric materials were found later than conventional materials, and their working mechanism and properties remain elusive at the moment, which means that much work needs to be done to figure them out. Thus, there is still a long way to go before considering them as candidates for commercialization.

The emerging of ferroelectric materials based on HfO_2 again draws lots of attention to NC-FET as a promising steep switch transistor. In 2011, T. S. Boscke demonstrated ferroelectric characteristics in Si doped HfO_2 materials [51], and ferroelectric behavior had also been found in Zr doped HfO_2 in the same year [52]. After that, Al, Y, Cd, La and Sr [52], [53], [54], [55], [56] doped HfO_2 all have been demonstrated to display ferroelectric characteristics. In particular, Zr doped HfO_2 ferroelectric materials received much attention due to their scalability to ultrathin films, while retaining strong enough ferroelectricity. In 2018, the discovery of ferroelectric materials based on Zr doped HfO_2 made it possible to scale the thickness of the ferroelectric material layer below 5 nm, while still allowing the material to possess a strong enough polarization intensity [57], which was indispensable to include NC effect in ultra-scaled transistor devices. In 2019, Daewoong Kwon fabricated a NC-FET with 1.8 nm thick Zr-doped HfO_2 and achieved 20 mV/dec steep SS and 10 times reduction in I_{off} at 30 nm channel length with condign I_{on} compared with baseline transistors based on undoped HfO_2 [26]. In 2020, Daewoong Kwon and coworkers demonstrated the persistence of spontaneous, switchable polarization down to a thickness of one nanometer in Zr doped HfO_2 deposited by the atom layer deposition method [58]. The ferroelectric materials based on Zr doped HfO_2 (HZO) display several advantages over other ferroelectric materials found till now; compatible with the modern semiconductor industry fabrication process; thermally stable; higher dielectric permittivity; wide bandgap to suppress leakage current; scalability to reduce to 1 nm thick or less with polarization intensity maintained and the like. These findings manifest the potential of NC effect being used in ultra-scaled low power consumption transistors.

3) NC-FET DEVICE TYPE

As is known, the NC effect can be integrated in a transistor by simply inserting a ferroelectric material layer in the gate stack, thus the NC effect has the advantage of high compatibility with all kinds of transistor structures. Until

now, planar NC-FET, 2D NC-FET, NC-FinFET, NC-TFET, NC GAA-FET and NC GAA-TFET, NC JLGAA-FET [59], [60], [61], [62], [63], [64], [65], [66], [67], [68], [69] all have been proposed and experimentally demonstrated with sub-60 mV/dec SS and improved I_{on}. Besides, the NC effect also proves to be compatible with all kinds of semiconductor channel materials, from 3D Si, Ge, 2D (transition metal dichalcogenides) TMDCs such as MoS_2, WSe_2, black phosphorus to 1D carbon nanotube. Prospective results have been achieved both theoretically and experimentally [70], [71], [72], [73], [74]. But one exception exists: there hasn't been an experiment that has achieved sub-60 mV/dec SS in NC-FETs based on III-V group semiconductors until now due to the serious interface states between ferroelectric materials and III-V semiconductor layers.

III. RECENT FINDINGS

From 22 nm to 5 nm technology nodes, the FinFET structure dominates the semiconductor industry due to its ability to constraint the SCE. Corresponding to the prevalence of FinFET, NC-FinFET has also drawn tremendous attention since it was put forth in 2016 by Chenming Hu [75]. Enormous amounts of research works have been done on NC-FinFET since then [76], [77]. NC-FinFET was treated as a promising ultra-low power consumption device candidate for a while. However, at 3 nm node and beyond, FinFET is to hand over its control over the semiconductor industry to GAA-FET due to the superiority of GAA-FET in suppressing SCE thanks to its surrounding gate structure [78]. As a consequence, NC GAA-FET also wins over NC-FinFET in the field of ultra-low power consumption devices. Fig. 5 (a) and (b) are standard schematic profile structures of a MFIS NC GAA-FET and GAA-FET along the channel direction.

It was M. H. Tang and X.P. Ouyang who first proposed to integrate the NC effect into GAA-FET structures. They theoretically investigated the negative capacitance surrounding gate FET (NC-SG-MFS-FET) compared with the traditional surrounding gate FET (SG-MIS-FET) and obtained better electrostatic control of the gate over the channel, smaller SS and higher I_{on} as well [79]. After that, there had been few research works on NC GAA-FET for a long while until in 2015, Renrong Liang from Tsinghua university published a conference paper in the 15th IEEE International Conference on Nanotechnology about a carrier based analytical theory for NC surrounding gate ferroelectric capacitors [80] and in the following year, they published the simulation result of the work in the Japanese Journal of Applied Physics with a title of ''Analytical Drain Current Model for Long-channel Gate-all-around Negative Capacitance Transistors with a Metal–ferroelectric–insulator–semiconductor Structure'' [81]. In the paper, they proposed a carrier-based analytical drain current model and by changing parameters such as ferroelectric film thickness, channel radius, insulator layer thickness, and permittivity of the insulator layer extensively to examine the electrostatic potential, gain of surface potential, and I_{on}, they obtained sub-60 mV/dec SS. From then on until 2019, the research works on NC GAA-FET were scarce. As GAA-FET is sure to replace FinFET in 3 nm node and beyond, works on NC GAA-FET begin to emerge in large numbers both in theoretical and experimental fields [82], [83], [84], [85]. Table 1 summarizes the outline of main device design consideration items, focusing on which the following test will discuss the recent simulation and experimental findings of NC GAA-FET devices sufficiently.

A. SIMULATION STATUS OF NC GAA-FET

The theoretical investigations mainly focus on the following aspects: firstly, the channel material selection. Conventionally, silicon is preferred as a channel material of NC GAA-FET device due to its mature fabrication techniques [81]. Whereas, as the thickness of silicon reduces to below 5 nm, the electron and hole mobilities are severely degraded due to the surface scattering effect, and what is more, the hole mobility in silicon is much smaller than that of electron. NC GAA-FET for NMOS and PMOS may need different channel materials for comparable performance when the transistor further scales to the sub 3 nm node region and beyond. Besides, semiconductors with special characteristics can be used under some extreme conditions. The 4H-SiC nanowire junctionless negative capacitance gate all around field effect transistor (NC JLNW-GAA) has been suggested to be a good candidate for solving the low performance problem of high-voltage applications due to its large bandgap and high electron saturation drift speed of $\sim 2 \times 10^7$cm/s [86]. GaAs/InN nanowire heterostructures were used in a nanowire gate-all-around negative capacitance tunnel field-effect transistor (NC NWGAA-TFET) in a simulation study by Md. Sherajul Islam and his coworkers in 2022, and promising results have been obtained by incorporating 9 nm hafnium zirconium oxide (HZO) ferroelectric layers [87].

The second aspect of the simulation focuses on gate stack structure selection. When the NC effect was proposed to be integrated in GAA-FETs in 2012 by M. H. Tang and X.P. Ouyang, they used the Metal-ferroelectric-semiconductor (MFS) gate structure, which was given up later due to serious interface states caused by misalignment between the ferroelectric material and the semiconductor layer, though it was easy to be fabricated. They ignored the interface states for simplification in the study and obtained sub-60 mV/dec SS and improved I_{on} compared with the baseline surrounding gate transistors [79]. Metal-ferroelectric-insulator-semiconductor (MFIS) gate stack structures were introduced at the right moment, with an interfacial insulator layer inserted between the ferroelectric material layer and the semiconductor channel, the interface trap states were effectively suppressed [80], [81]. The MFIS gate stack NC GAA-FET structure also has its limitations, as there exists a potential drop under the ferroelectric material along the channel direction, causing asymmetric internal voltage amplification, which degrades the steep switch behavior of the transistor and decreases I_{on}. The problem is solved by

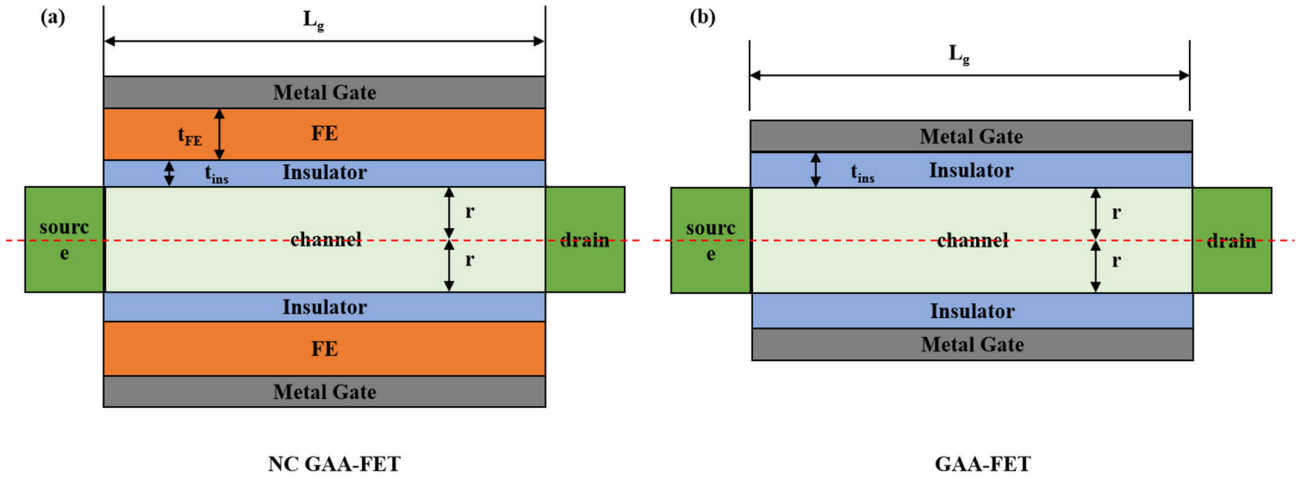

FIGURE 5. The schematic profile of MFIS NC GAA-FET and corresponding GAA-FET structures along the channel direction.

TABLE 1. The device design consideration items and their merits and limitations.

Device Design Considerations	Type	Main Merits	Limitations
Channel Materials	Si	Mature fabrication techniques	Carrier mobility degradation with thickness scaling
	Ge	Compatible with Si manufacturing technique; High carrier mobility	Carrier mobility degradation with thickness scaling; Narrower bandgap leading to larger leakage current
	III-V Semiconductors	High carrier mobility	Large interface states between III-V and Semiconductors and ferroelectric materials
	2D Materials	Atomic flat surface; dangling-bond free; sub-nm thickness; high carrier mobility maintaining ability with thickness scaling	Insufficient research work both from academic and industry
Gate Stack Structures	MFS	Simple Manufacturing process	Large interface states between ferroelectric materials and semiconductors channel materials and
	MFIS	Relatively simple gate stack structure; Overcoming large interface states between FE layer and semiconductor channel layer	Asymmetric internal gate voltage amplification effect caused by potential drop along the channel
	MFMIS	Smaller SS and improved I_{on} caused by equalized internal gate voltage amplification effect	Complicated gate manufacturing process; Stability issue; Limitation in gate thickness scaling down
Channel Structures	Nanosheet	Improved device performance with smaller footprint;	Corner effect; Large parasitic capacitance
	Nanowire	Easy fabricated; less serious parasitic capacitance effect	Device performance relatively inferior than NS NC GAA-FET
Hysteresis Avoidance and performance Improvements	Capacitance Matching	C_{fe} and C_{mos} be matched to guarantee improved SS and hysteresis free behavior; Appropriate FE materials parameters chosen; FE layer thickness optimization	

metal-ferroelectric-metal-insulator-semiconductor (MFMIS) gate stack structures. In 2020, Fahimul Islam Sakib et al simulated a negative capacitance nanosheet GAA FET in comparison with negative capacitance nanowire GAA-FET and NC FinFET with a MFMIS gate stack structure, and drew the conclusion that with the help of internal metal gate (IMG), ultra-steep switch behavior could be obtained in all NC NWGAA-FET, NC NSGAA-FET and NC-FinFET. Among these, NC NSGAA-FET performed the best [88]. MFMIS gate stacks can overcome the obstacles faced by MFIS gate stack structures and offer a uniformly distributed potential along the channel attributed to the IMG, leading to steeper subthreshold behavior and improved device performance [89]. Whereas, the MFMIS gate stack structure is apt to suffer from stability issue caused by large gate leakage current. Fortunately, this concern can be overcome by appropriate gate workfunction (WF) engineering between metals used in the external and intermediate gates [88]. Besides, the IMG complicates the gate fabrication process and constraints the scalability of the thickness of the gate layer, which poses a big challenge for MFMIS gate stack structure to be used commercially. There are controversial viewpoints about MFIS and MFMIS gate stack NC-FET structures when considering different L-K models of ferroelectric materials.

MFMIS NC-FET is considered to be prone to hysteresis behavior when considering domain formation, thus MFIS NC-FET structure is preferred when designing NC-FET devices [90], [91]. In another research work, MFMIS NC-FET was concluded to be superior over MFIS NC-FET both in SS and hysteresis inhibition aspects, single domain L-K model of FE material is used in this study [89]. Further simulation works need to be performed to check the performance superiority between MFIS and MFMIS NC GAA-FET device structures when multi-domain L-K models of FE materials are considered in the future.

The channel structure selection is also an important research topic of NC GAA-FET. Whether nanowire or nanosheet channel structure is better for NC GAA-FET being used in ultra-scaled gate length FET structure has remained a controversial issue. Nanowire channels are easy to fabricate and free from the problems of corner aggregation of charges and electric fields; the insulator/ferroelectric gate stacks can be deposited uniformly around nanowire channels by atom layer deposition techniques; besides, the large parasitic capacitance issue is not so serious as that in nanosheet based NC GAA-FET. Innovative simulation works on performance comparison between NC NSGAA-FET and NC NWGAA-FET were done by Abhinav Kranti's team in 2020 [88] and Mainul Hossain and his coworkers in 2021 [92]. They all drew the conclusion that NC NSGAA-FET showed better performance than NC NWGAA-FET in SS, I_{on} and other device figure of merits. Besides, Abhinav Kranti concluded that NC NSGAA-FET was more suitable for ultra-scaled transistors since the designing space was much larger for NC NSGAA-FET than those for both NC NWGAA-FET and NC-FinFET in the same technology node [88]. Vertically stacked nanowire FET was also integrated with the NC effect by Huang et al. to design a negative capacitance vertically stacked nanowire FET (NC VNWGAA-FET) with spacer-like negative capacitors for sub-5 nm node. They attained a conclusion that the capacitance matching could be easily achieved by adjusting the area of spacer-like negative capacitors and/or the thickness of ferroelectric films without significant modification of integration schemes, which was important for future application of nano-scaled electronics [93].

To improve device performance and avoid hysteresis are other research orientations of NC GAA-FET. There exists a tradeoff between steep SS and hysteresis in NC-FET due to capacitance matching. Lots of research work has been done to investigate the critical ferroelectric thickness at which SS is the smallest and simultaneously hysteresis behavior can be avoided. Abhinav Kranti et al investigated the device-dependent conditions for achieving hysteresis free sub-60 mV/dec SS in NC NWGAA-FET in 2020 by varying ferroelectric thickness, nanowire radii, the parameters of ferroelectric materials like remnant polarization P_r and coercive electric field E_c, and doping species in HfO_2 from Al, Zr to Y, and they found that a tiny variation in ferroelectric materials' parameters as P_r, E_c, doping species type, or doping ratio would cause a significant change in NC GAA-FET device performance [94]. Kyungmin Jang obtained 5 times higher I_{on}/I_{off} ratio in NC NWGAA-FET compared with NW GAA-FET and 2 times higher I_{on}/I_{off} ratio compared with double gate NC-FET with hysteresis free sub-60 mV/dec SS [95]. Mainul Hossain et al studied the effect of device structure on the performance of NC-FETs with single gate, double gate, tri-gate (FinFET) and gate-all-around (GAA) device architectures: by varying ferroelectric material thickness and optimizing capacitance matching, sub-60 mV/dec SS with hysteresis free behavior could be achieved for all NC-FETs structures, among which NC NWGAA-FET performed the best. In this work, they discussed at length about the vital role played by capacitance matching between C_{FE} and C_{MOS} in hysteresis inhibition and SS improvement. The body factor m, which was defined as the surface potential gain caused by gate voltage augment, must lie in the range $0 < m < 1$ to avoid instability issue and obtain steep switch behavior [96]. Weifeng Lü in Hangzhou Dianzi University demonstrated comprehensive performance enhancement in NC NSGAA-FET with steep SS in sub 5 nm node [97]. They found that inserting the NC effect in NS GAAFET could improve not only the device performance, but also lead to analog/radio frequency (RF) performance enhancement as well. Chenming Hu and coworkers simulated NC GAA-FET with TCAD, and they found that at 1.5 nm node, NC effect's integration in GAA-FET helped to reduce the minimum SS from 70 mV/dec to 63 mV/dec, bringing about a 7 mV/dec improvement. The device operating voltage could be reduced to 0.49 V under the on-state current requirement enacted by IRDS proposed in 2020 of "0.7 eq node" by making usage of internal voltage amplification effect induced by NC effect. They predicted that by incorporating the NC effect in GAA-FET, one could sustain Moore's law from 1.5 nm node to "0.7 eq node", and even fulfilled the requirements of "0.5 eq node" as well. The introduction of NC effect in GAA-FET led to improved SS and I_{on} vs I_{off} ratio, as obtained from figure 6 (a) and (b), which benefited device performance vice versa [98]. Negative drain induced barrier lowering (n-DIBL), negative differential resistance (NDR) are unique properties of NC-FETs, which were thoroughly investigated in 2020 by Huilong Zhu el al combined with Miller effect in NC NWGAA-FET structures. They obtained a minimum SS of 40 mV/dec and three times larger I_{on} in NC NWGAA-FET. Besides, overshoot and the propagation delay of the NC NWGAA-FET based inverter were ∼43.1% and ∼73.1% less than those of the NW GAA-FET based inverter at ferroelectric thickness T_{FE} of 3 nm [99].

Last but not least, an integrated spice model created for NC GAA-FET has long been a target pursued by researchers both in academia and industry. An integrated NC GAA-FET spice model can help with the design and performance improvement of NC GAA-FET. In 2016, Renrong Liang from Tsinghua University proposed a carrier-based analytical

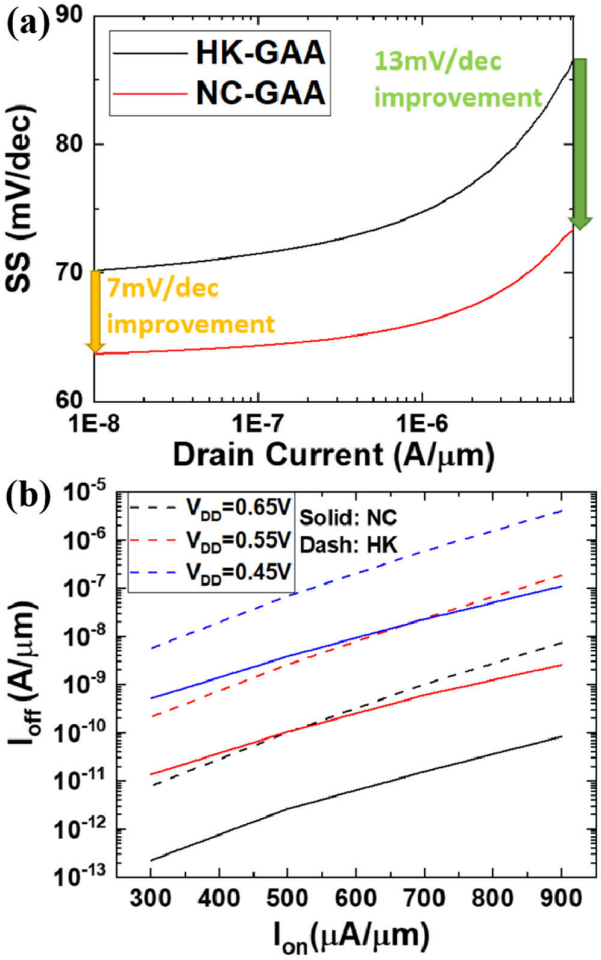

FIGURE 6. (a) The SS vs I_d trends both for GAA and NC GAA-FET structure with the same device parameters simulated by TCAD. (b) I_{off} vs I_{on} curves of GAA (doted lines) and NC GAA-FET (solid lines) simulated with TCAD under V_{DD} of 0.45 V, 0.55 V, and 0.65 V respectively. Reproduced with permission from [98].

drain current model for long channel negative capacitance surrounding gate capacitor by solving 1D Landau-Khalatnikov equation and Poisson's equation [81]. Two years later, Amol D. Gaidhane and coworkers proposed a surface potential-based explicit continuous model for long channel MFIS NC GAA-FET. They considered radial dependence of the electric field in the ferroelectric materials, which had been ignored in previous works, and accurately captured ferroelectric material parameters variation in the non-hysteresis regime [100]. In 2020, A. D. Gaidhane proposed a compact model with quasi-ballistic transport considered for sub-7 nm technology node. They found that quasi ballistic transport exacerbated the capacitance matching in NC GAA-FET compared to that in the drift-diffusion only case [101]. In 2021, Jongwook Jeon et al proposed a compact model of NC GAA-FET describing current–voltage (I–V) with interface trap effects considered for the first time, and the proposed model showed good alignment with the results of implicit numerical calculations [102].

NC GAA-FET was first brought up more than 10 years ago. Though promising simulation results have been obtained, there still is much theoretical work to be done in device performance improvement, unique characteristics investigation and model creation.

B. EXPERIMENT STATUS OF NC GAA-FET

Contrary to the phenomenon that simulation research works of NC GAA-FET bloom everywhere, experimental works of NC GAA-FET are limited to several groups worldwide due to the harsh experiment conditions needed. Traditionally, Si or poly-Si nanowire/nanosheet are preferred as channel materials in NC GAA-FET devices thanks to their mature manufacturing procedure and low cost. There exist a series of NC GAA-FET research works fabricated with Si or poly-Si channel materials, mainly come from research groups in Taiwan.

1) SILICON CHANNEL MATERIALS

In 2018, M. H. Lee from National Taiwan Normal University fabricated NC NSGAA-FET and NC-FinFET with extremely steep switch properties, presenting SS_{avg}/SS_{min} = 22/14 mV/dec and SS_{avg}/SS_{min} = 38/21 mV/dec, respectively. Typical NC effects: n-DIBL and NDR had been observed both in NC NSGAA-FET and NC-FinFET, which complied well with the simulation work by Huilong Zhu et al [99]. They also simulated stacked NC NSGAA-FET with quantum confinement effect considered, which was believed to be caused by T_{NS} (nanosheet thickness) scaling down. They concluded that the uniformity of T_{NS} of each nanosheet was crucial for capacitance matching [103]. Tien-Sheng Chao from Taiwan National Chiao Tung University conducted a series of studies on NC GAA-FET devices based on Si or poly-Si channels. In 2019, his team fabricated a two-layer stacked nanowire NC GAA-FET with ultra-scaled poly-Si channel, and obtained an I_{on}/I_{off} ratio of more than 10^8, while the minimum and average SS were 43.85 and 26.84 mV/dec, respectively. They also found that an additional ZrO_2 seed layer inserted under the $Hf_{1-x}Zr_xO_2$ layer could improve ferroelectric crystallization, thus the conventional crystallization annealing step could be omitted [104]. In 2020, Tien-Sheng Chao compared MFIS and MFMIS gate structures for single-layer-stacked and double-layer-stacked NC GAA-FETs, and obtained enhanced electrical performance in MFMIS structures owing to the uniform dipole polarization induced by symmetrical electric fields. This phenomenon had also been verified in the simulation research work by Fahimul Islam Sakib and coworkers in the same year [88]. On the other hand, they found that the 2-layer-stacked channel could provide a significant improvement in I_{on} within the same channel footprint area attributed to the increased effective channel width (W_{eff}). Unfortunately, the amplification of I_{on} was less than the numbers of the stacked nanosheet layers due to the series resistance increment resulted from the bottom nanosheet. An average SS of

43.85 mV/dec within 4 orders of I_{on} in the 2-layer-stacked NC NSGAA-FET had been achieved [84]. In the same year, they explored the effect of a seed layer on MFMIS and MFIS NC NWGAA-FET, and also compared planar, tri-gate and GAA structures.The sub-V_{th} behavior and I_{on} of the NC NWGAA structure were preferable because of its superior gate controllability and larger effective width. The inserted IMG benefited the NC NWGAA-FET performance by improving SS, boosting I_{on} and inducing typical NC effects, such as n-DIBL and NDR. The reasons lied in that the inserted IMG could equalize the potential under FE HZO layer, thus leading to an eliminated voltage drop along the channel from source to drain under the FE layer. An enhanced channel conductance had also been observed thanks to the IMG layer [105]. In 2021, they fabricated a MFMIS gate stack NC NW GAA-FET with a sub-5 nm $Hf_{1-x}Zr_xO_2$ (HZO) ferroelectric layer, and the total thickness of the gate stack was 9 nm while the minimum SS of 49.3 mV/dec had been achieved with an IMG. The reduction of HZO thickness used in NC NW GAA-FET offered more opportunities for NC GAA-FET to be used commercially in sub-3 nm and beyond technology nodes. And according to their findings, the insertion of IMG also mitigated the device-to-device variation problem. Besides, they proposed that the stacked-channel structure was the most effective approach to increase W_{eff} without degrading the electrical properties [106]. In 2022, they demonstrated a hysteresis-free poly-Si NC NSGAA-FET with $Hf_{1-x}Zr_xO_2$ (HZO) ferroelectric layer and IMG structure. With NH_3 plasma treatment, the HZO ferroelectricity and quality could be improved and the interface states between metal/HZO and HZO/metal could be decreased, thus leading to increased average SS, I_{on}/I_{off} ratio and breakdown voltage. NC NSGAA-FET with NH_3 plasma treatment at both metal/HZO and HZO/metal interfaces showed best reliability, the V_{th} hysteresis between forward and reverse sweep is as small as 1.8 mV [31].

2) GERMANIUM CHANNEL MATERIALS

Recently, germanium (Ge) nanowire/nanosheet channels have sprung up to draw researchers' attention due to their high electron/hole mobilities, compatibility with modern semiconductor industry manufacturing process and relatively low cost. SCE and leakage current large issues have long been agonizing Ge FET and preventing it from commercial usage. However, the emerging NC GAA-FET structure offers the opportunity to help Ge FET to overcome serious SCE and leakage current large problems, which are attributed to the smaller Bandgap (0.66 eV), smaller carriers effective mass, and large permittivity ($\varepsilon_r = 16.0$). Intensive studies of Ge NC GAA-FET have been reported nowdays [107], [108], [109], [110]. As a matter of fact, the experimental demonstration of Ge NC GAA-FET structure was earlier than that of Si channel NC GAA-FET.

In 2017, C.-J. Su in National Nano Device Laboratories in Taiwan experimentally demonstrated a Ge nanowire based NC NWGAA-FET with ferroelectric $HfZrO_x$ (FE-HZO) gate stack for the first time and achieved a 54 mV/dec SS at room temperature. High I_{on}/I_{off} ratios greater than 10^7 and 10^6 for p- and n- NC NWGAA-FETs, respectively were obtained, they also discussed the reliability problem of FE-HZO and drew the conclusion that the interface charge trapping and stress polarization effects were the main factors responsible for the reliability of FE-HZO materials [107]. In 2018, Peide D. Ye and coworkers from Purdu University firstly launched a direct experimental study on the polarization response speed of ferroelectric $Hf_{0.5}Zr_{0.5}O_2$ in Ge Nanowire NC GAA-FET device. They found that HZO could switch its polarization directly by a pulse with a width as narrow as 3.6 ns, and what was more, a 100 ps pulse was enough to initial polarization in HZO. Their work opened the root of studying the dynamics of FE materials with pulse width as narrow as 100 ps or beyond [108]. In 2019, Yung-Chun Wu et al from National Tsing Hua University experimently demonstrated a p type negative capacitance germanium nanosheet channel gate all around FET (Ge NS-NC GAA-FET) with 2 nm $Hf_{0.5}Zr_{0.5}O_2$ (HZO), achieving a high I_{on}, steep SS ($SS_{min} = 55$ mV/dec) and a high I_{on}/I_{off} ratio ($>10^6$) [109]. In 2021, they fabricated a n-type Ge nanowire ferroelectric-$Hf_{0.5}Zr_{0.5}O_2$ field effect transistor (Ge NW FE-HZO FET), they found microwave annealed (MWA) samples had better FE-HZO uniformity properties than those of samples treated with rapid thermal annealing (RTA), a minimum SS of 55 mV/dec, I_{on}/I_{off} ratio of 8.1×10^4 with low hysteresis (30 mV) had been obtained for Ge NW FE-HZO FET under a drain bias of 0.1 V [110].

3) NOVEL MATERIAL CHANNELS

The experimental demonstration of NC GAA-FET based on high mobility III-V semiconductors, 4H-SiC and other novel semiconductor materials are still missing at the moment, though their simulation research has already been performed sufficiently [86], [87], enormous efforts are waited to be put into experimental research of NC GAA-FET to keep up with the developing step of theoretical research.

In a word, the experimental works on NC GAA-FET are rare at the moment, but the meaning is significant for the development of ultra-low power consumption devices. Researchers are looking for other ways to conduct experimental studies on NC GAA-FET devices, for example, cooperating with companies to do research using the equipment of the companies, increasing cooperation between different research groups and the like.

C. THE RELATION BETWEEN SIMULATION AND EXPERIMENTAL STUDY OF NC GAA-FET

Both simulation and experimental research works are vital for the development of NC GAA-FET. Although it seems that the experimental research of NC GAA-FET lags far behind of simulation research at the moment, the final commercial application of NC GAA-FET in ultra-low power consumption device field needs both of their mature research works.

In one way, the simulation research can open the gateway and act as a beacon for the experimental research. On one hand, simulation research works set lists of standards for devices figure of merits in every technology node, which serve as the guidelines for the experimental research. On the other hand, simulation research also predicts new phenomenons, such as n-DIBL, NDR and Miller effects in NC GAA-FET, which draw the attention of experimental researchers to study and verify; Simulation research also contributes a lot to new device structures design and device performance optimization. The other way around, experimental research of NC GAA-FET can verify the view points put forward by simulation research; at the same time, experimental research also brings up new issues and challenges for simulation researchers to resolve. The setup and perfection of simulation models of NC GAA-FET also depend on the experimental results.

All in all, the evolution of NC GAA-FET depends not only on the dedication of researchers from the experimental fields, but also rely on the contributions made by the theoretical works. It is a double edged sword, and theoretical investigation of NC GAA-FET should run side-by-side with experimental study to the final destination of the commercial application of NC GAA-FET in ultra-low power device field.

IV. CONCLUSION

A. CHALLENGES AND OPPORTUNITIES

With the trend that FinFET is to be replaced by GAA-FET in 3 nm node and beyond, NC GAA-FET is also uprising like a star among steep switch ultra-low power consumption devices. Though it is promising to sustain Moore's law to 0.5 nm node as predicted by Chenming Hu in 2021 [98], there are several challenges faced by NC GAA-FET if it is to be used commercially in the future. a), The gate stack thickness should be scaled down proportionately with the gate length scaling, that is to say, ultrathin ferroelectric materials should be used. As is known, the ferroelectricity is weakened if the ferroelectric material thickness reduces, so new ferroelectric materials with strong enough ferroelectricity (though they might be thinned to sub-nanometer level) that are compatible with the industry fabrication process are urgently needed; b), Capacitance matching between ferroelectric materials and equivalent MOS capacitance should be optimized to attain a steep SS without hysteresis effect, which is vital to the performance and stability of NC GAA-FET; c), Until now, all related research, no matter experimental or theoretical, has proved that NC NSGAA-FET outperforms NC NWGAA-FET in almost all aspects of device figure of merits, thus NC NSGAA-FET is the most lucrative candidate in ultra-scaled transistors. However, NC NSGAA-FET has long suffered from large parasitic capacitance, which delays the transistor speed. A new method must be found to overcome this shortcoming if NC NSGAA-FET is to be commercialized in the future. d), Temperature reliability problems of ferroelectric materials should be conquered. The parameters of ferroelectric materials can be easily impacted by temperature increase, and a small variation of P_r and E_c may cause significant change in the I_d-V_g curve of NC GAAFET. Thus finding a kind of ferroelectric material with a large thermally stable window is indispensable for future commercialization of NC GAA-FET.

B. FUTURE OUTLOOK

Samsung massively produces 3 nm Si GAA-FET in 2022, and according to their foundry's roadmap, they plan to produce 2 nm and 1.4 nm nodes transistor in large scale in 2025 and 2027 respectively. They all possess GAA-FET structures. And what is more, they will continue to sustain the life of Moore's law further to sub-1 nm nodes, novel device structure as NC GAA-FET or new channel materials such as 2D materials or carbon nanotube might come to Si GAA-FET's rescue once it reaches scaling limit, which is also the case for TSMC and other giant semiconductor foundries. In conclusion, the NC GAA-FET is predicted to overcome the obstacles and dominate the ultra-scaled low power consumption transistor field some day in the future thanks to the advances both in ferroelectric materials and GAA-FET devices. In this article, we give a thorough summary of the ferroelectric materials' development and recent developments of the NC GAA-FET both in the theoretical and experimental fields. Simulation works are abundant and covers from device structure optimization, device performance improvement, capacitance matching between C_{FE} and C_S to increase SS and avoid hysteresis, negative DIBL, NDR, Miller effect investigation, to compact spice model creation. However, due to the harsh experiment conditions needed to fabricate ultra-scaled NC GAA-FET, the experimental works are few, and mainly come from several particular research groups in the world. But the encouraging thing is, all experimental works, though scarce as mentioned, have obtained promising results, and demonstrated the potential of NC GAA-FET to be used as ultra-scaled steep switch transistors in the future.

REFERENCES

[1] L. Tu, X. Wang, J. Wang, X. Meng, and J. Chu, "Ferroelectric negative capacitance field effect transistor," *Adv. Electron. Mater.*, vol. 4, pp. 1800231–1800247, Aug. 2018.
[2] M. Kobayashi, "A perspective on steep-subthreshold-slope negative-capacitance field-effect transistor," *Appl. Phys. Exp.*, vol. 11, pp. 110101–110120, Oct. 2018.
[3] A. Nowbahar, A. Roy, and L. Marchetti, "Junctionless transistors: State-of-the-art," *Electronics*, vol. 9, pp. 1174–1195, Jul. 2020.
[4] Y. Zhai, Z. Feng, Y. Zhou, and S.-T. Han, "Energy-efficient transistors: Suppressing the subthreshold swing below the physical limit," *Mater. Horizons*, vol. 8, no. 6, pp. 1601–1617, Jun. 2021.
[5] A. M. Ionescu and H. Riel, "Tunnel field-effect transistors as energy-efficient electronic switches," *Nature*, vol. 479, pp. 329–337, Nov. 2011.
[6] W. Banerjee, A. Kashir, and S. Kamba, "Hafnium oxide (HfO_2)—A multifunctional oxide: A review on the prospect and challenges of hafnium oxide in resistive switching and ferroelectric memories," *Small*, vol. 18, pp. 2107575–2107625, Jul. 2022.
[7] T. E. Taouririt, A. Meftah, and N. Sengouga, "Effect of the interfacial (low-k SiO_2 vs high-k Al_2O_3) dielectrics on the electrical performance of a-ITZO TFT," *Appl. Nanosci.*, vol. 8, no. 8, pp. 1865–1875, Sep. 2018.

[8] D. Hisamoto, W. C. Lee, J. Kedzierski, H. Takeuchi, K. Asano, C. Kuo, E. Anderson, T. J. King, J. Bokor, and C. Hu, "FinFET-a self-aligned double-gate MOSFET scalable to 20 nm," *IEEE Trans. Electron Devices*, vol. 47, no. 12, pp. 2320–2325, Dec. 2000.

[9] A. Samal, S. L. Tripathi, and S. K. Mohapatra, "A journey from bulk MOSFET to 3 nm and beyond," *Trans. Electr. Electron. Mater.*, vol. 21, no. 5, pp. 443–455, Oct. 2020.

[10] G. Nazir, A. Rehman, and S.-J. Park, "Energy-efficient tunneling field-effect transistors for low-power device applications: Challenges and opportunities," *ACS Appl. Mater. Interfaces*, vol. 12, no. 42, pp. 47127–47163, Oct. 2020.

[11] Y.-W. Lan, C. M. Torres, S.-H. Tsai, X. Zhu, Y. Shi, M.-Y. Li, L.-J. Li, W.-K. Yeh, and K. L. Wang, "Atomic-monolayer MoS_2 band-to-band tunneling field-effect transistor," *Small*, vol. 12, no. 41, pp. 5676–5683, Nov. 2016.

[12] N. Kannan and M. J. Kumar, "Dielectric-modulated impact-ionization MOS transistor as a label-free biosensor," *IEEE Electron Device Lett.*, vol. 34, no. 12, pp. 1575–1577, Dec. 2013, doi: 10.1109/LED.2013.2283858.

[13] H. Kam and T.-J.-K. Liu, "Pull-in and release voltage design for nanoelectromechanical field-effect transistors," *IEEE Trans. Electron Devices*, vol. 56, no. 12, pp. 3072–3082, Dec. 2009.

[14] M. Liu, H. N. Jaiswal, S. Shahi, S. Wei, Y. Fu, C. Chang, A. Chakravarty, F. Yao, and H. Li, "Monolayer MoS_2 steep-slope transistors with record-high sub-60-mV/decade current density using dirac-source electron injection," in *IEDM Tech. Dig.*, Dec. 2020, pp. 12.5.1–12.5.4.

[15] W. Y. Choi, "Negative capacitance vacuum channel transistors for low operating voltage," *Micromachines*, vol. 11, no. 6, pp. 543–553, 2020, doi: 10.3390/mi11060543.

[16] S. Salahuddin and S. Datta, "Use of negative capacitance to provide voltage amplification for low power nanoscale devices," *Nano Lett.*, vol. 8, no. 2, pp. 405–410, 2008.

[17] G. A. Salvatore, D. Bouvet, and A. M. Ionescu, "Demonstration of subthrehold swing smaller than 60 mV/decade in Fe-FET with P(VDF-TrFE)/SiO_2 gate stack," in *IEDM Tech. Dig.*, Dec. 2008, pp. 1–4.

[18] R. R. Das, S. B. Majumder, and R. S. Katiyar, "Comparison of the electrical characteristics of PZT and SBT thin films," *Integr. Ferroelectr.*, vol. 42, no. 1, pp. 323–334, Jan. 2002.

[19] A. Saeidi, F. Jazaeri, F. Bellando, I. Stolichnov, G. V. Luong, Q.-T. Zhao, S. Mantl, C. C. Enz, and A. M. Ionescu, "Negative capacitance as performance booster for tunnel FETs and MOSFETs: An experimental study," *IEEE Electron Device Lett.*, vol. 38, no. 10, pp. 1485–1488, Oct. 2017, doi: 10.1109/LED.2017.2734943.

[20] Y. Liu and B. Paul, "A negative capacitance-based gate-round field-effect transistor and its fabrication method," China Patent CN 107 845 679 A, Mar. 2018.

[21] T. S. Böscke, J. Müller, D. Bräuhaus, U. Schröder, and U. Bottger, "Ferroelectricity in hafnium oxide: CMOS compatible ferroelectric field effect transistors," in *IEDM Tech. Dig.*, Dec. 2011, pp. 24.5.1–24.5.4, doi: 10.1109/IEDM.2011.6131606.

[22] S. Khandelwal, J. P. Duarte, A. I. Khan, S. Salahuddin, and C. Hu, "Impact of parasitic capacitance and ferroelectric parameters on negative capacitance FinFET characteristics," *IEEE Electron Device Lett.*, vol. 38, no. 1, pp. 142–144, Jan. 2017, doi: 10.1109/LED.2016.2628349.

[23] G. Pahwa, T. Dutta, A. Agarwal, and Y. S. Chauhan, "Energy-delay tradeoffs in negative capacitance FinFET based CMOS circuits," in *Proc. 3rd Int. Conf. Emerg. Electron. (ICEE)*, Dec. 2016, pp. 1–4, doi: 10.1109/ICEmElec.2016.8074416.

[24] J. Müller, T. S. Böscke, U. Schröder, S. Mueller, D. Bräuhaus, U. Böttger, L. Frey, and T. Mikolajick, "Ferroelectricity in simple binary ZrO_2 and HfO_2," *Nano Lett.*, vol. 12, no. 8, pp. 4318–4323, 2012.

[25] A. Nourbakhsh, A. Zubair, S. Joglekar, M. Dresselhaus, and T. Palacios, "Subthreshold swing improvement in MoS_2 transistors by the negative-capacitance effect in a ferroelectric Al-doped-HfO_2/HfO_2 gate dielectric stack," *Nanoscale*, vol. 9, no. 18, pp. 6122–6127, 2017.

[26] D. Kwon, S. Cheema, N. Shanker, K. Chatterjee, Y.-H. Liao, A. J. Tan, C. Hu, and S. Salahuddin, "Negative capacitance FET with 1.8-nm-thick Zr-doped HfO_2 oxide," *IEEE Electron Device Lett.*, vol. 40, no. 6, pp. 993–996, Jun. 2019, doi: 10.1109/LED.2019.2912413.

[27] U. Schroeder, M. H. Park, T. Mikolajick, and C. S. Hwang, "The fundamentals and applications of ferroelectric HfO_2," *Nature Rev. Mater.*, vol. 7, no. 8, pp. 653–669, Mar. 2022, doi: 10.1038/s41578-022-00431-2.

[28] M. H. Lee, Y.-T. Wei, C. Liu, J.-J. Huang, M. Tang, Y.-L. Chueh, K.-Y. Chu, M.-J. Chen, H.-Y. Lee, Y.-S. Chen, L.-H. Lee, and M.-J. Tsai, "Ferroelectricity of $HfZrO_2$ in energy landscape with surface potential gain for low-power steep-slope transistors," *IEEE J. Electron Device Soc.*, vol. 3, no. 4, pp. 377–381, Jul. 2015, doi: 10.1109/JEDS.2015.2435492.

[29] X. Liu, R. Liang, G. Gao, C. Pan, C. Jiang, Q. Xu, J. Luo, X. Zou, Z. Yang, L. Liao, and Z. L. Wang, "MoS_2 negative-capacitance field-effect transistors with subthreshold swing below the physics limit," *Adv. Mater.*, vol. 30, no. 28, pp. 1800932–1800939, 2018.

[30] H. Ota, T. Ikegami, J. Hattori, K. Fukuda, S. Migita, and A. Toriumi, "Fully coupled 3-D device simulation of negative capacitance FinFETs for sub 10 nm integration," in *IEDM Tech. Dig.*, Dec. 2016, pp. 12.4.1–12.4.4.

[31] C.-C. Lee, D.-R. Hsieh, S.-W. Li, Y.-S. Kuo, and T.-S. Chao, "Hysteresis-free gate-all-around stacked poly-Si nanosheet channel ferroelectric $Hf_xZr_{1-x}O_2$ negative capacitance FETs with internal metal gate and NH_3 plasma nitridation," *IEEE Trans. Electron Devices*, vol. 69, no. 3, pp. 1512–1518, Mar. 2022, doi: 10.1109/TED.2022.3147445.

[32] Y.-H. Lu, P.-Y. Kuo, Y.-H. Wu, Y.-H. Chen, and T.-S. Chao, "Novel sub-10-nm gate-all-around Si nanowire channel poly-Si TFTs with raised source/drain," *IEEE Electron Device Lett.*, vol. 32, no. 2, pp. 173–175, Feb. 2011, doi: 10.1109/LED.2010.2093557.

[33] A. I. Khan and C. Sciences, "Negative capacitance for ultra-low power computing," Ph.D. dissertation, Dept. Electr. Eng. Comput. Sci., California Univ., Berkeley, CA, USA, 2015.

[34] E. Ko, J. Shin, and C. Shin, "Steep switching devices for low power applications: Negative differential capacitance/resistance field effect transistors," *Nano Converg.*, vol. 5, no. 1, pp. 1–9, Dec. 2018.

[35] I. Luk'yanchuk, A. Razumnaya, A. Sené, Y. Tikhonov, and V. M. Vinokur, "The ferroelectric field-effect transistor with negative capacitance," *NPJ Comput. Mater.*, vol. 8, no. 1, pp. 52–57, Mar. 2022.

[36] E. Ko, J. W. Lee, and C. Shin, "Negative capacitance FinFET with sub-20-mV/decade subthreshold slope and minimal hysteresis of 0.48 V," *IEEE Electron Device Lett.*, vol. 38, no. 4, pp. 418–421, Apr. 2017, doi: 10.1109/LED.2017.2672967.

[37] Z. Zhang, G. Xu, Q. Zhang, Z. Hou, J. Li, Z. Kong, Y. Zhang, J. Xiang, Q. Xu, Z. Wu, H. Zhu, H. Yin, W. Wang, and T. Ye, "FinFET with improved subthreshold swing and drain current using 3-nm ferroelectric $Hf_{0.5}Zr_{0.5}O_2$," *IEEE Electron Device Lett.*, vol. 40, no. 3, pp. 367–370, Mar. 2019, doi: 10.1109/LED.2019.2891364.

[38] J. Gomez, S. Dutta, K. Ni, J. A. Smith, B. Grisafe, A. Khan, and S. Datta, "Hysteresis-free negative capacitance in the multi-domain scenario for logic applications," in *IEDM Tech. Dig.*, Dec. 2019, pp. 1–7.

[39] G.-Y. He, M.-H. Li, W.-D. Liu, L.-Y. Ying, B.-P. Zhang, Z.-W. Zheng, and C.-H. Cheng, "Simultaneous analysis of multi-variables effect on the performance of multi-domain MFIS negative capacitance field-effect transistors," *IEEE J. Electron Devices Soc.*, vol. 9, pp. 741–747, 2021.

[40] C. Liu, H.-H. Chen, C.-C. Hsu, C.-C. Fan, H.-H. Hsu, and C.-H. Cheng, "Negative capacitance CMOS field-effect transistors with non-hysteretic steep sub-60 mV/dec swing and defect-passivated multidomain switching," in *Proc. Symp. VLSI Technol.*, Jun. 2019, pp. T224–T225.

[41] K. J. Singh, A. Bulusu, and S. Dasgupta, "Multidomain negative capacitance effect in P(VDF-TrFE) ferroelectric capacitor and passive voltage amplification," *IEEE Trans. Electron Devices*, vol. 67, no. 11, pp. 4696–4700, Nov. 2020.

[42] A. M. Glazer, "The classification of tilted octahedra in perovskites," *Acta Crystallograph. B, Struct. Crystallogr. Crys. Chem.*, vol. 28, no. 11, pp. 3384–3392, Nov. 1972.

[43] A. Saeidi, F. Jazaeri, I. Stolichnov, and A. M. Ionescu, "Double-gate negative-capacitance MOSFET with PZT gate-stack on ultra thin body SOI: An experimentally calibrated simulation study of device performance," *IEEE Trans. Electron Devices*, vol. 63, no. 12, pp. 4678–4684, Dec. 2016, doi: 10.1109/TED.2016.2616035.

[44] S. Singh, S. Singh, N. Kumar, N. K. Singh, R. Ranjan, and S. Anand, "Lead zirconium titanate (PZT)-based gate-all-around negative-capacitance junctionless nanowire FET for distortionless low-power applications," *J. Electron. Mater.*, vol. 51, no. 1, pp. 196–206, Jan. 2022.

[45] A. V. Bune, V. M. Fridkin, S. Ducharme, L. M. Blinov, S. P. Palto, A. V. Sorokin, S. G. Yudin, and A. Zlatkin, "Two-dimensional ferroelectric films," *Nature*, vol. 391, pp. 874–877, Feb. 1998, doi: 10.1038/36069.

[46] Y. Y. Choi, J. Hong, D. S. Leem, M. Park, H. Song, T. H. Sung, and K. No, "Spin-coated ultrathin poly(vinylidene fluoride-co-trifluoroethylene) films for flexible and transparent electronics," *J. Mater. Chem.*, vol. 21, pp. 5057–5062, Jan. 2011.

[47] F. A. McGuire, Z. Cheng, K. Price, and A. D. Franklin, "Sub-60 mV/decade switching in 2D negative capacitance field-effect transistors with integrated ferroelectric polymer," *Appl. Phys. Lett.*, vol. 109, no. 9, pp. 093101–093106, 2016.

[48] H. Ishiwara, "Current status of ferroelectric-gate Si transistors and challenge to ferroelectric-gate CNT transistors," *Curr. Appl. Phys.*, vol. 9, pp. 2–6, Jan. 2009.

[49] M. Si, P.-Y. Liao, G. Qiu, Y. Duan, and P. D. Ye, "Ferroelectric field-effect transistors based on MoS_2 and $CuInP_2S_6$ two-dimensional van der Waals heterostructure," *ACS Nano*, vol. 12, no. 7, pp. 6700–6705, Jul. 2018.

[50] A. Liaqat, Y. Yin, S. Hussain, W. Wen, J. Wu, Y. Guo, C. Dang, C.-H. Ho, Z. Liu, P. Yu, Z. Cheng, and L. Xie, "An all two-dimensional vertical heterostructure graphene/$CuInP_2S_6$/MoS_2 for negative capacitance field effect transistor," *Nanotechnology*, vol. 33, pp. 125703–125710, Dec. 2022.

[51] T. S. Böscke, S. Teichert, D. Bräuhaus, J. Müller, U. Schröder, U. Böttger, and T. Mikolajick, "Phase transitions in ferroelectric silicon doped hafnium oxide," *Appl. Phys. Lett.*, vol. 99, no. 11, pp. 112904–112906, 2011.

[52] J. Müller, T. S. Böscke, D. Bräuhaus, U. Schröder, U. Böttger, J. Sundqvist, P. Kücher, T. Mikolajick, and L. Frey, "Ferroelectric $Zr_{0.5}Hf_{0.5}O_2$ thin films for nonvolatile memory applications," *Appl. Phys. Lett.*, vol. 99, no. 11, pp. 112901–112903, 2011.

[53] S. Mueller, J. Mueller, A. Singh, S. Riedel, J. Sundqvist, U. Schroeder, and T. Mikolajick, "Incipient ferroelectricity in Al-doped HfO_2 thin films," *Adv. Funct. Mater.*, vol. 22, no. 11, pp. 2412–2417, Jun. 2012.

[54] S. Starschich and U. Boettger, "An extensive study of the influence of dopants on the ferroelectric properties of HfO_2," *J. Mater. Chem. C*, vol. 5, no. 2, pp. 333–338, 2017.

[55] U. Schroeder, S. Mueller, J. Mueller, E. Yurchuk, D. Martin, C. Adelmann, T. Schloesser, R. V. Bentum, and T. Mikolajick, "Hafnium oxide based CMOS compatible ferroelectric materials," *ECS J. Solid State Sci. Technol.*, vol. 2, no. 4, pp. N69–N72, 2013.

[56] U. Schroeder, E. Yurchuk, J. Müller, D. Martin, T. Schenk, P. Polakowski, C. Adelmann, M. I. Popovici, S. V. Kalinin, and T. Mikolajick, "Impact of different dopants on the switching properties of ferroelectric hafniumoxide," *Jpn. J. Appl. Phys.*, vol. 53, no. 8S1, pp. 08LE02–08LE06, 2014.

[57] G. Walters, A. Shekhawat, N. G. Rudawski, S. Moghaddam, and T. Nishida, "Tiered deposition of sub-5 nm ferroelectric $Hf_{1-x}Zr_xO_2$ films on metal and semiconductor substrates," *Appl. Phys. Lett.*, vol. 112, no. 19, pp. 192901–192905, 2018.

[58] S. S. Cheema et al., "Enhanced ferroelectricity in ultrathin films grown directly on silicon," *Nature*, vol. 580, no. 7804, pp. 478–482, 2020.

[59] C. Jundong, H. Weihua, Y. Chong, Z. Xiaosong, G. Yangyan, Z. Xiaodi, and Y. Fuhua, "Research progress of ferroelectric negative capacitance field effect transistor," *Acta Phys. Sinica*, vol. 69, no. 13, pp. 137701–137729, 2020.

[60] G. Pahwa, T. Dutta, A. Agarwal, and Y. S. Chauhan, "Compact model for ferroelectric negative capacitance transistor with MFIS structure," *IEEE Trans. Electron Devices*, vol. 64, no. 3, pp. 1366–1374, Mar. 2017, doi: 10.1109/TED.2017.2654066.

[61] G. Pahwa, A. Agarwal, and Y. S. Chauhan, "Numerical investigation of short-channel effects in negative capacitance MFIS and MFMIS transistors: Subthreshold behavior," *IEEE Trans. Electron Devices*, vol. 65, no. 11, pp. 5130–5136, Nov. 2018, doi: 10.1109/TED.2018.2870519.

[62] C. Gastaldi, A. Saeidi, M. Cavalieri, I. Stolichnov, P. Muralt, and A. M. Ionescu, "Transient negative capacitance of silicon-doped HfO_2 in MFMIS and MFIS structures: Experimental insights for hysteresis-free steep slope NC FETs," in *IEDM Tech. Dig.*, Dec. 2019, pp. 23.5.1–23.5.4.

[63] A. Singh and S. K. Sinha, "Performance analysis of device characteristics in negative capacitance field effect transistor," in *Proc. 2nd Int. Conf. Electron. Sustain. Commun. Syst. (ICESC)*, Aug. 2021, pp. 236–239.

[64] J. Dong, Z. Sheng, R. Yu, W. Hu, Y. Wang, H. Sun, D. W. Zhang, P. Zhou, and Z. Zhang, "WSe_2 N-type negative capacitance field-effect transistor with indium low Schottky barrier contact," *Adv. Electron. Mater.*, vol. 8, no. 2, pp. 2100829–2100835, 2022.

[65] J. Huo, W. Huang, F. Zhang, S. Zhang, W. Gan, Q. Huo, Y. Cai, Q. Zhang, Y. Li, H. Zhu, H. Yin, and Z. Wu, "Investigation on negative capacitance FinEFT beyond 7 nm node from device to circuit," *Microelectron. J.*, vol. 116, pp. 105196–105204, Aug. 2021.

[66] A. Singh, S. K. Sinha, and S. Chander, "Impact of Fe material thickness on performance of raised source overlapped negative capacitance tunnel field effect transistor (NCTFET)," *Silicon*, vol. 14, pp. 9083–9090, Jan. 2022, doi: 10.1007/s12633-022-01696-6.

[67] H. Mehta and H. Kaur, "Impact of interface layer and metal workfunction on device performance of ferroelectric junctionless cylindrical surrounding gate transistors," *Superlattices Microstruct.*, vol. 111, pp. 194–205, Nov. 2017.

[68] F. I. Sakib, M. A. Hasan, and M. Hossain, "Negative capacitance gate-all-around tunnel FETs for highly sensitive label-free biosensors," *IEEE Trans. Electron Devices*, vol. 69, no. 1, pp. 311–317, Jan. 2022.

[69] N. Thoti and Y. Li, "Design of GAA nanosheet ferroelectric area tunneling FET and its significance with DC/RF characteristics including linearity analyses," *Nanosc. Res. Lett.*, vol. 17, no. 1, p. 53, Dec. 2022.

[70] Y. Li, Y. Lian, K. Yao, and G. S. Samudra, "Evaluation and optimization of short channel ferroelectric MOSFET for low power circuit application with BSIM4 and Landau theory," *Solid State Electron.*, vol. 114, pp. 17–22, Dec. 2015.

[71] S. Choudhary, D. Schwarz, H. S. Funk, D. Weishaupt, R. Khosla, S. K. Sharma, and J. Schulze, "A steep slope MBE-grown thin p-Ge channel FETs on bulk Ge-on-Si using HZO internal voltage amplification," *IEEE Trans. Electron Devices*, vol. 69, no. 5, pp. 2725–2731, May 2022, doi: 10.1109/TED.2022.3161857.

[72] Y. C. Lin, G. B. Rayner, J. Cardenas, and A. D. Franklin, "Short-channel robustness from negative capacitance in 2D NC-FETs," *Appl. Phys. Lett.*, vol. 118, no. 10, pp. 101903–101907, 2021.

[73] H. Tian, Y.-X. Li, L. Li, X. Wang, R. Liang, Y. Yang, and T.-L. Ren, "Negative capacitance black phosphorus transistors with low SS," *IEEE Trans. Electron Devices*, vol. 66, no. 3, pp. 1579–1583, Mar. 2019, doi: 10.1109/TED.2018.2890576.

[74] K. Tamersit, M. K. Q. Jooq, and M. H. Moaiyeri, "Computational investigation of negative capacitance coaxially gated carbon nanotube field-effect transistors," *IEEE Trans. Electron Devices*, vol. 68, no. 1, pp. 376–384, Jan. 2021, doi: 10.1109/TED.2020.3037277.

[75] J. P. Duarte, S. Khandelwal, A. I. Khan, A. Sachid, Y.-K. Lin, H.-L. Chang, S. Salahuddin, and C. Hu, "Compact models of negative-capacitance FinFETs: Lumped and distributed charge models," in *IEDM Tech. Dig.*, Dec. 2016, pp. 30.5.1–30.5.4, doi: 10.1109/IEDM.2016.7838514.

[76] W.-X. You, P. Su, and C. Hu, "Evaluation of NC-FinFET based subsystem-level logic circuits," *IEEE Trans. Electron Devices*, vol. 66, no. 4, pp. 2004–2009, Apr. 2019, doi: 10.1109/TED.2019.2898445.

[77] M.-J. Tsai, P.-J. Chen, D.-B. Ruan, F.-J. Hou, P.-Y. Peng, L.-G. Chen, and Y.-C. Wu, "Investigation of 5-nm-Thick $Hf_{0.5}Zr_{0.5}O_2$ ferroelectric FinFET dimensions for sub-60-mV/decade subthreshold slope," *IEEE J. Electron Devices Soc.*, vol. 7, pp. 1033–1037, 2019, doi: 10.1109/JEDS.2019.2942381.

[78] S. Zhang, "Review of modern field effect transistor technologies for scaling," *J. Phys., Conf. Ser.*, vol. 1617, no. 1, Aug. 2020, Art. no. 012054.

[79] Y. G. Xiao, Z. J. Chen, M. H. Tang, Z. H. Tang, S. A. Yan, J. C. Li, X. C. Gu, Y. C. Zhou, and X. P. Ouyang, "Simulation of electrical characteristics in negative capacitance surrounding-gate ferroelectric field-effect transistors," *Appl. Phys. Lett.*, vol. 101, no. 25, pp. 253511–253514, 2012.

[80] C. Jiang, R. Liang, J. Wang, and J. Xu, "A carrier-based analytic theory for electrical simulation of negative capacitance surrounding gate ferroelectric capacitor," in *Proc. IEEE 15th Int. Conf. Nanotechnol. (IEEE-NANO)*, Jul. 2015, pp. 834–837, doi: 10.1109/NANO.2015.7388741.

[81] C. Jiang, R. Liang, J. Wang, and J. Xu, "Analytical drain current model for long-channel gate-all-around negative capacitance transistors with a metal–ferroelectric–insulator–semiconductor structure," *Jpn. J. Appl. Phys.*, vol. 55, no. 2, pp. 024201–024207, 2016.

[82] N. M. M. Hossain, S. Quader, A. B. Siddik, and M. I. B. Chowdhury, "TCAD based performance analysis of junctionless cylindrical double gate all around FET up to 5 nm technology node," in *Proc. 20th Int. Conf. Comput. Inf. Technol. (ICCIT)*, Dec. 2017, pp. 22–24.

[83] L. Wang, A. Shafaei, and M. Pedram, "Gate-all-around FET based 6T SRAM design using a device-circuit co-optimization framework," in *Proc. IEEE 60th Int. Midwest Symp. Circuits Syst. (MWSCAS)*, Aug. 2017, pp. 1113–1116.

[84] S.-Y. Lee, H.-W. Chen, C.-C. Chung, C.-H. Shen, P.-Y. Kuo, Y.-E. Huang, H.-Y. Chen, and T.-S. Chao, "Investigation of the impact of internal metal gate—From MFM capacitors to two-layer-stacked GAA poly-Si NW FE-FETs," in *Proc. Int. Symp. VLSI Technol., Syst. Appl. (VLSI-TSA)*, Aug. 2020, pp. 124–125.

[85] S.-Y. Lee, H.-W. Chen, C.-H. Shen, P.-Y. Kuo, C.-C. Chung, Y.-E. Huang, H.-Y. Chen, and T.-S. Chao, "Experimental demonstration of performance enhancement of MFMIS and MFIS for 5-nm × 12.5-nm poly-Si nanowire gate-all-around negative capacitance FETs featuring seed-layer and PMA-free process," in *Proc. Silicon Nanoelectronics Workshop (SNW)*, Jun. 2019, pp. 1–2, doi: 10.23919/SNW.2019.8782939.

[86] D. Madadi and A. A. Orouji, "Investigation of 4H-SiC gate-all-around cylindrical nanowire junctionless MOSFET including negative capacitance and quantum confinements," *Eur. Phys. J. Plus*, vol. 136, no. 7, p. 785, Jul. 2021.

[87] A. A. M. Mazumder, K. Hosen, M. S. Islam, and J. Park, "Numerical investigations of nanowire gate-all-around negative capacitance GaAs/InN tunnel FET," *IEEE Access*, vol. 10, pp. 30323–30334, 2022, doi: 10.1109/ACCESS.2022.3159809.

[88] F. I. Sakib, M. A. Hasan, and M. Hossain, "Exploration of negative capacitance in gate-all-around Si nanosheet transistors," *IEEE Trans. Electron Devices*, vol. 67, no. 11, pp. 5236–5242, Nov. 2020, doi: 10.1109/TED.2020.3025524.

[89] G. Pahwa, T. Dutta, A. Agarwal, and Y. S. Chauhan, "Physical insights on negative capacitance transistors in nonhysteresis and hysteresis regimes: MFMIS versus MFIS structures," *IEEE Trans. Electron Devices*, vol. 65, no. 3, pp. 867–873, Mar. 2018.

[90] M. Hoffmann, M. Pešić, S. Slesazeck, U. Schroeder, T. Mikolajick, and T. Mikolajick, "Modeling and design considerations for negative capacitance field-effect transistors," in *Proc. Joint Int. EUROSOI Workshop Int. Conf. Ultimate Integr. Silicon (EUROSOI-ULIS)*, Apr. 2017, pp. 1–4.

[91] M. Hoffmann, M. Pešić, S. Slesazeck, U. Schroeder, and T. Mikolajick, "On the stabilization of ferroelectric negative capacitance in nanoscale devices," *Nanoscale*, vol. 10, pp. 10891–10899, 2018.

[92] F. I. Sakib, M. A. Hasan, and M. Hossain, "Performance analysis of nanowire and nanosheet NCFETs for future technology nodes," *Eng. Res. Exp.*, vol. 3, no. 4, pp. 045022–045044, 2021.

[93] W. Huang, H. Zhu, K. Jia, X. Yin, C. Li, Y. Zhang, J. Xiang, Z. Wu, and L. Gan, "Simulations of VNW-FETs with adjustable spacer-like negative capacitors based on experimental data," *ECS J. Solid State Sci. Technol.*, vol. 8, no. 2, pp. Q38–Q42, 2019.

[94] S. Semwal, V. P. Reddy, N. Jaiswal, and A. Kranti, "Limits on hysteresis-free sub-60 mV/decade operation of MFIS nanowire transistor," *IEEE Trans. Electron Devices*, vol. 67, no. 9, pp. 3868–3875, Sep. 2020, doi: 10.1109/TED.2020.3008888.

[95] K. Jang, T. Saraya, M. Kobayashi, and T. Hiramoto, "I_{on}/I_{off} ratio enhancement and scalability of gate-all-around nanowire negative-capacitance FET with ferroelectric HfO_2," *Solid-State Electron.*, vol. 136, pp. 60–67, Oct. 2017, doi: 10.1016/j.sse.2017.06.011.

[96] F. I. Sakib, F. E. Mullick, S. Shahnewaz, S. Islam, and M. Hossain, "Influence of device architecture on the performance of negative capacitance MFMIS transistors," *Semicond. Sci. Technol.*, vol. 35, no. 2, pp. 025005–025011, 2020.

[97] W. Lü, X. Chen, B. Liu, Z. Xie, M. Guo, and M. Zhao, "Comprehensive performance enhancement of a negative-capacitance nanosheet field-effect transistor with a steep sub-threshold swing at the sub-5-nm node," *Microelectron. J.*, vol. 120, pp. 105363–105368, Feb. 2022.

[98] M. Y. Kao, S. Salahuddin, and C. Hu, "Negative capacitance enables GAA scaling VDD to 0.5 V," *Solid-State Electron.*, vols. 181–182, pp. 108010–108015, Apr. 2021.

[99] W. Huang, H. Zhu, Z. Wu, X. Yin, Q. Huo, K. Jia, Y. Li, and Y. Zhang, "Investigation of negative DIBL effect and Miller effect for negative capacitance nanowire field-effect-transistors," *IEEE J. Electron Devices Soc.*, vol. 8, pp. 879–884, 2020, doi: 10.1109/JEDS.2020.3015492.

[100] A. D. Gaidhane, G. Pahwa, A. Verma, and Y. S. Chauhan, "Compact modeling of drain current, charges, and capacitances in long-channel gate-all-around negative capacitance MFIS transistor," *IEEE Trans. Electron Devices*, vol. 65, no. 5, pp. 2024–2032, May 2018, doi: 10.1109/TED.2018.2813059.

[101] A. D. Gaidhane, G. Pahwa, A. Dasgupta, A. Verma, and Y. S. Chauhan, "Compact modeling of negative capacitance nanosheet FET including quasi-ballistic transport," in *Proc. 4th IEEE Electron Devices Technol. Manuf. Conf. (EDTM)*, Apr. 2020, pp. 1–4, doi: 10.1109/EDTM47692.2020.9117841.

[102] Y. Kim, Y. Seon, S. Kim, J. Kim, S. Bae, I. Yang, C. Yoo, J. Ham, J. Hong, and J. Jeon, "Analytical current–voltage modeling and analysis of the MFIS gate-all-around transistor featuring negative-capacitance," *Electron.*, vol. 10, no. 10, pp. 1177–1189, 2021, doi: 10.3390/electronics10101177.

[103] M. H. Lee, K.-T. Chen, C.-Y. Liao, S.-S. Gu, G.-Y. Siang, Y.-C. Chou, H.-Y. Chen, J. Le, R.-C. Hong, Z.-Y. Wang, S.-Y. Chen, P.-G. Chen, M. Tang, Y.-D. Lin, H.-Y. Lee, K.-S. Li, and C. W. Liu, "Extremely steep switch of negative-capacitance nanosheet GAA-FETs and Fin-FETs," in *IEDM Tech. Dig.*, Dec. 2018, pp. 31.8.1–31.8.4, doi: 10.1109/IEDM.2018.8614510.

[104] S.-Y. Lee, H. W. Chen, C. H. Shen, P. Y. Kuo, C. C. Chung, Y. E. Huang, H. Y. Chen, and T. S. Chao, "Experimental demonstration of stacked gate-all-around poly-Si nanowires negative capacitance FETs with internal gate featuring seed layer and free of post-metal annealing process," *IEEE Electron Device Lett.*, vol. 40, no. 11, pp. 1708–1711, Nov. 2019, doi: 10.1109/LED.2019.2940696.

[105] S.-Y. Lee, H.-W. Chen, C.-H. Shen, P.-Y. Kuo, C.-C. Chung, Y.-E. Huang, H.-Y. Chen, and T.-S. Chao, "Effect of seed layer on gate-all-around poly-Si nanowire negative-capacitance FETs with MFMIS and MFIS structures: Planar capacitors to 3-D FETs," *IEEE Trans. Electron Devices*, vol. 67, no. 2, pp. 711–716, Feb. 2020, doi: 10.1109/TED.2019.2958350.

[106] S.-Y. Lee, C.-C. Lee, Y.-S. Kuo, S.-W. Li, and T.-S. Chao, "Ultrathin sub-5-nm $Hf_{1-x}Zr_xO_2$ for a stacked gate-all-around nanowire ferroelectric FET with internal metal gate," *IEEE J. Electron Devices Soc.*, vol. 9, pp. 236–241, 2021, doi: 10.1109/JEDS.2021.3056438.

[107] C. J. Su et al., "Ge nanowire FETs with $HfZrO_x$ ferroelectric gate stack exhibiting SS of sub-60 mV/dec and biasing effects on ferroelectric reliability," in *IEDM Tech. Dig.*, Dec. 2017, pp. 15.4.1–15.4.4, doi: 10.1109/IEDM.2017.8268396.

[108] W. Chung, M. Si, P. R. Shrestha, J. P. Campbell, K. P. Cheung, and P. D. Ye, "First direct experimental studies of $Hf_{0.5}Zr_{0.5}O_2$ ferroelectric polarization switching down to 100-picosecond in sub-60 mV/dec germanium ferroelectric nanowire FETs," in *Proc. IEEE Symp. VLSI Technol.*, Jun. 2018, pp. 89–90.

[109] Y.-N. Chen, F.-J. Hou, C.-J. Su, and Y.-C. Wu, "Study of germanium nanosheet channel with negative capacitance field-effect-transistor," in *Proc. Silicon Nanoelectron. Workshop (SNW)*, Jun. 2019, pp. 1–2.

[110] Y.-W. Lin, T.-Y. Yu, C.-J. Su, Y.-N. Chen, H.-H. Chang, G.-L. Luo, C.-T. Wu, W.-F. Wu, K.-L. Lin, F.-J. Hou, Y.-C. Wu, and W.-K. Yeh, "Sub-60 mV/dec germanium nanowire field-effect transistors with 2-nm-thick ferroelectric $Hf_{0.5}Zr_{0.5}O_2$," in *Proc. IEEE Int. Symp. VLSI Technol., Syst. Appl. (VLSI-TSA)*, Apr. 2021, pp. 1–2.

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