IEEE Access
Multidisciplinary : Rapid Review : Open Access Journal

Received 28 December 2022, accepted 4 February 2023, date of publication 9 February 2023, date of current version 16 February 2023.

Digital Object Identifier 10.1109/ACCESS.2023.3243578

RESEARCH ARTICLE

Quantitative Hot Carrier Injection Analysis of N-Type Tunnel Field-Effect Transistors

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This work was supported by the National Research Foundation (NRF) of Korea funded by the Ministry of Science and ICT (MSIT) under Grant NRF-2021M3F3A2A01037927, NRF-2022M3F3A2A01073944 (Intelligent Semiconductor Technology Development Program), Grant NRF-2022M3I7A1078544 (Process-In-Memory Semiconductor Technology Development Program), and Grant NRF-2021R1A2C1007931 (Mid-Career Researcher Program).

ABSTRACT The hot carrier injection (HCI) of tunnel field-effect transistors (TFETs) is analyzed quantitatively under various conditions in terms of HCI-induced gate current (I_G), HCI probability (I_G/I_D), potential energy, and lateral/vertical electric field for the first time. For example, the I_G and I_G/I_D of TFETs are predicted in comparison with those of metal-oxide semiconductor FETs (MOSFETs) with the variation of gate voltage (V_G), drain voltage (V_D), gate insulator thickness (T_{ins}), and channel length (L_{ch}). According to the simulation results, TFETs show higher HCI probability than MOSFETs under the entire bias conditions because the former features strong peak lateral field at source-channel junction. For example, TFETs show $\sim 1.8 \times 10^2$x higher HCI current and $\sim 5.9 \times 10^6$x higher HCI probability than MOSFETs at $V_G = 4$ V and $V_D = 3$ V. The optimal HCI bias condition of TFETs is also analyzed.

INDEX TERMS Tunnel field-effect transistors (TFETs), metal-oxide field-effect transistors (MOSFETs), hot carrier injection.

I. INTRODUCTION

Tunnel field-effect transistors (TFET) have emerged as one of the most promising extremely low-power electron devices owing to their abrupt on-off switching, low off-current, weak temperature dependence, and CMOS process compatibility [1], [2]. Recently, reliability issues of TFETs have been studied extensively [3], [4], [5], [6], [7]. TFETs feature a strong peak electric field on the source side, leading to the following problems: work function variation [3], hot carrier degradation, and bulk/interface trap generation [4], [5], [6], [7]. It was revealed that the source-side bulk traps generated by the hot carrier injection (HCI) were the main causes of the threshold voltage shift of TFETs [6]. By contrast, HCI can contribute to TFET-based flash memory for extremely low-power applications [8], [9], [10]. Also, by using HCI, weight can be updated in both floating-gate memory and SONOS memory for analog in-memory-computing [10], [12], [13]. Thus, quantitative analysis of HCI has become an important research topic in TFETs. Although TFETs show more severe HCI than metal-oxide field-effect transistors (MOSFET), to the best of our knowledge, contrary to MOSFETs, the HCI of TFETs has rarely been analyzed quantitatively. Previously, for example, it was reported that TFETs have more serious hot carrier degradation effects \than MOSFETs [4], [6]. However, the HCI rate and its maximum bias condition of TFETs still remain unknown. Even though some papers discussed the HCI of TFET-based flash memory cells, they showed only the HCI probability with the drain voltage (V_D), gate insulator thickness (T_{ins}), and channel length (L_{ch}) fixed [14], [15]. Also, most of previous HCI analyses of TFETs were based on the lucky-electron model [16], which has a low model accuracy of gate current (I_G) and maximum HCI location.

In this work, the HCI of TFETs was analyzed quantitatively in comparison with that of MOSFETs. The current,

The associate editor coordinating the review of this manuscript and approving it for publication was Huamin Li.

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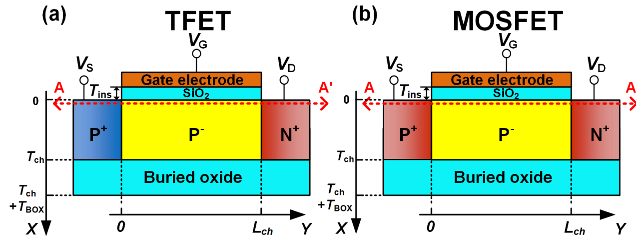

FIGURE 1. Simulated structure of (a) a TFET and (b) a MOSFET.

TABLE 1. Summarized reference device parameter values.

Parameters	TFETs	MOSFETs
L_{ch}	200 nm	200 nm
T_{ins}	3 nm	3 nm
T_{ch}	20 nm	20 nm
T_{BOX}	100 nm	100 nm
Source doping concentration (N_S)	1×10^{20} cm^{-3} (p-type)	1×10^{20} cm^{-3} (n-type)
Drain doping concentration (N_D)	1×10^{20} cm^{-3} (n-type)	1×10^{20} cm^{-3} (n-type)
Channel doping concentration	1×10^{16} cm^{-3} (p-type)	1×10^{16} cm^{-3} (p-type)

current density, and probability of HCI are discussed under various bias conditions and device dimensions using technology computer-aided design (TCAD) simulation. Using the accurate HCI model based on spherical harmonic expansion of the Boltzmann transport equation (SHE-BTE), the HCI of TFETs was analyzed quantitatively. Based on the simulation results, the bias condition for the optimal HCI of TFETs was analyzed. Also, HCI programming operations of both TFET-based and MOSFET-based flash memories were compared.

II. DEVICE STRUCTURE AND SIMULATION METHODOLOGY

For the quantitative HCI analysis, two-carrier and two-dimensional device simulations were performed using a commercial TCAD simulator [17]. Dynamic nonlocal band-to-band tunneling, Shockley-Read-Hall recombination, Philips unified mobility model, and Fermi distribution were used. Precisely calculated A and B parameters of Kane's model are used for band-to-band tunneling [18]. The I_G was calculated using the SHE-BTE HCI model, which includes the nonlocal carrier energy and carrier distribution [19]. Also, SHE-BTE model is used for the precise HCI analysis because it is the most accurate HCI model in commercial TCAD simulator which shows the consistent result with Monte-Carlo method even in the case of short channel MOSFETs [20].

Fig. 1 shows the simulated n-type fully depleted silicon-on-insulator (FD-SOI) TFET and MOSFET. For a fair comparison, both devices had the same device structure and parameters, except for the source doping type. T_{ch} and T_{BOX} represent the thicknesses of SOI and buried oxide (BOX) layers, respectively. The detailed simulation parameters are presented in Table 1.

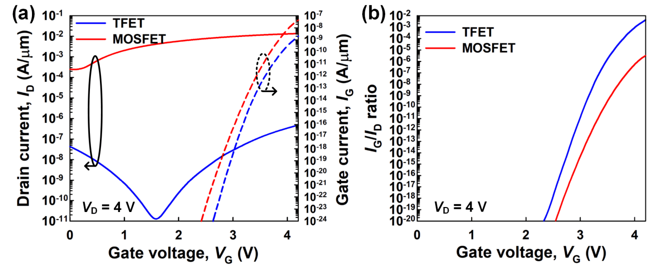

FIGURE 2. (a) I_D-*vs.*-V_G, I_G-*vs.*-V_G and (b) I_G/I_D-*vs.*-V_G curves of TFETs and MOSFETs.

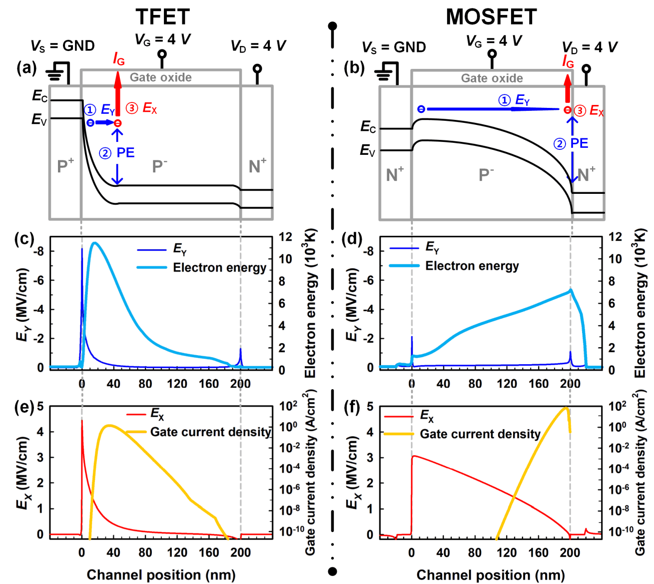

FIGURE 3. HCI mechanisms and their key parameters (E_Y, PE, and E_X) of (a) TFETs and (b) MOSFETs with the reference bias and dimension. First, electrons accelerated by peak E_Y gain electron energy from PE and become hot electrons. Second, HCI occurs by redirection of electron movement to gate electrode because of E_X. E_Y and electron energy of (c) TFETs and (d) MOSFETs. E_X and gate current density of (e) TFETs and (f) MOSFETs. Maximum HCI point of TFETs and MOSFETs are located at 34 nm and 195 nm in the channel position, respectively.

All electrical properties are extracted at the silicon channel surface following A-A' cutline, as shown in Fig. 1. In this study, only hot electron injection is considered because avalanche-generated holes and secondary electrons are negligible in both n-channel FD-SOI TFETs [21] and MOSFETs without body bias [19], [22]. Thus, I_G and the ratio of I_G to the drain current (I_D) correspond to the HCI current and HCI probability, respectively. The electron energy is the average electron kinetic energy calculated using SHE-BTE. The source voltage (V_S) is fixed at 0 V.

III. RESULTS AND DISCUSSION

Before discussing the influence of bias conditions and device dimensions on the HCI, TFETs and MOSFETs were compared under the reference bias and dimension conditions. The reference bias condition was $V_G = V_D = 4$ V, and the reference device dimensions are summarized in Table 1. Fig. 2 shows the simulated I_D-*vs.*-V_G, I_G-*vs.*-V_G, and

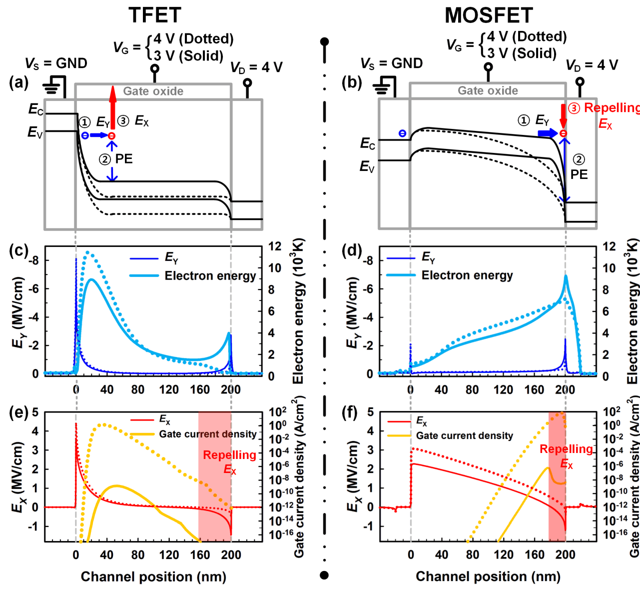

FIGURE 4. Three key HCI parameters with the variation of V_G in the case of (a) TFETs and (b) MOSFETs. As V_G decreases, both E_Y and PE decrease in TFETs while only E_Y increases in MOSFETs. However, because of negative V_{GD}, E_X repels the hot electrons away from the gate electrode in MOSFETs. E_Y and electron energy of (c) MOSFETs and (d) TFETs. E_X and gate current density of (e) MOSFETs and (f) TFETs. Maximum HCI point of MOSFETs and are located at 51 nm and 176 nm in the channel position, respectively.

I_G/I_D-*vs.*-V_G curves of TFETs and MOSFETs. At the reference bias, the I_D of TFETs and MOSFETs are $\sim$0.341 μA/μm and $\sim$13 mA/μm, respectively. Thus, TFETs feature a $\sim 3.8 \times 10^4$x lower I_D than MOSFETs. The significantly low I_D of TFET is induced because of the current mechanism [23]. The I_g of TFETs and MOSFETs are $\sim$0.314 nA/μm and $\sim$7.04 nA/μm, respectively. TFETs show more lower I_G than that of the MOSFETs because I_G, which is a result of HCI, is a function of the I_D [18]. Therefore, TFETs feature a $\sim$22.4x lower I_G and $\sim 1.7 \times 10^3$x higher I_G/I_D than MOSFETs at $V_G = V_D = 4$ V reference bias condition. The higher I_G/I_D implies that TFETs have a higher HCI efficiency than MOSFETs. The underlying physics is explained in Fig. 3, which compares the HCI mechanisms of MOSFETs and TFETs under the reference bias condition. As shown in Figs. 3a and 3b, the HCI is affected by the following three HCI parameters: peak lateral electric field (E_Y), potential energy (PE), and vertical electric field (E_X) [16], [24]. The first two HCI parameters determine the electron energy required to overcome the 3.1-eV Si-SiO$_2$ energy barrier height. The probability that electrons gain energy by the first two HCI parameters can be expressed as follows [24]:

$$P = \exp\left[-\frac{1}{eE}\int_0^{\varepsilon}\frac{d\varepsilon'}{v(\varepsilon')\tau(\varepsilon')}\right] \tag{1}$$

where e and E are electronic charge the lateral electric field, respectively; v is electron velocity; τ is the mean time between scatterings; ε is the electron energy.

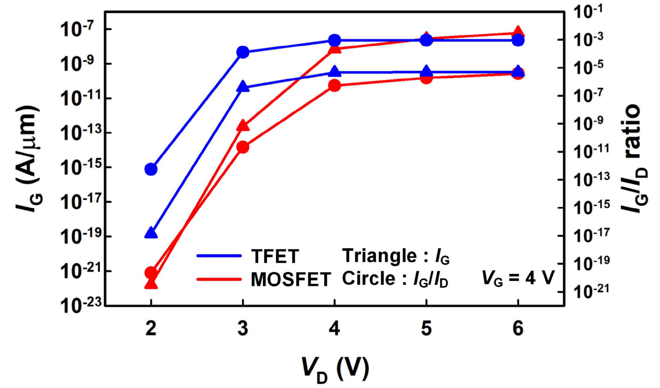

FIGURE 5. I_G and I_G/I_D ratio of TFETs and MOSFETs with the variation of V_D at $V_G = 4$ V.

While the third parameter determines the probability of momentum redirection and transmission towards the gate and image barrier height, which can be expressed as follows [19]:

$$\Gamma(\varepsilon) = \exp\left(-\frac{2}{\hbar}\int_0^{t_{ins}}\sqrt{2m_{ins}[E_B(r)-\varepsilon]}\Theta\left[E_B(r)-\varepsilon\right]dr\right) \tag{2}$$

$$E_B(r) = E_{B0} + qF_{ins} + E_{im}(r) \tag{3}$$

where m_{ins} is the insulator effective mass; F_{ins} is the insulator field, E_{im} and E_{B0} are the image barrier lowering effect and the 3.1-eV Si-SiO$_2$ energy barrier height, respectively; τ is the mean time between scatterings; Θ is the step function. In the case of TFETs, the peak E_Y and abrupt PE drop occur around the source-to-channel junction owing to their p-i-n structure [25], [26]. This induces a lag in the electron energy behind the peak E_Y, resulting in strong electron velocity overshoots and eventually high electron energy as the probability of gaining energy increases following (1) [27]. Thus, the electrons accelerated by E_Y obtain the highest electron energy around the source-channel junction where strong E_X induced by the positive gate-source voltage (V_{GS}) is applied, as shown in Figs. 3c and 3e. It is observed that the peak HCI of TFETs occurs around the source-channel junction. Note that the peak HCI point corresponds to the location where I_G density is maximum. In contrast, in the case of MOSFETs, peak E_Y and PE drop are observed around the drain pinch-off region where weak E_X is applied due to the gate-drain voltage (V_{GD}), as shown in Figs. 3d and 3f. Thus, the hot electrons are more easily delivered towards gate electrode in TFETs than MOSFETs as the higher probability of momentum redirection is induced following (2) thanks to stronger E_Y. In summary, TFETs are more HCI-efficient than MOSFETs because all three and only the two HCI parameters contribute to the HCI process in the case of the former and latter, respectively. Moreover, MOSFETs have dispersed E_Y and PE drop over the channel under the reference bias condition, which lowers electron energy.

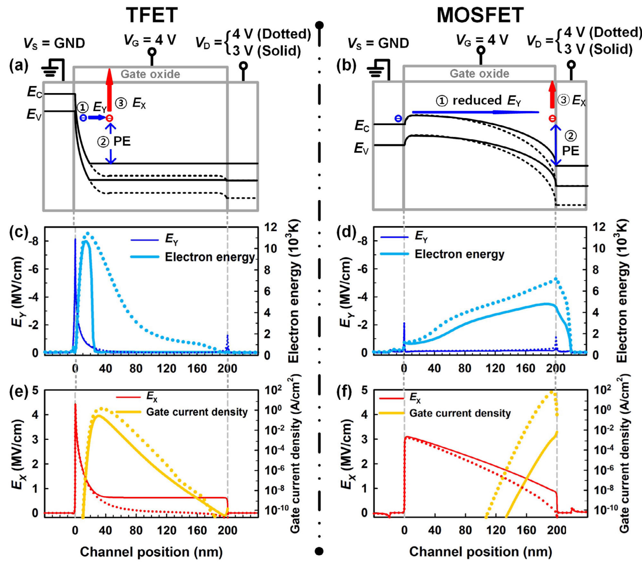

FIGURE 6. HCI mechanisms and their key parameters of (a) TFETs and (b) MOSFETs as a function of V_D. Only PE decreases in TFETs while both E_Y and PE decrease in MOSFETs. E_Y and electron energy of (c) MOSFETs and (d) TFETs. E_X and gate current density of (e) MOSFETs and (f) TFETs. Maximum HCI point of TFETs and MOSFETs are located at 30 nm and 200 nm in the channel position, respectively.

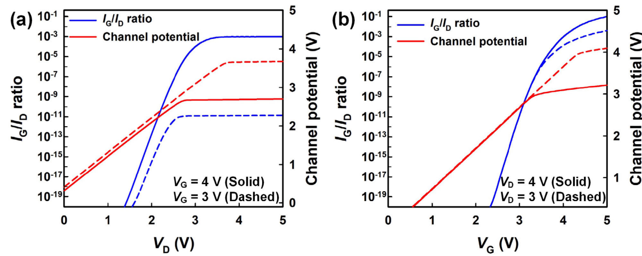

FIGURE 7. I_G/I_D and Ψ_{CH} of TFETs with the variation of (a) V_D and (b) V_G.

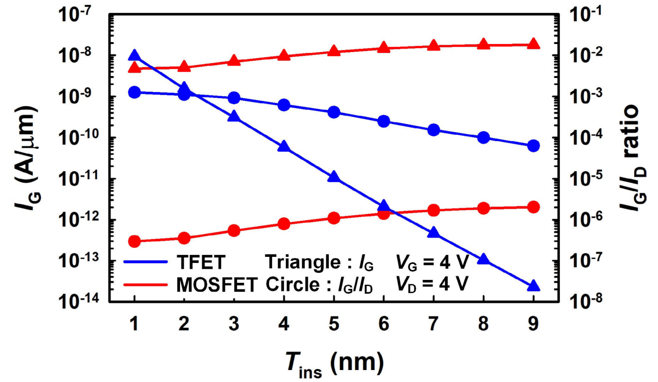

FIGURE 8. I_G and I_G/I_D ratio of TFETs and MOSFETs with the variation of T_{ins} at V_G = 4 V and V_D = 4 V.

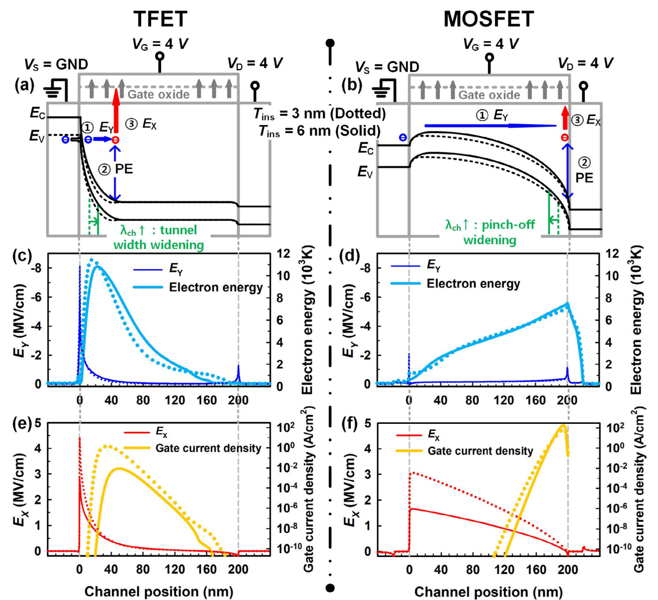

FIGURE 9. HCI mechanisms and their key parameters of (a) TFETs and (b) MOSFETs as a function of T_{ins}. E_Y decreases in TFETs while E_Y increases in MOSFETs. E_Y and electron energy of (c) MOSFETs and (d) TFETs. E_X and gate current density of (e) MOSFETs and (f) TFETs. Maximum HCI point of TFETs and MOSFETs are located at 50 nm and 194 nm in the channel position, respectively.

A. HCI WITH THE VARIATION OF BIAS CONDITIONS

In this section, V_G becomes lower than that of the reference bias condition to compare the HCI of TFETs and MOSFETs under the $V_G < V_D$ condition. When V_G and V_D are 3 and 4 V, respectively, TFETs have ∼19.8x lower I_G and ∼4.8 × 10^3x higher I_G/I_D than MOSFETs, as shown in Fig. 2. This implies that TFETs exhibit higher HCI efficiency than MOSFETs, even under $V_G < V_D$ conditions. Fig. 4 shows the reason for this. Negative V_{GD} induces negative E_X around the channel-drain junction, which repels hot electrons away from the gate. In the case of MOSFETs, even if the electron energy increases as V_G decreases owing to the increased peak E_Y as shown in Fig. 4d, the peak HCI occurring at the channel-drain junction is disturbed by the negative E_X as shown in Fig. 4f. In contrast, the HCI of TFETs is rarely affected by the negative E_X. Thus, even if a lower V_G reduces E_Y, PE, and finally the electron energy in the case of TFETs, the peak HCI occurs around the source-channel junction where high electron energy and strong positive E_X remain, as shown in Figs. 4c and 4e.

Subsequently, the HCI of TFETs and MOSFETs were compared under the $V_G > V_D$ condition by lowering V_D as shown in Fig. 5. MOSFETs exhibit more abrupt I_G and I_G/I_D reductions than TFETs as V_D decreases. Note that TFETs show ∼1.8 × 10^2x higher I_G and ∼5.9 × 10^6x higher I_G/I_D than MOSFETs at V_G = 4 V and V_D = 3 V. Figs. 6a and 6b show the reason for this. Among the three HCI parameters, as V_D decreases, TFETs experience only PE reduction, whereas MOSFETs experience both E_Y and PE reduction. The peak E_Y of TFETs rarely changes because it depends only on V_G. Thus, lower V_D reduces the electron energy of MOSFETs more than that of the TFETs, as shown in Figs. 6c and 6d. In addition, the strong E_X of TFETs lowers the Si-SiO_2 energy barrier height owing to the image charge

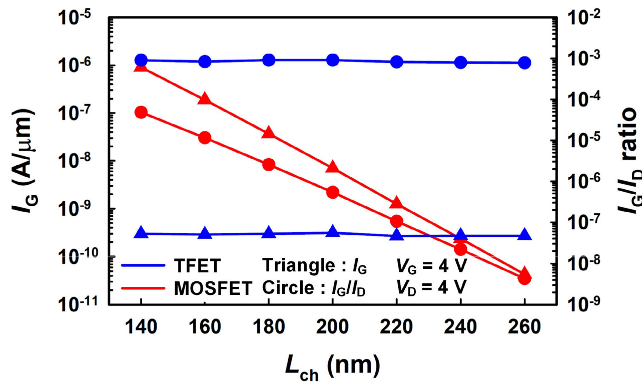

FIGURE 10. I_G and I_G/I_D ratio of TFETs and MOSFETs with the variation of L_{ch}.

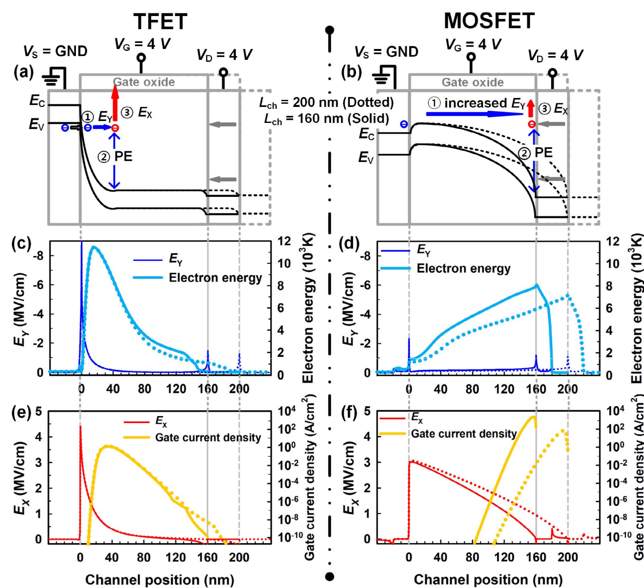

FIGURE 11. HCI mechanisms and their key parameters of (a) TFETs and (b) MOSFETs as a function of L_{ch}. All three parameters of TFETs do not change while E_Y increases in MOSFETs as L_{ch} decreases. E_Y and electron energy of (c) MOSFETs and (d) TFETs. E_X and gate current density of (e) MOSFETs and (f) TFETs. Maximum HCI point of TFETs and MOSFETs are located at 34 nm and 157 nm in the channel position, respectively.

effects [19], [24]. This makes the HCI of TFETs efficient even at V_D = 3V, while high V_D is needed for the HCI programming of MOSFET-based flash memory [28], [29]. Thus, TFETs are more HCI-efficient than MOSFETs under all bias conditions.

Finally, the optimal HCI bias condition of the TFETs can be determined where the PE saturates. Fig. 7 shows I_G/I_D and channel potential (Ψ_{CH}) as functions of V_D and V_G. Ψ_{CH} is used to extract PE because PE is $q\cdot(\Psi_{CH} - V_S)$ in TFETs [30], which becomes $q \cdot \Psi_{CH}$ at $V_S = 0$ V. Ψ_{CH} is extracted in the middle of the channel. Fig. 7 shows that both I_G/I_D and Ψ_{CH} saturate when V_G - V_D is equal to 0.26 V, which corresponds to threshold voltage (V_{th}). The V_{th} of TFETs is defined as V_G when Ψ_{CH} saturates [30], [31]. Thus, the optimal HCI condition of TFETs is $V_G - V_{th} = V_D$.

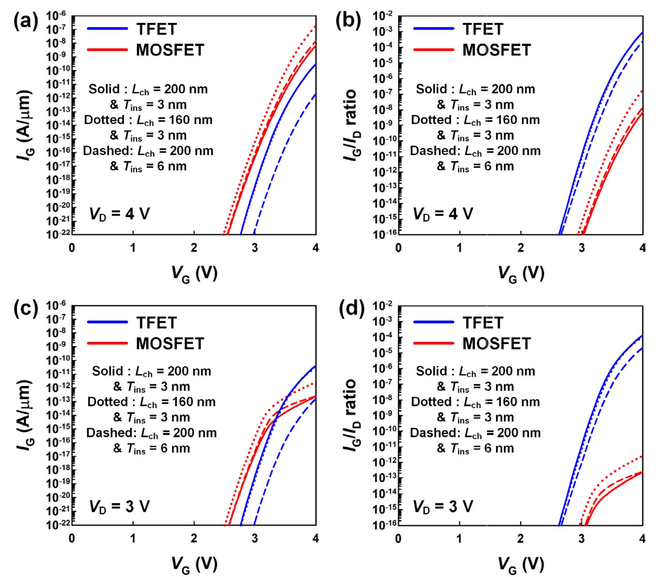

FIGURE 12. (a) I_G-*vs.*-V_G curves and (b) I_G/I_D-*vs.*-V_G curves of TFETs and MOSFETs with various device dimensions at V_D = 4 V. (c) I_G-*vs.*-V_G curves and (d) I_G/I_D-*vs.*-V_G curves of TFETs and MOSFETs with various device dimensions at V_D = 3 V.

B. HCI WITH THE VARIATION OF DEVICE DIMENSIONS

The HCI of TFETs and MOSFETs were compared for various device dimensions: T_{ins} and L_{ch}. First, the dependency of HCI on T_{ins} is discussed. Under the reference bias condition, with the increment of T_{ins}, both I_G and I_G/I_D of TFETs decrease, while those of MOSFETs increase, as shown in Fig. 8. T_{ins} affect the channel screening length (λ_{ch}) by adjusting the gate controllability [32], [33]. Larger T_{ins} lowers the peak E_Y of TFETs because of λ_{ch} increase, which decreases the peak electron energy, as shown in Figs. 9a and 9c. Thus, in the case of TFETs, large T_{ins} lowers the peak E_Y and electron energy as well as the peak E_X, which suppresses HCI, as shown in Fig. 9e. However, MOSFETs exhibit the opposite trend because of the widening of the pinch-off region. Larger T_{ins} boost the peak E_Y at the channel-drain junction owing to λ_{ch} increase and raises the electron energy, as shown in Fig. 9d. Thus, E_X weakened by T_{ins} increase is compensated by the higher electron energy [34]. Thus, contrary to MOSFETs, TFETs become more HCI-efficient as T_{ins} decreases. This implies that TFET-based flash memory can achieve a low operating voltage with high immunity to short-channel effects.

Subsequently, Fig. 10 compares the HCI s of both the devices in terms of L_{ch}. It is observed that L_{ch} reduction rarely affects the I_G and I_G/I_D of TFETs, whereas it significantly increases those of MOSFETs because the former has stronger short-channel effect immunity than the latter [35]. In the case of TFETs, all the three HCI parameters are independent of L_{ch} as shown in Fig. 11a. In contrast, in the case of MOSFETs, short-channel effects boost the peak E_Y, electron energy, and HCI rate while reducing E_X as L_{ch} decreases. In other words, the higher electron energy limited by the weak E_X makes

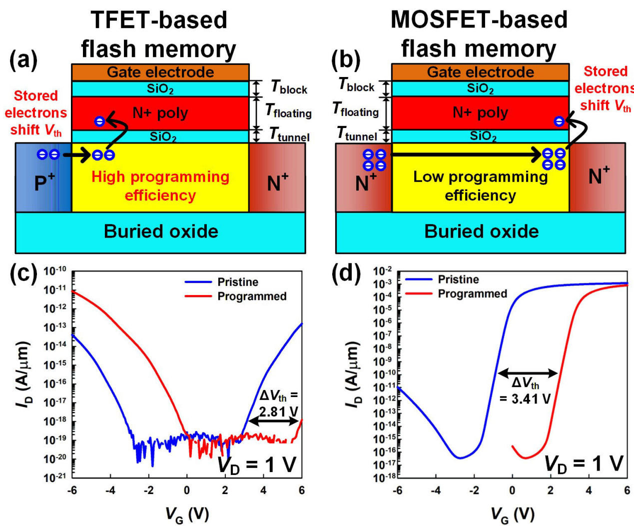

FIGURE 13. Structure and program mechanism of (a) TFET-based flash and (b) MOSFET-based flash memories. By using HCI, electrons are injected in the floating gate region (N^+ poly silicon). Transfer curves of (c) TFET-based flash and (d) MOSFET-based flash memories.

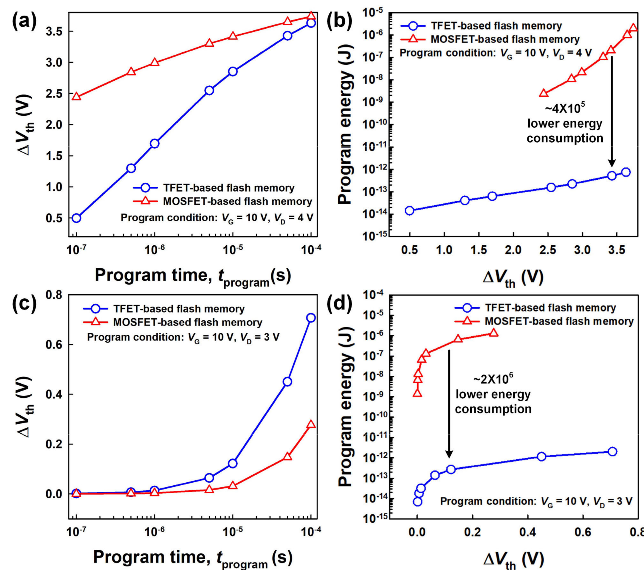

FIGURE 14. Simulated (a) ΔV_{th} as a function of $t_{program}$ and (b) program energy as a function of ΔV_{th} in both TFET-based and MOSFET-based flash memories at $V_G = 10$ V, $V_D = 4$ V program bias condition. Simulated (c) ΔV_{th} as a function of $t_{program}$ and (d) program energy as a function of ΔV_{th} in both TFET-based and MOSFET-based flash memories at $V_G = 10$ V, $V_D = 3$ V program bias condition.

MOSFETs less HCI efficient than TFETs. Also, although high HCI efficiency is expected in the case of short-channel MOSFET-based flash memory, severe short channel effects induce poor gate controllability which limits the downscaling of MOSFET-based flash memory [36].

Finally, the HCIs of TFETs and MOSFETs were compared under various bias and dimension conditions. As shown in Figs. 12a and 12b, even if TFETs have a lower I_G than MOSFETs, the former shows higher I_G/I_D than the latter, regardless of the dimensions under the reference bias. Furthermore, under the $V_G > V_D$ condition, TFETs show higher I_G and I_G/I_D than MOSFETs, regardless of the dimension conditions, as shown in Figs. 12c and 12d. It is confirmed that TFETs show higher I_G/I_D under all simulated conditions and higher I_G under $V_G > V_D$ conditions than MOSFETs.

C. EXTREMELY LOW POWER PROGRAMMING OPERATION IN TFET-BASED FLASH MEMORY

The high HCI probability of TFETs can be utilized for the implementation of TFET-based flash memory for extremely-low power programming. TFET-based flash memory will be compared with MOSFET-based one. Figs. 13a and 13b show the simulated structures and program mechanism of both kinds of memory cells. N^+ poly-silicon floating gates are used whose doping concentration is 1×10^{20} cm^{-3}. T_{tunnel}, $T_{floating}$, and T_{block} mean the bottom oxide thickness, floating gate thickness, and blocking oxide thickness, respectively. T_{tunnel}, $T_{floating}$ and T_{block} are 8 nm, 20 nm, and 15 nm, respectively [37], [38]. L_{ch}, T_{ch}, T_{box}, N_S, and N_D of both kinds of flash memory cells are the same as in Table 1. Figs. 13c and 13d show the simulated I_D-*vs.*-V_G curves of TFET-based and MOSFET-based flash memory cells under the pristine and programmed state. Using constant current method, V_{th} is extracted at $I_D = 10^{-17}$ A/μm for TFET-based flash and 10^{-10}A/μm for MOSFET-based one. By performing HCI program ($V_G = 10$ V, $V_D = 4$ V, and $t_{program} = 10$ μs, where $t_{program}$ means program time), V_{th} shifts (ΔV_{th}'s) of TFET-based and MOSFET-based flash memory cells are 2.85 V and 3.41 V, respectively. Even if TFET-based flash shows smaller ΔV_{th}'s than MOSFET-based one due to lower I_G, the former is superior to the latter in terms of program energy thanks to HCI-efficient program. Fig. 14 shows ΔV_{th}'s of both cases as a function of $t_{program}$ and program energy ($V_D \cdot I_D \cdot t_{program}$). As shown in Figs. 14a and 14b, despite longer $t_{program}$, TFET-based flash memory only consumes 0.52 pJ to achieve $\Delta V_{th} = 3.42$ V at $V_G = 10$ V, $V_D = 4$ V program condition, which is $\sim 4 \times 10^5$x lower than MOSFET-based one. Figs. 14c and 14d show the program case with lower V_D ($V_G = 10$ V, $V_D = 3$ V program condition), TFET-based flash memory shows $\sim 2 \times 10^6$x lower program energy than MOSFET-based one in addition to shorter $t_{program}$ because the HCI of TFETs is less sensitive to V_D than that of MOSFETs. High HCI program efficiency of TFET-based flash memory will be helpful for extremely low-power neuromorphic applications where on-chip weight training is frequently occurs.

IV. CONCLUSION

The HCI of TFETs was quantitatively analyzed in comparison with that of MOSFETs with variations in V_G, V_D, T_{ins}, and L_{ch}. TFETs show higher I_G/I_D than MOSFETs under the entire bias condition, meeting the two requirements simultaneously: high electron energy and strong E_X. However, MOSFETs can satisfy only one of these requirements. It was

revealed that the optimal HCI bias condition of TFETs is $V_G - V_{th} = V_D$. It is confirmed that TFET-based flash memory features lower program power consumption and higher program efficiency than MOSFET-based flash memory.

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