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RESEARCH ARTICLE

Analysis and Design of a 2-40.5 GHz Low Noise Amplifier With Multiple Bandwidth Expansion Techniques

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ABSTRACT This paper analyzes the main factors limiting the bandwidth expansion of low-noise amplifiers (LNA) and designs a broadband LNA with a bandwidth of 2-40.5 GHz. The LNA is designed using multiple bandwidth expansion methods, including cascode, resistance feedback, and cascode Darlington amplifier. The amplitude-frequency characteristics and bandwidth expansion principle of the three structures are studied theoretically based on the small-signal equivalent circuit model. Thanks to these techniques, a three-stage LNA is designed in a 0.15-μm GaAs pseudomorphic high-electron-mobility (pHEMT) process. The measured results show that the designed LNA achieves an average gain of 21.6 dB in 2-40.5 GHz while maintaining a noise figure (NF) below 3.6 dB. The measured output 1-dB gain compression point (OP1 dB) is from 4.5 to 12.8 dBm and the input/output return loss are better than 5 dB. The chip area is only 1.57 mm^2, including input and output test pads.

INDEX TERMS Bandwidth expansion, broadband amplifier, gain roll-off of the transistor, monolithic microwave integrated circuit (MMIC), low-noise amplifier (LNA), parasitic capacitance.

I. INTRODUCTION

Ultra-wideband communication (UWC) is a short- and medium-range wireless interconnection technology developed in recent years [1], [2]. Due to its advantages such as higher data transmission rate, less power consumption, and stronger anti-interference capability, UWC has become a hot spot for research and development in the field of wireless communication today and is considered as one of the key technologies for next-generation wireless communication. With the development of the UWC, the markets demand for lower power consumption, smaller sizes, and lower-cost wireless communication devices are gradually increasing. Wideband transceivers for multiple vendors and applications can significantly reduce costs, which has accelerated the research and manufacturing of wideband transceivers [3], [4]. As an important component of the radio frequency (RF) front-end of ultra-wideband wireless communication systems, it is important to promote the design of high-performance wideband low-noise amplifiers (LNA).

Academically, many high-performance broadband low-noise amplifiers are reported. In [5], a cascode distributed amplifier (DA) is designed to achieve a 0.1-45 GHz low noise amplifier. However, the loss of the artificial transmission line is inevitable, making it difficult for DA to achieve a high gain. And DA is not suitable in many cases because of low unity-gain bandwidth, high noise figure (NF), and large area. In [6], a transformer feedback technique is proposed to compensate for transistor gain roll-off with frequency, and a broadband LNA is finally realized for 18-43 GHz applications. A frequency-dependent feedback structure is employed to achieve a 0.1-23 GHz LNA in [7]. Nevertheless, the thermal noise of the resistors introduced in this configuration deteriorates the NF. An alternative seven-octave bandwidth LNA using combination techniques of feedback and inductive peaking techniques is

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proposed in [8]. However, its bandwidth is only extended to 20 GHz.

In this paper, we analyze the effect of the parasitic capacitance of transistors on bandwidth detailly and propose a three-stage broadband LNA. In the designed LNA, different amplification structures are used for the three-stage amplifier, the amplitude-frequency characteristics of the three structures are analyzed separately, and the rationality of the theoretical derivation is verified by experimental simulation. Finally, the designed LNA achieves a bandwidth range of 2-40.5 GHz.

The remainder of this paper is organized as follows: Section II investigates the effect of the three parasitic capacitances of the transistor on the bandwidth of the transistor; Section III analyzes the amplitude-frequency properties and bandwidth expansion principles of the three proposed amplification structures. Section IV presents the simulation and measurement results; Section V summarizes the conclusions drawn from this study.

II. ANALYSIS OF THE FACTORS AFFECTING AMPLIFIER BANDWIDTH EXPANSION

The gain roll-off characteristic [9] of transistors is an important aspect that influences the bandwidth of the amplifier. It means that the maximum available gain (MAG) of the transistor does not remain the same as the frequency increases, but will show a gradual decrease in an approximately inverse relationship, as shown in Fig. 1. The gain roll-off of the transistor causes an uneven gain in broadband, which is unacceptable in the design of a broadband LNA. To further explore the factors affecting the bandwidth expansion of the amplifier, this paper studies the effects of gate-drain parasitic capacitance C_{gd}, source-drain parasitic capacitance C_{ds} and gate-source parasitic capacitance C_{gs} on the basis of the small-signal equivalent circuit model of the common-source amplifier. The equivalent small-signal circuit model of the common-source amplifier is shown in Fig. 2.

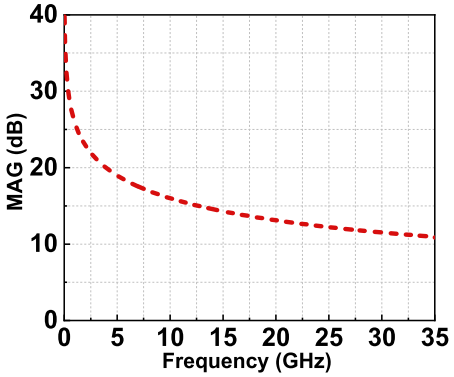

FIGURE 1. The characteristic curve of the transistor gain roll-off. (The simulation results are based on 0.15-μm GaAs pHEMT process, and the size of the transistor is 4 × 50 μm).

The gate-drain parasitic capacitance C_{gd} is the main contributor causing the gain roll-off [10]. The expression for the characteristic impedance of the parasitic

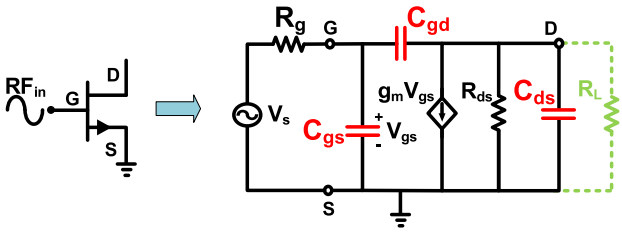

FIGURE 2. The small-signal equivalent circuit of the common source amplifier.

capacitance C_{gd} is:

$$Z_{gd} = \frac{1}{j\omega C_{gd}} \tag{1}$$

where ω is the angular frequency. As can be seen from (1), $|Z_{gd}|$ will gradually decrease as the frequency increases. Therefore, the presence of C_{gd} will provide a path from the input to the output for high-frequency signals, leading to the signals leaking directly to the output without amplification. In addition, the C_{gd} also produces a feedback loop from the output to the input, which severely affects the reverse isolation [11], and the isolation continues to deteriorate with increasing frequency. The impact of isolation on circuit design is primarily in impedance matching, where poor reverse isolation can lead to interactions when performing input impedance matching and output impedance matching [12]. To further investigate the effect of C_{gd} on the gain of the amplifier, we decompose C_{gd} into the input and output terminations with Miller's theorem [13], as shown in Fig. 3. The presence of $m_1 C_{gd}$ will affect the drain current, which can be expressed as:

$$\begin{aligned} i_{ds} \approx g_m V_{gs} &= g_m i_s \left(\frac{1}{j\omega m_1 C_{gd}} \parallel \frac{1}{j\omega C_{gs}} \right) \\ &= g_m i_s \left(\frac{1}{j\omega \left(m_1 C_{gd} + C_{gs} \right)} \right) \end{aligned} \tag{2}$$

where i_s is the input current and m_1 is the Miller multiplication factor. As can be seen from (2), the drain current is smaller at higher frequencies, and can seriously affect the gain of the amplifier. In addition, the presence of $m_2 C_{gd}$ will affect the gain of the amplifier, and the gain can be expressed as:

$$\begin{aligned} A_V &= g_m \cdot Z_{out} = g_m \cdot (R_L \parallel \frac{1}{j\omega C_{ds}} \parallel R_{ds} \parallel \frac{1}{j\omega m_2 C_{gd}}) \\ &= \frac{g_m R_{ds} R_L}{(R_{ds} + R_L) + j\omega R_{ds} R_L (C_{ds} + m_2 C_{gd})} \end{aligned} \tag{3}$$

where R_{ds} is the drain-source parasitic resistance, m_2 is the Miller multiplication factor and R_L is the load impedance. It can be seen from (3) that the gain of the common-source amplifier will continue to decrease as the frequency increases due to the presence of C_{gd} and C_{ds}.

Based on the above analysis, there are two ways to solved the gain roll-off problem: One is to improve the gain flatness

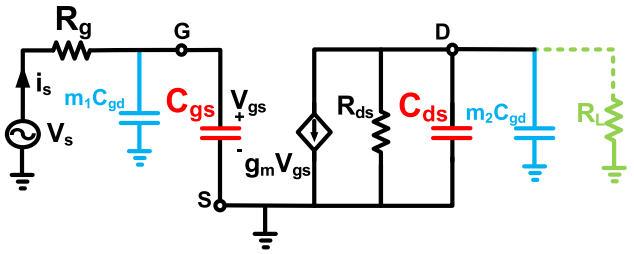

FIGURE 3. The small-signal equivalent circuit of the common source amplifier, where Cgd is decomposed into input and output terminations with Miller's theorem.

in the broadband range by losing a part of the gain in the low frequency band, the other one is to improve the gain flatness in the broadband range by increasing the high-frequency gain.

III. ANALYSIS AND DESIGN OF THE PROPOSED LNA

The simplified schematic of the proposed wideband LNA is shown in Fig. 4. The first stage is a common-source and common-gate amplifier with a resistive feedback network (CSGF). The second stage uses a common-source amplifier with a resistive feedback network (CSF). And the third stage introduces a common-source and common-gate Darlington amplifier (CSGD). The analysis and derivation procedure are shown in sections A, B, and C.

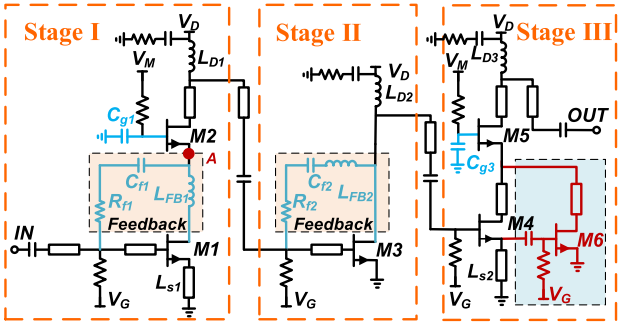

FIGURE 4. The simplified schematic of the proposed wideband LNA.

A. ANALYSIS OF THE CSGF

For CSGF, we can intuitively see that it is constructed by connecting a common-gate amplifier to a conventional common-source amplifier. This can significantly improve the isolation between the input port and the output port [11], [14], and then the gain roll-off characteristic of the amplifier is improved effectively. In addition, the low-frequency power gain can be tuned by the resistance feedback [15].

To facilitate the analysis of the CSGF, we consider it as a common-source amplifier and a common-gate amplifier. As shown in stage I in Fig. 4, the two structures of the amplifier are combined through point A, and their small-signal equivalent circuits are illustrated in Fig. 5.

The small-signal equivalent circuit of the common-source amplifier is illustrated in Fig. 5(b), where R_{f1} in the feedback network is decomposed into input and output terminations

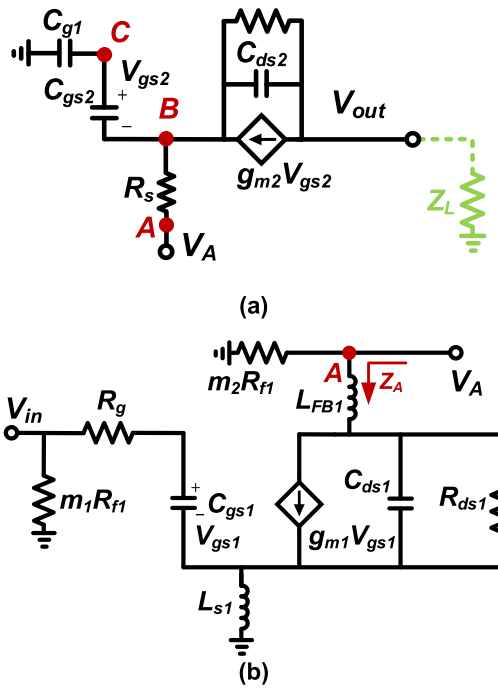

FIGURE 5. The small-signal equivalent circuit of the first stage in Fig. 4, where (a) is the small-signal equivalent model of the common-gate amplifier circuit and (b) is the small-signal equivalent model of the common-source amplifier circuit.

with Miller's theorem. Assuming that the input and output ports are well-matched. The power gain can be expressed as:

$$\begin{aligned} A_V &= g_{m1} Z_A \\ &= g_{m1}\left[m_2 R_{f1} \parallel \left(sL_{FB1} + \frac{1}{sC_{ds1}} \parallel R_{ds1} + sL_{s1}\right)\right] \\ &\approx g_{m1} \frac{m_2 R_{f1}\left[1 + s^2 C_{ds1}\left(L_{FB1} + L_{s1}\right)\right]}{1 + sC_{ds1}\left(sL_{s1} + sL_{FB1} + m_2 R_{f1}\right)}; s = j * \omega \end{aligned} \tag{4}$$

where g_{m1}, C_{ds1}, and R_{ds1} are the transconductance, drain-source parasitic capacitance, and drain-source parasitic resistance. m_1 is the Miller multiplication factor. Once the transistor size and bias voltage are determined, the parasitic capacitance and parasitic resistance of the circuit will be determined, and the frequency response of the circuit will mainly depend on the resistance R_{f1} in the feedback network.

In Equation (4), the power gain will decrease with the decrease of R_{f1}. In order to verify (4), we simulate the MAG changes of the first-stage amplifier under different R_{f1} values, as shown in Fig. 5. In the CSGF, the transistor sizes of M1 and M2 are 2×100 μm and 2×90 μm, respectively, where the value of C_{g1} is kept constant at 0.12 pF. The studied band is set in the range of 0- 50 GHz, which fully covers the operating band of the designed LNA. The simulation results are shown in Fig. 6. It is shown that the resistance value of R_{f1} has a significant impact on the MAG below 25 GHz. The MAG at 10 GHz decreases from 12.3 dB to 8.1 dB as the R_{f1}

changes from 250 to 100 Ω, and then the gain flatness over a wide band range can be tuned by varying the value of R_{f1}.

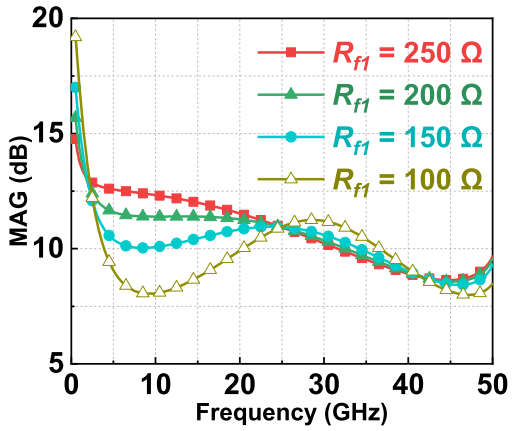

FIGURE 6. The simulated MAG for different values of Rf1 (Rf1 is varied, Cg1 = 0.10 pF, Ls1 = 74 pH).

In addition, for cascaded multistage amplifiers, the noise figure (NF) is formulated [16] as:

$$F = F_1 + \frac{F_2 - 1}{G_1} + \frac{F_3 - 1}{G_1 G_2} + \cdots + \frac{F_n - 1}{G_1 G_2 \cdots G_{n-1}} \quad (5)$$

where F_{n} and G_{n} are the NF and the power gain of the n_{th} stage amplifier, respectively. From (5), it can be seen that the NF of the multi-stage amplifier depends mainly on the first stage. In this design, the thermal noise introduced by the feedback network in the first-stage amplifier causes the deterioration of the noise factor, which needs to be taken care of in the design. Therefore, we simulated the effect of the resistor values in the feedback network on the $\mathrm{NF_{min}}$ of the first-stage amplifier, and the simulation results are shown in Fig. 7. The simulation results show that the smaller the resistance value of R_{f1}, the larger the $\mathrm{NF_{min}}$. In summary, it is almost impossible to obtain the minimum NF and the best gain flatness at the same time, so the value of R_f needs to be chosen reasonably to achieve the optimal design.

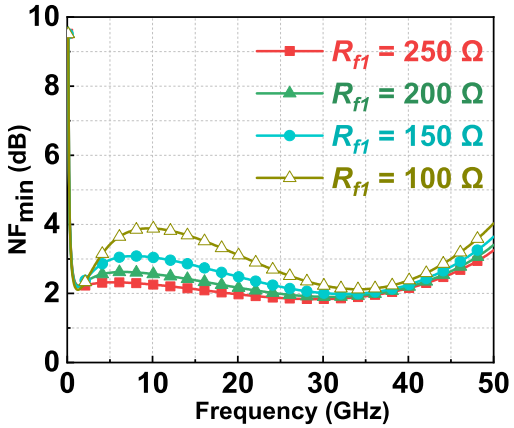

FIGURE 7. The simulated NFmin of the CSGF for different values of Rf1 (Rf1 is varied, Cg1 = 0.10 pF, Ls1 = 74 pH).

The CSGF is used as the input stage of the designed three-stage amplifier, and it is necessary to achieve a good input impedance matching in the broadband range. Therefore, we analyzed the role of the source feedback inductor for input impedance matching [17], [18], and the input impedance of the common-source amplifier can be expressed as:

$$\begin{aligned} Z_{in} &= R_{in} + jX_{in} \\ &= m_1 R_{f1} \parallel \left(R_g + \frac{1}{sC_{gs1}} + sL_{s1} + \frac{g_{m1} L_{s1}}{C_{gs1}} \right) \\ &= m_1 R_{f1} \parallel \left(R_g + \frac{g_{m1} L_{s1}}{C_{gs1}} + \underbrace{j * \left(\omega L_{s1} - \frac{1}{\omega C_{gs1}} \right)}_{imaginary part} \right) \end{aligned} \quad (6)$$

From (6), it can be concluded that the source inductance can offset the imaginary part of the impedance introduced by C_{gs} to a certain extent, making it much easier to achieve a good impedance matching in the broadband range. The effect of different source inductance values on the input impedance matching is simulated and the results are shown in Fig. 8. With the increasing value of source inductance, the input impedance will gradually approach to the impedance matching point, which is conducive to the input impedance matching in the broadband range, and the presence of Ls does not cause a deterioration of the noise factor. [8], [19].

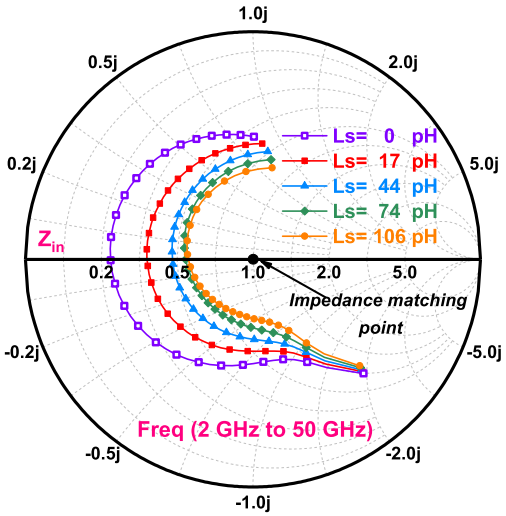

FIGURE 8. The simulated Zin for different values of Ls1 (Ls1 is varied, Cg1 = 0.10 pF, Rf1 = 200 Ω).

The small-signal equivalent model of the common-gate amplifier is shown in Fig. 5(a), and the voltages [20] at nodes B and C can be expressed as:

$$\begin{aligned} V_B &\approx \frac{\frac{1}{sC_{g1}} + \frac{1}{sC_{gs2}}}{\frac{1}{sC_{g1}} + \frac{1}{sC_{gs2}} + R_s} \\ V_A &= \frac{C_{g1} + C_{gs2}}{C_{g1} + C_{gs2} + sC_{g1}C_{gs2}R_s} V_A \end{aligned} \quad (7)$$

$$V_C \approx \frac{\frac{1}{sC_{g1}}}{\frac{1}{sC_{g1}}+\frac{1}{sC_{gs2}}}V_B = \frac{C_{g2}}{C_{g1}+C_{gs2}}V_B \quad (8)$$

$$V_{gs2} = V_C - V_B = -\frac{C_{g1}}{C_{g1}+C_{gs2}+sC_{g1}C_{gs2}R_s}V_A \quad (9)$$

As indicated by (9), V_{gs2} can be changed by adjusting the value of the external capacitor C_{g1}, and thus the gain of the common-gate amplifier can be adjusted. Specifically, the relationship between V_{gs2} and C_{g1} is positively correlated. Fig. 9 presents the simulated MAG at different C_{g1} for the CSGF. The simulated results show that the gain improves significantly after 2.5 GHz for C_{g1} = 0.12 pF relative to C_{g1} = 0.04 pF. The gain roll-off characteristics of the amplifier can be improved by increasing the capacitance of C_{g1}.

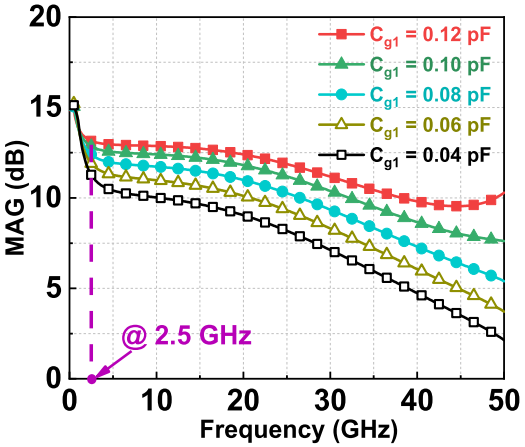

FIGURE 9. The simulated MAG for different values of Cg1 (Cg1 is varied, Ls1 = 74 pH, Rf1 = 200 Ω).

The theoretical analysis and simulation verification in Section III-A indicate that the CSGF can improve the gain roll-off and input impedance matching of the amplifier and realize bandwidth extension by optimizing C_{g1}, R_{f1}, and L_{s1}.

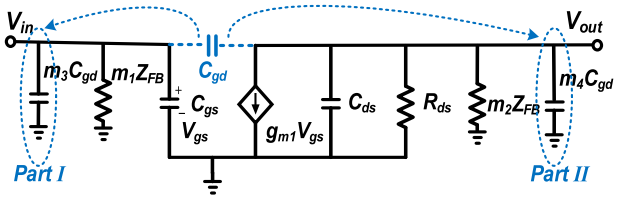

FIGURE 10. The small-signal equivalent circuit of the second stage in Fig. 4.

B. ANALYSIS OF THE CSF

The frequency response of the CSF is mainly determined by the feedback network in the circuit, where the effect of the resistance R_{f2} on the amplitude and frequency characteristics of the amplifier has been described detailly in Section III-A, so we will not repeat it in this subsection. We focus on the effect of the inductor L_{FB2} in the feedback network on the frequency response [7] of the circuit in Section III-B and further indicated the advantages of CSF in the broadband LNA design. The equivalent small-signal circuit model of CSF is shown in Fig. 10. We decompose the feedback network and the gate-drain parasitic capacitance into the input and output terminals with Miller's theorem to simplify the analysis. Then the gain of CSF can be expressed as:

$$A_V = g_m Z_{out} = g_m\left[m_2 Z_{FB} \parallel R_{ds} \parallel \frac{1}{sC_{ds}} \parallel \frac{1}{sm_4 C_{gd}}\right] \quad (10)$$

$$Z_{FB} = \frac{1}{sC_{f2}} + R_{f2} + sL_{FB2} \approx R_{f2} + sL_{FB2} \quad (11)$$

In the feedback network, the effect of C_{f2} on the frequency response is negligible. Here, the main role of C_{f2} is to isolate the DC bias of the gate and drain. Therefore, C_{f2} in (11) is neglected. The gain can be further formulated as:

$$A_V \approx \frac{g_m R_{ds}}{\frac{R_{ds}}{Z_{FB}} + 1 + sR_{ds}\left(C_{ds} + m_4 C_{gd}\right)} \quad (12)$$

As demonstrated by (11), Z_{FB} increases with L_{FB2}, and the increase of Z_{FB} will successively enlarge A_v as indicated by (12). Intuitively, the effect of L_{FB2} on the gain is easily understood. The presence of the inductor inhibits the feedback of the high-frequency signals, and the curtailment effect becomes more significant as the inductor value increases.

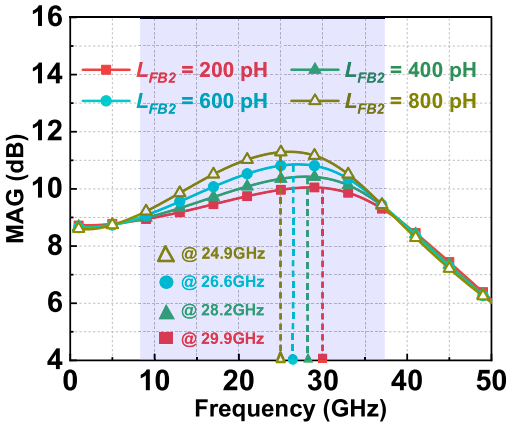

FIGURE 11. The simulated MAG for different values of LFB2 (LFB2 is varied, Rf2 = 150 Ω).

To verify the above analysis, the MAG of the CSF is simulated for different L_{FB2}, and the results are shown in Fig. 11, where M3 is 2 × 100 μm, R_{f2} = 150 Ω, and C_{f2} = 1.5 pF. As demonstrated by Fig. 11, when L_{FB2} increases from 200 pH to 800 pH, the maximum value of MAG will change from 10.2 dB to 11.3 dB. In addition, the frequency point corresponding to the maximum value of MAG gradually shifts to lower frequencies. In Fig. 11, this frequency point gradually decreases from 29.9 GHz to 24.9 GHz. Based on this feature, it is very convenient to compensate the gain at certain frequencies and thus adjust the gain flatness of the multi-stage amplifier.

C. ANALYSIS OF THE CSGD

To simplify the analysis of the CSGD, we use the same study method as in Section III-A. The CSGD is decomposed into two components consisting of a Darlington amplifier and a common-gate amplifier, and it's small-signal equivalent circuit is illustrated in Fig. 12. The characteristics of the common-gate amplifier have been analyzed in detail in Section III-A, so in this subsection we will focus on the characteristics of the Darlington amplifier.

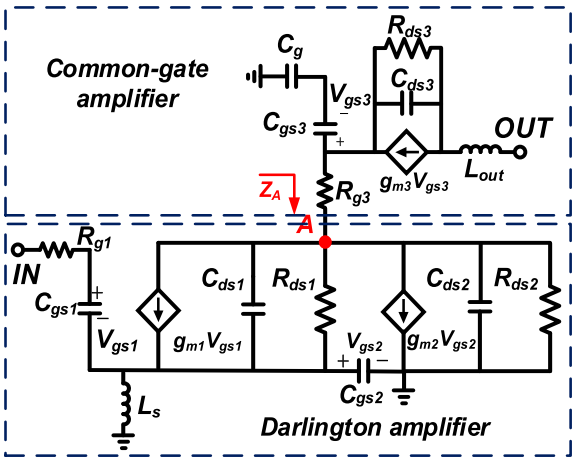

FIGURE 12. The small-signal equivalent circuit of the third stage in Fig. 4.

For a single transistor, the expression for the characteristic frequency is

$$F_T \approx \frac{g_m}{2\pi C_{gs}} \tag{13}$$

where g_{m1} and C_{gs} are the transconductance and gate-source parasitic capacitance. C_{gs1} and C_{gs2} in the Darlington amplifier are connected in series, making the gate-source parasitic capacitance of the Darlington amplifier approximately equal to half of the original one. According to (13), the characteristic frequency of the Darlington amplifier is also approximately equal to twice that of a single transistor without considering the g_m variation [21]. (In fact, the g_m is influenced by the frequency and the operating state of the transistor.) In addition, the bandwidth expansion principle of the Darlington amplifier can be understood by analyzing the equivalent transconductance of the amplifier. Assuming that the drain-source parasitic resistance of the amplifier is neglected, the equivalent transconductance of the Darlington amplifier can be expressed as [22]:

$$G_m = \frac{i_{out}}{v_{in}} \approx \frac{g_{m1}\left(1 + s^2 L_s C_{gs2} + s g_{m2} L_s\right)}{1 + s^2 L_s C_{gs2} + s g_{m1} L_s} \tag{14}$$

where g_{m1} and g_{m2} are the transconductance of M4 and M6. C_{gs2} is the gate-source capacitance of the transistor. As the g_{m1}, g_{m2} and C_{gs2} are determined by the transistor's size and bias voltage, and then the enhancement of the equivalent transconductance G_m can be achieved by adjusting the size and bias voltage conditions of the M4 and M6 transistors.

Then, the gain expression of the Darlington amplifier can be further expressed as:

$$\begin{aligned} A_V &= G_m Z_A \\ &= G_m \left\{ \left[\left(\frac{1}{sC_{ds1}} \parallel R_{ds1} \right) + \left(\frac{1}{sC_{gs2}} + L_s \right) \right] \right. \\ &\qquad \left. \parallel \frac{1}{sC_{ds2}} \parallel R_{ds2} \right\} \end{aligned} \tag{15}$$

According to (15), the gain of the Darlington amplifier is closely related to the parasitic parameters of M6 [23], [24]. Therefore, we simulated the effect of different sizes of M6 on MAG, and the simulation results are shown in Fig. 13.

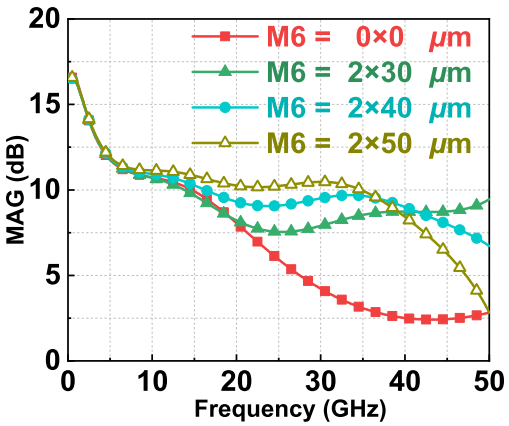

FIGURE 13. The simulated MAG of the CSGD for different sizes of M6.

Based on the simulation results we can conclude that the gain roll-off in the frequency range of 10-50 GHz can be significantly improved when M6 = 2 × 40 μm compared to M6 = 0 × 0 μm (It is a common-source amplifier in this state). When the size of M6 is increased to 2 × 50 μm, it will further improve the gain roll-off in 10-35GHz, but it will cause more drastic gain roll-off in the frequency band range greater than 35 GHz. Therefore, it is necessary to choose the size of M6 to achieve a compromise between gain and gain flatness when designing the amplifier.

D. CIRCUIT DESIGN

To validate the proposed techniques, a three-stage LNA is designed and implemented by 0.15-μm GaAs pHEMT process. Transistors M1-M3 have equal size of 2 × 100 μm, and transistors M4, M5 and M6 have sizes of 2 × 75 μm, 2 × 100 μm and 2 × 40 μm, respectively. The drain to source (V_D) and gate to source (V_G) voltages of M1-M6 are set to 3 V and −0.5 V with a total current of 46 mA. The V_G of all transistors are supplied through by a large resistance of 5980 Ω. In addition, large inductors are connected to the drain nodes of the transistors to prevent RF signals leakage to the drain supply DC terminals [11]. Here, L_{D1} = 1.2 nH, L_{D2} = 0.8 nH and L_{D3} = 1.3 nH. Moreover, for a multi-stage LNA, checking the stability of the input and output ports alone cannot strictly guarantee the stable operation of the amplifier. Therefore, it is necessary to ensure that each

TABLE 1. Performance of Broadband Multistage GaAs MMIC LNAs.

Reference	BW (GHz)	BW* (%)	Gain& (dB)	NF (dB)	OP1dB (dBm)	Pdc (mW)	Area (mm^2)	FOM	GaAs Process
[27] TMTT'2014	2-39.5	180	19.2	2.3-4$^+$	9-12.6+	131	1.76	33.3	0.1-μm pHEMT
[25] TMTT'2015	11-39	112	23	2.1-3.0	8.6	80	2.25	28.2	0.1-μm pHEMT
[6] MWCL'2016	18-43	164	21.6	1.8-2.7	11.5	140	2.00	31.8	0.1-μm pHEMT
[28] TCAS-II'2018	2-43.5	182	15.2	2-2.8	9.5	110	1.88	18.4	0.1-μm pHEMT
[7] TCAS-II'2019	0.1-23	198	27.4	2.7-4$^+$	6.7-8.6	335	1.36	4.2	0.15-μm pHEMT
[29] MWCL'2021	0.01-22	199	23	NA	21	NA	3.75	NA	0.15-μm pHEMT
[30] TCAS-II'2022	2-42	182	14.1	2.1-4.4	14.7	129	1.53	36.6	0.15-μm pHEMT
This work	**2-40.5**	**181**	**21.6**	**3.0-3.6**	**4.5-12.8**	**213**	**1.59**	**30.4**	**0.15-μm pHEMT**

* Defined as the ratio of the bandwidth to center frequency. & Average gain.

stage in the amplifier meets the stability factor $\mu > 1$ [25]. So, we simulated the stability factor μ for each single stage, and the simulation results show that μ is greater than 1 in the frequency band of 0.01-100 GHz.

IV. MEASUREMENT RESULTS

The proposed broadband LNA is designed and fabricated by 0.15-μm pHEMT process. The thickness of the substrate is 100 μm. Fig. 14 shows a micrograph of the LNA with compact 2.1×0.76 mm^2 chip size, including the input/output testing pads and the DC power pads. The measurement setup includes a probe station (Cascade Summit 11000M), a vector network analyzer (Agilent N5244A) and a noise analyzer (Keysight N8976B).

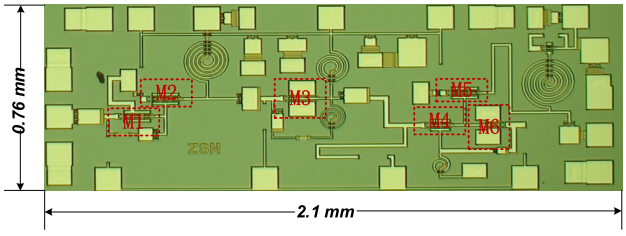

FIGURE 14. The micrograph of the proposed LNA.

A. S-PARAMETERS AND NF SIMULATION AND MEASUREMENT

Fig. 15 presents the simulated and measured S-parameters and the NF of the proposed broadband LNA. The broadband LNA achieves a small-signal gain of 20.1-24.9 dB in 2-40.5 GHz, and the input and output return-loss are better than 5 dB. The measurements show that the designed LNA achieves a NF of less than 3.6 dB in the wideband range.

B. OP1DB MEASUREMENT

Fig. 16 presents the simulated and measured op1db of the proposed broadband lna. The measured results show that the

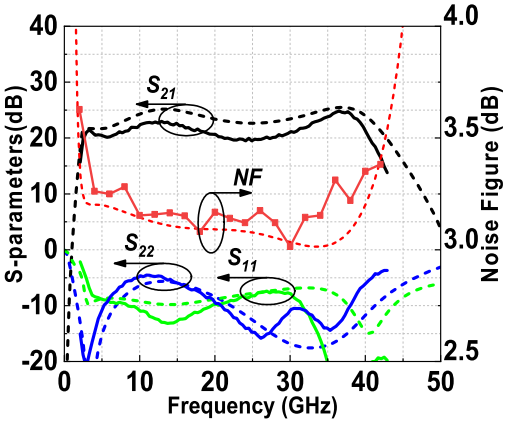

FIGURE 15. Simulated (dashed line) and measured (solid line) S-parameters and NF of the proposed broadband LNA.

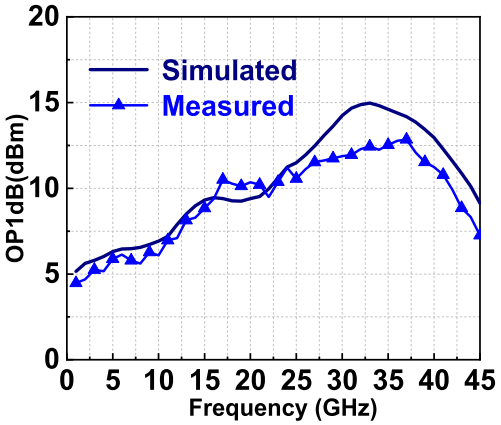

FIGURE 16. Simulated and measured OP1dB of the proposed LNA.

op1db versus frequency is 4.5-12.8 dbm. For wideband lna design, it is difficult to achieve a better than 20db return loss in the operating band. the output return loss in this design is better than 5db, which results in large output power loss and large op1db deviation.

Table 1 summarizes and compares the designed LNA with the reported broadband LNAs. It should be mentioned that the designed broadband LNA not only provides a wide bandwidth of 38.5 GHz, but also achieves a high gain and a low NF. The definition of figure of merit (FOM) can be written as [26]:

$$FOM = \frac{Gain[abs] \cdot OP1dB[mW] \cdot BW_{3dB}[GHz]}{P_{DC}[mW] \cdot (NF - 1)[abs]} \quad (16)$$

V. CONCLUSION

In this paper, the main factors that limiting the bandwidth expansion of LNAs are analyzed theoretically. Various low-noise amplifier structures that can expand the bandwidth are analyzed in detail, including: common-source and common-gate amplifier, resistive feedback structure, source feedback inductors and Darlington amplifier. Their improvements in bandwidth expansion and impedance matching are investigated. Finally, a three-stage broadband LNA is demonstrated and fabricated in a 0.15-μm pHEMT GaAs process based on the above analysis. The final measurements show that the designed LNA has a bandwidth of 2-40.5 GHz, an average gain of 21.6 dB, a minimum NF of 3.0 dB, and a maximum OP1dB of 12.8 dBm. The proposed LNA can be a good candidate for broadband applications.

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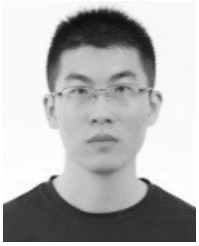

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