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RESEARCH ARTICLE

Analytical Modeling and Design of 27.12 MHz Single-Switch DC–DC Converter With PCB Transformer

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ABSTRACT This paper proposes analytical modeling and design of a 27.12 MHz single-switch dc-dc converter with galvanic isolation using a PCB transformer. The ODE-based analytical approach provides a more accurate circuit design by considering the high-order harmonics and non-ideal components such as the diode capacitances. The proposed dimensionless mathematical model simplifies the design of the desired circuit model and requires less tuning procedure. In addition, the effective analytical model offers the design curves to obtain the optimized circuit parameters at any duty ratio. Meanwhile, the multilayer planar PCB transformer is designed to achieve the isolation and high power density for the high-frequency dc-dc converter. Based on Neumann's formula, the analytical model of the PCB transformer is proposed to calculate the inductances for the spiral structure accurately in the high-frequency conditions. As a result, the computational burden for calculating the coil inductances is alleviated using the proposed method. The simulation and experimental results using a 3W converter prototype verify the effectiveness and feasibility of the analytical modeling and design of the proposed converter.

INDEX TERMS Analytical model, high-frequency, planar PCB transformer, single-switch DC-DC converter, soft-switching.

I. INTRODUCTION

Achieving high power density to reduce the size of devices is becoming increasingly crucial in power electronics. The passive components take a large volume in power converters, especially the magnetic components occupying a significant space in the system. In order to decrease the volume of the passive components, increasing the switching frequency is one efficient way [1], [2], [3], [4].

However, the high switching loss which is proportional to the frequency affects the system's efficiency under high-frequency conditions. Hence, the resonant converter, especially the class E converter with the single-switch topology, has been widely used to relieve the switching loss by achieving soft switching such as zero voltage switching (ZVS) and zero voltage derivative switching (ZVDS) [5], [6], [7]. Since the class E converter leads to the high switch voltage stress up to 3.6−4.4 times of input voltage [8], [9], [10], the other topologies such as class F and class Φ_2 are proposed, which use the high-order harmonic components to reduce the peak of the switch voltage [11], [12], [13], [14], [15], [16]. The design concepts of the resonant converters are also applied to the galvanic isolated converters such as the magnetically isolated class Φ_2 converter using a transformer [17], [18], [19].

The design procedure of the resonant converter in most of the conventional class E and class Φ_2 researches depends on numerous simplifications and assumptions, such as the common sinusoidal approximations and ideal passive components. In particular, with the approximate design procedures

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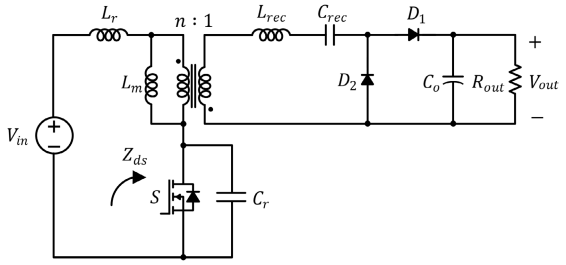

FIGURE 1. Schematic of the isolated dc − dc converter.

in [11], [12], [13], [14], [15], [16], [17], [18], and [19], only the ZVS operation was satisfied, while the complex tuning processes were required. Moreover, when the switching frequency increases, the decreased values of capacitors and inductors become similar to those of the parasitic elements which means the parasitic values have to be considered in the circuit design and analysis. Therefore, as the assumptions induce the differences between the analysis and real-time experiment, considerable parameter tuning is needed after setting an initial value to obtain the optimal operation point empirically.

To solve this problem, previous research used the analytical approach to design the resonant dc-dc converters using ODE-based analysis or harmonic analysis [20], [21]. Since the analytical design procedure does not require such assumptions, the theoretical model shows highly similar tendencies to the actual circuit. However, the parasitic capacitance of the diodes was not considered, which is critical when the switching frequency increases above 10MHz. Besides, the switch duty ratio is not included in the degrees of freedom during the design procedure in [21], which affects the circuit behavior.

Meanwhile, increasing the switching frequency above 10MHz affects the structure of the transformer for the galvanic isolated converter. The core and copper losses of the conventional wire-wound transformer are increased due to the skin and proximity effects under high-frequency conditions. In order to eliminate the core losses, a coreless PCB transformer has been getting attention for high-frequency applications, providing isolation and power transfer [22], [23], [24], [25], [26], [27]. Furthermore, the planar PCB transformer reduces the volume and vertical dimension of the power electronic circuits, which increases the power density. In addition, using PCB traces makes designing and manufacturing inductors and transformers more precise by achieving well consistency and reducing deviation. Previous research investigated the winding loss, core loss, and stray capacitance to achieve optimal parameters of PCB transformers in [32], [33], [34], [35], and [36]. This paper focuses more on the accurate analytical model instead of achieving high efficiency through loss analysis. Since the previous research often uses 3D FEM tools to design the transformer without an accurate PCB model, they suffer from numerous tuning processes. The 3D Finite Element Method (FEM) simulations are more time-consuming than the analytical calculations due to the computational burden and complexity. Therefore, analytical inductance calculation methods such as Neumann's formula, Grover's formula, and Elliptic integrals are used in the design processes [28], [29], [30]. For the spiral planar PCB transformer, the methods in [28] and [29] are used to calculate the inductances, assuming a complete circle or an octagonal structure. For large radii and a number of winding turns, fairly accurate results are given using the approximations; however, a more accurate method is needed to design the smaller spiral PCB transformer.

This paper proposes the analytical modeling and design of the single-switch high-frequency dc-dc converter. The design model with ODE-based circuit analysis reduces the extensive tuning processes and takes into account the high-order harmonics for achieving the low-voltage stress across the switch. The mathematical analysis indicates that the circuit non-idealities and parasitic elements, including the parasitic capacitance of the diodes, play a critical role in the operation modes of the dc-dc converter. The dimensionless system design curves are presented as a function of the duty ratio. These curves help to simplify the converter design process, including the duty ratio as the degree of freedom. Then, the analytical method is proposed to design and analyze the spiral planar PCB transformer for the magnetically isolated converter topology more precisely. When using the design curves of self and mutual inductances calculated by the analytical method, the desired model of the transformer is obtained quickly without any computational burden of 3D FEM simulations. At last, the simulation and experimental results verify the proposed analytical methods of the converter system and planar PCB transformer.

II. DESIGN APPROACH OF THE PROPOSED SYSTEM

FIGURE 1 shows the topology of the isolated dc-dc converter, which consists of two stages: the inverter stage and the rectifier stage. For the rectifier stage, diodes D_1 and D_2 form a half-wave rectifier. The inverter stage is composed of several passive elements and a single-ended switch. The equivalent model of the transformer with the turns ratio of n, is expressed with the magnetizing inductance L_m and leakage inductances absorbed by L_r and L_{rec}. In this paper, the analysis focuses on selecting the duty ratio of the single switch S and values of passive elements in the resonant network to satisfy the low-voltage stress with the ZVS and ZVDS operation.

Using the higher-order harmonic components helps to achieve the low voltage stress and ZVS [14]. FIGURE 2 shows that the third-order harmonic component lowers the peak of the fundamental component. On the other hand, the asymmetric waveform of the second-order harmonic component increases the voltage stress.

Focusing on Z_{ds}, the equivalent impedance seen by the drain-source node of the switch in FIGURE 1, the location of the system pole and zero affects the voltage waveform [14]. Locating the zero at the second-order harmonic and two poles near the fundamental and third-order harmonic realizes the

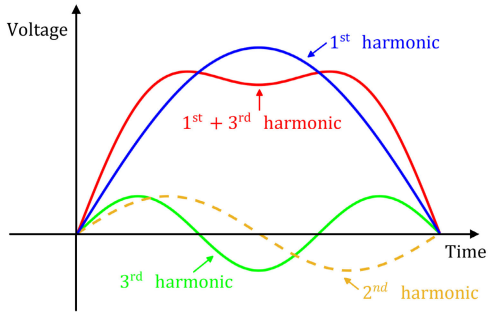

FIGURE 2. Waveform with higher-order harmonic components.

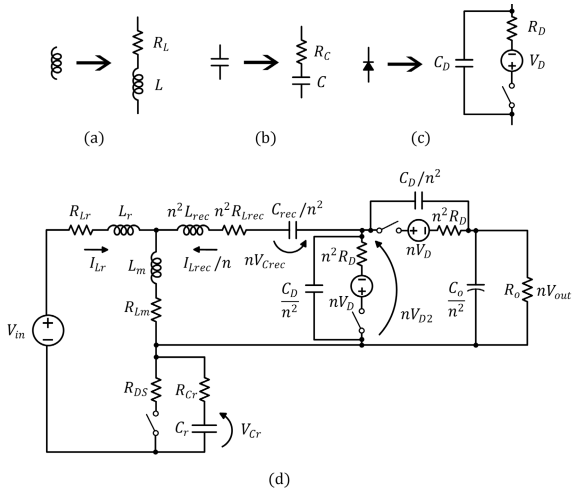

FIGURE 3. Equivalent circuit model of real devices (a) Inductors. (b) Capacitors. (c) Diodes. (d) Equivalent schematic circuit of the isolated dc-dc converter topology of FIGURE 1, including parasitic components

desired voltage waveform shown in FIGURE 2. From [19], Z_{ds} is given by

$$Z_{ds}(s) = \frac{N_1 s^3 + N_2 s}{K_1 s^4 + K_2 s^2 + K_3}$$
$$\begin{cases} N_1 = \left(L_r L_{rec} + L_m L_r/n^2 + L_m L_{rec}\right) C_{rec} \\ N_2 = (L_m + L_r) \\ K_1 = \left(L_r L_{rec} + L_m L_r/n^2 + L_m L_{rec}\right) C_r C_{rec} \\ K_2 = \left(L_r C_r + L_m C_r + L_{rec} C_{rec} + L_m C_{rec}/n^2\right) \\ K_3 = 1 \end{cases} \tag{1}$$

To place the zero of Z_{ds} at second-order harmonic which is $2\omega_{sw}$, where ω_{sw} is the switching frequency, ω_{sw} is derived as

$$\omega_{sw} = \frac{1}{2}\sqrt{\frac{L_m + L_r}{\left(L_r L_{rec} + L_m L_r/n^2 + L_m L_{rec}\right) C_{rec}}}. \tag{2}$$

Defining the first pole near the fundamental as $m_1\omega_{sw}$ and the other pole near the third-order harmonic as $m_3\omega_{sw}$, the conditions derived from the denominator of K_1, K_2, and K_3 in (1) are given by

$$\frac{K_2}{K_1} = \left(m_1^2 + m_2^2\right)\omega_{sw}^2,$$
$$\frac{K_3}{K_1} = m_1^2 m_2^2 \omega_{sw}^4. \tag{3}$$

To minimize the number of passive components, Chung [19] replaced L_r and L_{rec} with $L_{p,lk}$ and $L_{s,lk}$ which are the leakage inductances of the equivalent model transformer. Using the coupling coefficient of the transformer k, the relationships between the magnetizing inductance and leakage inductances are as follows:

$$L_r = L_{p,lk} = \frac{1-k}{k} L_m,$$
$$L_{rec} = L_{s,lk} = \frac{1-k}{n^2 k} L_m. \tag{4}$$

III. ODE-BASED CIRCUIT ANALYSIS

In this paper, the optimized circuit design method is proposed by using the dimensionless approach of the analytical model while satisfying ZVS and ZVDS operation without tuning procedure. When using dimensionless circuit analysis, the values of passive elements are easily calculated under various conditions such as switching frequency, output power, input voltage, and output voltage.

A. MODE ANALYSIS

In order to analyze the converter accurately with a mathematical model, the parasitic effects of devices are considered. FIGURE 3 shows the equivalent model of real devices and the equivalent schematic circuit of the converter. As shown in FIGURE 3(c), the diodes are replaced with a series resistance R_D and an ideal voltage source V_D when the diodes turn ON, and replaced with a parallel capacitance C_D when the diodes turn OFF. When the switch turns ON, it is represented by a small resistance R_{DS} and an open circuit when OFF. For inductors and capacitors in FIGURE 3(a) and (b), equivalent series resistances (ESRs) are considered by the quality factors, Q_L and Q_C, which are given by

$$Q_L = \frac{\omega_{sw} L}{R_L},\ Q_C = \frac{1}{\omega_{sw} C R_C}. \tag{5}$$

FIGURE 4 shows the eight operation modes of the converter. Using Kirchhoff's current law (KCL) and Kirchhoff's voltage law (KVL), the ordinary differential equations (ODEs) that relate V_{Cr}, V_{Crec}, I_{Lr}, and I_{Lrec} are obtained. With a normalized time $\theta = \omega_{sw} t$, the normalized current and voltage are as follows:

$$i_{Lr}(\theta) = \frac{I_{Lr}\left(\theta/\omega_{sw}\right)}{I_{out}/n},$$
$$i_{Lrec}(\theta) = \frac{I_{Lrec}\left(\theta/\omega_{sw}\right)}{I_{out}},$$
$$v_{Cr}(\theta) = \frac{V_{Cr}\left(\theta/\omega_{sw}\right)}{nV_{out}},$$
$$v_{Crec}(\theta) = \frac{V_{Crec}\left(\theta/\omega_{sw}\right)}{V_{out}}, \tag{6}$$

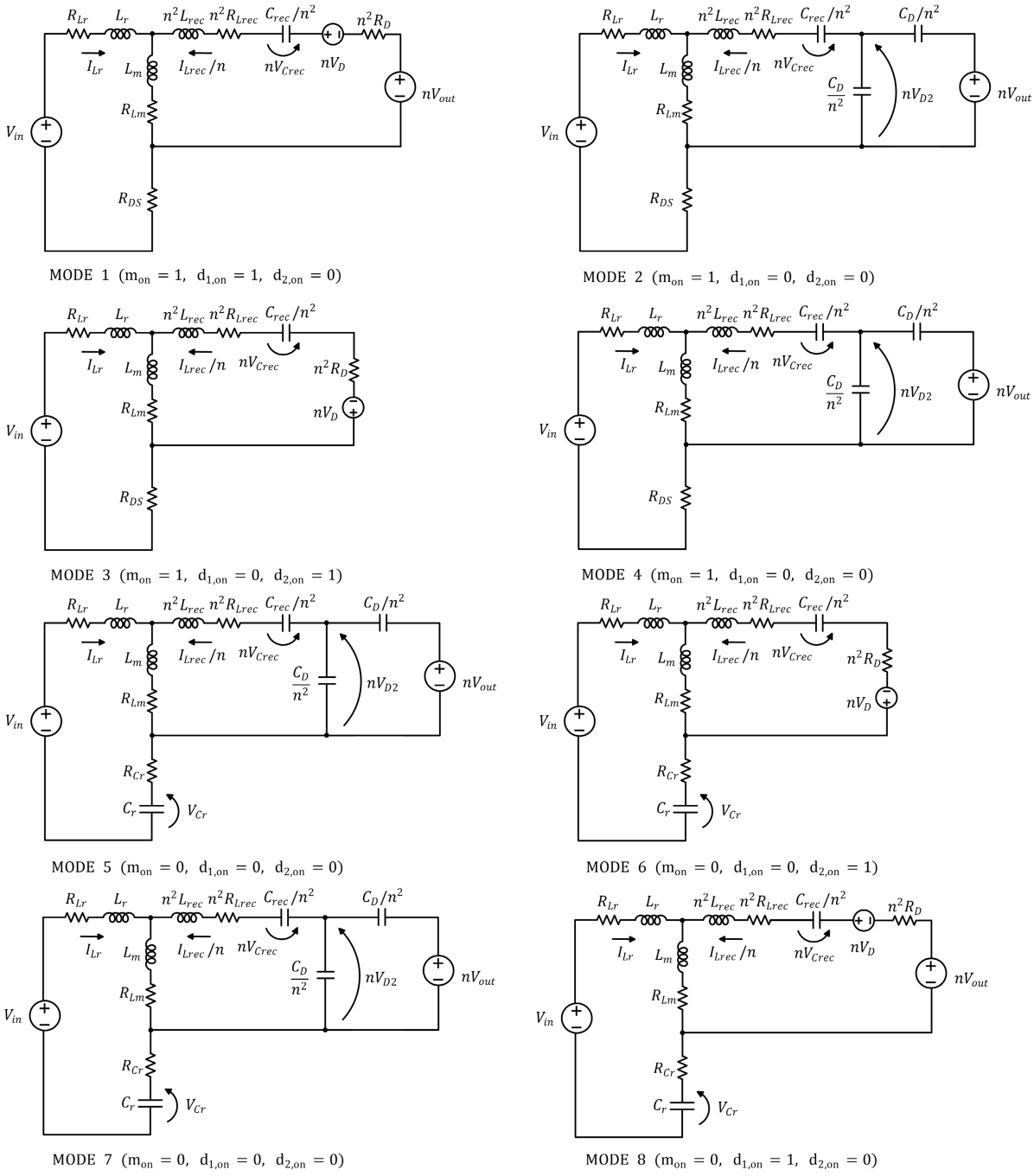

FIGURE 4. The eight operaion modes of equivalent schematic circuit: Mode 1 to 8.

where n is the turn ratio of the transformer. To normalize the other terms, the dimensionless parameters are defined by

$$R_o = n^2 \frac{V_{out}}{I_{out}},$$
$$q_r = \frac{1}{\omega_{sw} C_r R_o}, q_{rec} = \frac{n^2}{\omega_{sw} C_{rec} R_o}, q_D = \frac{n^2}{\omega_{sw} C_D R_o},$$
$$q_m = \frac{\omega_{sw} L_m}{R_o}, k_r = \frac{L_m}{L_r + L_m}, k_{rec} = \frac{L_m}{n^2 L_{rec} + L_m},$$
$$g_{DS} = \frac{R_o}{R_{DS}}, g_D = \frac{R_o}{n^2 R_D}, \mu = \frac{V_{in}}{nV_{out}}, v_D = \frac{V_D}{V_{out}}. \quad (7)$$

The quality factors Q_{Lr}, Q_{Lrec}, Q_{Lm}, Q_{Cr}, and Q_{Crec} are defined as in (5).

In order to incorporate the equations derived from KCL and KVL in FIGURE 4, m_{on} and d_{on} are defined. Here, $m_{on} = 1$ when the switch is ON, and $m_{on} = 0$ when the switch is OFF. For the diodes, $d_{1,on} = 1$ and $d_{2,on} = 1$ when the diode D1 turns ON and D2 turns ON, respectively. Also,

TABLE 1. The eight operation modes and θ conditions.

	m_{on}	$d_{1,on}$	$d_{2,on}$	θ_i conditions
MODE 1 (θ_0~θ_1)	1	1	0	$i_{Lrec}(\theta_1) = 0$
MODE 2 (θ_1~θ_2)	1	0	0	$v_{D2}(\theta_2) = -v_D$
MODE 3 (θ_2~θ_3)	1	0	1	$i_{Lrec}(\theta_3) = 0$
MODE 4 (θ_3~θ_4)	1	0	0	$\theta_4 = 2\pi D$
MODE 5 (θ_4~θ_5)	0	0	0	$v_{D2}(\theta_5) = -v_D$
MODE 6 (θ_5~θ_6)	0	0	1	$i_{Lrec}(\theta_6) = 0$
MODE 7 (θ_6~θ_7)	0	0	0	$v_{D2}(\theta_7) = 1 + v_D$
MODE 8 (θ_7~θ_8)	0	1	0	$\theta_8 = 2\pi$

$d_{1,on} = 0$ and $d_{2,on} = 0$ when the diode D1 is OFF and D2 is OFF, respectively. Using the parameters mentioned above, (8) shown at the bottom of the page is obtained.

The system of ODEs in (8) can be formulated in the matrix form, with coefficient matrix **A** and vector **B**, as follows:

$$\frac{d}{d\theta}\begin{pmatrix} i_{Lr}\ (\theta) \\ i_{Lrec}\ (\theta) \\ v_{Cr}\ (\theta) \\ v_{Crec}\ (\theta) \end{pmatrix} = \mathbf{A}\begin{pmatrix} i_{Lr}\ (\theta) \\ i_{Lrec}\ (\theta) \\ v_{Cr}\ (\theta) \\ v_{Crec}\ (\theta) \end{pmatrix} + \mathbf{B}. \quad (9)$$

Using eigenvalues and corresponding eigenvectors of matrix **A**, the solution of (9) can be found.

The eight operation modes' conditions are in Table 1. The number of the operation modes depends on the diodes' parasitic capacitance magnitude. If the parasitic capacitance C_D is negligibly small, some modes are removed. In this paper, since the value of C_D is assumed to be similar to the values of the other resonant elements in high-frequency conditions, the eight operation modes are analyzed.

Mode 1 starts by setting $\theta = \theta_0 = 0$ when $m_{on} = 1$, $d_{1,on} = 1$ and $d_{2,on} = 0$. In mode 1, the switch turns on under ZVS condition so that $v_{Cr}\ (\theta) = 0$. The initial values are defined as

$$i_{Lr}\ (0) = i_{Lr}^0,\ i_{Lrec}\ (0) = i_{Lrec}^0,\ v_{Crec}\ (0) = v_{Crec}^0. \quad (10)$$

Mode 1 finishes at $\theta = \theta_1$ when D1 turns OFF. The value of θ_1 is calculated by solving $i_{Lrec}\ (\theta_1) = 0$.

Mode 2 operates when $m_{on} = 1$, $d_{1,on} = 0$ and $d_{2,on} = 0$. In mode 2, C_{D1} and C_{D2}, the parasitic capacitance of the diode D1 and D2, is charged and discharged, respectively. Then, v_{D2}, the voltage across the diode D2, drops from $1 + v_D$ to $-v_D$. Mode 2 finishes at $\theta = \theta_2$ when v_{D2} reaches $-v_D$ and the diode D2 turns ON.

Similarly, i_{Lr}, i_{Lrec}, v_{Cr}, and v_{Crec} of Mode 3, 4, 5, 6, 7 and 8 are obtained by solving (9). As shown in (8), the voltage across the switch resonates in mode 5, 6, 7 and 8 when the switch is OFF. Note that the continuity of the capacitor voltages and inductor currents at θ_1, θ_2, θ_3, $\theta_4 = 2\pi D$, θ_5, θ_6,and θ_7 offers the initial values of each mode. FIGURE 5 shows key waveforms at each mode.

B. CIRCUIT DESIGN CONDITIONS

In order to ensure the continuity of the capacitor voltages and inductor currents waveform, stationary conditions should be satisfied as follows:

$$\begin{aligned} i_{Lr}\ (2\pi) &= i_{Lr}\ (0)\,, \\ i_{Lrec}\ (2\pi) &= i_{Lrec}\ (0)\,, \\ v_{Crec}\ (2\pi) &= v_{Crec}\ (0)\,. \end{aligned} \quad (11)$$

In the steady-state conditions, the output current I_{out} is directly related to the average value of current flowing through the diode D1 since the average current of the output capacitor is zero. With the normalization, the equations are derived as

$$\begin{aligned} I_{out} &= -\ <\ I_{Lrec}(t)\ |_{d_{1,on}=1}\ >, \\ -1 &= \frac{1}{2\pi}\left(\int_0^{\theta_1} i_{Lrec}\ (\theta)\,d\theta + \int_{\theta_7}^{2\pi} i_{Lrec}\ (\theta)\,d\theta\right. \\ &\quad + \frac{1}{2}\left(\int_{\theta_1}^{\theta_2} i_{Lrec}\ (\theta)\,d\theta + \int_{\theta_3}^{\theta_4} i_{Lrec}\ (\theta)\,d\theta\right. \\ &\quad \left.\left. + \int_{\theta_4}^{\theta_5} i_{Lrec}\ (\theta)\,d\theta + \int_{\theta_6}^{\theta_7} i_{Lrec}\ (\theta)\,d\theta\right)\right). \end{aligned} \quad (12)$$

To achieve the ZVS characteristics, the switch voltage V_{ds} should satisfy the following condition as

$$v_{Cr}\ (2\pi) = 0. \quad (13)$$

$$\begin{aligned} &(1 - m_{on})\ v_{Cr}\ (\theta) \\ &\quad + \left(\frac{1 - k_r}{k_r}\frac{q_m}{Q_{Lr}} + \frac{q_m}{Q_{Lm}} + m_{on}\frac{1}{g_{DS}} + (1 - m_{on})\ \frac{q_r}{Q_{Cr}}\right) i_{Lr}\ (\theta) + \frac{q_m}{k_r}\frac{di_{Lr}\ (\theta)}{d\theta} + q_m\frac{di_{Lrec}\ (\theta)}{d\theta} + \frac{q_m}{Q_{Lm}} i_{Lrec}\ (\theta) = \mu \\ &v_{Crec}\ (\theta) + \left(d_{2,on} - d_{1,on}\right) v_D + \left(\left(d_{1,on} + d_{2,on}\right)\frac{1}{g_D} + \frac{1 - k_{rec}}{k_{rec}}\frac{q_m}{Q_{Lrec}} + \frac{q_{rec}}{Q_{Crec}} + \frac{q_m}{Q_{Lm}}\right) i_{Lrec}\ (\theta) + \frac{q_m}{Q_{Lm}} i_{Lrec}\ (\theta) \\ &+ \frac{q_m}{k_{rec}}\frac{di_{Lrec}\ (\theta)}{d\theta} + q_m\frac{di_{Lr}\ (\theta)}{d\theta} = d_{1,on} + \left(1 - d_{1,on}\right)\left(1 - d_{2,on}\right) v_{D2} \\ &i_{Lr}\ (\theta) = \frac{1}{q_r}\frac{dv_{Cr}\ (\theta)}{d\theta}\ (\textit{Mode 5, 6, 7 and 8 only}) \\ &i_{Lrec}\ (\theta) = \frac{1}{q_{rec}}\frac{dv_{Crec}\ (\theta)}{d\theta},\ i_{Lrec}\ (\theta) = -\frac{2}{q_D}\frac{dv_{D2}\ (\theta)}{d\theta}\ (\textit{Mode 2, 4, 5 and 7 only}) \end{aligned} \quad (8)$$

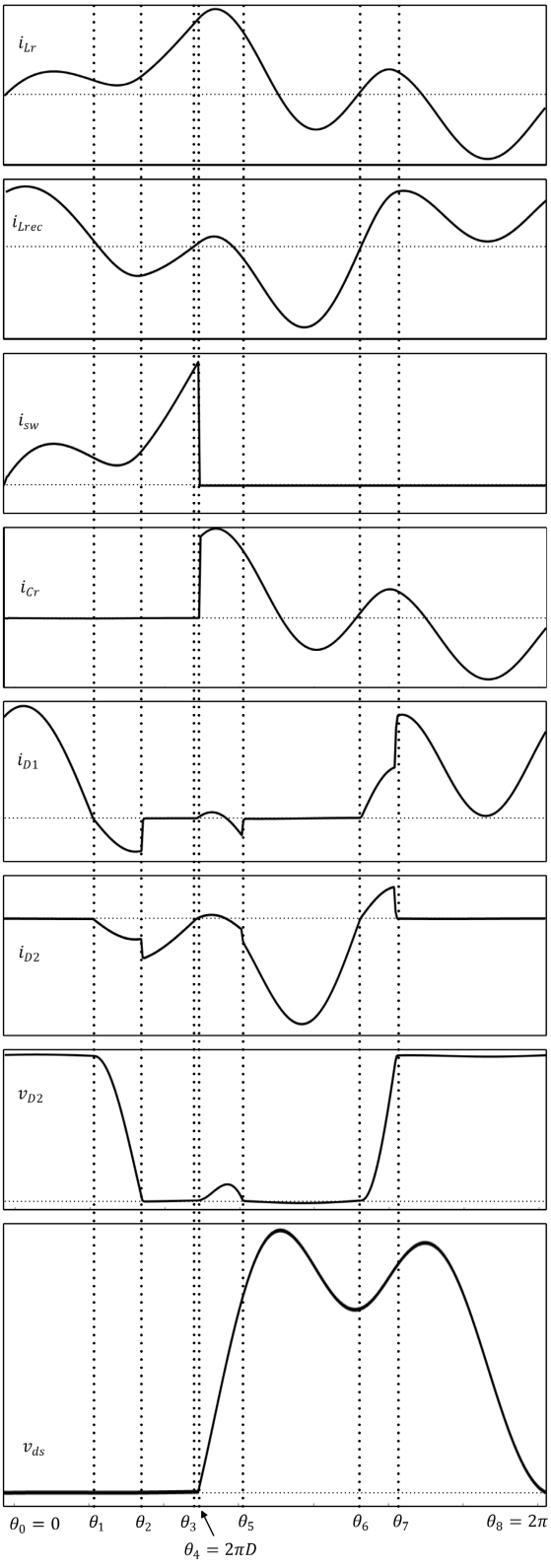

FIGURE 5. Key waveforms of voltage and current at each mode.

As the ZVDS is expected when the differential value of voltage V_{ds} is zero, the inductor current is expressed as

$$i_{Lr}(2\pi) = i_{Lr}^0 = 0. \tag{14}$$

For locating the poles and zero of Z_{ds} in the proper location, (2) and (3) are normalized as

$$\begin{aligned} 4 &= \frac{q_{rec}k_{rec}}{q_m(1-k_rk_{rec})}, \\ m_1^2 + m_2^2 &= \frac{q_rk_r + q_{rec}k_{rec}}{q_m(1-k_rk_{rec})}, \\ m_1^2m_2^2 &= \frac{q_rk_rq_{rec}k_{rec}}{q_m^2(1-k_rk_{rec})}. \end{aligned} \tag{15}$$

In this circuit design procedure, ODEs and design conditions depend on dimensionless parameters:

$$\begin{aligned} &\mu, D, m_1, m_2, q_r, q_{rec}, q_m, k_r, k_{rec}, i_{Lr}^0, i_{Lrec}^0, v_{Crec}^0, \\ &q_D, v_D, Q_{Lr}, Q_{Lrec}, Q_{Lm}, Q_{Cr}, Q_{Crec}, g_{DS}, g_D. \end{aligned} \tag{16}$$

The quality factors of inductors and capacitors are technologically constrained as well as the parasitic components of the diodes and the switch. If the input and output voltage is determined, the value of μ is fixed. For k_r and k_{rec} in (7), $k_r = k_{rec} = k$ which is the coupling coefficient of the equivalent model transformer. The other parameters in (16) are used to achieve the ZVS and ZVDS.

Equations (11) - (15) show the nine nonlinear equations with ten unconstrained parameters:

$$D, m_1, m_2, q_r, q_{rec}, q_m, k, i_{Lr}^0, i_{Lrec}^0, v_{Crec}^0, \tag{17}$$

which means that the degree of freedom is only one. The numerical solutions are obtained using the numerical solver, such as MATLAB or Wolfram Mathematica notebook software.

With the normalized variables and dimensionless parameters, the design curves of the general analysis are obtained without considering any actual circuit parameters. Thus, only the denormalization process with the actual values of V_{out}, I_{out}, n and ω_{sw} is needed to calculate the specific solution of the designed circuit.

FIGURE 6 shows the design curves as a function of μ and D. The values of the plots in FIGURE 6 are m_1, m_2, q_r, i_{Lrec}^0, v_{Crec}^0 and k, from top to bottom. The dimensionless parameter values on design curves satisfy the ZVS and ZVDS behavior in steady-state conditions. FIGURE 6(a) shows the parameter values in the lossless system that all quality factors are infinite, and FIGURE 6(b) shows the parameter values of the actual system with the passive and active elements' parasitic values.

IV. PCB TRANSFORMER DESIGN

In the high-frequency resonant converter, the stored energy required for the resonant elements decreases as the switching frequency increases. Then, the design values of inductors are sufficiently reduced to utilize the copper traces on PCB in the air-core transformer model, achieving high power density. Since designing the accurate self and mutual inductance values is required for the planar PCB transformer, the calculation methods such as the analytical modeling and 3D FEM simulation are needed.

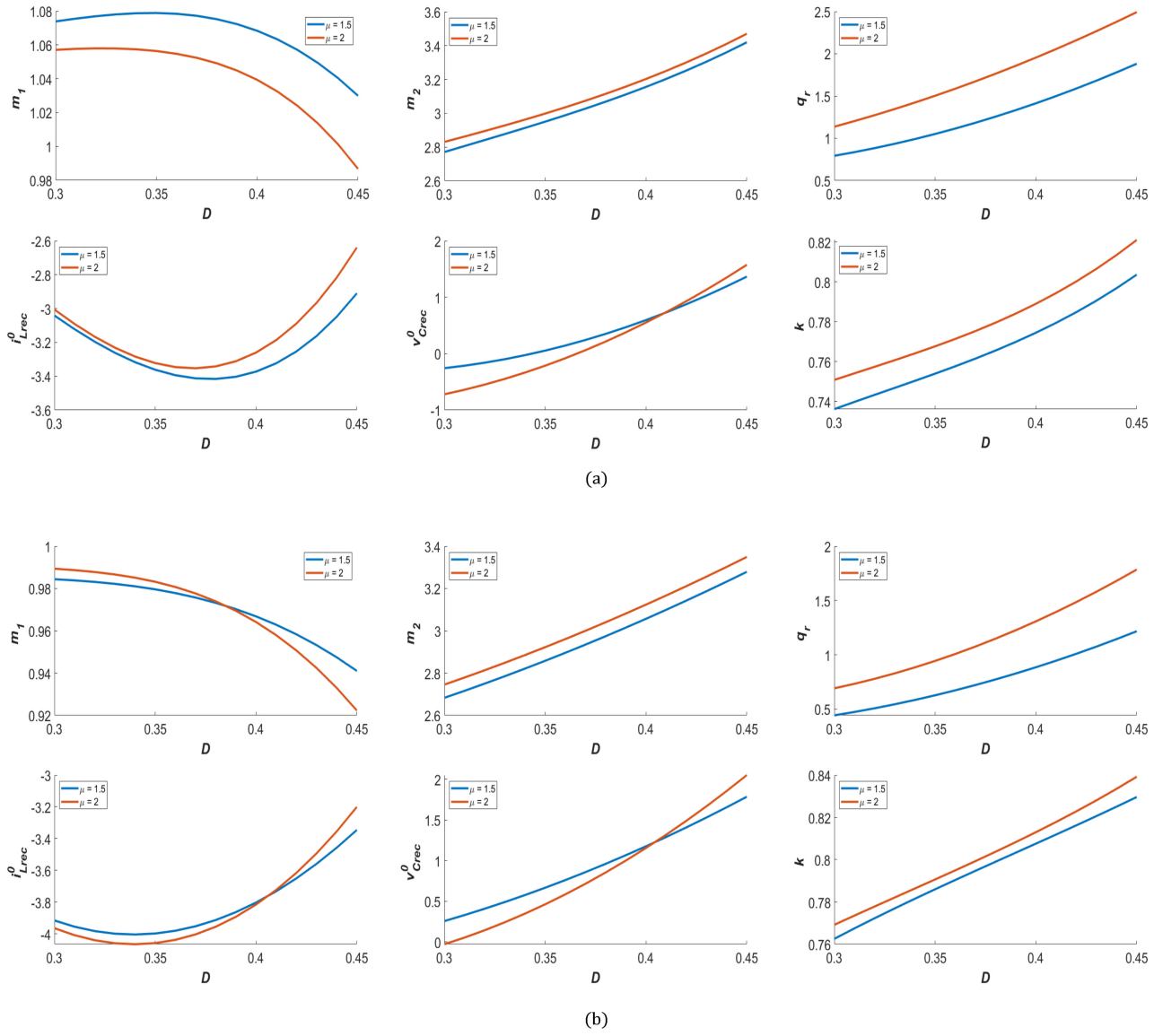

FIGURE 6. Design curves as a function of μ and D for dimensionless system. (a) Ideal lossless system. (b) For $Q_{Lr} = 10.53$, $Q_{Lrec} = 11.01$, $Q_{Lm} = 61.73$, $Q_{Cr} = Q_{Crec} = 1000$, 10001000 *rec sless systemg*$_{DS} = 469$, $g_D = 219$, $v_D = 0.025$, and $q_D = 1.043$. This design curve is used to model the prototype in Section.

A. INDUCTANCE CALCULATION METHOD

In the planar PCB transformers, the leakage and mutual inductances depend on the winding structures. For spiral structure, previous researches calculate the inductances assuming a complete circle or an octagonal structure [28], [29]. Although these approximations give highly accurate results for large radii, more accurate methods are needed when the smaller size of planar PCB transformers are used at higher frequencies. In this paper, the leakage and mutual inductances are calculated using numerical methods with Neumann's formula in the spiral structure. Furthermore, the inductances of the designed transformer are verified by 3D FEM tools (Ansys Maxwell). FIGURE 7 shows the spiral structure model of the PCB transformer. Using the exact

$$M_{ij} = \frac{\mu_0}{4\pi W_1 W_2 H_1 H_2} \int_{r_j}^{r_j+W_2} \int_0^{H_2} \int_{\varphi_j}^{\varphi_j+\Delta\varphi} \int_{R_i}^{R_i+W_1} \int_H^{H+H_1} \int_{\theta_i}^{\theta_i+\Delta\theta} \frac{Rr\cos(\varphi-\theta)}{\sqrt{\rho^2+(Z-z)^2}} d\theta dZ dR d\varphi dz dr,$$
$$\rho = \sqrt{d^2 - 2d(r\cos\varphi - R\cos\theta) + R^2 + r^2 - 2Rr\cos(\varphi-\theta)}. \quad (18)$$

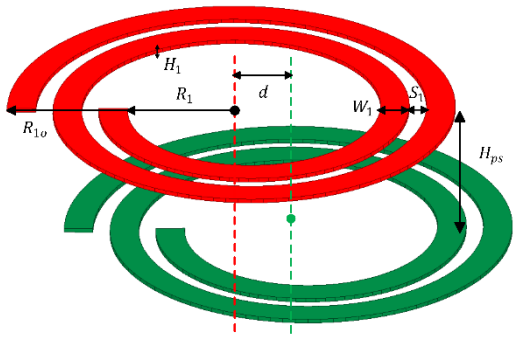

FIGURE 7. Spiral structure model of PCB transformer using 3D FEM tool (Maxwell Ansys).

inductance equations for rectangular conductors from [31], (18) is derived at the bottom of the previous page, are derived at the bottom of the page. Here, M_{ij} is the mutual inductance between the i_{th} conductor and j_{th} conductor of the primary and the secondary windings, respectively. H_1, W_1, S_1, H_2, W_2 and S_2 represent the thickness, width and the separation between the tracks of the primary and the secondary windings, respectively. R_i, θ_i, r_j and φ_j represent the radial and angular distances of the i_{th} conductor and j_{th} conductor from the central axis, respectively. Also, d represents the central misalignment between the primary and the secondary windings, and H_{ps} represents the separation between the height of the windings. Since the structure of the windings is spiral, the equations between the radial and angular distances are as follows:

$$\begin{aligned} R_i &= \theta_i \left(W_1 + S_1\right) + R_1, \\ r_j &= \varphi_j \left(W_2 + S_2\right) + R_2, \end{aligned} \tag{19}$$

where R_1 and R_2 are the inner radius of the primary and the secondary windings, respectively.

To solve (18), the numerical method is needed. Gaussian quadrature rule helps to transform the equation in integral form into summation form, which is expressed as

$$\int_{-1}^{1} f\left(x\right) dx \approx \sum_{i=1}^{n} w_i f\left(x_i\right), \tag{20}$$

where w_i is the i_{th} weight.

Using (20), M_{ij} becomes (21), as shown at the bottom of the page. The calculations of inductances using the analytical method are implemented by MATLAB. The total mutual inductance is given by:

$$M = \sum_{i=1}^{N_i} \sum_{j=1}^{N_j} M_{ij}, \textit{for all } i \textit{ and } j. \tag{22}$$

The calculation of the self-inductance is similar to (21). When the i_{th} and j_{th} conductors belong to the same coil, (21) becomes

$$L_{self} = \sum_{i=1}^{N_i} \sum_{j=1}^{N_j} M_{ij}, \textit{for } i \neq j. \tag{23}$$

To determine the parameters of the desired transformer from the circuit analysis, the design procedure is required. The values of the inductances of the transformer depend on the parameters such as the number of turns (N), separation between the tracks (S), separation between the height of the windings (H_{ps}), conductor width (W), thickness (H), inner radius (R), and the central misalignment between the coils (d).

FIGURE 8(a)-8(f) shows the design curves of the self and mutual inductances. As can be seen from the general formula of inductance, the value of inductance forms a proportional relationship with the inner radius R and the number of the turns N. FIGURE 8(b) and 8(c) show that the slope of the larger S and W is small. As the hollow area becomes larger at wide S and W, the variation of the self-inductance reduces. FIGURE 8(d)-8(f) show the relationship between the mutual inductances M, separation between the height of the windings H_{ps}, and the central misalignment d. The mutual inductances go to zero when H_{ps} and d increase since the magnetic flux produced by the primary coil does not affect the secondary coil anymore. FIGURE 8(f) shows the negative mutual inductances above the certain value of d because the magnetic flux of the primary coil flows to the secondary coil in the opposite direction. Using the above parameters as the degrees of freedom, the self and mutual inductances can be adjusted flexibly.

To increase the quality factors of the windings, the conductor width W and conductor separation S should be as small as possible [32]. Also, under the high-frequency conditions, the inner windings in a spiral coil have higher ac resistance compared to outer windings due to the higher flux density. Thus, the ratio of the inner radius to the outer radius, called the hollow factor, is considered to increase the quality factor.

The analytical calculation results are compared with the FEM simulation results. The theoretical values and simulation values of inductances are illustrated in Figure 9. The results show that the proposed method is effective and provides an accurate analytical model without a computational burden for simulation.

$$\begin{aligned} M_{ij} = {} & \frac{\mu_0}{4\pi W_1 W_2 H_1 H_2} \sum\nolimits_n w_n \sum\nolimits_m w_m \sum\nolimits_k w_k \sum\nolimits_l w_l \\ & \times \left\{ R_l r_k \cos\left(\varphi_n - \theta_m\right) \left(g\left(H_{ps}\right) - g\left(H_{ps} + H_1\right) - g\left(H_{ps} - H_2\right) + g\left(H_{ps} + H_1 - H_2\right)\right)\right\}, \\ g\left(x\right) = {} & \sqrt{x^2 + \rho^2} + x \log\left(\sqrt{x^2 + \rho^2} - x\right). \end{aligned} \tag{21}$$

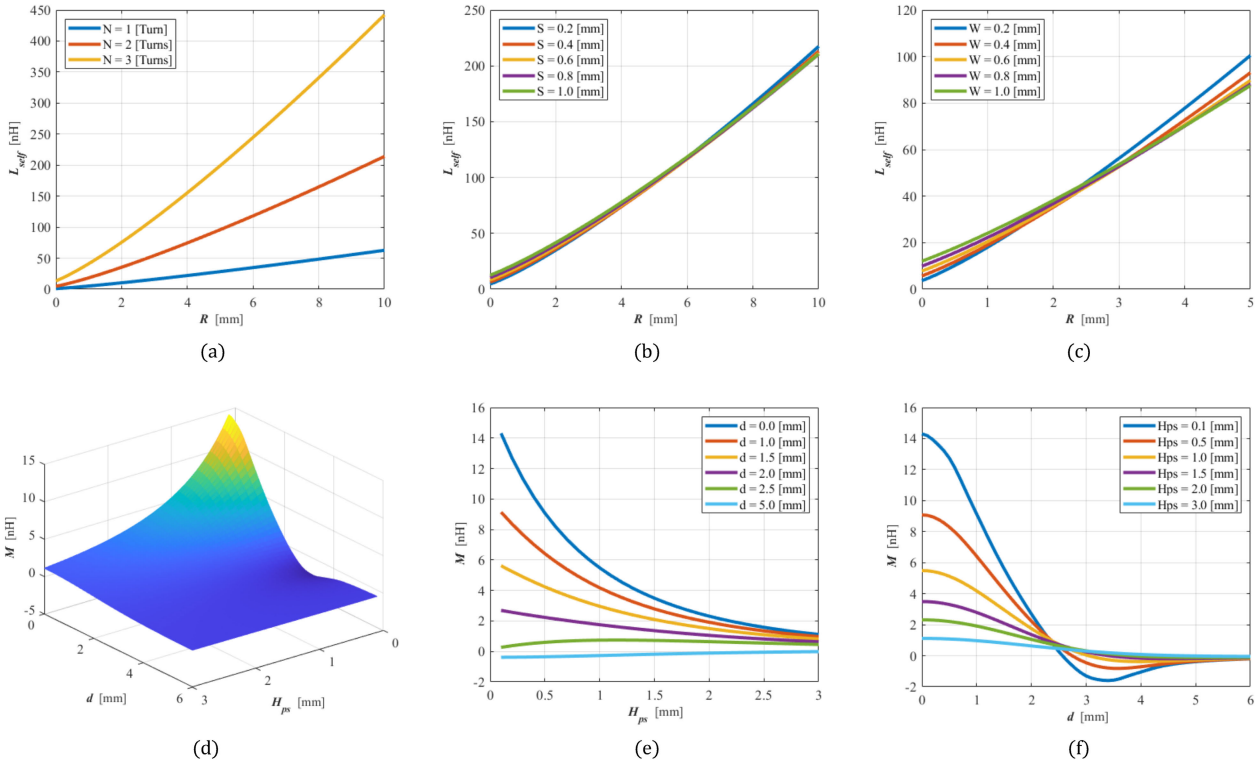

FIGURE 8. Design curves of self and mutual inductances. Self inductance L_{self} [nH](H_{ps}= 0, d = 0), (a) R − N curve ($S = 0.2$mm, $W = 0.3$mm), (b) R − S curve ($N = 2$, $W = 0.3$mm), (c) R − W curve ($N = 2$, $S = 0.2$mm). Mutual inductance M[nH]($N = 2$, $R = 1.0$mm,$S = 0.2$mm, $W = 0.3$mm), (d) $H_{ps} - d - M3Dplot$, (e) H_{ps}−d curve, (f) d−H_{ps} curve.

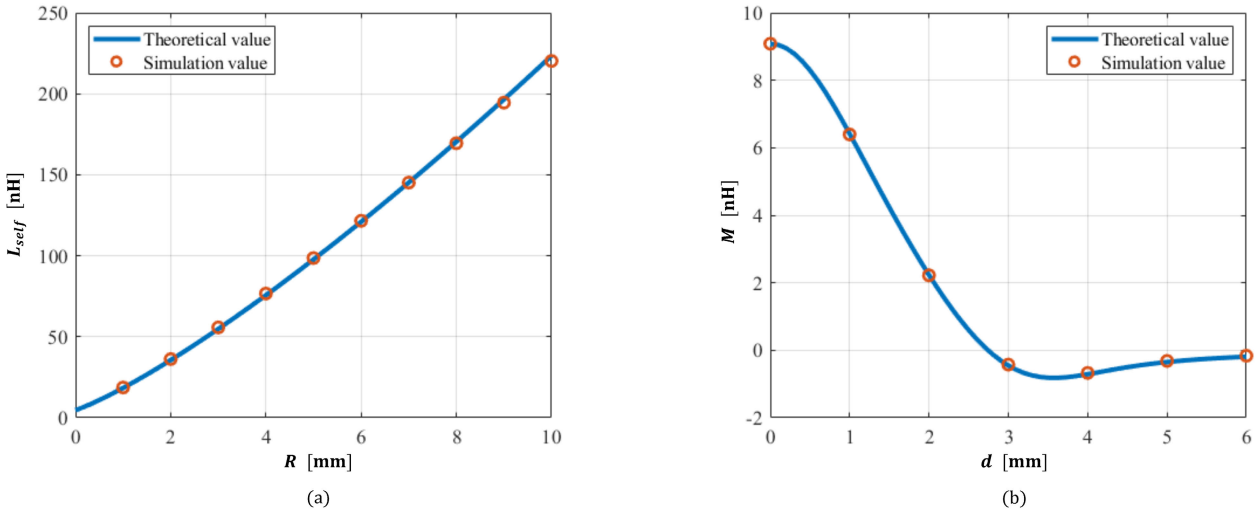

FIGURE 9. Theoretical and simulation results of self and mutual inductances. (a) Self inductance L_{self} [nH]($H_{ps} = 0$, $d = 0$, $N = 2$, $S = 0.2$mm, $W = 0.3mm$). (b) Mutual inductance M[nH]($N = 2$, $R = 1.0$mm,$S = 0.2$mm, $W = 0.3$mm,$H_{ps} = 0.5mm$).

B. MULTILAYER CORELESS PCB TRANSFORMER

In the high-frequency converter, using only a single layer of PCB conductors for the transformer is not recommended for high current and low voltage applications [24]; thus, the multilayer coreless PCB transformer is employed to increase the current carrying capacity. From [33], [34], [35], [36], the interleaving structure for the primary and the secondary coils minimizes the leakage inductance and ac winding loss. Since the transformer for the proposed circuit requires a high coupling coefficient above 0.7, the interleaving structure of

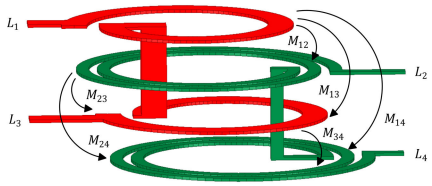

FIGURE 10. 3D design model of multilayer(4-layer) coreless PCB transformer.

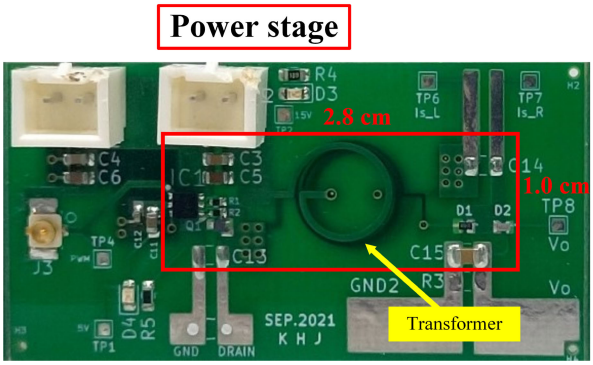

FIGURE 11. The photography of the 27.12MHz dc-dc converter prototype.

TABLE 2. Dimensionless input parameters.

Symbol	Value	Symbol	Value
Q_{Lr}	10.53	g_{DS}	469
Q_{Lrec}	11.01	g_D	219
Q_{Lm}	61.73	v_D	0.025
Q_{Cr}	1000	q_D	1.043
Q_{Crec}	1000	μ	2

TABLE 3. Normalized output parameters.

Symbol	Value	Symbol	Value
D	0.3	m_1	0.989
k	0.769	m_2	2.746
q_r	0.687	i^0_{Lr}	0
q_{rec}	0.608	i^0_{Lrec}	-3.964
q_m	0.286	v^0_{Crec}	-0.032

the multilayer transformer brings about a desirable result. Considering the cost and the complexity of the analysis, the 4-layer PCB transformer is suitable for the high-frequency dc-dc converter. FIGURE 10 shows the design of the 4-layer transformer. The turns ratio n is 0.5 since the value of μ is determined to be two from the circuit design. Therefore, one turn and two turns are selected for the primary and secondary sides, respectively.

The self and mutual inductances of the primary and secondary coils are calculated as follows:

$$L_{p,self} = L_1 + L_3 + 2M_{13},$$

TABLE 4. Resonant system parameters.

Symbol	Value	Symbol	Value
L_r	9.454 nH	C_r	455.6 pF
L_{rec}	37.82 nH	C_{rec}	128.7 pF
L_m	31.52 nH		

TABLE 5. Parameters of pcb transformer.

Symbol	Value	Symbol	Value
R_1	3.2 mm	R_2	3.35 mm
W_1	0.6 mm	W_2	0.3 mm
S_1	0.3 mm	S_2	0.2 mm
H_1	0.035 mm	H_2	0.035 mm
$H_{ps1,2}$	0.2 mm	$H_{ps2,3}$	0.6 mm
$H_{ps3.4}$	0.2 mm	d	0.4 mm
$L_{p,self}$	41.88 nH	$L_{s,self}$	168.5 nH
M	64.67 nH	k	0.77

TABLE 6. Power stage components.

Symbol	Description	Value
S	Switch	EPC2035
D_1, D_2	Diode	PMEG6010AESB
C_o	Output capacitor	4.7 µF
R_o	Output resistor	73 Ω
C_{ext}	Resonant capacitor	240 pF
C_{rec}	Resonant capacitor	120 pF

$$\begin{aligned} L_{s,self} &= L_2 + L_4 + 2M_{24}, \\ M &= M_{12} + M_{14} + M_{23} + M_{34}. \end{aligned} \tag{24}$$

From (24), primary leakage, secondary leakage, magnetizing inductances, and coupling coefficient are derived as

$$\begin{aligned} L_{p,lk} &= L_{p,self} - L_m, \\ L_{s,lk} &= L_{s,self} - \frac{L_m}{n^2}, \\ L_m &= k \cdot L_{p,self}, \\ k &= \frac{|M|}{\sqrt{L_{p,self} L_{s,self}}}. \end{aligned} \tag{25}$$

V. PROTOTYPE DESIGN AND EXPERIMENTAL RESULTS

The 27.12MHz/3W single-switch converter prototype with $V_{in} = 15$V and $V_{out} = 15$V is implemented as a design example. FIGURE 11 shows the prototype of the isolated dc-dc converter with a planar PCB transformer. After the normalization process, the dimensionless input parameters of the design condition are listed in Table 2. Also, as shown in FIGURE 6(b), the normalized output parameters are calculated using Wolfram Mathematica notebook software and

TABLE 7. Properties comparison of high-frequency topologies.

Topology	Switching frequency	Normalized Switch voltage stress	Inductors/ transformer number	Non-ideality analysis	PCB transformer	Efficiency	Power density
Proposed	27.12 MHz	2.29	0/1	O	O	69.5%	90 W/in^3
Single-switch [19]	10 MHz	2.26	0/1	X	X	69%	15 W/in^3
Isolated Class E resonant [21]	1.25 MHz	3.4	1/1	O	X	75%	1 W/in^3
Current-driven Class E [10]	20 MHz	4.5	3/0	X	-*	81.5%*	40 W/in^3

* As the topology is the non-isolated converter, no transformer was used.

listed in Table 3. By denormalization process using (7), the values of capacitors and inductors in the circuit are in Table 4.

From the inductance values in Table 4, the 4-layer spiral coreless PCB transformer is designed. By using the analytical method and simulation, the self and mutual inductances are calculated. The design parameters and inductance values are in Table 5.

The system parameters for the power stage are calculated based on the analytical models and design methods of the converter system and PCB transformer. The components used in the prototype are shown in Table 6. Here, a 60-V GaN device (EPC 2035) is used as a switch device. Because of the output junction capacitance of the switch device (C_{oss}), the external capacitance (C_{ext}) connected to the switch in parallel is needed to compensate for the resonant capacitance (C_r). In the experiment, C_{oss} is determined as the value at the normal operating condition, and C_{ext} is determined by 240 pF.

The switch voltage V_{ds} and gate voltage V_{gs} waveforms from ODE-based analysis, PSIM, and experiment are shown in FIGURE 12. The experimental result of the drain-source switch voltage waveform in FIGURE 12(c) shows that the switch device achieves ZVS. Also, the peak voltage is reduced to 34.40 V, 2.29 times the input voltage.

The measured output voltage and output current are 14.6 V and 200 mA, respectively. In the rated conditions with a full load, the measured efficiency is 69.5%. Measurement shows a similar result to the theoretical analysis (15 V,200mA, 71.4%). The loss analysis is shown in FIGURE 13. The switch losses include the conduction loss ($P_{S,con}$) and the switching loss ($P_{S,sw}$). For the rectifier stage, the conduction losses of two diodes take up about 20% of the total losses. The transformer losses take the largest portion of the losses in the converter system. Under the high-frequency condition, the ac resistance of the transformer becomes much higher than the dc resistance because of the skin and proximity effect. The ac losses could be relieved through the design optimization of PCB transformer windings to improve the efficiency of the converter. The remaining 3% loss is due to the conduction loss of copper trace on PCB.

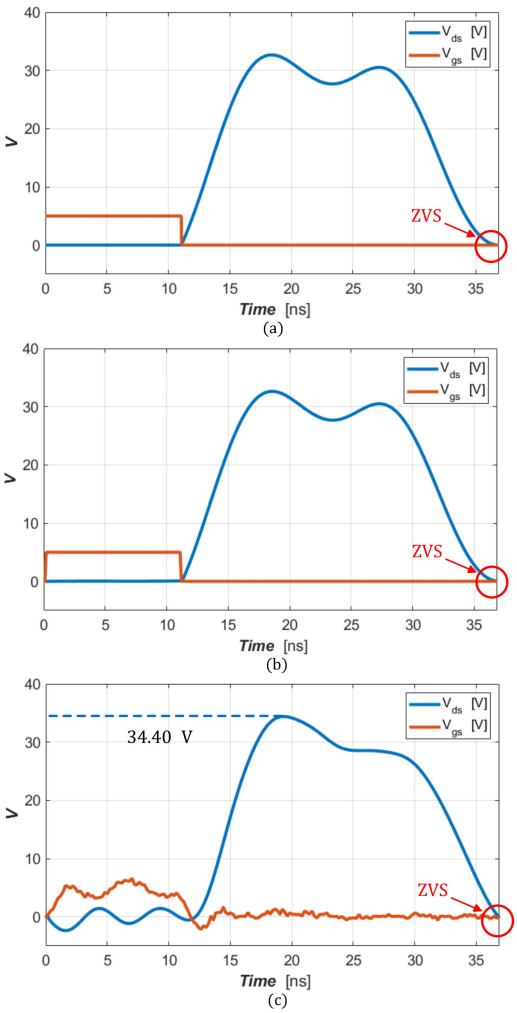

FIGURE 12. Output waveforms. (a) ODE-based analysis, (b) PSIM, (c) experiment.

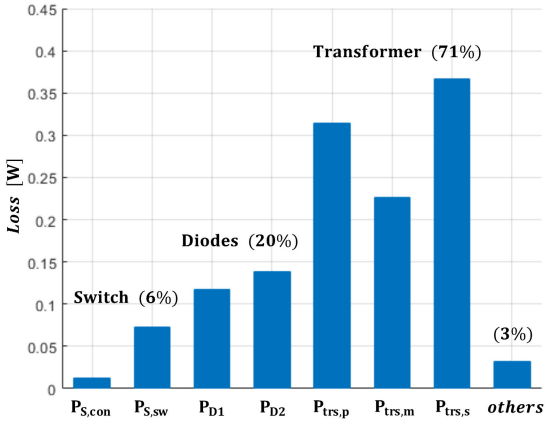

FIGURE 13. Estimated loss distribution of the converter system.

The properties of the proposed converter have been compared with other high-frequency single-switch converter research, as shown in Table 7. The proposed 27.12MHz DC-DC converter significantly reduces normalized switch voltage stress and the inductor number. Also, by utilizing the planar coreless PCB transformer, the proposed converter has a higher power density than the isolated converters in Table 7. As a result, the experiment results verify the accuracy of the analytical models and the design methods of the converter and the PCB transformer.

VI. CONCLUSION

This paper proposes the analytical method and design of the single-switch isolated dc-dc converter and spiral planar PCB transformer. The analytical approach helps to reduce the voltage stress while achieving ZVS and ZVDS at any duty ratio. Also, more exact analysis and results are obtained in the proposed dimensionless system by considering the parasitic elements, such as the diode capacitances. In addition, the planar PCB transformer is designed based on the accurate calculation method to reduce the size and increase the power density. The accurate analytical modeling of the PCB transformer allows for the practical design of the multilayer spiral transformer without the computational burden of the 3D FEM simulation. A 27.12 MHz prototype is implemented and shows that the peak voltage of the single-switch is reduced to 2.29 times the input voltage. The converter achieves an efficiency of 69.5%, and the experimental results verify the analytical model.

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