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RESEARCH ARTICLE

An Improved Non-Isolated Quadratic DC–DC Boost Converter With Ultra High Gain Ability

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ABSTRACT This paper introduces an improved quadratic DC-DC boost converter to provide an ultra-high level voltage gain with the switched-capacitor cell based structure. The proposed converter has the ability to excel the output voltage gain to the ultra-high level without any voltage doubler circuit. Hence, the total number of components is less compared to the conventional topologies. The proposed converter offers reduced voltage stress on the capacitors, diodes, and semiconductor switches while generating a high voltage gain effect with a low duty cycle. In addition, the continuous source current (CSC) and input-to-output side ground-sharing features are also available for renewable energy applications. The steady-state and comparative performance analysis with similar topologies and power loss calculations are presented in this paper. Furthermore, the simulation results extracted from the Matlab/Simulink are compared and analyzed with the conventional topology. Finally, the experiments are carried out by designing a 150 W laboratory prototype where the peak efficiency is found 90% while delivering 80 W power to the load side.

INDEX TERMS DC-DC converter, high voltage gain, non-isolated, voltage stress, quadratic boost converter.

I. INTRODUCTION

Recently, the power harnessing process from several green energy sources has become very attractive due to the issues, such as climate change and the continuous depletion of conventional fuels. As a result, an energy transition has become very important to achieve the global strategic sustainable goals [1]. The advancement of power electronic converter technology has established a promising solution in this regard. Employing the power electronic system interface depicted in Figure 1, the power generated from renewable energy sources can be transferred to the power grid ranging from small to large scale [2], [3]. It is very well known that the voltage received from the photo-voltaic source is intermittent type, hence a power electronic boost converter plays a crucial role in the intermediate system to uplift the input voltage [4]. The most fundamental topology of the boost and buck-boost converters can enhance the low input voltage of the converter to a required level by utilizing the pulse width modulation (PWM) control. Unfortunately, these conventional converters cannot meet the voltage boosting requirement of the real-time application [5], [6], [7]. To uplift the voltage gain, the converters need to be operated at a high duty cycle, which creates the diode's reverse recovery issue [8]. In addition to that, the electric stress on the semiconductor switch and diode become large while operating at a large duty cycle. By considering the isolation factor, the classification of DC-DC boost converter can be seen from two different aspects, namely the transformer-based and transformer-less structure. In the transformer-based configuration, the output voltage is lifted

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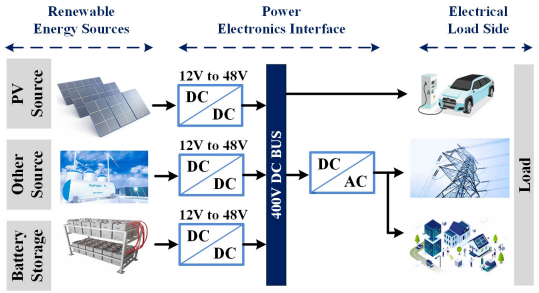

FIGURE 1. Typical application of DC-DC converter.

with a correct turn ratio [9], [10], [11] but the problem of the bulky transformer makes the converter design costly. Similarly, the converter containing the coupled-inductor on the design, arises the concern of switching transients due to leakage inductance of the coupled-inductor [12], [13], [14]. With a strong aim to improve the voltage gain of the converter, the topology introduced in [15], [16], [17], and [18] provides the cascaded structure where two similar boost converters are connected back to back to enhance the overall output voltage. However, the large number of components accommodated in this model increases the converter's size and cost. On the other hand, the interleaved boost converters proposed in [19], [20], and [21], have two or more converter stages in a parallel fashion to uplift the overall voltage and output power along with the improved profile of the input side current ripple. However, the hard PWM switching strategy in such converters ultimately shrinks the final efficiency. In order to mitigate the switching loss of the semiconductor devices, soft switching interleaved high voltage gain boost converters are proposed in [22], [23], and [24]. These soft switching converters have enabled the operation of the power conversion with reduced voltage and current stress on semiconductor devices at the higher PWM switching frequency. Furthermore, the voltage multiplier cell (VMC) based technique reported in [35], [36], and [37] provides an alternate solution to the gain enhancement where they contain one or more switched inductor/capacitor cells. The switched capacitor or charged pump techniques have been utilized in [25], [26], and [27], where the output voltage is increased by the energy transferring process between the capacitor-diode cells. Also, the switched inductor based topologies presented in [28], [29], [30], [31], and [32] utilize the parallel-series magnetizing and demagnetizing function to charge the specific capacitor for higher output voltage. Similarly, the quadratic converters developed in [29], [38], [39], [40], [41], [42], [43], [44], and [45], provide time-befitting solutions against the current issues. The topologies presented in [29], [41], and [42], convey favorable solutions to continuous source current (CSC) along with shared ground (SG) facility. However, to attain a voltage gain of around 10, the converter proposed in [40] and [41], need to run at a very high duty cycle, which introduces large voltage and current stress on the devices and ultimately shrinks the converter efficiency. In contrast, the topology reported in [29] and [42] generate a moderate output voltage gain of around 6 at 50% duty cycle along with the CSC feature. It can be seen that the topologies studied in [37] and [41], do not inherit the SG facility in the stricture. Additionally, a voltage doubler circuit (VDC) based quadratic boost converter has been presented in [44], where the output voltage of the quadratic structure is further made double with the help of VDC arrangement. This topology takes the voltage gain of the quadratic converter to an ultra-high level and that becomes 12 at 50% duty cycle having a total number of 14 components. Nonetheless, the increased number of components and the absence of an SG facility became major drawbacks of this converter. Recently, in [45], a customized voltage doubler structure-based quadratic boost converter shown in Figure 2(a), solves the high voltage gain issue with a concept of merging the conventional boost, Luo, and modified voltage doubler circuit. The topology has also the capability to uplift the voltage gain to an ultra-high level of around 10 at the same duty cycle having both the CSC and SG features. However, due to the presence of a bulky voltage doubler structure with 1 inductor, 3 capacitors, and 2 diodes, the overall component count becomes 16. Such a high component number is the highest so far according to the literature. On the other hand, another recently proposed quadratic converter according to [42], depicted in Figure 2(b), utilizes a capacitor-diode cell in the conventional cascaded boost converter structure and provides a moderate voltage gain of 6 with the same duty cycle used in [44] and [45]. The topology provides a fair voltage stress outcome on the passive and semiconductor devices at a lower duty cycle. Unfortunately, while attaining an ultra voltage gain like [44] and [45], the converter needs to be operated at a duty ratio of 54% which largely increases the overall electric stress on several components. According to the literature, the main research concern has become the attainment of the simultaneous outcome of high voltage gain with low voltage stress on the devices. Hence, a good trade-off is important to balance between the converter's voltage gain and device voltage stress by maintaining other features such as CSC and SG while modeling the converter. An optimized converter model having high voltage gain capability with a low duty cycle can ensure superior converter performance in renewable energy applications. In order to provide the most viable solution to the aforesaid limitations, this paper presents an improved ultra-high gain quadratic boost converter with lower component counts and reduced voltage stress on the device. The main features of the proposed topology are as follows:

- Ultra high voltage gain with low voltage stress on devices.
- Continuous source current and shared ground facility between the input and load side.
- Utilization of same PWM pulse for both switches and hence converter control is simple.
- The total component number is less compared to the conventional ultra-high gain topologies reported in [44] and [45].

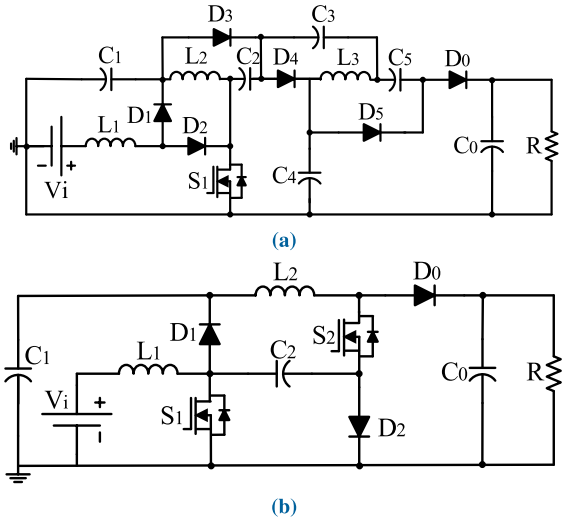

FIGURE 2. (a) Conventional topology [45], and (b) Conventional topology [42].

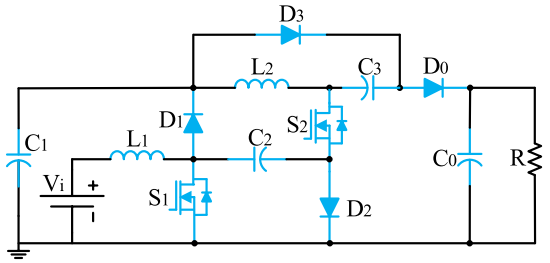

FIGURE 3. Proposed converter.

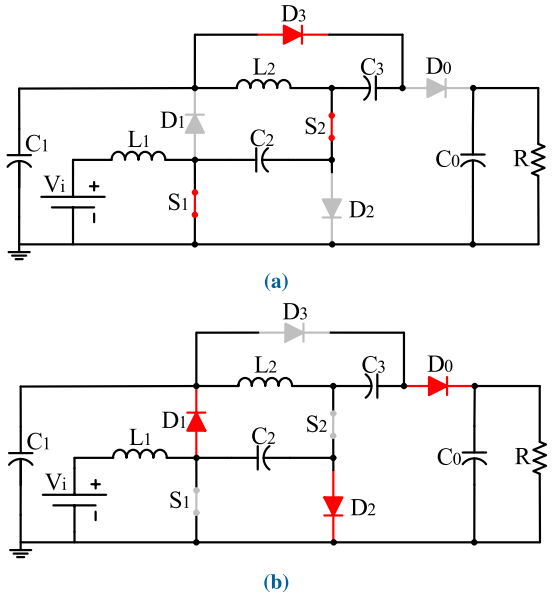

FIGURE 4. Equivalent circuits: (a) Mode-I (ON), and (b) Mode-II (OFF).

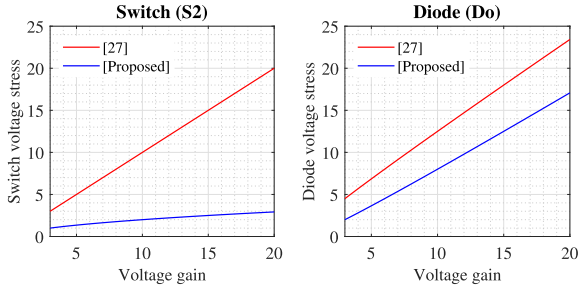

FIGURE 5. Voltage gain to components stress ratio curves.

This paper is outlined as follows: The recent literature review of the relevant converter topologies is equipped in Section I. The operating principle of the proposed topology is explained in Section II followed by the power loss analysis in Section III. Section IV covered the performance analysis of the proposed converter with various similar topologies and the result section is organized in section V with the simulation and experimental outcomes of the proposed converter. Finally, the paper ended up with the conclusion in section VI.

II. PROPOSED CONVERTER

A. CONFIGURATION OF PROPOSED CONVERTER

The proposed circuit configuration shown in Figure 3, is a VDC less ultra high gain quadratic boost converter which has been modeled with a total of 12 components, including an additional capacitor C_3 and a diode D_3 compared to the conventional model [42], shown in Figure 2(b) that utilized a total of 10 components. Besides, the converter structure shown in Figure 2(a) provides a VDC-based quadratic topology in [45], having a large number of components, i.e., 16 components in the converter design. Such a bulky VDC structure (L_3-D_4-D_5-C_3-C_4-C_5) shown in Figure 2(a), doubles the voltage gain of its quadratic network. On the other hand, the conventional converter according to Figure 2(b), utilized a switched-capacitor network (C_2-D_2) with the secondary boost converter stage. Although this network improved the traditional quadratic voltage gain of $1/(1-D)^2$ to $(1+D)/(1-D)^2$, it cannot attain the ultra-high voltage gain as proposed in [45]. The proposed circuit has introduced a switched-capacitor-based charge pump network (C_3-D_3) along with the secondary boost converter part. Hence, the proposed converter adds up the gain of $2/(1-D)$ times more with $(1+D)/(1-D)^2$. As a result, the overall converter gain has successfully reached an ultra-high level, i.e., $(3-D)/(1-D)^2$. While achieving the ultra-high level gain, i.e., 10 at a duty ratio of 0.5, the switch and diode voltage stress of the proposed converter for S_2 and D_0 is significantly reduced than the conventional model [42], which can be observed in Figure 5. The stress on the diode D_1, D_2, and D_0 and capacitor C_1 and C_2 are equal as [42] with no change in the configuration. However, due to the voltage lifting effect, the diode D_3 and capacitor C_3 experience moderate voltage stress in the proposed topology. It is notable from the configuration of the proposed converter that the voltage stress on the switch S_2 and diode D_0 are fairly distributed by

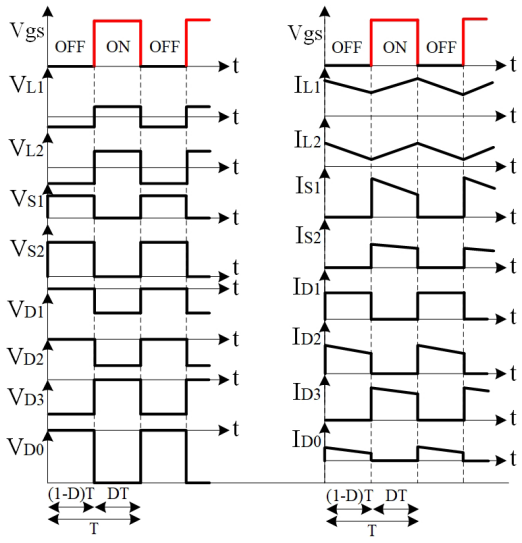

FIGURE 6. Switching waveform of proposed converter.

the newly introduced switched capacitor network (C_3-D_3). Hence, the proposed converter configuration offers a low voltage-rated component selection for designing an ultra-high gain quadratic converter. In addition, due to the same position of inductor L_1 and input to output ground terminal connection as [42], the CSC and SG facilities are still available. Hence, the performance of the proposed converter has been ultimately elevated compared to its counterparts. The switching characteristics and waves of the proposed converter can be found in Figure 6, where it is depicted that the proposed converter utilized the same PWM pulse for switching both the semiconductor switches S_1 and S_2. Hence, the control algorithm is simple for the proposed quadratic converter. The operation of the proposed converter can be divided into two states, namely mode-I (ON) and mode-II (OFF) which is explained in the next subsections.

B. MODE-I (ON) OPERATION

The mode-I state of operation can be realized with the help of Figure 4(a), where both the switches S_1 and S_2 are turned ON by the positive gate pulse V_{gs}. During this time interval, the energy storing operation on both the inductors L_1 and L_2 takes place and the inductor currents ramp up by the energy of capacitors C_1 and C_2. The diodes D_1, D_2 and D_0 get reverse biased and D_3 becomes forward biased. As the diode D_0 is OFF, hence the energy is supplied to the load by the output capacitor C_0 during this moment. The Kirchhoff's Voltage Law (KVL) equations for mode-I are derived from Figure 4(a) and can be written as follows:

$$\begin{cases} V_{L1} = L_1 \dfrac{dI_{L1}}{dt} = V_i \\ V_{L2} = L_2 \dfrac{dI_{L2}}{dt} = V_{C3} \end{cases} \tag{1}$$

The operation mode for $(1 - D)$ interval, i.e., mode-II is discussed in the following subsection.

C. MODE-II (OFF) OPERATION

The mode-II operation of the proposed converter is analyzed by following the equivalent circuit shown in Figure 4(b). At this time, both the switches are OFF and diode D_1, D_2 and D_0 become activated due to forward biased condition. The stored energy in the inductors is now transferred to the load by the capacitors C_1 and C_2. During this time, the diode D_0 becomes forward-biased and capacitor C_3 delivers energy to the output loop. The mathematical expressions for the mode-II of operation can be derived from Figure 4(b), which are as follows:

$$\begin{cases} V_{L1} = L_1 \dfrac{dI_{L1}}{dt} = V_i - V_{C1} \\ V_{L2} = L_2 \dfrac{dI_{L2}}{dt} = V_{C1} + V_{C3} - V_{C0} \end{cases} \tag{2}$$

The following subsection deals with the mathematical expression of the voltage gain of the proposed converter.

D. VOLTAGE GAIN EQUATION

To achieve the steady-state condition, the average voltage across the inductor should be zero over one complete switching period. Applying the volt-sec balance principle on inductor L_1 and L_2 with the help of the mathematical equations obtained from (1) and (2), the following expressions are found.

$$DV_i + (1 - D)(V_i - V_{C1}) = 0 \tag{3}$$

$$DV_{C3} + (1 - D)(V_{C1} + V_{C3} - V_0) = 0 \tag{4}$$

By using (1), (2), (3), and (4), the following expressions are derived for the voltage equations of capacitors C_1 C_2 and C_3.

$$V_{C1} = V_{C2} = \frac{1}{(1 - D)} V_i \tag{5}$$

$$V_{C3} = \frac{2}{(1 - D)} V_i \tag{6}$$

Finally, the mathematical expression of the voltage gain for the proposed converter comes out with the help of equations (3), (4), (5), and (6), which can be expressed as follows:

$$M = \frac{V_{C0}}{V_i} = \frac{V_0}{V_i} = \frac{(3 - D)}{(1 - D)^2} \tag{7}$$

where, V_i, V_{C0}, V_0, M, and D refer to the input voltage, output voltage, voltage gain, and duty ratio of the proposed converter. Hence, the final output voltage of the proposed converter can be determined by the following expression.

$$V_0 = \frac{(3 - D)}{(1 - D)^2} V_i \tag{8}$$

Furthermore, the voltage stress calculation, component selection, and boundary condition of the inductors are demonstrated in the subsequent sections.

E. VOLTAGE STRESS CALCULATION

During the OFF time condition, the semiconductor switches S_1 and S_2 and diodes D_1, D_2, D_3, and D_0 experience different values of voltage stress according to the design of the converter. The switch and diode voltage stress of the proposed converter can be found by the following mathematical expressions.

$$\begin{cases} V_{S1} = \dfrac{1}{(1-D)} V_i \\ V_{S2} = \dfrac{(2-D)}{(1-D)^2} V_i \\ V_{D1} = V_{D2} = \dfrac{1}{(1-D)} V_i \\ V_{D3} = V_{D0} = \dfrac{2}{(1-D)^2} V_i \end{cases} \tag{9}$$

For the lossless condition, the power should be equal for both the input to the load side, and hence, it can be expressed as follows:

$$\begin{cases} P_i = P_0 \\ \dfrac{Ii}{I_0} = \dfrac{V_0}{Vi} = M = \dfrac{(3-D)}{(1-D)^2} \\ Ii = I_{L1} = \dfrac{(3-D)}{(1-D)^2} I_0 \\ I_{L1} = \dfrac{(3-D)}{(1-D)^2} I_0 \end{cases} \tag{10}$$

where, P_i, P_0, I_i, and I_{L1} are presented as the input power, output power, input current, and inductor L_1 current. Moreover, the current expression for the inductor L_2 can be written as below:

$$I_{L2} = \frac{1}{(1-D)} I_0 \tag{11}$$

The mathematical expressions of the converter components are presented in the next subsection.

F. DESIGN OF THE COMPONENTS

The value for the inductor and capacitor can be determined with the help of the parameters, D, f_S, V_i, V_0, and R and their mathematical expressions can be written as follows:

$$\begin{cases} L_1 = \dfrac{V_i D}{\Delta I_{L1} f_S} \\ L_2 = \dfrac{2V_{C1} D}{\Delta I_{L2} f_S} \\ C_1 = C_2 = \dfrac{I_{C1}(1-D)}{\Delta V_{C1} f_S} \\ C_3 = \dfrac{I_{C3}(1-D)}{\Delta V_{C3} f_S} \end{cases} \tag{12}$$

The determination of the boundary condition for the proposed converter has been explained in the next subsection.

G. BOUNDARY CONDITION

In order to determine the desired continuous conduction mode (CCM) operation, the converter should maintain the following conditions. The relevant boundary relations of the proposed converter are provided in the subsequent mathematical equations in (14)-(15).

$$\begin{cases} \tau > \tau_B : CCMmode \\ \tau < \tau_B : DCMmode \\ \tau = \tau_B : Boundary\ mode \end{cases} \tag{13}$$

$$\begin{cases} I_{L1} = \dfrac{(3-D) I_0}{(1-D)^2} \\ \Delta I_{L1} = \dfrac{V_i D}{L_1 f_S} \\ I_{L1(min)} = I_{L1} - \dfrac{\Delta I_{L1}}{2} \\ L_1 \geq \dfrac{D(1-D)^4 R}{2(3-D) f_S} \end{cases} \tag{14}$$

$$\begin{cases} I_{L2} = \dfrac{I_0}{(1-D)} \\ \Delta I_{L2} = \dfrac{2V_{C1} D}{L_2 f_S} \\ I_{L2(min)} = I_{L2} - \dfrac{\Delta I_{L2}}{2} \\ L_2 \geq \dfrac{D(1-D)^2 R}{(3-D) f_S} \end{cases} \tag{15}$$

The normalized inductor time constant for inductors L_1 and L_2 can be written as follows:

$$\begin{cases} \tau_1 = \dfrac{2L_1 f_S}{R} \\ \tau_2 = \dfrac{L_2 f_S}{R} \end{cases} \tag{16}$$

The boundary normalized inductor time constant (τ_{B1}) and (τ_{B2}) can be finally written as follows:

$$\begin{cases} \tau_{B1} = \dfrac{D(1-D)^4}{(3-D)} \\ \tau_{B2} = \dfrac{D(1-D)^2}{(3-D)} \end{cases} \tag{17}$$

From Figure 7, the boundary condition for the proposed converter can be determined for the CCM mode of operation.

H. DISCONTINUOUS CONDUCTION MODE OF PROPOSED CONVERTER

The discontinuous conduction mode (DCM) of operation takes place when the inductor's current becomes zero. According to Figure 8, the proposed converter has three states in DCM operation. In mode-I ($0 < t < DT_S$), when the two semiconductor switches (S_1 and S_2) are ON, the CCM and DCM are the same. The inductor current ramps up according to the CCM mode-I as depicted in Figure 4(a). The peak inductor current values can be written as follows:

$$I_{L1(peak)} = \frac{Vi}{L_1} DT \tag{18}$$

$$I_{L2(peak)} = V_{C3} = 2V_{C1} = \frac{2Vi}{(1-D)L_2} DT \tag{19}$$

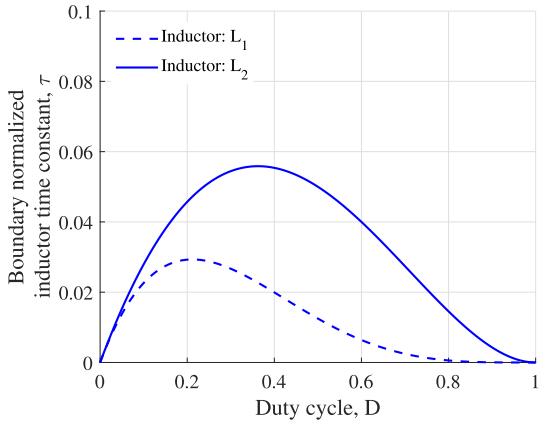

FIGURE 7. Boundary condition curves.

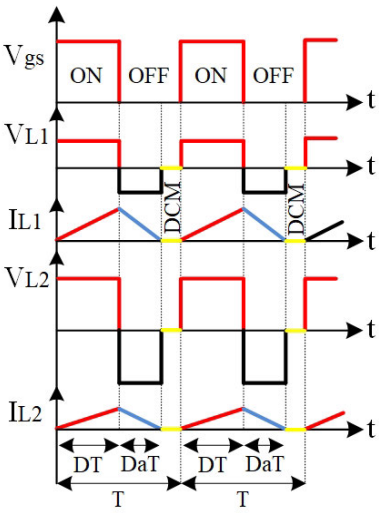

FIGURE 8. Switching waveform in DCM.

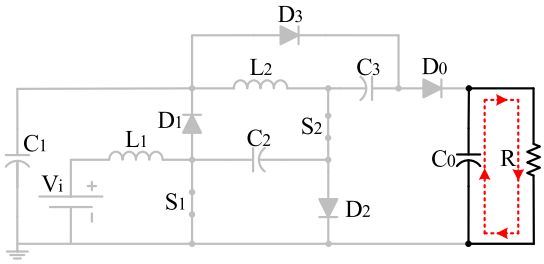

FIGURE 9. Equivalent circuit in DCM.

In mode-II ($DT_S < t < D_aT_S$), both the switches are turned OFF and inductors are demagnetized. Consequently, the inductor current reaches zero similar to the mode-II operation of CCM as shown in Figure 4(b). The peak inductor current can be written in terms of D_a as follows:

$$I_{L2(peak)} = \frac{3Vi - V_0(1-D)}{(1-D)L_2} D_a T \tag{20}$$

In mode-III ($D_aT_S < t < T_S$), both the switches remain in the OFF state and there will be no current flow through the inductors. During this period, the load current will be fed by the output capacitor as seen from Figure 9. By using equations (18), (19), and (20), the (D_a) can be expressed as follows:

$$D_a = \frac{2ViD}{3Vi - V_0(1-D)} \tag{21}$$

Again, the output capacitor current can be written by the following expression:

$$I_{C0} = \frac{1}{2} D_a I_{L2(peak)} - I_0 \tag{22}$$

By substituting (20) and (21) in (22), the output capacitor current can be rewritten as follows:

$$I_{C0} = \frac{2Vi^2 D^2 T_S}{[3Vi - V_0(1-D)](1-D)L_2} - I_0 \tag{23}$$

Further simplifying the equation of (23), the voltage gain for the proposed converter in DCM mode can be expressed as follows:

$$M_{DCM} = \frac{1}{2(1-D)} [3 \pm \frac{\sqrt{9\tau_{L2}^2 + 4D^2}}{\tau_{L2}}] \tag{24}$$

where the inductor (L_2) time constant (τ_{L2}) is $\frac{L_2 f_S}{2R}$.

I. NON-IDEAL VOLTAGE GAIN OF PROPOSED CONVERTER

The non-ideal behavior of the proposed converter shows a practical voltage gain scenario and range that can be utilized during the converter's operation. The nature of the non-ideal gain of the proposed converter is to provide a peak value of gain at a certain duty cycle. The non-ideal nature of the converter is caused by the inductor's equivalent series resistance (ESR), drain-to-source resistance of MOSFET, and forward voltage drop of diodes. The ESR of the inductors has more impact on the gain of the proposed converter which can be found in Figure 10. As from Figure 10, it can be seen that the gain of the proposed converter remains the same until the duty cycle 0.5 and the non-ideal gain starts to appear after 0.5 and onward. The difference between the ideal and non-ideal gain of the proposed converter increases with the increase of the duty cycle. The proposed converter reached its maximum gain at a duty cycle of nearly 0.72. However, keeping the output voltage constant, when the output power is increased, the non-ideal effects get increased on the gain of the proposed converter. As a result, the non-ideal gain of the proposed converter is different at different output power after the duty cycle of 0.5. Furthermore, by keeping the ESR value of the inductor lower, the gain profile of the proposed converter can be increased further.

III. POWER LOSS CALCULATION

The power loss computation of the proposed converter has been carried out by considering the equivalent circuit of the proposed converter, depicted in Figure 11. From the circuit, the non-ideal behavior of the proposed converter can be

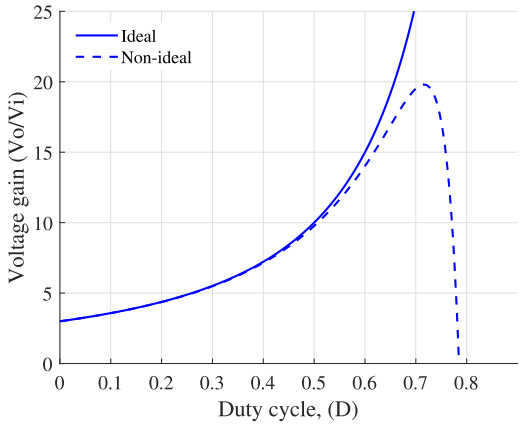

FIGURE 10. Voltage gain at non-ideal condition.

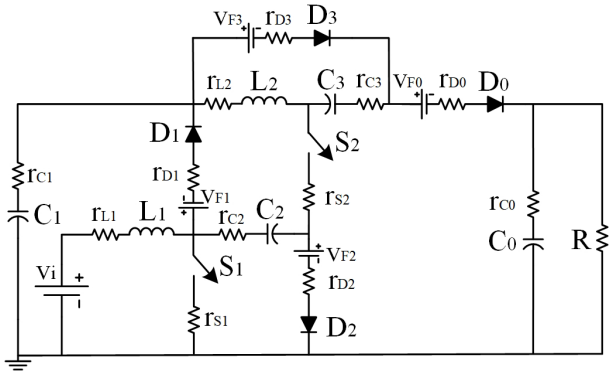

FIGURE 11. Equivalent circuit for non-ideal condition.

analyzed by considering the relevant factors such as the ESR of the inductor and capacitor, the conduction and switching loss of the semiconductor switch, and the forward voltage drop of the diodes. When both the switches S_1 and S_2 are ON, switching and conduction loss take place and that can be expressed by the following equations:

$$\begin{cases} P_{S(cond)} = [I^2_{S1(rms)} + I^2_{S2(rms)}]\, r_S \\ P_{S(sw)} = \dfrac{P_{S1}T_{(ON+OFF)}fs}{2} + \dfrac{P_{S2}T_{(ON+OFF)}fs}{2} \\ P_{S(total)} = P_{S(cond)} + P_{S(sw)} \end{cases} \tag{25}$$

where (r_S) is the ON time resistance of the switch. The power loss of the diodes are calculated by considering the diode's ON time resistance (r_D) and forward voltage drop (V_F). The diode power loss can be expressed by the following mathematical expressions.

$$\begin{cases} P_{D(r_D)} = [I^2_{D1(rms)} + I^2_{D2(rms)} + I^2_{D3(rms)} + I^2_{D0(rms)}]\, r_D \\ P_{D(V_F)} = [I_{D1(avg)} + I_{D1(avg)} + I_{D1(avg)} + I_{D1(avg)}]\, V_F \\ P_{D(total)} = P_{D(r_D)} + P_{D(V_F)} \end{cases} \tag{26}$$

Similarly, the ESR (r_L) and (r_C) of inductors and capacitors are responsible for the power loss of these passive components and can be expressed as follows:

$$P_{L(total)} = [I^2_{L1(rms)} + I^2_{L2(rms)}]\, r_L \tag{27}$$

$$P_{C(total)} = [I^2_{C1(rms)} + I^2_{C2(rms)} + I^2_{C3(rms)} + I^2_{C0(rms)}]\, r_C \tag{28}$$

At this point forward, the total power loss contributed by all the components can be calculated from the equations (25)-(28), which is written as below:

$$P_{(Total-Loss)} = P_{S(total)} + P_{D(total)} + P_{L(total)} + P_{C(total)} \tag{29}$$

Finally, the efficiency of the proposed converter can be evaluated from the following expression.

$$\eta = \frac{P_0}{P_0 + P_{(Total-Loss)}} \times 100\% \tag{30}$$

The next section provides the comparative performance analysis of the proposed converter along with the similar conventional converters.

IV. COMPARISON WITH CONVENTIONAL HIGH GAIN TOPOLOGIES

The notable features of the proposed converter have been summarized in Table 1 along with other recently proposed similar high voltage gain quadratic and cascaded converters presented in [29], [37], [40], [41], [42], [44], and [45]. Additionally, the relevant performance analysis of the proposed converter is compared, considering the voltage gain, semiconductor switch, diode, and capacitor voltage stress. From Figure 12(a), the input-to-output voltage conversion, i.e., voltage gain (M) of the converter is analyzed with respect to the duty cycle (D). It can be seen that the converters proposed in [7], [29], [33], [34], [37], [40], and [41] have the lowest voltage gain profile compared to others in the outcome. On the other hand, the gain range has been improved in [7], [34], and [42], where the initial gain was high in [42] unto a duty ratio of 0.5 but [7] showed a decent rise after 0.5 compared to [42]. Furthermore, the voltage gain has been much improved in [45] and the proposed converter, compared to all the previous topologies. It can be noted that the proposed topology can attain a voltage gain of around 10 which is the same as [45] and 1.67 times more than [42]. For achieving such an ultra-high level voltage gain, the proposed converter only utilizes 2 more components (1 capacitor and 1 diode) on its structure as compared to [42] but reduced 4 components compared to [45]. In contrast, the topology in [44] shows the highest voltage gain profile among all topologies. However, it can be seen that the total number of components utilized, is more in [44] than the proposed topology. In terms of the electric voltage stress on the semiconductor switches S_1 and S_2, the proposed converter shows superior performance than others, which can be observed from Figure 12(b) and (c). Although the conventional converter suggested in [42] provides a good voltage stress profile for switch S_1, it generates the highest stress profile for the other switch S_2. Furthermore, in most of the conventional topologies, the voltage stress on the capacitors C_1 and C_2 are the same and hence, the

TABLE 1. Comparison with different topologies.

Topology	Ref- [40]	Ref- [33]	Ref- [7]	Ref- [34]	Ref- [44]	Ref- [45]	Ref- [42]	Proposed
Switch	2	2	2	2	1	1	2	2
Diode	3	2	3	3	6	6	3	4
Inductor	2	2	4	3	2	3	2	2
Capacitor	3	3	5	4	5	6	3	4
Total	10	10	14	12	14	16	10	12
V_0/Vi	$\frac{1-D+D^2}{(1-D)^2}$	$\frac{D^2}{(1-D)^2}$	$\frac{2D(2-D)}{(1-D)^2}$	$\frac{D(1+D)}{(1-D)^2}$	$\frac{2(2-D)}{(1-D)^2}$	$\frac{3-D}{(1-D)^2}$	$\frac{1+D}{(1-D)^2}$	$\frac{3-D}{(1-D)^2}$
V_{S1}/Vi V_{S2}/Vi	$\frac{1}{(1-D)}$ $\frac{3D-2}{(1-D)^2}$	$\frac{1}{(1-D)}$ $\frac{1}{(1-D)^2}$	$\frac{1}{(1-D)}$ $\frac{1}{(1-D)^2}$	$\frac{1}{(1-D)}$ $\frac{D}{(1-D)^2}$	$\frac{1}{(1-D)}$	$\frac{D}{(1-D)^2}$	$\frac{1}{(1-D)}$ $\frac{1+D}{(1-D)^2}$	$\frac{1}{(1-D)}$ $\frac{2-D}{(1-D)^2}$
V_{D1}/Vi V_{D2}/Vi V_{D3}/Vi V_{D0}/Vi	$\frac{1}{(1-D)}$ $\frac{1-2D}{(1-D)}$ × $\frac{2D-1}{(1-D)^2}$	$\frac{1}{(1-D)}$ —— —— $\frac{D}{(1-D)^2}$	$\frac{1}{(1-D)}$ $\frac{(2-D)}{(1-D)^2}$ × $\frac{(2-D)}{(1-D)^2}$	$\frac{1}{(1-D)}$ $\frac{D}{(1-D)^2}$ —— $\frac{D}{(1-D)^2}$	$\frac{1}{(1-D)^2}$ $\frac{1}{(1-D)}$ $\frac{1}{(1-D)}$ $\frac{2-D}{(1-D)^2}$	$\frac{1}{(1-D)}$ $\frac{1}{(1-D)^2}$ $\frac{1}{(1-D)^2}$ $\frac{1}{(1-D)^2}$	$\frac{1}{(1-D)}$ $\frac{1}{(1-D)}$ × $\frac{2}{(1-D)^2}$	$\frac{1}{(1-D)}$ $\frac{1}{(1-D)}$ $\frac{2}{(1-D)^2}$ $\frac{2}{(1-D)^2}$
V_{C1}/Vi V_{C2}/Vi V_{C3}/Vi	$\frac{-1}{(1-D)}$ $\frac{1}{(1-D)}$ ——	$\frac{1}{(1-D)}$ $\frac{D}{(1-D)^2}$ $\frac{D^2}{(1-D)^2}$	$\frac{1}{(1-D)}$ $\frac{D(2-D)}{(1-D)^2}$ $\frac{(2-D)}{(1-D)^2}$	$\frac{1}{(1-D)}$ $\frac{D}{(1-D)^2}$ $\frac{D(1+D)}{(1-D)^2}$	$\frac{1}{(1-D)}$ $\frac{-1}{(1-D)}$ ×	$\frac{1}{(1-D)}$ $\frac{1}{(1-D)}$ $\frac{D}{(1-D)^2}$	$\frac{1}{(1-D)}$ $\frac{1}{(1-D)}$ ×	$\frac{1}{(1-D)}$ $\frac{1}{(1-D)}$ $\frac{2}{(1-D)}$
CSC	✓	✓	✓	✓	✓	✓	✓	✓
SG	✓	✓	✓	✓	×	✓	✓	✓

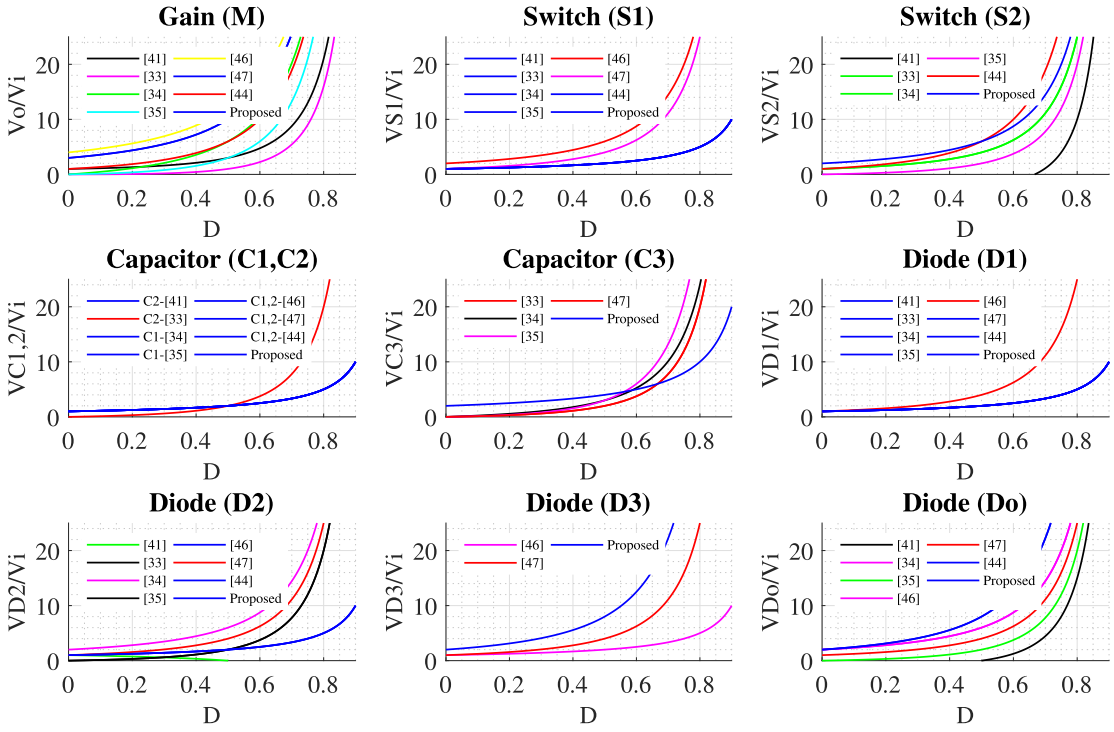

FIGURE 12. Comparative performance curves: (a) D vs V_0/V_i, (b) D vs V_{S1}/V_i, (c) D vs V_{S2}/V_i, (d) D vs $V_{C1,2}/V_i$, (e) D vs V_{C3}/V_i, (f) D vs V_{D1}/V_i, (g) D vs V_{D2}/V_i, (h) D vs V_{D3}/V_i, and (i) D vs V_{D0}/V_i.

outcome can be visualized from Figure 12(d), where it is seen that almost all the topologies have the same voltage stress on capacitors C_1 and C_2 except [33]. On the other hand, the same analysis has been carried out for the capacitor C_3 utilized in [7], [33], [34], and [45] and proposed converter, which is depicted in Figure 12(e). From Figure 12(e), it can be observed that initially, the proposed converter exhibits a tendency to generate more capacitor voltage stress compared to all, but eventually, the outcome gets settled below the range of [45]. In Figure 12(f) and (g), the voltage stress

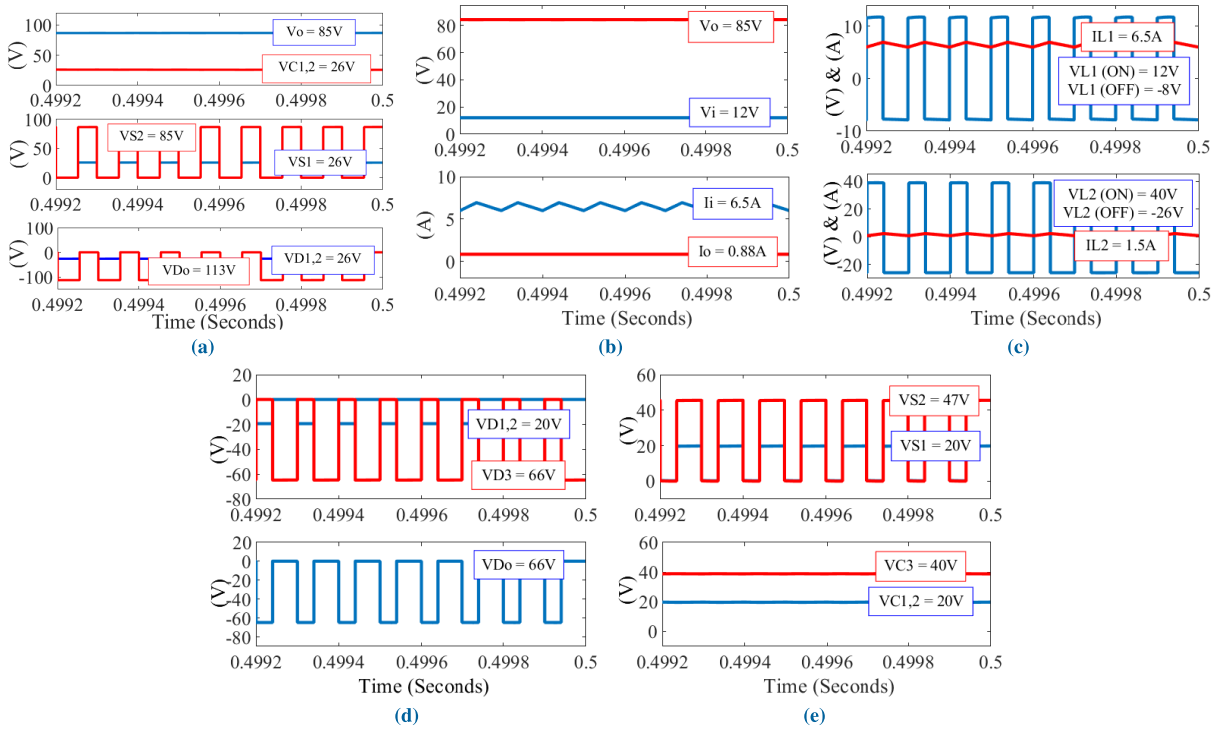

FIGURE 13. Simulation results: (a) Conventional topology: V_0, $V_{C1,2}$, $V_{S1,2}$, $V_{D1,2}$ and V_{D0}, (b) Proposed topology: V_i, V_0, I_i and I_0, (c) Proposed topology: V_{L1}, I_{L1}, V_{L2} and I_{L2} (d) Proposed topology: $V_{D1,2}$, V_{D3}, and V_{D0}, (e) Proposed topology: V_{S1}, V_{S2}, $V_{C1,2}$ and V_{C3}.

on diode D_1 and D_2 are compared and from the outcomes, it can be found that the proposed converter has very low stress profile compared to [7], [33], [34], [44], and [45] for the diodes D_1 and D_2 respectively. In contrast, the voltage stresses on the diode D_3 and D_0 of the proposed converter along with the converter [42] for diode D_0, are higher than other conventional converters which can be found in Figure 12(h) and (i). From the overall comparison, it can be summarized that the proposed converter shows comparatively superior advantages compared to the two switched-based cascaded boost converters [7], [34], where the total number of the components are the same as the proposed in [34] and more in [7]. Furthermore, other ultra-high gain converter topologies suggested in [44] and [45], utilized far more components compared to the proposed converter, hence the effective index, which indicates the ratio of the voltage gain to the total component number of the converter, is reduced. Although the proposed converter used two more components than [42], the overall performance in terms of voltage stress on the components S_1, S_2, D_1, D_2, C_1, and C_2 are significantly improved while attaining high output voltage gain with a lower value of duty cycle. The next section provides the detailed results and analysis, obtained from the simulation and experimental studies along with the efficiency outcome.

V. SIMULATION AND EXPERIMENTAL RESULTS

A. SIMULATION RESULTS

The simulation study has been performed using the Matlab/Simulink software. To evaluate the performance of the proposed converter, the input voltage (V_i) was taken as 12 V along with the duty ratio (D) of 0.4. The proposed converter can attain a voltage gain, $M = 7$ at 40% duty cycle. According to the mathematical equation (7), the gain can be counted as nearly 7.22. In order to compare the performance during the ultra-high voltage gain operation, the simulation results of the conventional converter [42] are presented in Figure 13(a). From Figure 13(a), it is evident that the conventional converter is required to operate at a duty cycle of 54% to generate the same voltage gain as the proposed converter. Notably, the conventional converter had to utilize 14% more ON time to generate that targeted ultra-high level voltage gain. During this time, the output voltage became $V_0 = 85$ V with a capacitor voltage of around $V_{C1,2} = 26$ V, which can be observed from Figure 13(a). Furthermore, the switch voltage stress is found as $V_{S1} = 26$ V and $V_{S2} = 85$ V. In addition, the voltage across diodes $D_{1,2}$ and D_0 are found as 26 V and 113 V respectively. In contrast, the simulation results of the proposed converter have been presented in Figure 13(b)-(e), where from Figure 13(b), it can be found that the proposed converter is capable of generating an output voltage of around $V_0 = 85$ V with the same input voltage and a duty ratio of 0.4. Moreover, the input and output current (I_i) and (I_0) were found as 6.5 A and 0.88 A respectively. From Figure 13(c), the inductor L_1 voltage during the ON and OFF time was found as $V_{L1(ON)} = 12$ V and $V_{L1(OFF)} = -8$ V whereas, the voltage across inductor L_2 was $V_{L2(ON)} = 40$ V and $V_{L2(OFF)} = -26$ V according to (1) and (2). The inductor currents (I_{L1}) and (I_{L2}) during this operation were found as 6.5 A and 1.5 A respectively. Due to the utilization of a

TABLE 2. Specification of components.

Components	Specifications
Inductor (L_1, L_2)	1 mH, 490 μH
Capacitor (C_1, C_2, C_3, C_0)	100 μF
Switching Frequency (f_S)	10 KHz
Load Resistance (R)	100 Ω
Semiconductor Switch (S_1, S_2)	HGTG20N60A4D
Diode (D_1, D_2, D_3, D_0)	MUR840
Gate Driver IC	TLP250
Digital Signal Processor	TMS-320F28027F

lower duty cycle, the voltage stress became less on diodes, semiconductor switches, and capacitors, compared to the conventional converter. From Figure 13(d), it can be found that the diode $D_{1,2}$ and D_0 voltages became 20 V and 66 V respectively. In addition, the switch S_1 and S_2 voltages were found as $V_{S1} = 47$ V and $V_{S2} = 20$ V from the Figure 13(e) whereas, the capacitor voltage for $C_{1,2}$ and C_3 were $V_{C1,2} = 20$ V and $V_{C3} = 40$ V respectively. From the overall simulation results and analysis, it can be noted that the voltage stress on D_0 and S_2 of the proposed converter are reduced by 41.6% and 44.7% respectively to the conventional one. Apart from that the capacitors $C_{1,2}$ and diodes $D_{1,2}$ were found to experience less voltage stress compared to the conventional topology during a high voltage gain operation.

B. EXPERIMENTAL RESULTS

A 150 W laboratory prototype has been developed to validate the performance of the proposed converter that is shown in Figure 14(a) along with the overall experimental setup given in Figure 14(b). The specification of the components is provided in Table 2. During the experiment, the PWM signal with a 40% duty cycle was applied to generate the same voltage gain achieved from the simulation results according to the theoretical equation (7). From Figure 15(a), the output voltage (V_0) and current (I_0) can be found around 80 V and 0.85 A respectively, which generates the voltage gain of around 6.67 from an input DC voltage of 12 V. From Figure 15(a), it is found that the output voltage was slightly less than expected, i.e, 6.6 V due to voltage drops across other components. However, the experimental outcome closely matches the theoretical and simulated outcomes.

The inductor L_1 voltage during the ON and OFF period was $V_{L1(ON)} = 12$ V and $V_{L1(OFF)} = -8$ V with a continuous current of 6.3 A, which can be found in Figure 15(b). On the other hand, the voltage and current values for inductor L_2 can be found in Figure 15(c), where $V_{L2(ON)} = 36$ V, $V_{L2(OFF)} = -25$ V and $I_{L2} = 1.46$ A respectively. During the high voltage gain operation, the voltage generated across the terminals of capacitor C_1 and C_2 are the same and can be found in Figure 16(a), where $V_{C1,2} = 19$ V and also the switch S_1 voltage became $V_{S1} = 18$ V. Furthermore, from Figure 16(b) and (c), the capacitor C_3 voltage and switch

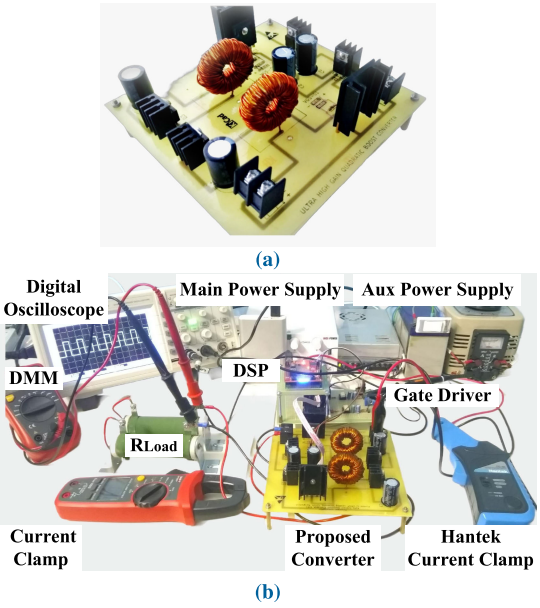

FIGURE 14. (a) Prototype of proposed converter, and (b) Experimental setup.

S_2 voltage (V_{S2}) can be found as 36 V and 46 V voltage respectively. There was a slight voltage drop of around 4 V and 7.3 V across the C_3 and S_2 according to the theoretical equation (9). In contrast, the diode voltage across D_1 and D_2 are the same and that can be observed from Figure 17(a) where, the voltage across both the diodes was found as 19 V. On the other hand, the voltage experienced by diode D_3 was $V_{D3} = 62$ V according to Figure 17(b). Although the voltage stress on diode D_3 is high compared to D_1 and D_2, the value is less for the output diode D_0, which is around $V_{D0} = 63$ V. It should be noted that D_0 experienced less voltage compared to the conventional converter while generating the same high voltage boost. As a result, the diode voltage stress V_{D0}/V_i became 5.55 according to equation (9) and which is 5.25 as per the experimental outcome shown in Figure 17(c). This phenomenon is the same for S_2 also, as the voltage stress for switch S_2 follows the voltage gain formula in the conventional converter. In that case, the proposed converter reduced the switch voltage stress V_{S2}/V_i to 4.44 according to equation (9) and Figure 16(c). Although it can be found that all the experimental outcomes shown in Figure 15-17 nearly align well with the theoretical framework and the simulation results demonstrated in Figure 13(a)-(e), still there exist some discrepancies between them due to the non-ideal behavior of the components. There is a percentage deviation of around 5.88% between the simulation and experimental values of the output voltage. This difference is mainly due to the forward voltage drop of diodes, MOSFETs, and the voltage drop across inductors and capacitors. The equivalent series resistance of the capacitors and inductors caused around 10% and 3.85% of the voltage drop which ultimately affects the output voltage. Furthermore, the drain to source

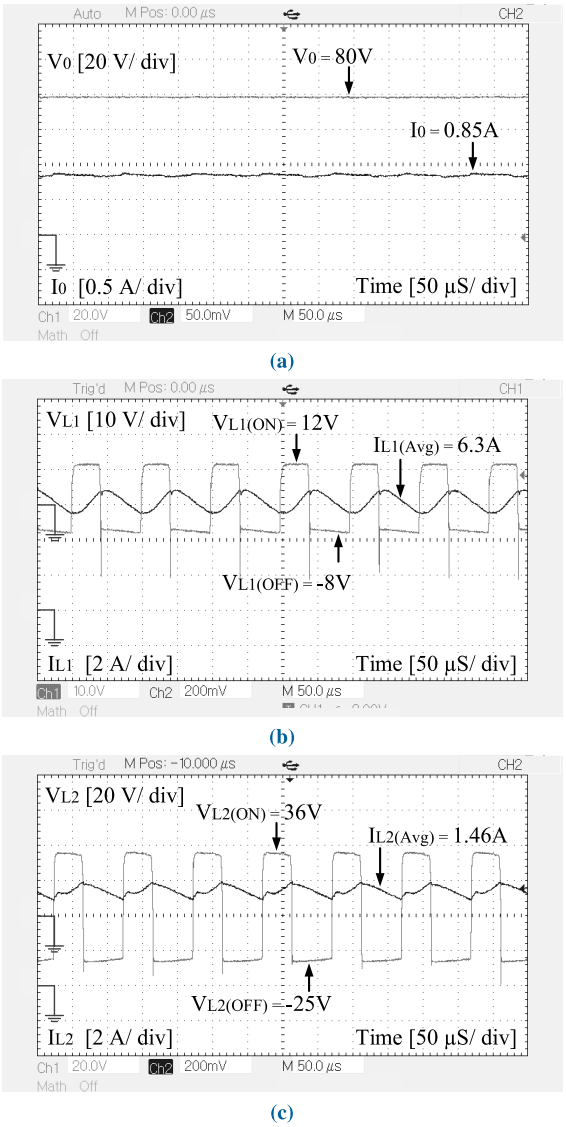

FIGURE 15. Experimental results: (a) Output voltage (V_0) and current (I_0), (b) Inductor, L_1 voltage (V_{L1}) and current (I_{L1}), and (c) Inductor, L_2 voltage (V_{L2}) and current (I_{L2}).

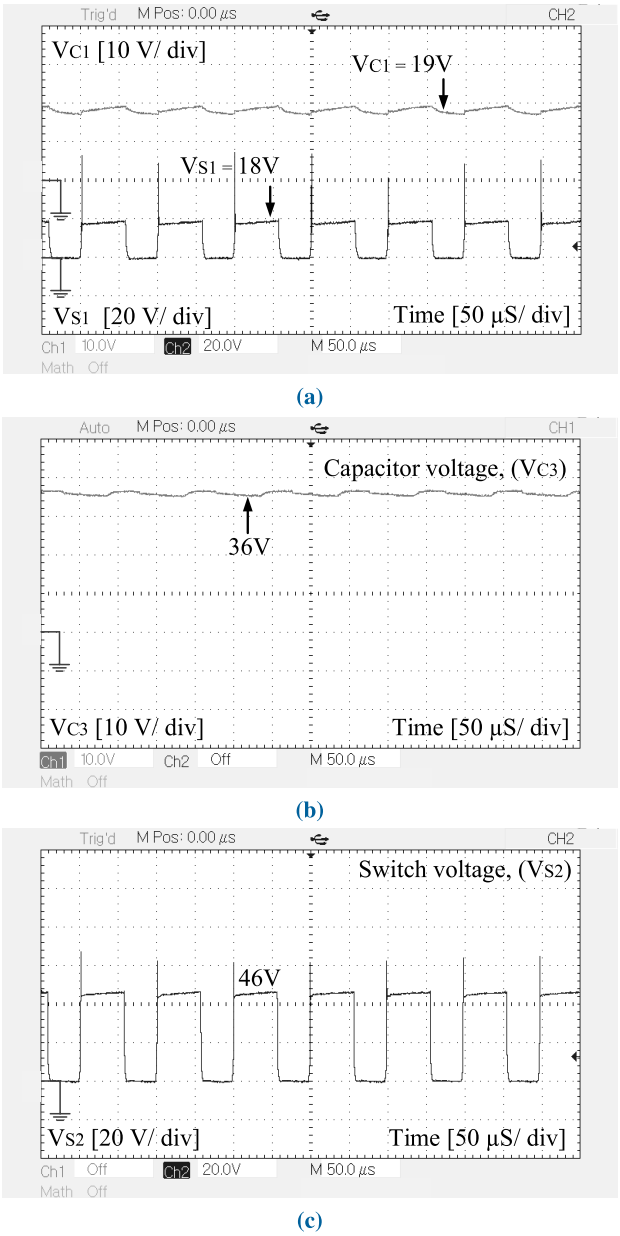

FIGURE 16. Experimental results: (a) Capacitor, C_1 voltage (V_{C1}) and switch, S_2 voltage (V_{S2}), (b) Capacitor, C_3 voltage (V_{C3}), and (c) Switch, S_2 voltage (V_{S2}).

resistance (Rds) of the MOSFETs caused around 10% and 2.12% deviation on the experimental results. It is noteworthy that toroidal inductors, switching diodes, and semiconductor devices play important roles in getting promising experimental outcomes. Hence, the performance of the converter can be further improved by ensuring high-quality inductors having lower internal resistance, fast recovery diodes with lower forward voltage drop, and MOSFET with lower Rds value.

The efficiency outcome of the conventional converter [42] and the proposed converter were carried out with a fair condition in the simulation platform and the outcome has been shown in Figure 18. From Figure 18, it can be found that the proposed converter possesses higher efficiency outcome unto a duty cycle of 0.4 whereas the conventional converter's highest efficiency peaked at around 93.4% by a duty cycle of 0.5. After the value of 0.5 and onward, the efficiency of both converters starts to decrease for the high load current. The experimental efficiency outcome from Figure 19 shows that the proposed converter reaches the highest efficiency of 90% while delivering power of 80W from the source. Furthermore, the efficiency of the proposed converter under different duty cycles has been extracted and shown in Figure 20, where the efficiency of the proposed converter shows the same characteristics as the simulated outcome shown in Figure 18. However, due to the practical losses associated with the converter's components, the proposed converter reached a maximum efficiency of 90% at 0.4 duty cycle. It should be noted that the efficiency of the proposed converter can be further improved by using high-quality circuit elements. The

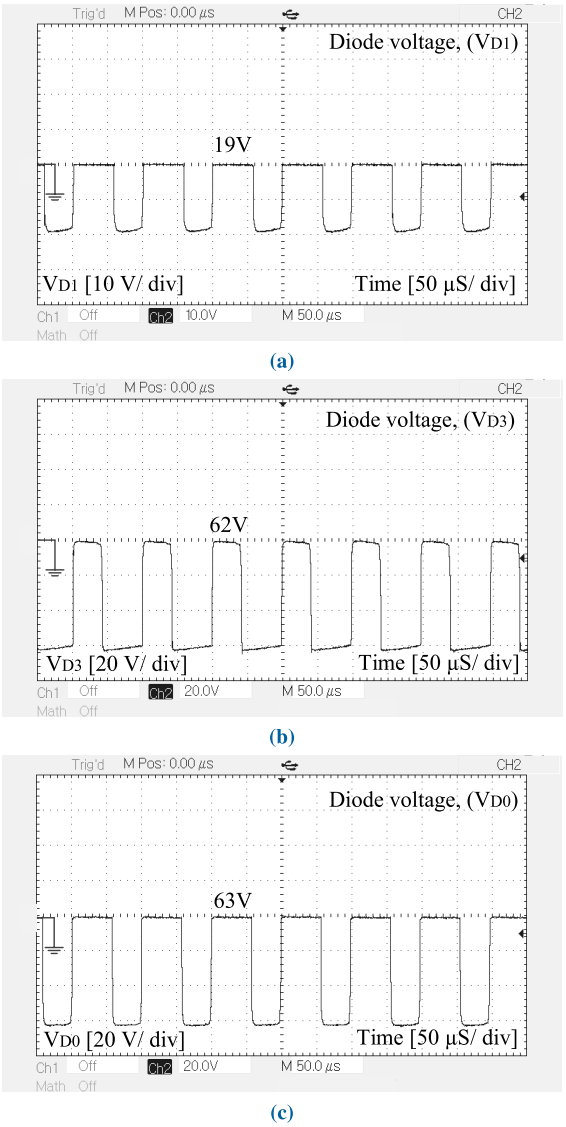

FIGURE 17. Experimental results: (a) Diode, D_1 voltage (V_{D1}), (b) Diode, D_3 voltage (V_{D3}), and (c) Diode, D_0 voltage (V_{D0}).

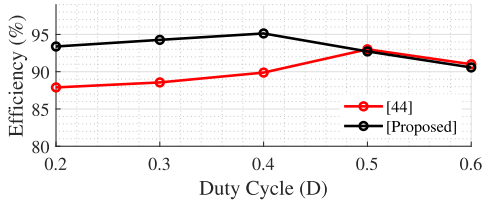

FIGURE 18. Efficiency comparison.

power loss distribution shown in Figure 21, illustrates that the diodes contributed 4% of the power loss whereas, the semiconductor switches accounted an amount of 2% to the overall loss. On the other hand, the inductors and capacitors curtailed 3% and 1% to the overall loss respectively. According to the findings and analysis, the proposed converter shows

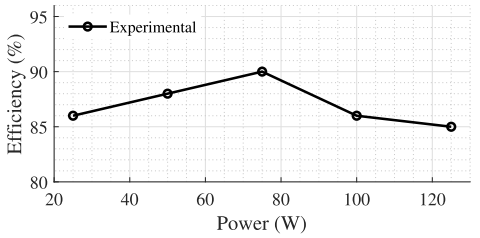

FIGURE 19. Efficiency curve.

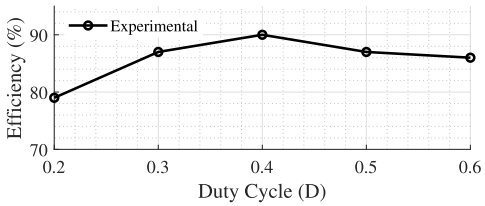

FIGURE 20. Efficiency curve at different duty cycle.

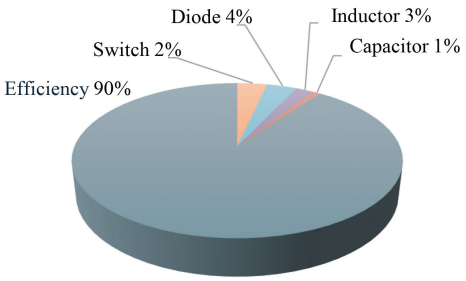

FIGURE 21. Power loss distribution.

a competitive efficiency outcome besides high voltage gain and reduced device voltage stress performance.

VI. CONCLUSION

In this article, an improved non-inverting quadratic boost converter has been proposed. The proposed converter attained an ultra-high level of voltage gain with a low-duty cycle and hence, the generated voltage stresses on the devices were low. The proposed converter established a good trade-off between the voltage gain and the overall size of the design, due to the low device voltage stress and less component utilization compared to the conventional topologies. In addition, the CSC facility ensured the prolonged life of the source as well as omitted the need for the input filter in renewable energy applications. Although the voltage stress of capacitor C_3 and diode D_3 are relatively higher, i.e., 2 and 3.3 times respectively than $C_{1,2}$ and $D_{1,2}$, the stress value became significantly lower for D_0 and switch S_2, i.e., 41.6% and 44.7% compared to the conventional topologies. The proposed converter has demonstrated very superior outcomes in terms of most of the factors accounted for during the comparative performance analysis with relevant conventional topologies. However, the proposed converter requires two separate control power supplies due to the utilization of two semiconductor switches without common ground. Hence, the overall system cost gets hampered for the lower budget converter applications. As the same issue exists in both the conventional [42] and proposed

structure, so future work will deal with the solution to ensure the common ground between the switches, which ensures the reduced system cost of the converter setup. Based on the power loss analysis, the efficiency outcome of the proposed converter was found 90% while delivering the power of around 80 W with a 150W prototype. The results from both simulation and experiment well aligned with the theoretical studies and proved the credibility of the proposed converter as a suitable high voltage gain power electronic converter for the photovoltaic applications.

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REFERENCES

[1] Z. Tang, Y. Yang, and F. Blaabjerg, "Power electronics: The enabling technology for renewable energy integration," *CSEE J. Power Energy Syst.*, vol. 8, no. 1, pp. 39–52, Jan. 2022.

[2] M. Forouzesh, Y. P. Siwakoti, S. A. Gorji, F. Blaabjerg, and B. Lehman, "Step-up DC–DC converters: A comprehensive review of voltage-boosting techniques, topologies, and applications," *IEEE Trans. Power Electron.*, vol. 32, no. 12, pp. 9143–9178, Dec. 2017.

[3] M. A. B. Kumar and V. Krishnasamy, "Quadratic boost converter with less input current ripple and rear-end capacitor voltage stress for renewable energy applications," *IEEE J. Emerg. Sel. Topics Power Electron.*, vol. 10, no. 2, pp. 2265–2275, Apr. 2022.

[4] M. S. Bhaskar, V. K. Ramachandaramurthy, S. Padmanaban, F. Blaabjerg, D. M. Ionel, M. Mitolo, and D. Almakhles, "Survey of DC–DC non-isolated topologies for unidirectional power flow in fuel cell vehicles," *IEEE Access*, vol. 8, pp. 178130–178166, 2020.

[5] A. D. Nguyen, J.-S. Jason Lai, and H.-J. Chiu, "Analysis and implementation of a new non-isolated high-voltage-gain boost converter," in *Proc. IEEE Energy Convers. Congr. Expo. (ECCE)*, Sep. 2019, pp. 1251–1255.

[6] J. Li and J. Liu, "A novel buck–boost converter with low electric stress on components," *IEEE Trans. Ind. Electron.*, vol. 66, no. 4, pp. 2703–2713, Apr. 2019.

[7] K. Yari, S. H. Shahalami, and H. Mojallali, "A novel nonisolated buck–boost converter with continuous input current and semiquadratic voltage gain," *IEEE J. Emerg. Sel. Topics Power Electron.*, vol. 9, no. 5, pp. 6124–6138, Oct. 2021.

[8] N. Elsayad, H. Moradisizkoohi, and O. A. Mohammed, "A new single-switch structure of a DC–DC converter with wide conversion ratio for fuel cell vehicles: Analysis and development," *IEEE J. Emerg. Sel. Topics Power Electron.*, vol. 8, no. 3, pp. 2785–2800, Sep. 2020.

[9] Y. Wang, Y. Qiu, Q. Bian, Y. Guan, and D. Xu, "A single switch quadratic boost high step up DC–DC converter," *IEEE Trans. Ind. Electron.*, vol. 66, no. 6, pp. 4387–4397, Jun. 2019.

[10] S.-W. Lee and H.-L. Do, "Quadratic boost DC–DC converter with high voltage gain and reduced voltage stresses," *IEEE Trans. Power Electron.*, vol. 34, no. 3, pp. 2397–2404, Mar. 2019.

[11] M. Nguyen, T. Duong, Y. Lim, and Y. Kim, "Isolated boost DC–DC converter with three switches," *IEEE Trans. Power Electron.*, vol. 33, no. 2, pp. 1389–1398, Feb. 2018.

[12] S. Hasanpour, Y. Siwakoti, and F. Blaabjerg, "New single-switch quadratic boost DC/DC converter with low voltage stress for renewable energy applications," *IET Power Electron.*, vol. 13, no. 19, pp. 4592–4600, Feb. 2021.

[13] X. Fan, H. Sun, Z. Yuan, Z. Li, R. Shi, and N. Ghadimi, "High voltage gain DC/DC converter using coupled inductor and VM techniques," *IEEE Access*, vol. 8, pp. 131975–131987, 2020.

[14] R. Afzal, Y. Tang, H. Tong, and Y. Guo, "A high step-up integrated coupled inductor-capacitor DC–DC converter," *IEEE Access*, vol. 9, pp. 11080–11090, 2021.

[15] S. Poshtkouhi, A. Biswas, and O. Trescases, "DC–DC converter for high granularity, sub-string MPPT in photovoltaic applications using a virtual-parallel connection," in *Proc. 27th Annu. IEEE Appl. Power Electron. Conf. Expo. (APEC)*, Feb. 2012, pp. 86–92.

[16] S. V. K. Naresh and S. Peddapati, "New family of transformer-less quadratic buck–boost converters with wide conversion ratio," *Int. Trans. Electr. Energy Syst.*, vol. 31, no. 11, pp. 1–21, Nov. 2021.

[17] S. Ahmad, M. Nasir, J. Dąbrowski, and J. M. Guerrero, "Improved topology of high voltage gain DC–DC converter with boost stages," *Int. J. Electron. Lett.*, vol. 9, no. 3, pp. 1–13, 2020.

[18] N. Tewari and V. T. Sreedevi, "A novel single switch DC–DC converter with high voltage gain capability for solar PV based power generation systems," *Sol. Energy*, vol. 171, pp. 466–477, Sep. 2018.

[19] B. N. Alajmi, M. I. Marei, I. Abdelsalam, and N. A. Ahmed, "Multiphase interleaved converter based on cascaded non-inverting buck–boost converter," *IEEE Access*, vol. 10, pp. 42497–42506, 2022.

[20] F. Gómez-Olguín, I. Araujo-Vargas, T. Granados-Luna, P. Velázquez-Elizondo, K. Cano-Pulido, and A. Villarruel-Parra, "Design and assessment of a 30 kW/75 kHz DC-DC, two-phase dual interleaved buck—Boost converter," in *Proc. IEEE Texas Power and Energy Conf. (TPEC)*, Feb. 2018, pp. 1–6.

[21] T.-R. Granados-Luna, I. Araujo-Vargas, A. J. Forsyth, K. Cano-Pulido, P.-E. Velazquez-Elizondo, I. Cervantes, F. Gomez-Olguin, and A. Villarruel-Parra, "Two-phase, dual interleaved buck–boost DC–DC converter for automotive applications," *IEEE Trans. Ind. Appl.*, vol. 56, no. 1, pp. 390–402, Jan. 2020.

[22] N. A. Ahmed, B. N. Alajmi, I. Abdelsalam, and M. I. Marei, "Soft switching multiphase interleaved boost converter with high voltage gain for EV applications," *IEEE Access*, vol. 10, pp. 27698–27716, 2022.

[23] H. Li, H. Du, Y. Zeng, Z. Qiu, X. Jiang, and Z. Chen, "A modified interleaved capacitor clamped DC–DC converter with non-resonant soft switching," *IEEE Trans. Power Electron.*, vol. 37, no. 10, pp. 12221–12236, Oct. 2022.

[24] X.-F. Cheng, C. Liu, D. Wang, and Y. Zhang, "State-of-the-art review on soft-switching technologies for non-isolated DC–DC converters," *IEEE Access*, vol. 9, pp. 119235–119249, 2021.

[25] Y. Zeng, H. Li, W. Wang, B. Zhang, and T. Q. Zheng, "High-efficient high-voltage-gain capacitor clamped DC–DC converters and their construction method," *IEEE Trans. Ind. Electron.*, vol. 68, no. 5, pp. 3992–4003, May 2021.

[26] S. Gopinathan, V. S. Rao, and K. Sundaramoorthy, "Family of non-isolated quadratic high gain DC–DC converters based on extended capacitor-diode network for renewable energy source integration," *IEEE J. Emerg. Sel. Topics Power Electron.*, vol. 10, no. 5, pp. 6218–6230, Oct. 2022.

[27] P. Kumar and M. Veerachary, "Z-network plus switched-capacitor boost DC–DC converter," *IEEE J. Emerg. Sel. Topics Power Electron.*, vol. 9, no. 1, pp. 791–803, Feb. 2021.

[28] M. A. Salvador, J. M. De Andrade, T. B. Lazzarin, and R. F. Coelho, "Non-isolated high-step-up DC–DC converter derived from switched-inductors and switched-capacitors," *IEEE Trans. Ind. Electron.*, vol. 67, no. 10, pp. 8506–8516, Oct. 2020.

[29] G. G. Kumar, K. Sundaramoorthy, V. Karthikeyan, and E. Babaei, "Switched capacitor–inductor network based ultra-gain DC–DC converter using single switch," in *IEEE Transactions on Industrial Electronics*, vol. 67, no. 12, pp. 10274–10283, Dec. 2020.

[30] B. Faridpak, M. Bayat, M. Nasiri, R. Samanbakhsh, and M. Farrokhifar, "Improved hybrid switched inductor/switched capacitor DC–DC converters," *IEEE Trans. Power Electron.*, vol. 36, no. 3, pp. 3053–3062, Mar. 2021.

[31] S. Pirpoor, S. Rahimpour, M. Andi, N. Kanagaraj, S. Pirouzi, and A. H. Mohammed, "A novel and high-gain switched-capacitor and switched-inductor-based DC/DC boost converter with low input current ripple and mitigated voltage stresses," *IEEE Access*, vol. 10, pp. 32782–32802, 2022.

[32] S. Sadaf, M. S. Bhaskar, M. Meraj, A. Iqbal, and N. Al-Emadi, "A novel modified switched inductor boost converter with reduced switch voltage stress," *IEEE Trans. Ind. Electron.*, vol. 68, no. 2, pp. 1275–1289, Feb. 2021.

[33] M. Veerachary and M. R. Khuntia, "Design and analysis of two-switch-based enhanced gain buck–boost converters," *IEEE Trans. Ind. Electron.*, vol. 69, no. 4, pp. 3577–3587, Apr. 2022.

[34] P. M. García-Vite, J. C. Rosas-Caro, A. L. Martínez-Salazar, J. D. J. Chavez, A. Valderrábano-González, and V. M. Sánchez-Huerta, "Quadratic buck–boost converter with reduced input current ripple and wide conversion range," *IET Power Electron.*, vol. 12, no. 15, pp. 3977–3986, Dec. 2019.

[35] M. L. Alghaythi, R. M. O'Connell, N. E. Islam, M. M. S. Khan, and J. M. Guerrero, "A high step-up interleaved DC-DC converter with voltage multiplier and coupled inductors for renewable energy systems," *IEEE Access*, vol. 8, pp. 123165–123174, 2020.
[36] A. Alzahrani, M. Ferdowsi, and P. Shamsi, "A family of scalable non-isolated interleaved DC-DC boost converters with voltage multiplier cells," *IEEE Access*, vol. 7, pp. 11707–11721, 2019.
[37] J. Leyva-Ramos, R. Mota-Varona, M. G. Ortiz-Lopez, L. H. Diaz-Saldierna, and D. Langarica-Cordoba, "Control strategy of a quadratic boost converter with voltage multiplier cell for high-voltage gain," *IEEE J. Emerg. Sel. Topics Power Electron.*, vol. 5, no. 4, pp. 1761–1770, Dec. 2017.
[38] S. Miao, F. Wang, and X. Ma, "A new transformer less buck–boost converter with positive output voltage," *IEEE Trans. Ind. Electron.*, vol. 63, no. 5, pp. 2965–2975, May 2016.
[39] J. C. Rosas-Caro, J. E. Valdez-Resendiz, J. C. Mayo-Maldonado, A. Alejo-Reyes, and A. Valderrabano-Gonzalez, "Quadratic buck–boost converter with positive output voltage and minimum ripple point design," *IET Power Electron.*, vol. 11, no. 7, pp. 1306–1313, Jun. 2018.
[40] M. Veerachary and N. Kumar, "Analysis and design of quadratic following boost converter," *IEEE Trans. Ind. Appl.*, vol. 56, no. 6, pp. 6657–6673, Nov. 2020.
[41] G. Li, X. Jin, X. Chen, and X. Mu, "A novel quadratic boost converter with low inductor currents," *CPSS Trans. Power Electron. Appl.*, vol. 5, no. 1, pp. 1–10, Mar. 2020.
[42] S. V. K. Naresh, S. Peddapati, and M. L. Alghaythi, "Non-isolated high gain quadratic boost converter based on Inductor's asymmetric input voltage," *IEEE Access*, vol. 9, pp. 162108–162121, 2021.
[43] J. D. Navamani, A. Geetha, D. Almakhles, A. Lavanya, and J. S. M. Ali, "Modified LUO high gain DC–DC converter with minimal capacitor stress for electric vehicle application," *IEEE Access*, vol. 9, pp. 122335–122350, 2021.
[44] A. Mahmood, M. Zaid, J. Ahmad, M. A. Khan, S. Khan, Z. Sifat, C.-H. Lin, A. Sarwar, M. Tariq, and B. Alamri, "A non-inverting high gain DC–DC converter with continuous input current," *IEEE Access*, vol. 9, pp. 54710–54721, 2021.
[45] T. Rahimi, L. Ding, H. Gholizadeh, R. S. Shahrivar, and R. Faraji, "An ultra high step-up DC–DC converter based on the boost, Luo, and voltage doubler structure: Mathematical expression, simulation, and experimental," *IEEE Access*, vol. 9, pp. 132011–132024, 2021.

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