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RESEARCH ARTICLE

Impact of Fin Width on Low-Frequency Noise in AlGaN/GaN FinFETs: Evidence for Bulk Conduction

KI-SIK IM, (Member, IEEE)
Department of Green Semiconductor System, Daegu Campus, Korea Polytechnics, Daegu 41765, South Korea

e-mail: ksim3492@gmail.com

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ABSTRACT AlGaN/GaN Fin-shaped field-effect transistors (FinFETs) with nano-sized Fin width (W_{Fin}) from 20 nm to 230 nm are characterized using low-frequency noise (LFN) measurement. All devices exhibit 1/*f* noise shape with Hooge mobility fluctuations (HMF) at subthreshold region and carrier number fluctuations (CNF) at accumulation region. However, the lowest normalized drain current noise spectral densities (S_{Id}/I_d^2) are obtained in the narrow Fin device (W_{Fin} = 20 nm). This is due to significant contribution of bulk channel without the 2-dimensional electron gas density (2DEG) channel and two sidewall metal-oxide-semiconductor (MOS) channels. It is also noticed that the lowest trap density (N_t) and a large separation in CNF noise model clearly indicate to the volume accumulation effect caused by bulk conduction in narrow device. The Hooge constants (α_H) extracted by HMF noise model for the narrow device are one-order higher than those of the wide Fin device, which tells that the narrow device suffers from the strong phonon scattering in the bulk channel. From the product of (S_{Id} × frequency (*f*)) versus I_d curves, the volume accumulation phenomenon is also clearly observed in narrow Fin device.

INDEX TERMS AlGaN/GaN FinFET, fin width, low-frequency noise, bulk conduction, volume accumulation.

I. INTRODUCTION

AlGaN/GaN heterojunction makes the enhanced carrier confinements at the interface between AlGaN and GaN layer, which improves the device performances for high-frequency electronics and light-emitting diodes (LED) applications [1], [2], [3], [4]. The conventional planar AlGaN/GaN-based heterojunction field-effect transistors (HFETs) have a large 2-dimensional electron gas density (2DEG) of 10^{13} cm^{-2} with high electron mobility of 2000 $cm^2/V{\cdot}s$. It enables them to exhibit the normally-on operation with negative threshold voltage (V_{th}) for high current device application [1]. On the other hand, GaN metal-oxide-semiconductor FETs (MOSFETs) presents the relatively low mobility of 300 $cm^2/V{\cdot}s$, but the normally-off operation, which is very suitable for power switching application [5], [6].

On the other hand, GaN-based nanowire FETs have several applications, such as low-power electronics and flexible devices due to their superior material properties, such as high piezoelectrical properties, large effective mass, and low permittivity compared to the Si, GaAs, and all oxide semiconductors [7], [8], [9]. Recently, several groups reported about the non-planar AlGaN/GaN-based Fin-shaped FETs (FinFETs), which consists of two channels; one is top 2DEG channel formed at AlGaN/GaN heterojunction and the other is two MOS channels on oxide/GaN sidewalls [10], [11], [12]. The fabricated AlGaN/GaN FinFETs showed superior device performances, such as the excellent off-state performances and broaden transconductance (g_m) with the reduced current collapse, due to the coupling effect of two channels and the improved gate controllability. In addition, Fin width (W_{Fin})

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dependent physical models for AlGaN/GaN FinFETs were proposed in order to verify the experimental data from the literatures [10], [11], [12] and derive the equation of V_{th} and drain current (I_d) for 2DEG and MOS channels [13], [14].

Our group has already reported on the low-frequency noise (LFN) analysis in AlGaN/GaN nanowire FinFETs in order to find the dominance of the channel conduction mechanisms (2DEG versus MOS conduction) and also calculate the trap density (N_t) [15], [16]. These fabricated Fin devices showed the carrier number fluctuations (CNF) regardless of W_{Fin} and N_t of $2.4 \times 10^{21}/4.3 \times 10^{21}$ $cm^{-3} \cdot eV^{-1}$ for the narrow/wide Fin device [15]. This reduced N_t in narrow Fin device proved to be the significant volume accumulation effect, which is similar with the volume inversion phenomenon in Si FinFETs [17].

However, there are no detailed noise examinations about the bulk channel in AlGaN/GaN FinFETs. Moreover, the volume accumulation behavior in the bulk channel are not conducted and thus are needed to discuss. In this paper, we investigate the detailed W_{Fin} dependent $I_d - V_g$ and noise characterizations in order to observe the dominant contribution for various channels according to the W_{Fin} and prove the existence of bulk channel in the proposed device. These detailed noise analyses provide the accurate noise models and device reliability to the analog circuit designers and device engineers for future low-power logic applications.

II. EPITAXY GROWTH AND DEVICE FABRICATION

The detailed epitaxy growth and device fabrication were depicted in our previous reports [11], [12]. However, the brief explanations are following. The $Al_{0.3}Ga_{0.7}N$/GaN (30 nm/80 nm) heterojunction with 1-nm thick AlN interlayer was grown on 3 μm-thick GaN/sapphire substrate using metal organic chemical vapor deposition (Fig. 1(a)).

For device fabrication, Fin arrays were patterned on the AlGaN/GaN epitaxial layer using a polymethyl methacrylate (PMMA) by electron-beam lithography and then mesa isolation was formed by dry etching using Cl_2 gas. After then, surface treatment with tetramethyl-ammonium hydroxide chemical solution was following in order to smooth the etched sidewall surface of Fin arrays [6]. A 20 nm-thick Al_2O_3 gate oxide was then deposited using atomic layer deposition (ALD) machine. After the source/drain area opening, the ohmic metal (Ti/Al/Ni/Au) was deposited and directly annealed by rapid thermal process. Finally, the gate metal was deposited.

W_{Fin} are varied with from 20 nm to 230 nm and Fin height (H_{Fin}) is 200 nm with the number of Fin (N_{Fin}) of 36. The gate length (L_g)/gate-to-drain distance (L_{gd}) are 2/5 μm. The fabricated devices consist of top 2DEG channel at AlGaN/GaN heterostructure (Fig. 1(b) and Fig. 1(c)), two sidewall MOS channels at Al_2O_3/GaN interface, and bulk channel in the center of GaN Fin, as previously described (Fig. 1(b) and Fig. 1(d)). The schematic cross-sectional device structure and transmission electron microscopy (TEM) image were shown in Fig. 1(a) and Fig. 1(e).

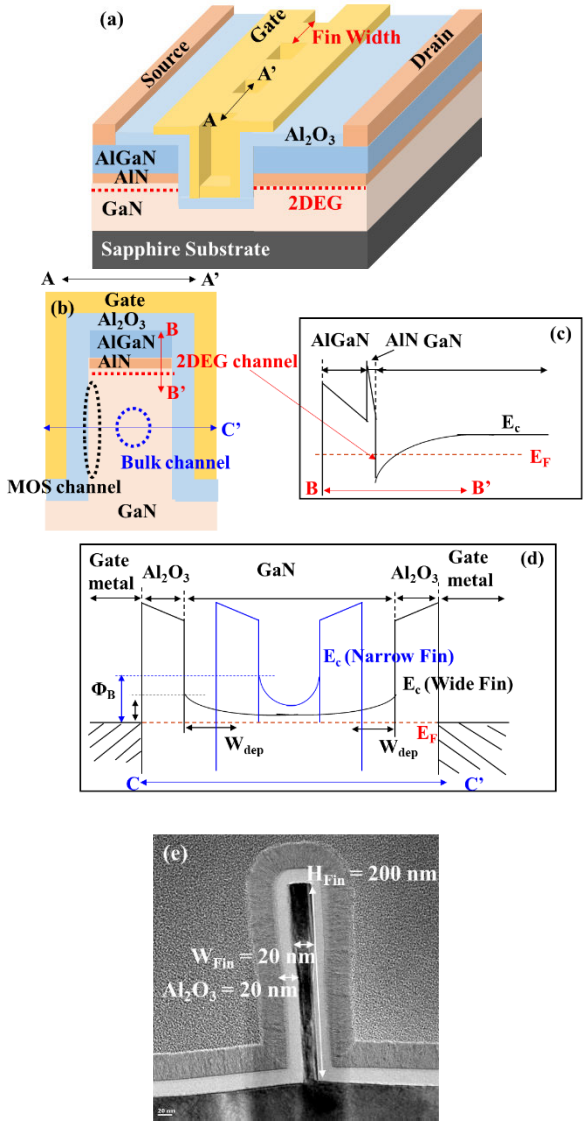

FIGURE 1. (a) Schematic illustration of the epitaxial and device structure for the proposed device. The figure of (b) shows the cross-sectional image of Fin region (A - A'), which consists of top 2DEG channel, two MOS sidewall channels, and the bulk channel. Corresponding energy band diagram of (c) AlGaN/GaN heterostructure (B - B') and (d) Al_2O_3/GaN interfaces (C - C') at $V_g = 0$ V. (e) Cross-sectional TEM image of fabricated AlGaN/GaN FinFET with $W_{Fin} = 20$ nm.

III. CHARACTERIZATION RESULTS AND DISCUSSION

Fig. 2 shows the normalized $I_d - V_g$ curves of the fabricated AlGaN/GaN FinFETs according to the W_{Fin} at $V_d = 0.1$ V. When W_{Fin} is relatively wide, the 2DEG channel in the device is significant, which results that the device presents the normally-on operation with negative V_{th}. As decreasing W_{Fin}, the V_{th} shifts to positive and also I_d decreases due to the depleted 2DEG channel caused by the fringing electric field of the wrapped gate metal in AlGaN/GaN FinFETs [10], [12].

In addition, two sidewall MOS channels with positive V_{th} become the dominant channels of device and thus contribute to the positive V_{th} shift of the proposed devices (as shown in the energy band diagram of two sidewall MOS channels

of Fig. 1(d)). From computer-based simulation in the literature [13], the calculated V_{th} of the sidewall MOS channel is expected to be approximately 0.3 V caused by the sidewall depletion regions. The bulk current through the neutral channel in the center of the GaN Fin (bulk channel) can be further shifted the V_{th} to the positive direction depending on the W_{Fin}. Although the existence of three parallel conduction paths, there are no showing a change in slope in $I_d - V_g$ curves because of the limited positive gate voltage sweeping up to 1 V caused by the quality issue of gate dielectric layer and/or the high electric field at the corner of Fin structure.

On the other hand, all Fin devices exhibit the excellent off-state leakage current and steep subthreshold slope of almost 60 mV/decade with near ideal value, thanks to the wrapped gate metal in 3D Fin structure, as shown in Fig. 2(b). The combination effects for the simultaneous turn-on of the 2DEG channel and accumulation channel at very smooth GaN sidewall surface lead to the superior subthreshold properties in the devices [18], [19].

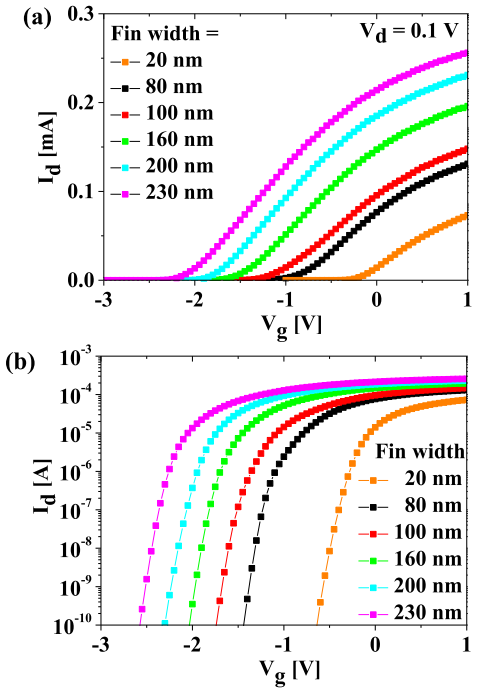

FIGURE 2. (a) Linear and (b) logarithmic scale of the normalized drain current as a function of V_g in the AlGaN/GaN FinFETs according to the W_{Fin} at V_d = 0.1 V. (The drain currents are not normalized to Fin width because three conduction channels cannot be added linearly at all bias points.)

To analyze the W_{Fin} dependent characteristics in the proposed devices, the low-frequency noise (LFN) measurements are investigated using fully automatic noise system (Synergie-concept, NOISYS7) at room temperature [20]. The measured conditions are the frequency (f) of $4 \sim 10^4$ Hz at $V_g = -3 \sim 1$ V (from deep-subthreshold to accumulation region). In order to minimize the noise fluctuations caused by the high electric field, the drain voltage is set to be 0.1 V (linear region), rather than the large voltage of over 5 V (saturation region). Fig. 3(a) exhibits the normalized drain-current noise spectral densities (S_{Id}/I_d^2) as a function of frequency at V_d = 0.1 V and ($V_g - V_{th}$) = 0.25 V, showing clearly $1/f$ dependence for varying Fin widths. This noise behavior can be explained by CNF noise model (McWhorter's model) [21], [22]. The CNF noise model is attributed to the fluctuations caused by the electron trapping/detrapping between the oxide/barrier layer and the channel and thus can be expressed as following equations [21], [22],

$$\frac{S_{Id}}{I_d^2} = \left(\frac{g_m}{I_d}\right)^2 S_{Vfb} \tag{1}$$

$$S_{Vfb} = \frac{q^2 kT\lambda N_t}{WLC_{ox}^2 f} \tag{2}$$

where g_m is transconductance and S_{Vfb} is the flat-band voltage fluctuations including q is the electron charge, kT is the thermal energy, λ is the oxide tunneling attenuation distance ($\sim$ 0.137 nm), N_t is the volumetric oxide trap density, WL is the channel area, and C_{ox} is the gate dielectric capacitance per unit area. On the other hand, the one of the possible explanations for $1/f$ noise is attributed to be due to the Hooge mobility fluctuations (HMF) using the following equation [23], [24],

$$\frac{S_{Id}}{I_d^2} = \left(\frac{g_m}{I_d}\right)\left(\frac{q\alpha_H V_{th}}{fWLC_{ox}}\right) \tag{3}$$

where α_H is Hooge parameter. The significant contribution for the HMF noise mechanism is due to the mobility fluctuation in the channel induced by the carrier-phonon interactions and their scattering.

To investigate the main contribution of the noise models for the AlGaN/GaN FinFETs with various W_{Fin}, the S_{Id}/I_d^2 are plotted in Fig. 3(b) according to the I_d. The fabricated devices exhibit the decreasing S_{Id}/I_d^2 values at subthreshold region, which are clearly confirmed to the dominance of the HMF noise model. On the other hand, the S_{Id}/I_d^2 at strong accumulation region are exponentially decreased, which can be explained by CNF mechanism. It is also interesting that all devices have almost same S_{Id}/I_d^2 values at strong accumulation region, but the lowest S_{Id}/I_d^2 values for the device with $W_{Fin} = 20$ nm are observed at subthreshold region. The reason for the lowest noise levels for the narrow Fin device at $I_d < 10^{-5}$ A is because of the volume accumulation effect in the bulk channel [15], [17]. In the narrow Fin structure, the accumulated carriers in MOS channels are repelled from the interface toward the center of the body, causing the narrow Fin device to have reduced noise [15], [17]. In addition, when the Fin width becomes very narrow ($W_{Fin} <\sim 50$ nm), the Fin device has no 2DEG channel due to the partially strain relaxation of AlGaN layer and the sidewall depletion effect induced by the fringing gate electric field, as described before [11]. In our device with narrow Fin structure, the most of currents flow through the volume of the Fin, not the surface region near Al_2O_3 gate insulator because of the maximum gate voltage of 1 V. 3D numerical simulation of AlGaN/GaN

FinFET in the range $V_g < 1$ V was supported to this phenomenon in our previous papers [18], [25]. On the other hand, the relatively large Fin devices exhibit the enhanced noise levels due to the complex channel conductions.

In order to compare the trap density (N_t) between the narrow and wide Fin devices, S_{Id}/I_d^2 values are matched with $(g_m/I_d)^2$ and then the S_{Vfb} value can be obtained in Eq. (1) (Fig. 4(a) and 4(b)). These S_{Vfb} values are divided into two drain current levels to better fit with the S_{Id}/I_d^2 values because two different noise models are involved according to the I_d. The obtained S_{Vfb} value for the relatively low drain current is 9×10^{-9} V^2/Hz, whereas for high current level in the narrow Fin device is 7×10^{-10} V^2/Hz. On the other hand, the corresponding S_{Vfb} values for wide Fin device are 3×10^{-9} V^2/Hz and 7×10^{-10} V^2/Hz, respectively. When the effective C_{ox} considers the deposited Al_2O_3 oxide layer at Al_2O_3/GaN interface and the S_{Vfb} values for the high current levels are applied in Eq. (2), the corresponding N_t are calculated to be 3.6×10^{19} $cm^{-3}\cdot eV^{-1}$ for the narrow device and 5.2×10^{19} $cm^{-3}\cdot eV^{-1}$ for the wide device. The lowest N_t value in the narrow device also proves to less charge trapping in the bulk channel due to the volume accumulation effect.

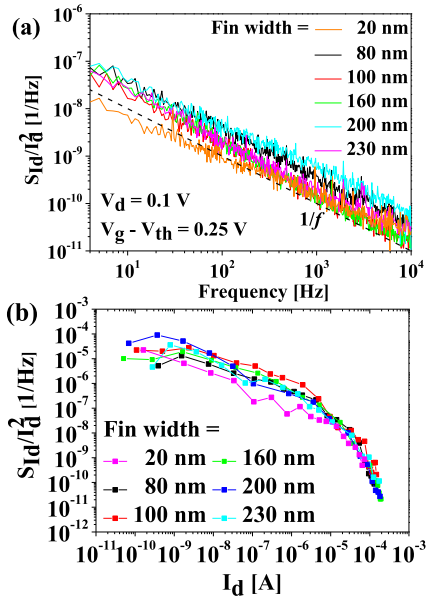

FIGURE 3. Normalized drain-current spectral density (S_{Id}/I_d^2) according to the (a) frequency and (b) I_d for the AlGaN/GaN FinFETs with various Fin widths at f = 10 Hz and V_d = 0.1 V.

It is also noticed that the S_{Id}/I_d^2 at low current levels for the narrow Fin device has a large separation from the values of $(g_m/I_d)^2 \times S_{Vfb2}$ (red color) (Fig. 4(a)). On the other hand, a small deviation between S_{Id}/I_d^2 and $(g_m/I_d)^2 \times S_{Vfb2}$ is observed in subthreshold region, as displayed in Fig. 4(b). When W_{Fin} is decreasing, the separation between S_{Id}/I_d^2 and $(g_m/I_d)^2 \times S_{Vfb2}$ is oppositely increased. This tendency is consistent with noise results in Si-based FinFETs [17], which reflects that the mobility fluctuations in the narrow Fin device are more prevailed. The reason for the dominant HMF according to the decreased Fin width is because the carriers in the channel of the narrow Fin structure are more localized in the center of body. This is believed to be due to the volume accumulation in the narrow device, as mentioned before.

Fig. 5 plots and compares the Hooge constant (α_H) for the narrow and wide devices according to the drain current. The α_H for two devices can be calculated using Eq. (3) until the relatively low drain current of 10^{-7} A because the HMF is pronounced at subthreshold region. The extracted α_H values for the narrow Fin device are obtained to be $0.5 \sim 20$, which is approximately one-order higher than those of the wide Fin device. The reason for the large α_H values of the narrow Fin device is believed that the device increases the phonon scattering in the bulk channel. On the other hand, the wide device mitigates the phonon scattering due to the superiority of the 2DEG channel with high quality.

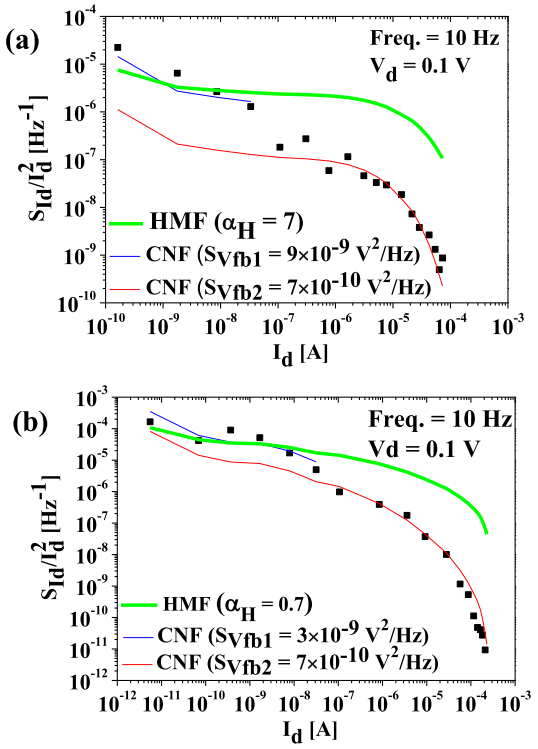

FIGURE 4. S_{Id}/I_d^2 (black square, left axis), HMF (green line), and CNF model (blue and red lines) for the (a) narrow (W_{Fin} = 20 nm) and (b) wide device (W_{Fin} = 230 nm). (the obtained noise data are measured at f = 10 Hz and V_d = 0.1 V.)

Furthermore, in order to analyze the volume accumulation in AlGaN/GaN FinFETs, the product of $S_{Id} \times f$ according to the I_d for narrow and wide Fin devices are plotted in Fig. 6. $S_{Id} \times f$ of both devices depends on the I_d^2. However, there is no observation of hump, but linearly decreasing of the $S_{Id} \times f$ at high current for narrow Fin device. This noise behavior is contributed to be due to the bulk conduction caused by the volume accumulation of narrow Fin device. On the other hand, wide Fin device exhibits a decreased

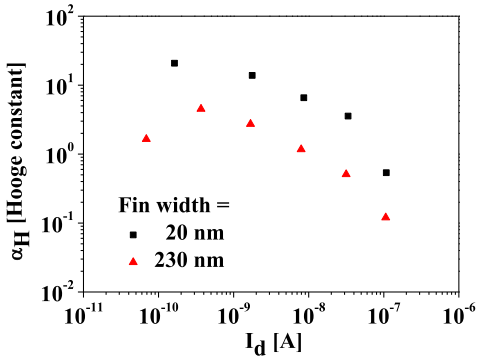

FIGURE 5. The extracted Hooge constant values according to the relatively low drain current ($I_d < 10^{-7}$ A) for the narrow and wide device at f = 10 Hz and V_d = 0.1 V.

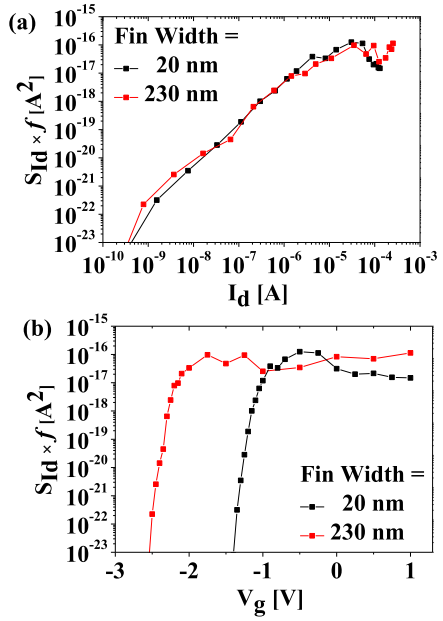

FIGURE 6. (a) $S_{Id} \times f$ versus I_d and (b) the $S_{Id} \times f$ curves according to the V_g for narrow (black rectangular) and wide (red rectangular) Fin devices. (the obtained noise data are measured at f = 10 Hz and V_d = 0.1 V.)

$S_{Id} \times f$ and hump at large drain current, which indicates to the surface conduction due to the dominance of 2DEG channel [26], [27].

IV. CONCLUSION

AlGaN/GaN FinFETs according to the W_{Fin} are characterized through noise measurements. S_{Id}/I_d^2 values for the smallest device (W_{Fin} = 20 nm) are the lowest compared to those of the other devices, which reveals to the volume accumulation effect in bulk channel of the narrow Fin device. The calculated N_t with the lowest value and a large separation in CNF noise model tell to the significant volume accumulation effect caused by bulk conduction. In addition, when compared to the product of $S_{Id} \times f$ dependent on W_{Fin}, it is clearly observed to the volume accumulation effect in the narrow Fin device. Using these noise results, the fabricated AlGaN/GaN FinFET with nano-sized W_{Fin} is mainly governed by the bulk conduction in center of GaN Fin, rather than top 2DEG channel at AlGaN/GaN heterostructure and two sidewall MOS channels at Al_2O_3/GaN interface. From these observations, the Fin width in the AlGaN/GaN FinFETs should be optimized and designed for low-power logic device and analog circuit applications.

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KI-SIK IM (Member, IEEE) received the M.S. and Ph.D. degrees in electronic engineering from Kyungpook National University, Daegu, South Korea, in 2005 and 2012, respectively. He is currently an Assistant Professor with the Department of Green Semiconductor System, Daegu Campus, Korea Polytechnics, Daegu. He has authored or coauthored over 65 articles in peer-reviewed journals. His current research interests include GaN-based electronic nanodevices and physics of III-nitride compounds.