RESEARCH ARTICLE

Active Impedance Network Buck-Boost Three-Level T-Type Inverter With Enhanced Voltage Gain

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ABSTRACT This paper proposes a new PWM technique for a reduced-component-count active impedance network (RCC-AIN) three-level inverter to maximize the input/output (I/O) voltage gain. Although the max boost control (MBC) technique offers the same I/O voltage gain, it suffers from the drawback of low-frequency (LF) ripples of the source current. In contrast, the proposed PWM technique is a combination of improved MBC (IMBC) and a new switching state pattern that eliminates this drawback and offers up to 79% reduction in the peak-to-peak ripple value of the source current while maintaining the same I/O voltage gain as MBC. The cumulative sum of ripple components is used to find the exact maximum and minimum peaks of the source current over the fundamental period. The proposed switching pattern doubles the switching frequency of a boosting switch to limit the current spikes of capacitors during state change-over. The RCC-AIN topology was analyzed in various voltage-boosting techniques, and the proposed PWM technique utilizes the full potential of the RCC-AIN topology in a better way. The findings have been verified using theoretical calculations, simulation, and experimental results.

INDEX TERMS Active impedance network, space vector PWM, shoot-through, switched boost inverter, three-level T-type inverter, Z-source inverter.

I. INTRODUCTION

Single-stage buck-boost multilevel inverters for DC-AC power conversion have a broad range of potential applications, such as distributed power generation (PV, wind, fuel cell), electric drives/vehicles, UPS, etc. [1], [2], [3], [4]. These inverters not only retain the advantages of multilevel voltage source inverters (VSIs) (low dv/dt across switches and better output voltage quality), but also offer some additional benefits such as shoot-through immunity, buck-boost operation, reduced complexity of control, and reduced number of elements compared to a conventional two-stage converter (DC-DC-AC) [5]. The essential feature of these inverters is the presence of an impedance network (IN) and the provision of short-circuiting the IN using the same PWM pattern that is used for rear-end VSI power switches. There-

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fore, a single PWM technique is sufficient for controlling the input/output (I/O) voltage gain and generating the output voltage levels.

In recent years, researchers have explored various aspects of buck-boost three-level inverters (BBTLIs) related to topologies and PWM control techniques [6], [7], [8], [9], [10], [11], [12], [13], [14], [15], [16], [17], [18]. Depending on the type of IN, these inverters can be classified into two categories: active IN (AIN) and passive IN (PIN) structures. The features that decide the performance of these inverters are the I/O gain, continuous/discontinuous input current, number and size of passive elements in the IN, IN capacitor voltage stress, common ground, neutral point capacitor voltage balancing capability (specific for more than two-level inverter), power losses, and efficiency. The I/O gain of a BBTLI depends on the configuration of the IN and shoot-through (ST) duty ratio.

The available ST duty ratio is limited by the type of control technique. A higher I/O gain at the upper modulation index
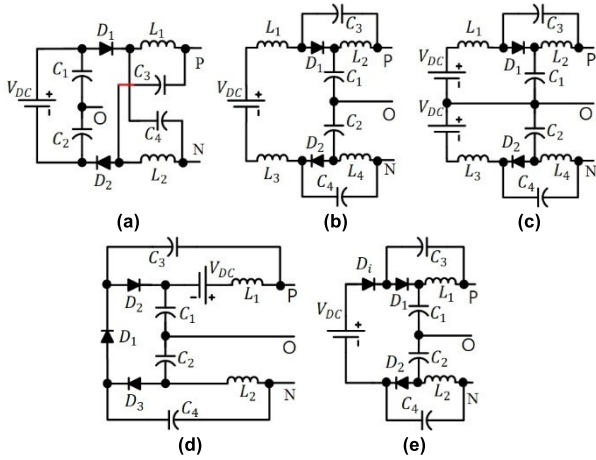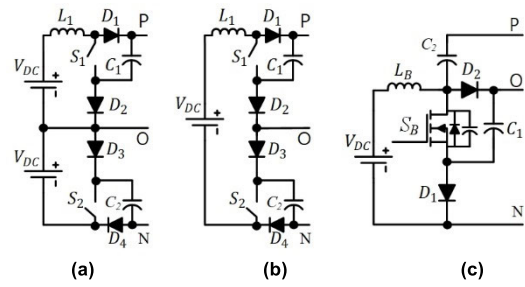
FIGURE 1. Some passive INs used in single-stage three-level inverters: (a) ZSI [6], [7], (b) qZSI [8], [9], [10], [11], [12], (c) improved qZSI [13], (d) modified ZSI (D1) [14], (e) embedded modified ZSI [15].

FIGURE 2. Topologies of some active INs used in single-stage buck-boost three-level inverters. (a) LC IN [17], (b) reduced LC count [18], [19], [20], (c) reduced component count AIN [21].

range is always desired so that power switches encounter lower voltage stress. But achieving high I/O gain by increasing the number of input DC sources and the size and number of passive elements (L and C) is not considered a good option because of size and cost. Some PIN structures have been summarized in Fig. 1. The conventional configurations of ZSI [6], [7], qZSI [8], [9], [10], [11], [12], and improved qZSI [13] are shown in Fig. 1(a), (b), and (c), respectively. The qZSI structure is more popular because it offers some benefits over ZSI, such as reduced capacitor voltage stress and continuous source current

But qZSI does not improve the I/O gain even with the addition of two more inductors.

The topology of modified ZSI (MZSI) [14] shown in Fig. 1(d) offers two times the I/O gain compared to the ZSI/qZSI. In terms of components, MZSI replaces 2 inductors in qZSI with a single diode. These features of low component count and high I/O gain make MZSI a better alternative to ZSI/qZSI. However, MZSI also suffers from the drawbacks of discontinuous input current and no common ground. Embedded MZSI [15] is shown in Fig. 1(e) and is another variant of MZSI in which the DC source has been placed in the IN to make the source current continuous. Some PINs with a transformer in them have been reported as LCCT-derived inverters [16]. The turns-ratio of the transformer decides the boost factor of these topologies. For example, for a transformer with a 1:1 ratio, the boost factor is the same as that of ZSI/qZSI.

Another class of BBTLIs uses the AIN structure. Fig. 2 shows some three-level AIN structures. These IN structures use power switches for voltage-boosting operation. These power switches have to be operated in synchronization with rear-end inverter switching states. An important thing is that all these topologies draw continuous currents from the source. The AIN structures shown in Fig. 2(a) [17] and Fig. 2(b) [18]

are similar to each other except for the number of DC sources and inductors. However, both of these configurations offer no improvement in gain and power quality compared to ZSI/qZSI. One study [19] used the same AIN as in Fig. 2(b) and proposed new switching states so that the gain can be increased. But the IN contained too many components (4 diodes, 2 capacitors, 2 active switches, and 1 inductor). The same topology has been studied for fault-tolerant operation [20].

Another study [21] proposed an optimized AIN structure and called the topology a reduced-component-count (RCC)

AIN three-level T-type inverter. The RCC-AIN inverter offers the same gain as MZSI (twice that of other AIN and PIN structures shown in Fig. 1 and Fig. 2). However, compared to the MZSI, it offers some additional features, such as reduced passive elements in the IN, continuous input current, common ground, and capacitor self-balancing. But like other AIN topologies, RCC-AIN 3L-TTalso suffers from drawbacks of non-nearest three-vector (NTV) switching. Due to this, the line voltage THD is high.

The maximum boost factor of MZSI and EMZSI from the PIN category and RCC-AIN of the AIN category is:

$$B = \frac{2}{1 - 2D} \qquad (1)$$

where D is the ST duty ratio. D depends on the type of voltage-boosting control technique. For example, the maximum boost control (MBC) technique of voltage boosting offers full utilization of null intervals for ST state insertion. The MZSI/EMZSI topology [14], [15] achieved the highest limit of I/O gain using the MBC technique. But due to the inherited drawback of MBC, the low frequency (LF) ripple components (dominant 3rd and 6th frequency) in the IN inductor and capacitors' currents and voltages have been reported [14], [15]. Additionally, the IN inductor and capacitors' currents and voltages are completely out of phase with a frequency of 3 times the fundamental frequency (F1).

The improved MBC (IMBC) [22] technique of voltage boosting has an excellent feature in that it draws smooth current from a source, but its switching pattern requires a full DC link short circuit (FST). However, the analysis of MZSI/EMZSI indicates that FST is not possible for them.

TABLE 1. Switching states of RCC-AIN 3L inverter.

ST type	State	ON Switch	V_{xo} (pole voltage)
NST	P	S_{Y1}	$0.5BV_{DC}$
NST	O	S_{Y2}, S_{Y3}	0
NST	N	S_{Y4}	$-0.5BV_{DC}$
FST	FST	S_{Y1}, S_{Y4}	0

Y=A, B, C.

Thus, the desired features of a high-gain inverter satisfying eq. (1) can be summarized as follows:

1) Minimum passive elements in the IN
2) Continuous source current and common ground structure
3) Being able to utilize the whole null interval for ST insertion without injecting LF ripple in the source current.

Analysis of RCC-AIN indicates that the gain of this topology can be extended with the IMBC technique of voltage boosting with a smooth source current.

This combination gives benefits in terms of increased power density and reduced peak-to-peak source current ripple while retaining the same I/O voltage gain as MZSI with MBC or RCC-AIN with MBC. Also, operation with a reduced CMV switching pattern is possible.

A new switching pattern is also proposed in this paper. The pattern increases the switching frequency of the boost switch without affecting the switching frequency of inverter power switches compared with RCC-AIN with SBC control used in a previous study [21]. This helps in reducing the current peaks caused by the IN capacitors during transitions from NST to ST states. To find the exact peak-to-peak ripple of the source current over the full fundamental period, theoretical calculation has been done using an approach with the cumulative sum of instantaneous ripple components. The theoretical calculations have good agreement with the simulation and experimental results.

This paper is arranged as follows. Section II reviews the operating principle of the RCC-AIN three-level T-type inverter. Section III discusses the details of the modified SVPWM and proposed switching state pattern. A comparative analysis of RCC-AIN under various voltage boost techniques has been done in section IV. Section V presents the results, and section VI concludes this paper.

II. RCC-AIN THREE-LEVEL T-TYPE INVERTER

The topology of the RCC-AIN three-level T-type inverter is shown in Fig. 3 [21]. The IN consists of 1 inductor, 2 capacitors, 2 diodes, and 1 power switch (SB). The power switch works in synchronization with the ST signal applied to the inverter phase legs. A T-type three-level inverter topology is connected at the rear end to generate three output voltage levels. The switching states are summarized in Table 1.
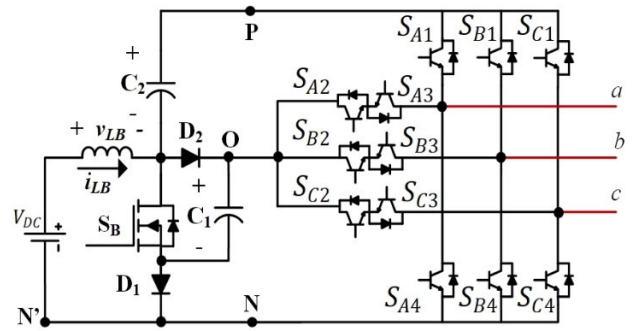

FIGURE 3. Configuration of RCC-AIN single-stage buck-boost three-level inverter [21].

TABLE 2. Length of switching vectors.

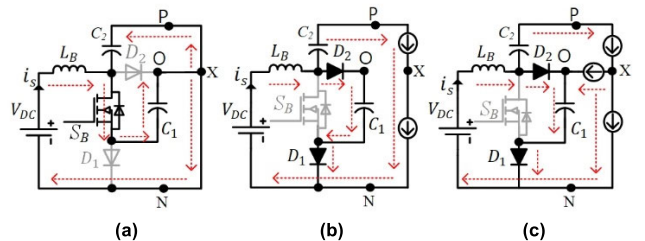| Switching vector	Switching vectors	Length (per BV_{DC})	Used length
Large	V_1 to V_6	$1.154 \times (BV_{DC})$ $= 1.154V_{DC}.$	$1.15 \times \left(\dfrac{1}{1.154}BV_{DC}\right)$ $= BV_{DC}.$
Medium	V_{13} to V_{18}	$1 \times (BV_{DC}) =$ $BV_{DC}.$	$1 \times (BV_{DC}) = BV_{DC}.$

FIGURE 4. Equivalent circuit diagrams: (a) during shoot through (ST) state, (b) when large vector applied (PNN), (c) when medium vector is applied (PON). NOTE- when null vectors are completely replaced by ST states, NST states contain only large and medium vectors.

A. OPERATING PRINCIPLE

There are two main operating modes of the inverter: shoot-through (ST) and non-shoot-through (NST) modes. The ST state has two types of classifications: FST and alternate upper- lower ST [14]. The FST method shorts the full DC-link, which ultimately requires a state [OOO] in the switching sequence. This results in a non-NTV switching sequence. The NTV switching can be preserved only if alternate upper-lower ST insertion states are used, as done in another study [14]. The FST method is more suitable for this configuration. The NST states contain the same switching states as three-level VSI.

Fig. 4 shows the equivalent circuit diagrams of the RCC-AIN inverter during ST (Fig. 4(a)) and NST states (Fig. 4(b) and (c)). The steady-state analysis of the inverter during these states gives the following expressions [21]:

During ST state:

$$\left.\begin{array}{l} v_{LB} = V_{DC} + V_{C1} \\ V_{C1} = V_{C2} \\ V_{PN} = 0 \\ i_{C1} + i_{C2} = -I_{LB} \end{array}\right\} \quad (2)$$

During ST state:

$$\left.\begin{array}{l} v_{LB} = V_{DC} + V_{C1} \\ V_{C1} = V_{C2} \\ V_{PN} = 0 \\ i_{C1} + i_{C2} = -I_{LB} \end{array}\right\} \quad (3)$$

During NST state:

$$\left.\begin{array}{l} v_{LB} = V_{DC} - V_{C1} \\ V_{PN} = V_{C1} + V_{C2} \\ i_{C1} = I_{LB} - I_o \\ i_{C2} = -I_o \end{array}\right\} \quad (4)$$

where I_o is the equivalent DC current on the inverter side.

The important expressions found from the steady state analysis of the inverter during ST state time (DT) and NST state time {(1-D)T} are as follows:

The average capacitor voltage is:

$$V_C = V_{C1} = V_{C2} = \frac{1}{1 - 2D} V_{DC} \quad (5)$$

The expression for average inductor current is:

$$I_{LB} = \frac{2(1 - D)}{1 - 2D} I_o \quad (6)$$

The DC-link voltage during NST state can be written as:

$$V_{PN} = V_{C1} + V_{C2} \Rightarrow \frac{2}{1 - 2D} V_{DC} \quad (7)$$

The boost factor B is defined as:

$$B = \frac{V_{PN}}{V_{DC}} = \frac{2}{1 - 2D} \quad (8)$$

III. IMPROVED MAXIMUM BOOST CONTROL (IMBC) AND PROPOSED SWITCHING PATTERN

The IMBC technique is based on the modified space vector (SV) switching state diagram. This technique was first reported for a conventional three-level ZSI [22] and has an excellent capability of reducing the LF ripple component in the IN inductor current for a three-level ZSI while utilizing the full duration of the null interval as an ST state. In the modified SV diagram, the length of large vectors is modified and considered equal to that of medium vectors. The conventional hexagon (the outermost hexagon) and modified 12-sided inner polygon are shown in Fig. 5. The inner 12-sided polygon was drawn based on the modified length of large vectors according to the instantaneous per-unit DC-link voltage [22]. Modified large vectors are indicated in Fig. 5 by V_x', where x=1 to 6. The complete SVPWM switching diagram is divided into 12 sectors. Fig. 5 contains 2 circles that are explained as follows:

Circle 1. This circle indicates the maximum available length of the reference vector for the conventional case. In this
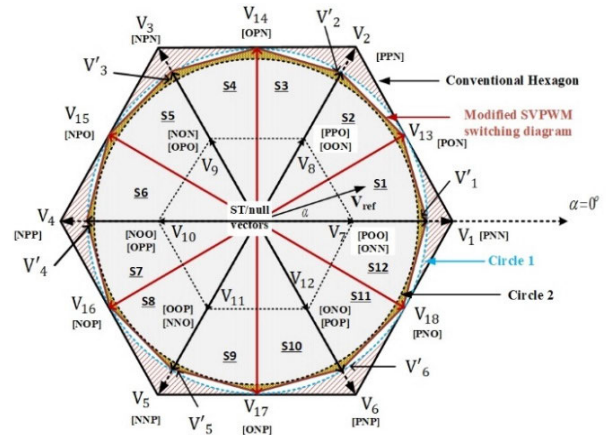

FIGURE 5. Switching state diagrams of conventional and modified SVPWM [22].
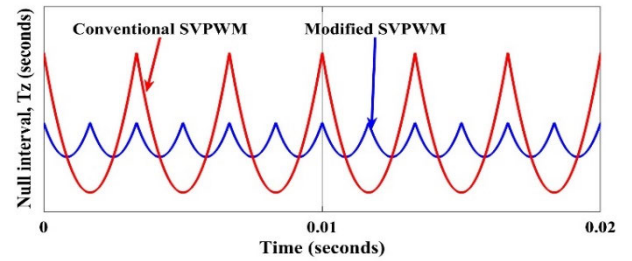

FIGURE 6. Behavior of null interval using conventional and modified SVPWM.

case, the per unit DC-link lengths of the large vector and medium vector are 1.15 and 1, respectively. The resultant maximum length of the reference vector is 0.866 in the linear modulation index region.

Circle 2. This circle indicates the maximum available length of the reference vector when both large and medium vectors have the same length (1 per unit DC-link voltage). In this case, the maximum length of the reference vector can be up to 0.96. The lengths of all vectors are shown in Table 2. The modification increases the frequency of the null interval from 6 to 12 times the fundamental frequency (F_1), as shown in Fig. 6.

A. DWELL TIME CALCULATION EQUATIONS

Consider, the reference vector (V_{ref}) is located in sector 1 of the inner SV diagram of Fig. 5. At this position, V_{ref} can be synthesized by switching vectors V_1 (large vector), V_{13} (medium vector), and V_0 (null vector) for the time durations of T_a, T_b, and T_z, respectively.

$$T_a = \left(\frac{V_{ref}}{BV_{DC}}\right)\left(\frac{Sin(\pi/6 - \alpha)}{Sin(\pi/6)}\right) T_s \quad (9)$$

$$T_b = \left(\frac{V_{ref}}{BV_{DC}}\right)\left(\frac{Sin(\alpha)}{Sin(\pi/6)}\right) T_s \quad (10)$$

$$T_z = T_s - T_a - T_b \quad (11)$$

TABLE 3. Comparison of RCC-AIN parameters with SBC, MBC and IMBC technique.

Parameter	RCC-AIN with SBC [21]	RCC-AIN with MBC and switching patterns same as of [21]	RCC-AIN with IMBC and proposed switching pattern
ST duty ratio, D	$D = 1 - M$	$\overline{D} = (2\pi - 3\sqrt{3}M)/(2\pi)$	$\overline{D} = (\pi(CF) - 9M_m(2 - \sqrt{3}))/(\pi(CF))$
Boost factor, B	$2/(2M - 1)$	$2\pi/(3\sqrt{3}M - \pi)$	$2\pi CF/(18M_m(2 - \sqrt{3}) - \pi CF)$
Voltage gain (G=MB)	$2M/(2M - 1)$	$2M\pi/(3\sqrt{3}M - \pi)$	$2M_m\pi CF/(18M_m(2 - \sqrt{3}) - \pi CF)$
Voltage stress across, boost switch (SB), diode, and capacitors	$V_{DC}/(2M - 1)$	$V_{DC}\pi/(3\sqrt{3}M - \pi)$	$\dfrac{V_{DC}\pi CF}{18M_m(2 - \sqrt{3}) - \pi CF}$
Peak-to-peak ST duty ratio, (D_{p2p})	0	$\dfrac{M(2\sqrt{3} - 3)}{4}$	$\dfrac{3M_m}{CF}\left(\sin\left(\dfrac{\pi}{12}\right) - \dfrac{1}{4}\right)$
ST current	$2M/(2M - 1)$	$3\sqrt{3}M/(3\sqrt{3}M - \pi)$	$\dfrac{18M_m(2 - \sqrt{3})}{18M_m(2 - \sqrt{3}) - \pi CF}$
6th-order ripples in the source current	no	yes	no
Switching frequency of 'SB',	fc	fc	2fc
Switching frequency of power switch (S_{X1}-S_{X4})	fs(S_{X1} & S_{X4})=fc fs(S_{X2} & S_{X3})=fc/3	fs(S_{X1} & S_{X4})=fc/3 fs(S_{X2} & S_{X3})=fc/3	fs(S_{X1} & S_{X4})=fc/2 fs(S_{X2} & S_{X3})=fc/6

Here fc is carrier frequency and fs is switching frequency

The null interval (T_z) was used for the insertion of the FST state. The state [OOO] is completely replaced by FST. The average value of the null interval over the fundamental cycle can be found by integrating (10) over one sector.

$$\overline{D}_m = \frac{6}{\pi}\int_0^{\pi/6}\left(\frac{T_z}{T_s}\right)d\alpha = 1 - \frac{12\left(2 - \sqrt{3}\right)V_{ref}}{\pi BV_{DC}}. \quad (12)$$

The maximum length of the reference vector with the modified SVPWM switching diagram is defined as:

$$V_{ref,max} = 0.96BV_{DC}. \quad (13)$$

Since V_{ref} does not have constant magnitude, it needs to be modified using a correction factor (CF=0.933) [22] to find a true value of the modulation index. The modulation index is defined as:

$$M_m = \frac{4V_{ref}}{3BV_{DC}}(CF). \quad (14)$$

Using the value of $V_{ref(max)}$ and CF, we find the maximum modulation index with the modified SVPWM as:

$$M_{m(max)} = 1.19. \quad (15)$$

The maximum available RMS value of the fundamental line voltage can be defined as:

$$V_{ab(RMS)(max)} = \frac{\sqrt{3}}{2\sqrt{2}}M_{m(max)}BV_{DC} = 0.728.BV_{DC} \quad (16)$$

The output voltage gain G of the inverter can be defined as:

$$G = \frac{\hat{v}_o}{V_{DC}/2} = M_mB. \quad (17)$$

where $\hat{v}_o$ is the peak output phase voltage.

The modulation index and available fundamental RMS line voltage using modified SVPWM are 1.19 and 0.728 BV_{DC},

respectively. These values are 3% more than in the conventional case.

Substituting (13) in (11), the average ST duty ratio is:

$$\overline{D}_m = \frac{\pi(CF) - 9M_m(2 - \sqrt{3})}{\pi(CF)}. \quad (18)$$

B. PROPOSED PATTERN OF SWITCHING STATES

The proposed switching pattern is shown in Fig. 7. The unique aspect of the proposed pattern is the placement of the ST state (the switching pattern of switch SB). This pattern doubles the switching frequency of SB without affecting the switching frequency of inverter switches compared with a previous pattern [21]. Additionally, the slew rate (rate of change of CMV) is also unaffected.

IV. COMPARISON

The RCC-AIN inverter was originally reported with the SBC technique of voltage boosting [21], but the I/O gain of the SBC technique is limited, as shown in Fig. 8(a). The MBC technique utilizes the full potential of the RCC-AIN inverter in terms of voltage gain, but due to the full utilization of the null interval, the instantaneous peak-to-peak difference of the ST duty ratio (D_{p2p}) is high. This introduces LF current ripples in the source current of the inverter. As a contender with high gain, the IMBC technique offers the same gain as MBC but with a reduced D_{p2p} (see Fig. 8(a) and (c)).

The voltage stress curves of IN capacitors, diodes, and power switch SB are plotted in Fig. 8(b) and indicate that MBC and IMBC cause the same stress for these components. For SBC, the curve is small as the gain of the inverter with SBC is limited. As discussed in section III, the modulation index of modified SVPWM is around 1.19 (3% more than conventional SVPWM). Therefore, the curves of IMBC in Fig. 8(a) and (b) extends up to 1.19.
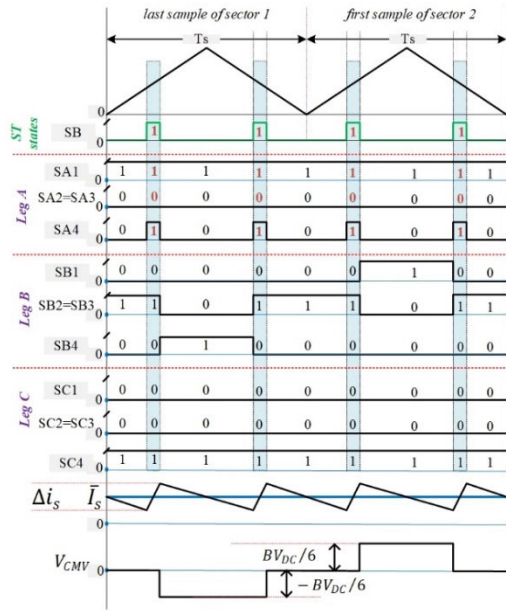
FIGURE 7. Proposed switching state pattern and corresponding source current and common mode voltage (CMV) magnitude for two consecutive carrier cycles.
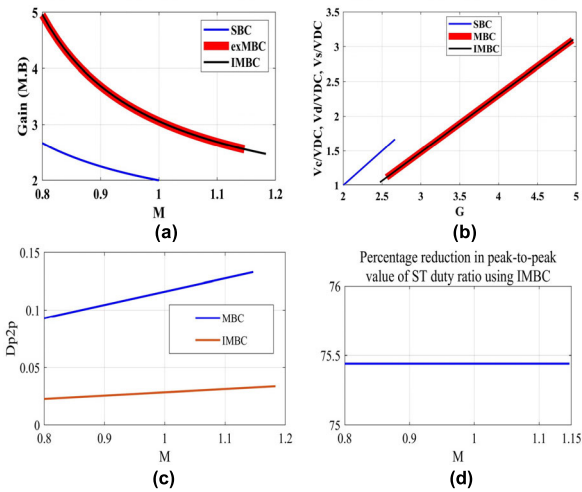

FIGURE 8. Comparison plots of inverter using SBC, MBC, and IMBC techniques: (a) gain G vs. modulation index M, (b) Capacitor/ diode/ switch voltage stress vs. voltage gain, (c) peak -to-peak ST duty ratio ripple vs. M, (d) percentage difference in peak-peak values of ST duty ratio ripple using MBC and IMBC.

The comparative analysis between the MBC and IMBC indicates that D_{p2p} is around 75% less when using IMBC (see Fig. 8(d)). The analysis of the switching frequency of the boost switch (SB) and inverter power switches is summarized in the last two rows of Table 3.

A. PEAK-TO-PEAK RIPPLE CALCULATIONS

For the exact calculations of the peak-to-peak ripple of the source current (Is), the cumulative sum of the instantaneous ripple components was used. The source current waveform
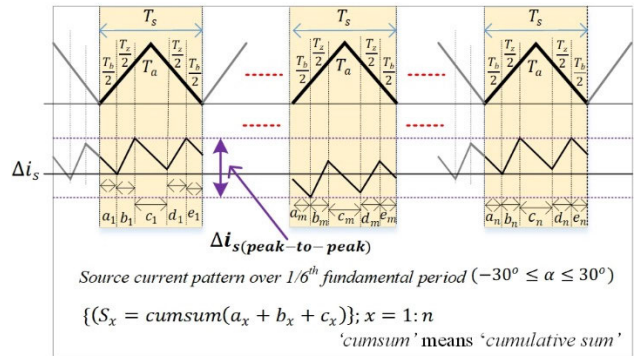
TABLE 4. Summary of theoretical results for peak-to-peak ripple of source current.

M; G; B	$\Delta i_{s(peak-peak)}$					
	MBC		IMBC		% Reduction	
	T	S	T	S	T	S
1.15; 2.54; 2.2	1.44	1.56	0.34	0.32	↓ 76.2	↓ 79.2
1.06; 2.79;2.61	1.93	1.95	0.7	0.66	↓ 63.8	↓ 66.0
1; 3.06; 3.06	2.41	2.41	1.0	0.99	↓ 57.2	↓ 58.7
0.86; 4.0; 4.6	3.91	3.88	2.0	1.99	↓ 47.5	↓ 48.5
0.8; 4.95; 6.1	5.32	5.20	2.9	2.88	↓ 44.1	↓ 44.5

T=theoretical, S=simulated.
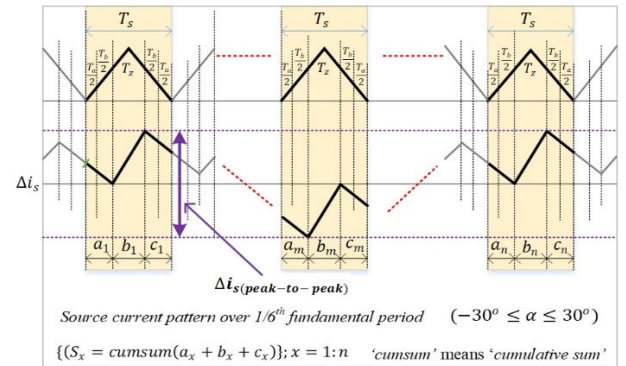
(a)

(b)

FIGURE 9. Source current waveform during 60-degree interval of fundamental cycle: (a) MBC, (b) IMBC with proposed switching pattern.

was analyzed for 1/6th of a period of the fundamental cycle to find the maximum and minimum peak values. Depending on the switching pattern of the PWM technique, charging and discharging current ripple components are defined as follows.

Case I. RCC-AIN with MBC and existing switching pattern [21]

The switching frequency ripple components for this case are shown in Fig. 9(a). Mathematically, these ripples are written as:

$$\begin{cases} a_x = (V_{DC} - V_C) \times (T_{ax} + T_{bx})/2L \\ b_x = (V_{DC} + V_C) \times (T_{zx})/L \\ c_x = a_x \end{cases}$$

where x = 1, 2, . . . , n.　　　　　(19)

The procedure is explained as follows:

Step 1. Find the cumulative sum of ripple components of individual carrier cycles:

In each carrier cycle, the cumulative sum of ripple components expressed in (18) is carried as:

$$S_x = \text{cumsum} (a_x + b_x + c_x \ldots..);$$
$$\{x = 1, 2 \ldots n\}. \tag{20}$$

Step 2. Find the cumulative sum of S_x :

The cumulative sum of S_x is defined as:

$$A = \text{cumsum} (S_x); \{x = 1, 2 \ldots n\}. \tag{21}$$

A plot of A (eq. 20) is shown in Fig. 10 for V_{ref} traversing from sector 12 and sector 1.

Step 3. Find A_{max} and A_{min}

The maximum and minimum peaks of A are then found using the following operation:

$$\begin{bmatrix} A_{max} = \max \{\text{cumsum} (S_x)\}; \\ A_{min} = \min \{\text{cumsum} (S_x)\}; \end{bmatrix} \{x = 1, 2 \ldots n\}. \tag{22}$$

Step 4. Find ΔA

The difference between the maximum and minimum values of A is defined as:

$$\Delta A = A_{max} - A_{min}. \tag{23}$$

Step 5. Find peak-to-peak ripple of the source current

Finally, the exact peak-to-peak difference of the source current is found by adding a specific instantaneous ripple in (22):

$$\Delta i_{s(p2p)\_MBC} = \Delta A + \{2 \times a_{n/2}\}, \tag{24}$$

where $a_{n/2}$ is the switching frequency ripple associated with the middle sample of a sector.

Case II. RCC-AIN with IMBC and proposed switching pattern (see Fig. 7)

For this case, the ripple components are shown in Fig. 9(b). Mathematically, these components are defined as

$$\begin{cases} a_x = (V_{in} - V_C) \times (T_{bx})/2L \\ b_x = (V_{in} + V_C) \times (T_{zx})/2L \\ c_x = (V_{in} - V_C) \times (T_{ax})/L \\ d_x = b_x \\ e_x = a_x \end{cases} \{x = 1, 2 \ldots n\}. \tag{25}$$

Step 1: Repeat steps 1 to step 4 of case I.

Step 2: Find a peak-to-peak ripple of source current

For this case, the specific factor for finding the exact peak-to-peak difference of the source current is different from (23):

$$i_{s(p2p)\_IMBC} = \Delta A + \{2 \times e_1\}, \tag{26}$$

where e_1 is the switching frequency ripple associated with the first sample in the considered region, $-30 \leq \alpha \leq 30$. The result of the theoretical calculations is summarized in Table 4. The percentage reduction in the peak-to-peak source current ripple is also shown.

TABLE 5. Simulation and experimental parameters.

Parameter	Value
Input voltage (V_{DC})	40 V
Carrier frequency, fc	4.8 kHz
Fundamental frequency	50 Hz
IN inductors and capacitors	3 mH, 1000 uF
Load	50 ohm, 1.2 mH

B. COMPONENT SELECTION

Here, the focus is given to the only inductor sizing. For the other parameters like capacitors C1 and C2, the diode, and the boost switch (SB), the general equations are already provided [21] and can be used after proper modification for the control technique. They are not repeated here as the focus of this paper is the source and inductor's current ripple and size.

For switching frequency ripple, the rate of change of current through the inductor for a maximum period of charging duration can be defined as:

$$\Delta i_{LB} = \frac{(V_{DC} + V_{C1})}{L_{B\_sw}} D_{max} T_s. \tag{27}$$

where L_{B_sw} is the inductor value for switching frequency ripples, and D_{max} is the maximum duty ratio encountered by the inductor over the fundamental cycle. It should be noted that:

$$\begin{cases} \Delta i_{LB} = \Delta i_s \\ I_{LB} = I_s \end{cases} \tag{28}$$

Using (4) in (26), we have:

$$\Delta i_{LB} = x\% I_{LB} \Rightarrow \frac{2V_{DC}(1-\overline{D})}{(1 - 2\overline{D})L_{B\_sw}} D_{max} T_s. \tag{29}$$

Using (5) in (27) and rearranging, we have:

$$L_{B\_sw} = \frac{V_{DC}}{x\% I_O} D_{max} T_s. \tag{30}$$

But the final inductor value calculations should also include the ripples due to LF components of current. Therefore, the final value of the inductor is defined as:

$$L_{B(final)} = L_{B\_sw} + y\% L_{B\_sw} \tag{31}$$

where $y\% = \Delta i_{LB(p2p)}/I_{LB}$. The value of $y\%$ can be found by (23), (5), and (27). Depending on the technique (MBC with the existing switching pattern or IMBC with the proposed pattern), these equations were modified for the calculation. It was found that when using IMBC with the proposed switching pattern, the minimum reduction in the inductor size is 44% at G=4.95. Similarly, the maximum reduction at G=2.54 is around 79%.

V. RESULTS

The RCC-AIN inverter was simulated using the parameters in Table 5. For any value of carrier frequency (fc), the switching frequency of all power switches can be found using the relations given in the last row of Table 4. Only MBC and IMBC
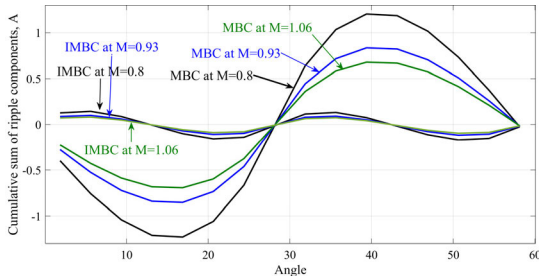
FIGURE 10. Plot of cumulative sum of ripple components (eq. (20)) w.r.t. angle of reference vector for MBC and IMBC approach at various values of modulation index.

techniques of voltage boosting were used for comparison since only these offers full utilization of the null interval. The proposed technique, which is a combination of IMBC and the new switching pattern, has been stated by IMBC only. On the other hand, MBC uses the existing switching pattern, in which the switching frequency of the boost switch (SB) is equal to the carrier frequency.

A. SIMULATION RESULTS

Case I. M=1.067, B=2.61, and G =2.79

Fig. 11 shows the various simulation waveforms of the RCC-AIN inverter. At 1.1 seconds, the PWM technique is changed from MBC to IMBC. It can be seen in Fig. 11 that the input capacitor voltages are balanced before and after 1.1 seconds. A very slight reduction in capacitor voltage ripple was also noticed. In the 2nd and 3rd waveforms, line voltages and pole voltages are shown to indicate the magnitudes are unaffected even after changing the PWM technique. The magnitude of the line and pole voltages are around 104 V and 52 V, respectively. These magnitudes match with the theoretical relation results. The 4th waveform shows the source current (I_s). It can be seen that before 1.1 seconds, the peak-to-peak ripple of the source current is 1.953 A, and after 1.1 seconds, the ripple is reduced to 0.633 A as the IMBC technique is applied.

This indicates a percentage reduction of around 67%. This matches the theoretical results in Table 4.

The IMBC technique is based on modified SVPWM, which eliminates the 6th frequency ripples of the source current. This is validated from the 5th waveform of Fig. 11 as it can be seen that the magnitude of the 6th F_1 ripple is eventually reduced after the instant IMBC is applied. The THD of the line voltage is shown in the last waveform. It was found that the line voltage THD is almost negligibly affected. In Fig. 12, an effect of increasing the switching frequency of the IN was noticed on the boost switch (SB) and capacitors C_1 and C_2's current spikes. A reduction in the switching frequency current spikes can be noticed after 1.1 seconds when the IMBC technique is applied. The proposed switching pattern (see Fig. 7) offers reduced CMV magnitude (limited to $1/6^{th}$ of the DC-link voltage), similar to the technique used in the original paper of RCC-AIN [21]. This can be verified
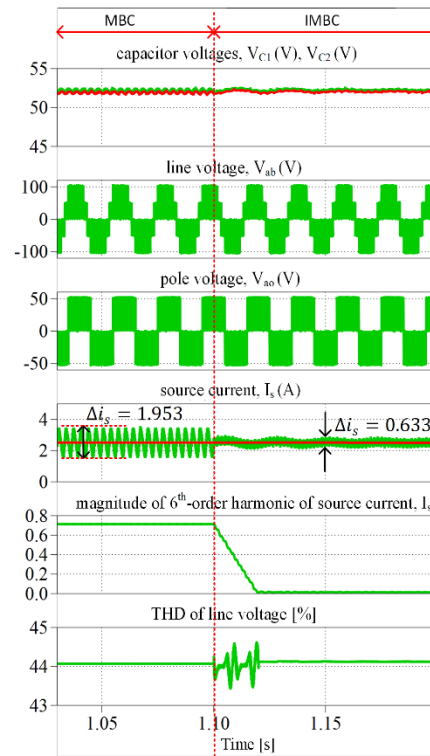
FIGURE 11. Simulation waveforms at M=1.067, B=2.61, and G=2.79: (from top) capacitor voltages, line-line voltage (V$_{ab}$), pole voltage (V$_{ao}$), source current (I$_s$), magnitude of 6th-order frequency component of source current, THD of line-line voltage.
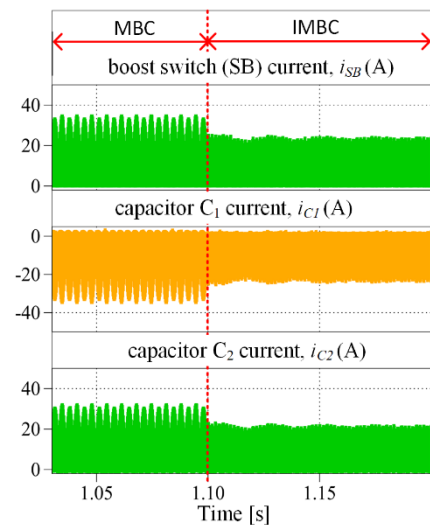
FIGURE 12. Simulation waveforms of current through (from top) boost switch (SB), capacitor C$_1$, and C$_2$.

from Fig. 13. The magnitude of the CMV is around 17 V, which verifies this result. In addition, the zoomed-in portion of the CMV waveform indicates that the transitions in CMV magnitude (frequency and rate of change of the CMV magnitude) are unaffected by the proposed pattern.
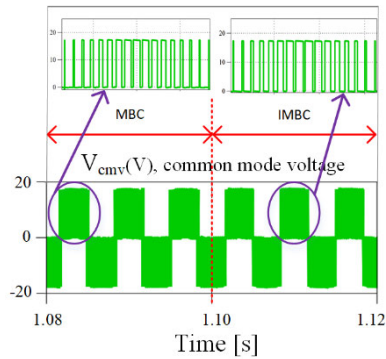
Case II. M = 1.154, B = 2.2, G=2.54

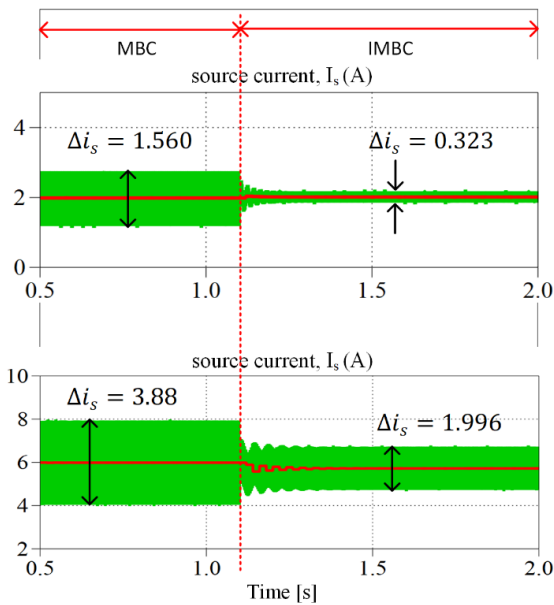**FIGURE 13.** Simulation waveform of common mode voltage (V_{cmv}).

FIGURE 14. Simulation waveform of source current (Is): (top) at M=1.154 and G = 2.54; (bottom) at M=0.866 and G = 4.

FIGURE 15. Comparison plots using MBC and IMBC: (a) line-line voltage THD vs. B, (b) magnitude of 6th-order ripple of source current vs. B.

FIGURE 16. The laboratory prototype of RCC-AIN three-level inverter.

For this case, the source current is shown in the top waveform of Fig. 14. The peak-to-peak ripples of the source current are 1.560 A and 0.323A before and after the 1.1seconds, respectively. This indicates around 79% reduction with the IMBC technique (this matches with the theoretically calculated values in Table 4). Similarly, the bottom waveform of Fig. 14 indicates a reduction of around 48%. This again matches with the theoretical finding in Table 4.

The performance of the IMBC technique was verified up to B=5. A plot of the line voltage and line current THD is shown in Fig. 15(a) and indicates that IMBC causes a negligible effect on line voltage/current THD. Fig. 15(b) indicates the magnitude of the 6th frequency component of the source current with MBC and IMBC. These components are almost zero with IMBC.

B. EXPERIMENTAL RESULTS

Fig. 16 shows the laboratory prototype of the RCC-AIN three-level inverter. Semikron SKM75GB12T4 IGBT modules were used as power switches. The task of PWM generation was accomplished by a Texas Instruments TMS320F28379D DSP.
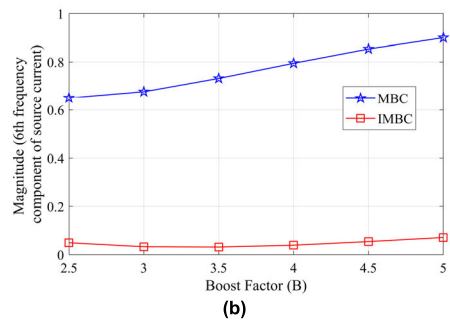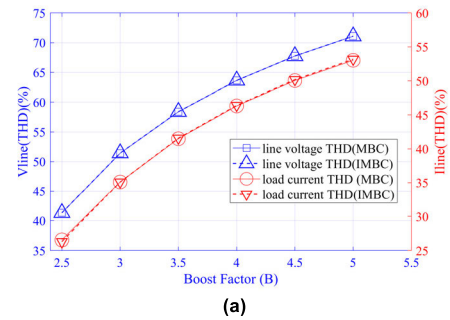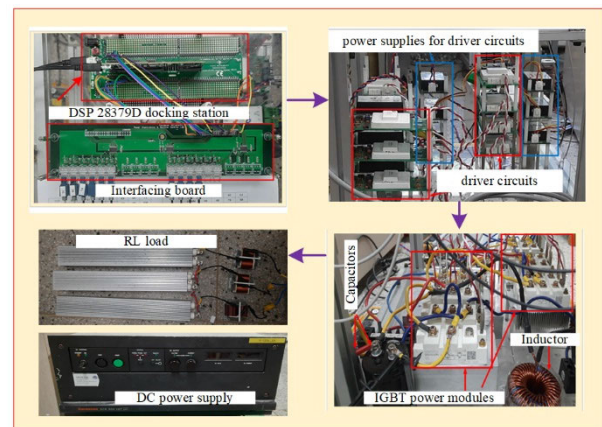
For the first case, M and B were set to 0.8 and 6.19, respectively. Fig. 17 shows the experimental waveforms for this case.

The inverter gain G is 4.95 at this value of the modulation index. It can be seen from Fig. 17 that both capacitors C_1 and C_2's voltages are balanced at around 120 V.As the input DC voltage is set to 40 V, the line voltage (V_{ab}) shows a peak of around 240 V. This indicates that the inverter is boosting based on the set boost factor. The last waveform in Fig. 17 shows the source current (Is). For the comparison of MBC with IMBC, the waveforms of both techniques are shown in the same figure.
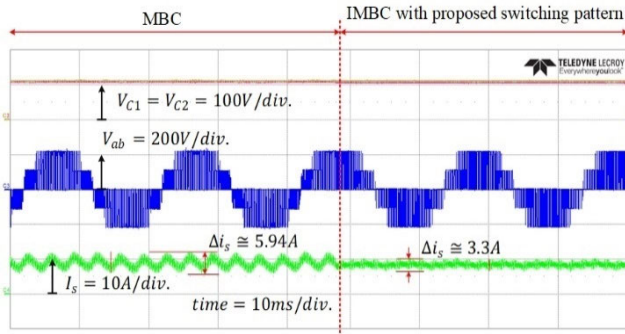
FIGURE 17. Experimental waveforms using MBC and IMBC at M=0.8, B=6.12, and G=4.95: (from top) capacitor (C_1, C_2) voltages, line voltage (V_{ab}), source current (I_S).
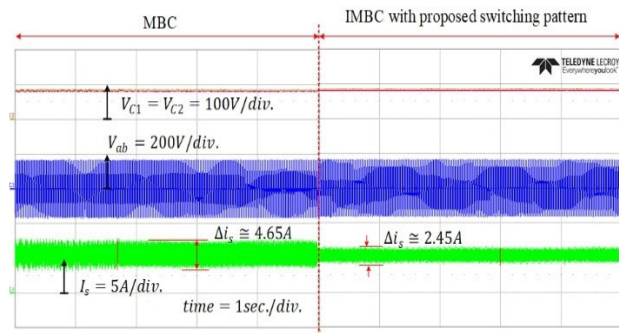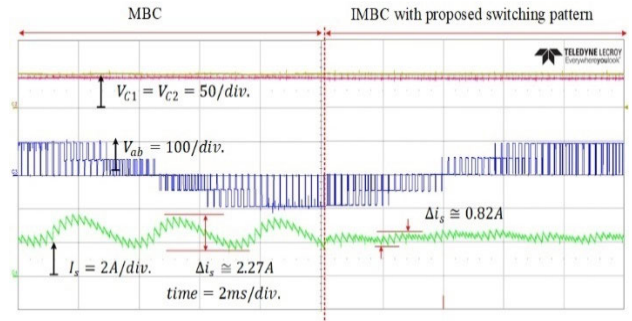

FIGURE 18. Experimental waveforms at M=0.866, B=4.6, and G=4, (from top) capacitor (C_1, C_2) voltages, line voltage (V_{ab}), source current (I_S).

FIGURE 19. Experimental waveforms at M=1.067, B=2.61, and G=2.79: (a) (from top) capacitor (C_1, C_2) voltages, line voltage (V_{ab}), source current (I_S), (b) pole voltage (V_{ao}) and common mode voltage (V_{cmv}), (c) current through capacitors C_1 and C_2 and boost switch SB.
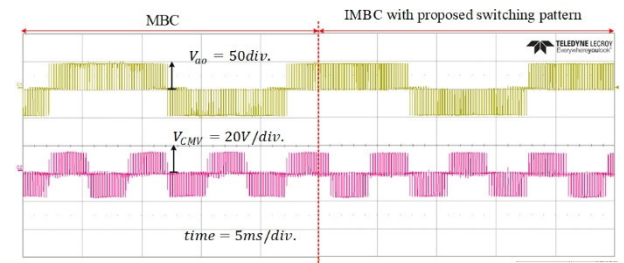
The first portion of Fig. 17 shows the quantities with MBC, and the second portion shows the quantities with IMBC. The conclusion from Fig. 17 is that although the capacitor voltages and line voltage magnitude are unaffected, the peak-to-peak ripple of the source current in the second portion is reduced by 44.4%. This verifies our theoretical calculations and simulation results (see Table 4, 5th row).

For the second case, M and B are set to 0.866 and 4.6, respectively. Fig. 18 shows the waveforms for this case. The peak magnitude of the capacitor voltages and line voltage matches the theoretical relations. Similar to the first case, the capacitor voltages and line voltage magnitudes are again the same in both halves, but the peak-to-peak ripple of the source current is 47.3% less in the second half. The theoretical/simulation results for this case are shown in Table 4, row 4.
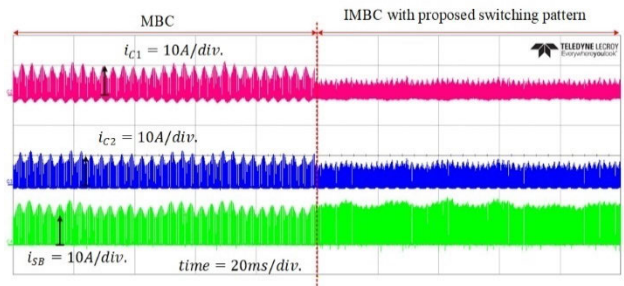
M and B were then set to 1.067 and 2.61, respectively. Fig. 19(a) shows that the peak-to-peak ripple of the source current in the second half of the figure is reduced by 63.8%. The waveforms of the pole voltage and common mode voltage are shown in Fig. 19(b). The magnitude of V_{ao} and V_{cmv} are approximately 50 V and 17 V, respectively. This proves that the proposed switching pattern limits the magnitude of the CMV to $1/6^{th}$ of the peak DC-link or peak line-voltage magnitude. The transitions in the CMV waveform in the first and second portion of Fig. 19(b) are almost the same (even

the proposed pattern causes 1 less transition compared to the existing one). Fig. 19(c) shows the effect of increasing the switching frequency of the boost switch (SB). The current spikes of C_1 and C_2 decrease significantly, which can be seen in the second half of Fig. 19(c). The simulation results of Fig. 12 show the reduction in current spikes of C_1, C_2, and switch SB. However, in the experimental verification, a reduction in only C_1 and C_2's current spikes was noticed.

Finally, to investigate the performance of the proposed PWM at the highest modulation index, M and B were set to 1.154 and 2.2, respectively. Fig. 20 shows the waveforms for this case. Fig. 20 indicates that the difference in the peak-to-peak ripple of the source in the first and second half is 76.1%. The simulation and experimental results prove the effectiveness of the theoretical calculation using the cumulative sum of the ripple components.

frequency ripple components, common ground feature, and a self-balancing capacitor voltage feature.
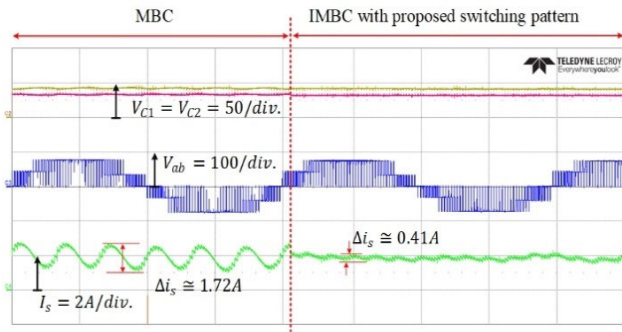
FIGURE 20. Experimental waveforms at M=1.154, B=2.2, and G=2.54 (from top): capacitor (C_1, C_2) voltages, line voltage (V_{ab}), source current (I_s).
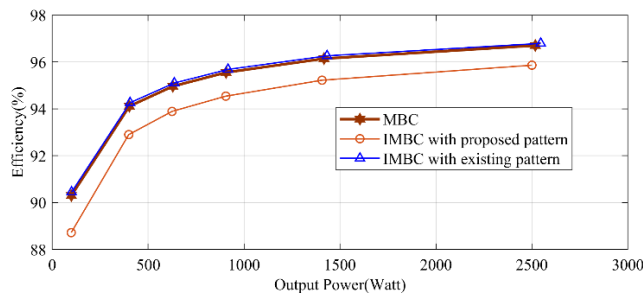
FIGURE 21. Efficiency plot of RCC-AIN three-level inverter with various PWM techniques.

For the analysis of the efficiency, three cases were considered. MBC with an existing switching pattern, IMBC with an existing switching pattern, and IMBC with the proposed switching pattern. As shown in Fig. 7, the proposed switching pattern doubles the switching frequency of switch SB. Therefore, the efficiency of the IMBC with the proposed switching pattern is reduced by around 1% (see Fig. 21). On the other hand, the IMBC with the existing pattern offers the maximum efficiency, which is the same as that of the MBC.

VI. CONCLUSION

In this paper, an RCC-AIN inverter topology was analyzed in its full I/O voltage gain potential. When the whole null duration was used for ST insertion to achieve maximum gain, the MBC method caused a large peak-to-peak ripple in the source current. The proposed PWM technique successfully reduced the source current ripples by 44 to 79% in the boost factor range of 6.1 to 2.2.

Theoretical calculation was done using the cumulative sum of the ripple components to find the exact maximum and minimum peak of the source current over a fundamental cycle and was proven correct by comparison with the simulation and experimental results. The common-mode voltage magnitude was limited to $1/6^{th}$ of the DC-link voltage. Also, due to the increased switching frequency of the boost switch SB, the switching frequency spikes of the capacitor current were reduced. Therefore, it is concluded that the RCC-AIN inverter with the proposed PWM technique is an optimal solution for a high-gain three-level inverter with minimal passive components, a continuous input current profile without low-

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