RESEARCH ARTICLE

Compact and Broadband ESD Protection I/O Pad Using Pad-Stacked Inductor

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ABSTRACT In this paper, a compact and broadband electrostatic discharge (ESD) protection input/output (I/O) pad for high-speed interfaces is designed and miniaturized using a pad-stacked inductor in a 28-nm CMOS technology. A π-diode with a single inductor is adopted to compensate for the parasitic capacitance and extend the bandwidth of ESD-protected I/O pad. To minimize the increase of the chip area by the inductor, the pad-stacked inductor is proposed, where the inductor is placed below I/O pad. The eddy current, then, is induced in the I/O pad by time-varying magnetic field by the inductor, degrading the performance of the inductor, such as the reduced inductance, increased resistance and capacitance. These effects are thoroughly investigated using the developed equivalent circuit model which is also utilized to design the pad-stacked inductor. The compact and broadband π-diode with the reduced eddy current is then designed by the proper selection of the inductor layer and a patterned I/O pad. Measurement of the designed π-diode with the pad-stacked inductor exhibits broadband impedance match and insertion loss, that is, a return loss better than 10 dB up to 26.5 GHz and a 3-dB bandwidth as large as 22.9 GHz. The chip area of the π-diode remains the same as that of the I/O pad thanks to the proposed pad-stacked inductor. Therefore, the designed π-diode can be applied for the compact high-speed I/O interface circuits.

INDEX TERMS Broadband, electrostatic discharge, high-speed, input/output pad.

I. INTRODUCTION

The data traffic is rapidly increasing year by year, which requires the development of high-speed interface circuits [1]. This is accelerated by the advance of nanoscale complementary metal-oxide-semiconductor (CMOS) technologies [2]. However, the nanoscale CMOS is more vulnerable to electrostatic discharge (ESD) stress, because of the reduced junction breakdown voltage, thin gate oxide, and the thin metal layers. Circuit damage by ESD is non-recoverable and thus ESD protection circuits are essential for high-speed input and output (I/O) circuits.

There are several devices used for ESD protection such as MOS field effect transistors (MOSFETs), diodes, and silicon-controlled rectifiers (SCRs) [3]. Diodes allow a high current-discharging ability, easy implementation, and low turn-on

voltage, so that they are widely used as ESD protection devices for high-speed I/O circuits [4], [5]. Large-size diode with a low turn-on resistance (R_{ON}) is required to sufficiently reduce the joule heat and clamping voltage when the ESD events occur. However, it entails a large parasitic capacitance that limits the bandwidth of the I/O pads and thus the speed of the entire I/O interface circuits.

Therefore, there has been a lot of research recovering the bandwidth of I/O pad with ESD diodes. CMOS inductors or coils are commonly used for this purpose, compensating for the parasitic capacitance of the diode and recovering the bandwidth. A T-diode where the ESD protection diode is connected to the center tap of T-coil, is a commonly used bandwidth extension technique. It allows a very broadband performance, or ideally all-pass networks [6], [7], [8]. However, it is found in [9] that mutual coupling between the primary and secondary inductors of the T-coil can cause voltage overshoot during ESD event, resulting in a gate-oxide

breakdown. This problem was alleviated by an inductive halving technique reducing the mutual coupling [9]. The ESD current flows into the diode at the center tap through the primary inductor, which increases R_{ON} of the ESD path. The modified T-coil was designed in [10], where the part of ESD diode was assigned to the I/O pad to initially discharge ESD current [11].

A π-diode with an inductor between two ESD diodes is another bandwidth extension technique allowing a broadband performance [12], [13]. The 1st ESD protection diode connected to I/O pad immediately discharges the ESD current which lowers R_{ON} [11]. In addition, it uses only a single inductor so that there is no mutual coupling producing voltage overshoot.

High-order LC filters are also used to broaden the reduced bandwidth of the I/O pad due to the capacitances of ESD diodes, bump, and driver circuits [14]. Especially, high-order Bessel-like filter allows a small group delay ripple as well as a broad bandwidth, so that it was utilized for high-speed I/O pads.

However, the inductors or T-coils used in the bandwidth extension of the ESD protection I/O pad occupy the large CMOS area which can be even larger than that of I/O pad itself. Therefore, the bandwidth extension circuit can significantly increase total CMOS chip area. This can be a very serious problem for the high-data rate I/O interfaces with a large number of I/O pads. Therefore, it is essential for high-speed I/O interfaces to miniaturize the bandwidth extension circuit of the ESD protection I/O pad.

In this work, the pad-stacked inductor is proposed to dramatically reduce the chip area of the ESD protection I/O pad. The inductor is placed below the I/O pad, so that there is no increase of the area by the inductor. This technique is applied to a π-diode. The effect of the eddy current induced in the I/O pad is thoroughly studied by 3-dimensional (3-D) electromagnetic (EM) simulations. Design methods are introduced to alleviate the performance degradation by the induced eddy current. The designed π-diode with the pad-stacked inductor is fabricated in a 28-nm fully-depleted silicon-on-insulator (FDSOI) CMOS technology. Equivalent circuit model is constructed based on the measured data of the pad-stacked inductor. The measurement of the π-diode is also presented, showing a broadband performance with a good agreement with the simulation results.

II. CIRCUIT DESIGN
A. BANDWIDTH EXTENSION USING π-DIODE
Fig. 1(a) shows a π-diode, the ESD protection I/O pad with diodes and inductor, where the ESD diodes are separated by the inductor (L). Contrary to the traditional T-diode where the diode is connected in the center tap of T-coil, this π-diode has a half of total ESD diode directly connected to I/O pad which can quickly discharge the part of ESD current, when an ESD event occurs at I/O pads. Therefore, it can be more immune to the parasitic resistance of the inductor and present better ESD
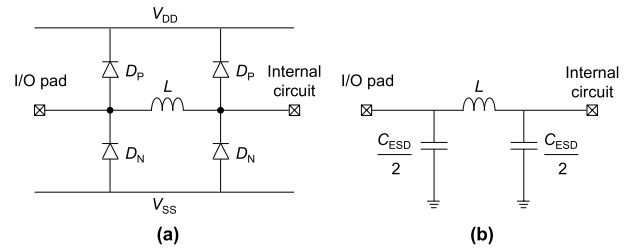

FIGURE 1. Broadband ESD protection I/O pad using π-diode. (a) Circuit schematic. (b) Simplified equivalent circuit.
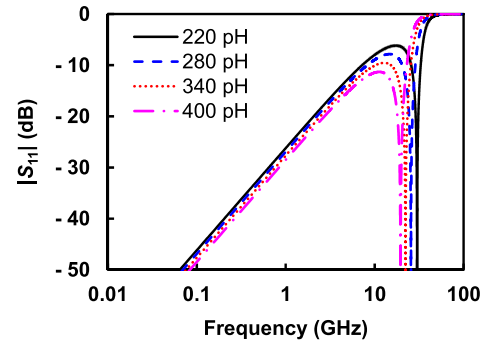

FIGURE 2. Simulated impedance matching performance ($|S_{11}|$) of π-diode as a function of frequency depending on the inductance.

robustness [11]. The simplified circuit model of the π-diode is presented in Fig. 1(b), where total capacitance of the ESD diodes (C_{ESD}) is equally split by the inductor to extend the bandwidth [15].

The π-diode in Fig. 1 is basically a low-pass filter which can be impedance-matched at two frequencies, one at DC and the other at impedance matching frequency (f_m) given as

$$f_m = \frac{1}{\pi}\sqrt{\frac{1}{LC_{ESD}} - \frac{1}{R^2 C_{ESD}^2}}, \qquad (1)$$

where R is a termination impedance at I/O pad and internal circuit and is normally 50 Ω. In this work, the diode with C_{ESD} of 380 fF is adopted to meet the general ESD protection requirement of > 2-kV in human body model [16]. According to (1), the inductance L can be determined for a given C_{ESD} if f_m is fixed. Fig. 2 shows the simulated $|S_{11}|$ versus frequency at various L's. The lower L, the higher f_m, implying impedance match at higher frequency. However, if L becomes lower than 340 pH, $|S_{11}|$ can exceed -10 dB at mid-frequencies between DC and f_m, as shown in Fig. 2. Therefore, L is determined to be 340 pH (or $f_m = 22.4$ GHz) in this work, so that $|S_{11}|$ is below -10 dB at any frequency from DC to 25.9 GHz. An ideal 3-dB bandwidth in $|S_{21}|$ is as high as 30.5 GHz.

B. PAD-STACKED INDUCTOR
The I/O pad is designed in a $\sim$2 μm-thick top metal layer (M10) of back-end-of-line in 28-nm FDSOI CMOS process as shown in Fig. 3. Initially, an octagonal inductor is designed in M9 ($\sim$3 μm-thick copper layer) to have an inductance of 340 pH, a 2.3-turn wire with a width of 4 μm, a spacing of

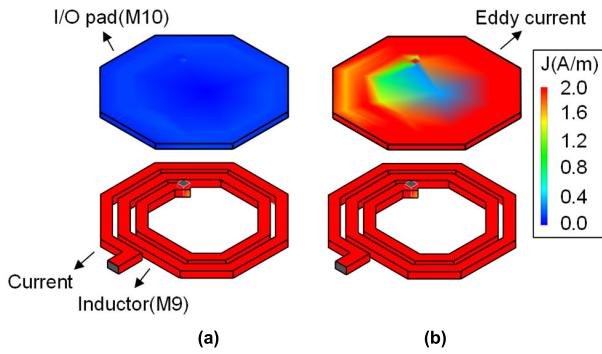**FIGURE 3.** Pad-stacked inductor and simulated surface current density J (A/m) at (a) 10 MHz and (b) 10 GHz.

FIGURE 4. High-frequency equivalent circuit of the pad-stacked inductor.

1.8 μm, and an inner radius of 15.3 μm. The dimension was determined by a 3-D EM simulation using high-frequency structure simulator (HFSS) by Ansoft, Inc. It occupies the circuit area of 62 μm $\times$ 62 μm which is almost the same as that of I/O pad. Therefore, the ESD protection I/O pad with a π-diode can occupy the doubled chip space, which can significantly increase the chip area of high-speed I/O circuits with a large number of I/O pads.

In this work, the I/O pad is stacked onto the inductor as shown in Fig. 3, to avoid the increase of the ESD protection I/O pad area by the inductor. It can dramatically reduce the chip area for high-speed I/O circuits with a large number of I/O pads. However, the I/O pad over the inductor can deteriorate the performance of the inductor and thus the bandwidth of a π-diode. Firstly, it reduces the effective inductance of the inductor due to the eddy current which is induced in the I/O pad by the time-varying magnetic flux generated by the inductor. According to Lenz's law, the eddy current is in the direction such that it opposes the change of magnetic flux and thus reduces total magnetic flux [17]. It leads to the reduction of the effective inductance of the inductor. This reduction is more serious at higher frequency, according to Faraday's law [18]. Fig. 3(a) and (b) show the simulated current density on the pad and inductor at a frequency of 10 MHz and 10 GHz, respectively. The current induced in the I/O pad is negligible at a low frequency of 10 MHz. On the contrary, there is a strong eddy current induced in the I/O pad at a high frequency of 10 GHz. Secondly, the eddy current in the I/O pad increases the ohmic loss, which can be reflected by the increase in the parasitic resistance of the inductor. Finally, the I/O pad itself increases the parasitic capacitance of the inductor.

In order to accurately predict the performance of the pad-stacked inductor, a high-frequency equivalent circuit model is constructed as shown in Fig. 4. In this figure, L_S represents the inductance of the inductor without the I/O pad, while L_{eddy} is included to reflect the reduction in the inductance due to the eddy current. C_B accounts for the capacitance between the inductor traces and I/O pad. The RL circuit (L_0, R_0, and R_S) is to model the parasitic resistance of the inductor. It can expect the increasing resistance with frequency due to the skin effect [19]. That is, this RL circuit is approximated to
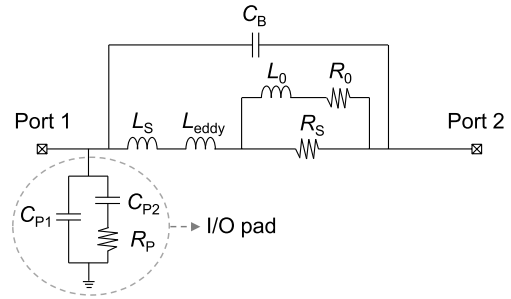
be $R_S // R_0$ and R_S at low and high frequencies, respectively. The RC circuit (C_{P1}, C_{P2}, and R_P) is added in parallel to the inductor to model the parasitic components of I/O pad [20].

Using the EM simulation data of the designed pad-stacked inductor of Fig. 3, the parameters of the equivalent circuit are extracted following the procedures presented in [21] and [22]. They are compared with those of the conventional inductor without I/O pad. Fig. 5 shows the extracted inductance ($L_S + L_{eddy}$) and Q-factor of the conventional and pad-stacked inductor. As shown in Fig. 5(a), two inductors have almost the same inductance of 354 pH at low frequency around 10 MHz, implying the negligible effect of the eddy current. However, the inductance of the pad-stacked inductor significantly decreases to 138 pH at high frequency of 10 GHz which corresponds to L_{eddy} of -216 pH, whereas the conventional inductor exhibits a nearly constant inductance up to high frequency. This result indicates the increased effect of the eddy current in the I/O pad on the inductance at high frequency. Note that the extracted inductance of the conventional inductor sharply increases around 95.1 GHz due to self-resonance. In the pad-stacked inductor, the resonant frequency is pushed up to 103.2 GHz by the reduced inductance. The increased ohmic loss in the I/O pad by the eddy current is also observed and reflected as the reduced Q-factor as shown in Fig. 5(b). The pad-stacked inductor exhibits Q-factor of 3.2 at 10 GHz, while it is 11.0 for the conventional inductor.

For the operation of the π-diode with a broad bandwidth, the inductance should be resorted to the original value of 340 pH. Increasing the number of wire turns is a simple solution. However, it leads to the increase of the circuit area, parasitic resistance, and capacitances of the inductor, degrading the performance of the π-diode. In this work, the performance degradation by the eddy current is alleviated by the proper selection of metal layer for the inductor and by designing the patterned I/O pad.

The selected CMOS process provides three thick metal layers (M7, M8, and M9) that can be used for inductor design, except for top metal layer for I/O pad. The other thin metal layers are excluded in the inductor design because of its high resistance. The vertical spacing between the I/O pad and the inductor is 6.58 μm for M7, 5.1 μm for M8, and 1.45 μm for M9. In order to reduce the effect of the eddy current, M7 layer is selected for the pad-stacked inductor. Fig. 6 shows the extracted inductance versus frequency depending
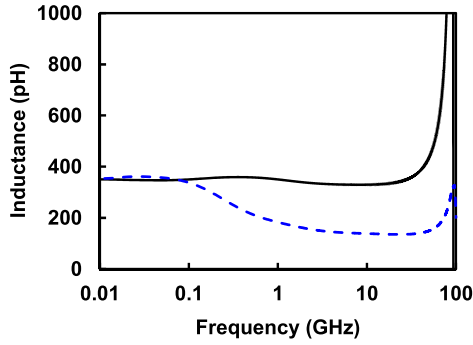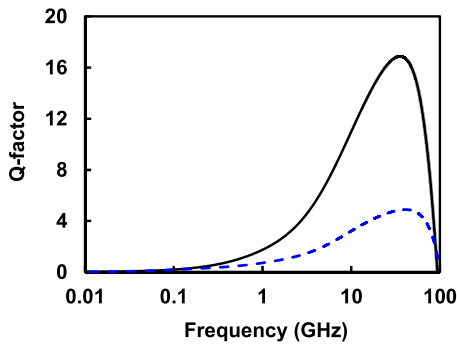
FIGURE 5. Extracted equivalent-circuit parameters of the inductors versus frequency (solid: conventional, slotted: pad-stacked). (a) Inductance. (b) Q-factor.
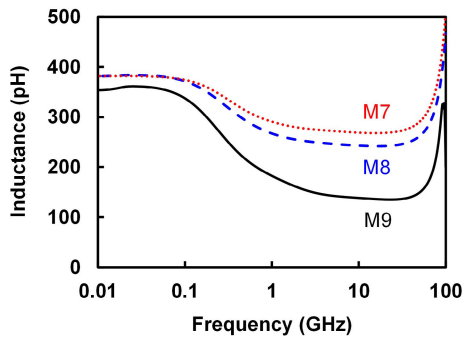

FIGURE 6. Extracted inductance versus frequency depending on the inductor metal layer.

on the selection of metal layer for the inductor. The inductor in M7 with the largest vertical spacing exhibits the highest inductance of 269.0 pH at 10 GHz which is almost a double of that in M9.

To further reduce the eddy current, a patterned I/O pad is designed, where the slots are inserted perpendicular to the edge of the I/O pad as shown in Fig. 7. They disturb the flow of the eddy current and alleviate inductance reduction [23]. Fig. 8 shows that the patterned I/O pad can increase the inductance from 269.0 to 300.7 pH at 10 GHz.

The final design of pad-stacked inductor with the patterned I/O pad is given in Fig. 7. An inductance of 340 pH is simply achieved by slightly increasing the number of wire turns from 2.3 to 2.6 with the other dimension unchanged, thanks to the proper selection of the metal layer and the patterned I/O pad.
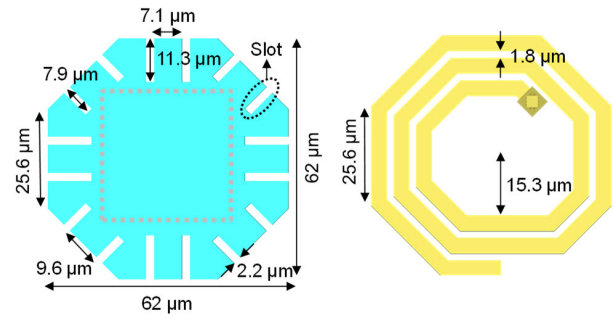

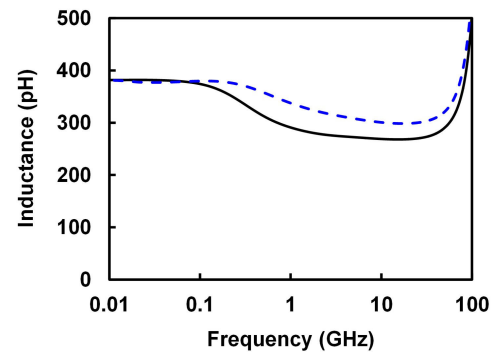FIGURE 7. Final design of the pad-stacked inductor with the patterned I/O pad.

FIGURE 8. Extracted inductance versus frequency depending on the I/O pad (solid: conventional I/O pad, slotted: patterned I/O pad).

C. SIMULATION RESULTS

Fig. 9(a) shows the simulated S-parameters of the designed π-diode with the pad-stacked inductor for bandwidth extension of ESD protection I/O pad, together with the results without the inductor. The S-parameters are obtained using 3-D EM simulation data. The ESD protection I/O pad without the inductor exhibits a very limited bandwidth due to the parasitic capacitance of the ESD diode and pad, or 5.5 GHz for $|S_{11}|$ meeting < -10 dB and 14.1 GHz for 3-dB gain ($|S_{21}|$) bandwidth. The respective bandwidth is significantly increased to 25.5 and 22.9 GHz by the designed π-diode, without increasing the circuit size thanks to the designed pad-stacked inductor. Therefore, the designed ESD protection I/O pad using a π-diode is expected to be used to for data transmission up to 32 Gb/s. This is based on the rule of thumb that a 3-dB gain bandwidth should be at least 70% of data rate [24]. The $|S_{11}|$ bandwidth meeting < -10 dB is also larger than Nyquist frequency of 16 GHz [25]. The simulated group delay is compared in Fig. 9(b), where the ESD protection I/O pad with the pad-stacked inductor exhibit a smaller ripple of 4.0 ps up to Nyquist frequency which is 2.7 ps smaller than that of the ESD protection I/O pad without the inductor.

III. MEASUREMENT

The designed π-diode was fabricated in a 28-nm FDSOI CMOS process. For the extraction of the equivalent circuit parameters of Fig. 4, one-port pad-stacked inductor was fab-
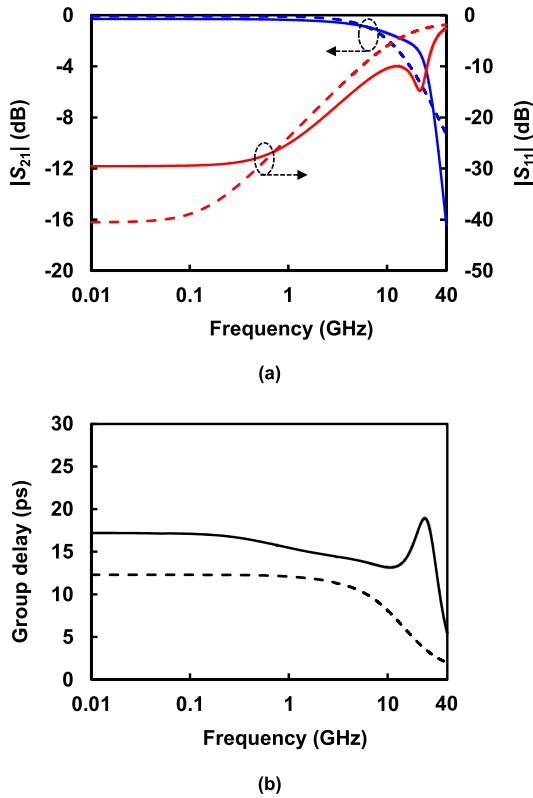
(a)

(b)

FIGURE 9. Simulated results of the ESD protection I/O pad (slotted: I/O pad without the inductor, solid: I/O pad with the pad-stacked inductor). (a) S-parameters. (b) Group delay.

TABLE 1. Extracted equivalent-circuit parameters of the pad-stacked inductor.

	L_S (pH)	L_{eddy} (pH)	C_B (fF)	L_0 (pH)	R_0 (Ω)	R_S (Ω)	C_{P1} (fF)	C_{P2} (fF)	R_P (Ω)
EM simulation	436.9	-98.5	4.8	80	4.8	7.7	11.6	10.3	6487
Measurement	440.9	-103.5	6.6	160	8	8.3	9.9	4.1	2182

ricated as shown in Fig. 10(a), where the port 2 was shorted to ground. The parasitic elements of I/O pad (C_{P1}, C_{P2}, and R_P) were firstly extracted using the measured S_{11} of the I/O pad itself. Then, the other parameters were obtained from the measured S_{11} of Fig. 10(a). Table 1 lists the extracted parameters of the equivalent circuit model of the pad-stacked inductors using both EM simulated and measured S_{11}. They show a good agreement between the simulation and measurement. The fabricated pad-stacked inductor exhibits the net inductance ($L_S + L_{eddy}$) of 337.3 pH which is very close to the target value of 340 pH. The accuracy of the extracted parameter values is confirmed by comparing the calculated S_{11} of the equivalent circuit with the measured one, as shown in Fig. 11. Note that the S_{11} of the equivalent circuit model with L_0 and R_0 well-fits the measured one even at high frequency.

Fig. 10(b) shows the photograph of the fabricated chip for the test of the π-diode with the pad-stacked inductor. Port 1
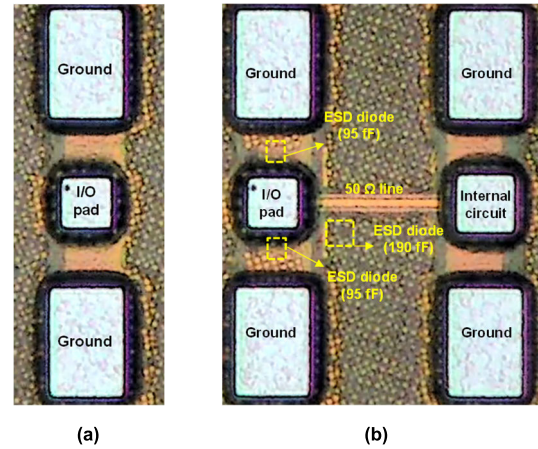

FIGURE 10. Photograph of the fabricated chip. (a) One-port pad-stacked inductor. (b) Two-port test chip for π-diode bandwidth extension circuit using the pad-stacked inductor.
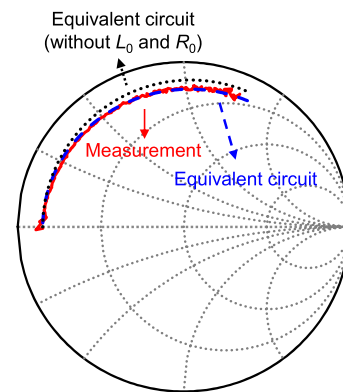

FIGURE 11. S_{11} of one-port pad-stacked inductor from 0.1 to 30 GHz. (solid: measurement, slotted and dotted: equivalent circuit).

is an ESD protection I/O pad with the π-diode where the inductor is placed below the I/O pad. Port 2 (internal circuit) has no ESD diode and is connected to port 1 through 50-Ω microstrip line for two-port measurement. The total chip size is 210 μm $\times$ 280 μm including the I/O and ground pads. Fig. 12 shows the measured and simulated S-parameters of the π-diode with the pad-stacked inductor of Fig. 10(b). The measured $|S_{11}|$ is below -10 dB up to 26.5 GHz, and the 3-dB bandwidth of $|S_{21}|$ is as large as 22.9 GHz. $|S_{21}|$ is -0.4 dB at 0.01 GHz. These results indicate that the fabricated π-diode with the pad-stacked inductor provides a broadband insertion and return loss performance, so that it can be applied for high-speed I/O circuits with a compact area. Note that the measurement is well-predicted by the simulation as shown in Fig. 12.

Fig. 13 presents the group delay of the test circuit in Fig. 10(b). The measured group delay was fitted to the polynomial function [26], [27]. It exhibits a small ripple of 3.4 ps up to Nyquist frequency.

The output eye diagram for the fabricated chip was obtained by the simulation using the measured S-parameters,
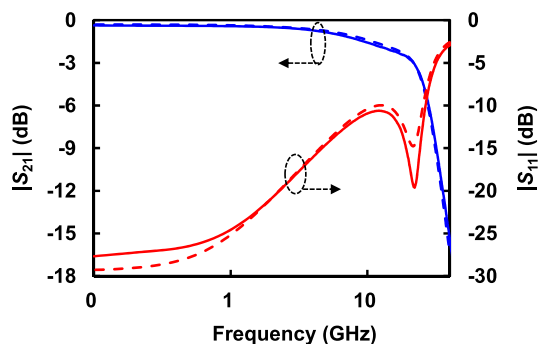
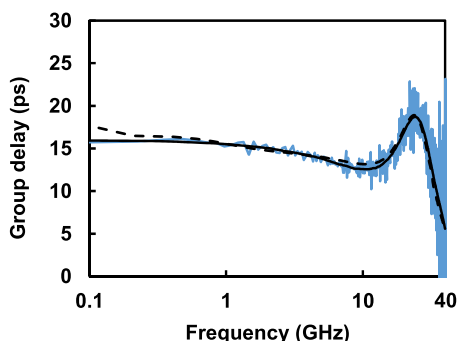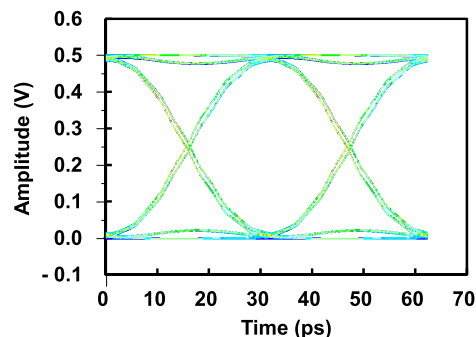FIGURE 12. Measured (solid) and simulated (slotted) S-parameters of the π-diode using the pad-stacked inductor.
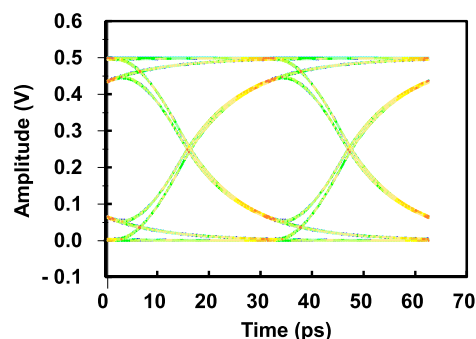

FIGURE 13. Measured and fitted group delay of the π-diode using the pad-stacked inductor with the simulation (slotted).

(a)

(b)

FIGURE 14. Simulated eye diagram at a data rate of 32 Gb/s. (a) π-diode using the pad-stacked inductor. (b) I/O pad without the inductor.
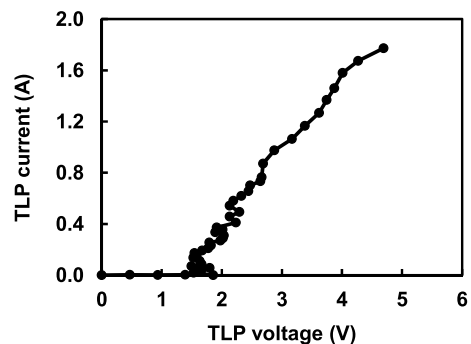

FIGURE 15. TLP test result for the π-diode using pad-stacked inductor.

as shown in Fig. 14. It can give estimates of the time-domain performance, even though S-parameters are small-signal parameters in the frequency-domain [27], [28]. Input is a 2^8-1 pseudo-random binary sequence of 1.0 V_{PP} with a 50 Ω resistance. Fig. 14(a) shows a simulated eye pattern at port 2 for 32 Gb/s non-return-to-zero signal and exhibits an eye height of 0.44 V_{PP}, eye width of 30.47 ps, and rise/fall time less than 12.26 ps. For the comparison, the simulated eye diagram of the ESD protection I/O pad without the inductor is also plotted in Fig. 14(b). It exhibits the reduced eye height of 0.34 V_{PP} with the increased rise/fall time of 13.9 ps. Therefore, the π-diode using the pad-stacked inductor improves the eye-opening characteristics suitable for a 32 Gb/s data transmission [29].

The ESD protection performance of the fabricated π-diode using the pad-stacked inductor was tested by using a transmission-line pulsing (TLP) system (by QRT Inc.). A 100-ns TLP signal with a rise time of 10 ns was used to obtain the TLP IV characteristics shown in Fig. 15. It exhibits a trigger voltage of 1.53 V and on-resistance of 1.67 Ω. The measured second breakdown current is as high as 1.77 A which is sufficient to sustain a 2-kV human-body model (HBM) ESD stress [2].

Table 2 compares the performance of the reported CMOS ESD protection I/O pads with bandwidth extension circuits. The bandwidth is highly dependent on the parasitic capacitance of the ESD device considered in each work.

Generally, the smaller parasitic capacitance, the broader bandwidth and the higher data rate. As mentioned earlier, the I/O pads with T-diodes or modified T-diodes allow relatively broad bandwidth [7], [9], [10], [30]. Two inductors were utilized in [11] to distribute the capacitances for broadband impedance match. A π-diode circuit was also employed to extend the bandwidth using a single inductor [12]. Note that the large T-coil or inductors in the previous works were placed outside of the pads, which greatly increases total chip area. On the contrary, in this work, the inductor is placed under the pad, so that there is no increase in the chip area by the inductor. Therefore, the chip area in this work is less than about the half of others, as compared in Table 2. In summary,

TABLE 2. Performance comparison of the reported bandwidth extension circuits of the CMOS ESD-protection I/O pad for high-speed interfaces.

	Technology	Topology	Total parasitic capacitance	3-dB bandwidth ($|S_{21}|$)	$|S_{11}|$ bandwidth (< -10 dB)	Data rate (NRZ)	Circuit area (I/O pad + inductor)
[7]	28-nm CMOS	T-diode	420 fF	33 GHz	-	100 Gb/s 200 Gb/s*	10×10^3 μm^2
[9]	65-nm CMOS	T-diode	230 fF	26 GHz	18.5 GHz	25 Gb/s	11.8×10^3 μm^2
[10]	65-nm CMOS	Modified T-diode	300 fF	40 GHz	-	40 Gb/s	8.1×10^3 μm^2
[30]	90-nm CMOS	Modified T-diode	215 fF	-	20.1 GHz	-	7.1×10^3 μm^2
[11]	40-nm CMOS	4th-order LC filter	700 fF	< 5 GHz	< 9 GHz	-	23.5×10^3 μm^2
[12]	0.18-μm CMOS	π-diode	-	> 20 GHz	> 20 GHz	-	10.8×10^3 μm^2
This work	28-nm CMOS	π-diode	380 fF	22.9 GHz	26.5 GHz	32 Gb/s	3.8×10^3 μm^2

* PAM-4

the proposed π-diode using the pad-stacked inductor can achieve a comparable bandwidth with a reduced chip area. It is also worthwhile to note that the miniaturization technique proposed in this work can be applied for the design of the broadband and compact T-diodes as well.

IV. CONCLUSION

The compact π-diode for broadband ESD protection I/O pad was presented in a 28-nm FDSOI CMOS technology. The designed pad-stacked inductor avoids the increase of the circuit size by the inductor. The effect of the eddy current induced in the I/O pad which degrades the performance of the inductor was thoroughly studied by both the simulation and measurement. The equivalent circuit of the pad-stacked inductor was successfully implemented and verified by the measurement results. It was utilized to accurately design the π-diode. The eddy current was reduced by selecting the thick metal layer distant from the pad metal layer. The designed patterned I/O pad further alleviates the performance degradation by the eddy current. The fabricated π-diode with the same size as that of the I/O pad presented a broadband return and insertion losses. The bandwidth performance was well-predicted by the equivalent circuit model of the pad-stacked inductor. The pad-stacked inductor proposed in this work can be applied for other bandwidth extension circuits using inductors such as T-diodes or LC filters. It will lead to the significant reduction of the CMOS chip-area for high-speed I/O interfaces with a large number of I/O pads.

ACKNOWLEDGMENT

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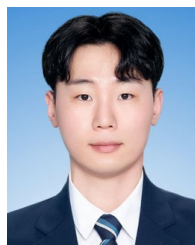
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