IEEE Access
Multidisciplinary | Rapid Review | Open Access Journal

Received 21 December 2022, accepted 8 January 2023, date of publication 16 January 2023, date of current version 23 January 2023.

Digital Object Identifier 10.1109/ACCESS.2023.3237647

RESEARCH ARTICLE

X-Band CMOS Rectifier With 4% Efficiency at −35 dBm for Wireless Power Transmission

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This work was supported by the Air Force Research Laboratory as Part of the Space Solar Power Incremental Demonstrations and Research (SSPIDR) Project.

ABSTRACT This paper proposes a radio frequency (RF) rectifier topology for low-power wireless power transmission (WPT) applications in the X band. The rectifier consists of a biased PMOS pair and is matched to the RF signal source impedance using a PCB transmission line (TL) matching network. It is demonstrated that a clever optimization of the bias voltage enables the rectifier to achieve greater sensitivity and efficiency than previous works at X band. The rectifier was designed in a 45 nm silicon-on-insulator (SOI) process and operates at a frequency of 9.64 GHz. It achieves a power conversion efficiency (PCE) of 4% and 46% at power levels of −35 dBm and −10 dBm, respectively.

INDEX TERMS Power conversion efficiency, rectifier, wireless power transmission, X band.

I. INTRODUCTION

In the past several years, there has been an increasing interest in the areas of RF energy harvesting and wireless power transmission (WPT), particularly for devices in the industrial, scientific, and medical (ISM) band [1]. The prevalence of devices operating in the ISM band provides many opportunities for applying energy harvesting and WPT methods within this frequency range. But, moving WPT into higher frequency bands would allow for smaller antennas and arrays since the aperture dimensions can be scaled down in proportion to wavelength [2]. However, WPT becomes more difficult at higher frequencies due to the increased effects of parasitic impedances of the devices. Additionally, atmospheric absorption of electromagnetic (EM) waves tends to increase with frequency [3]. As such, mitigating these effects often requires a lower frequency in order to maximize the power that is delivered to the receiving device. Since atmospheric losses increase more rapidly above 10 GHz, the X band range has recently gained interest for WPT demonstrations [4], [5].

There are a couple of factors primarily responsible for limiting the sensitivity and efficiency of RF rectifiers. One factor is the threshold voltage, V_{th}, of the rectifying device, which determines the minimum input signal amplitude that can generate DC output power with an acceptable conversion efficiency. Another limiting factor is current that flows away from the load and back towards the RF signal source, often referred to as reverse leakage current.

In light of these two factors, several CMOS RF rectifier topologies have built upon the Dickson voltage multiplier [6] by utilizing the gate connection to improve the efficiency at low input power levels. In [7], a bias voltage was added across the rectifying transistors using a network of capacitors and switches to connect the bias voltage to each device. Passive "V_{th}-cancellation" schemes have also been proposed, as in [8] and [9], which provide a simpler method of improving the rectifier's sensitivity compared to the implementation in [7]. However, the static nature of the V_{th}-canceling bias voltage results in increased reverse leakage during the negative half of the RF signal cycle. Further

The associate editor coordinating the review of this manuscript and approving it for publication was Alon Kuperman.

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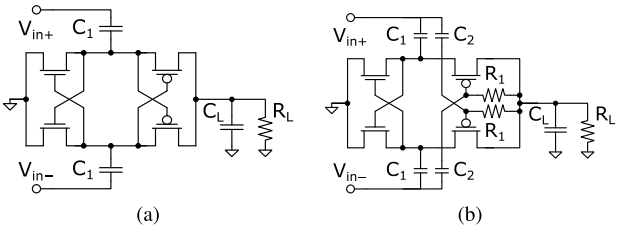

FIGURE 1. Previous RF rectifier topologies including (a) cross-coupled charge pump topology as in [10] and (b) cross-coupled charge pump with addition of self-biasing as in [12].

improvements are made in regard to the reverse leakage by the cross-coupled charge pump rectifier topology in [10], shown in Figure 1(a), which reduces reverse leakage during the negative half of the signal cycle. But, leakage is still problematic at higher signal power levels due to the increased DC voltage difference between the transistor gates and the output. To combat this effect and improve rectifier efficiency for higher power levels, self-biased cross-coupled rectifiers were proposed in [11] and [12], the latter of which is shown in Figure 1(b). Similarly, rectifiers utilizing an auxiliary charge pump to supply a bias voltage and improve efficiency have been proposed in [13] and [14]. It should be noted that in some of the above references, the term "V_{th}-canceling" is used even though the device V_{th} is not actually modified. In reality, the rectifier topology permits the application of a bias voltage which increases the conversion efficiency at low input power levels even though the transistor's V_{th} is unchanged. In contrast, designs have been proposed that utilize bulk biasing, as in [15], which are capable of modulating V_{th}. However, even when the addition of a gate or bulk bias voltage improves a rectifier's power efficiency, there is little indication, if any, whether the utilized bias voltage truly optimizes the rectifier's efficiency. Additionally, while these topologies reduce reverse leakage and improve efficiency for higher input power levels, the efficiency at lower power levels is still limited by the V_{th} of the transistors.

In this paper, we propose a rectifier utilizing an optimized DC gate bias voltage for further improving sensitivity and efficiency across a wide input power level range. An approximate expression for the optimal biasing condition involving both V_{th} and the output voltage is also provided. The proposed rectifier is designed for X-band frequencies.

The paper is organized as follows: section II provides an overview of the rectifier system operation and design challenges, section III discusses the design of the RF rectifier circuit and the bias voltage optimization, and section IV provides an overview of the matching network design. Following this, section V provides measurement results, and section VI concludes the paper.

II. SYSTEM OVERVIEW

A block diagram of a rectenna system architecture utilizing a differential rectifier is shown in Figure 2. Assuming the rectifier consists of ideal switches or diodes placed in series

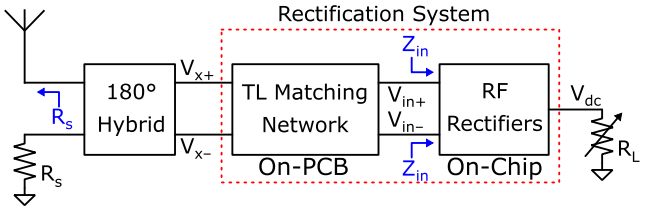

FIGURE 2. Block diagram of rectenna system architecture.

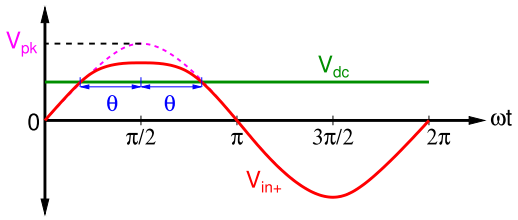

FIGURE 3. Example RF rectifier waveforms for showing how the conduction angle, θ, is defined. V_{in+} is the voltage at the positive input terminal of the rectifier.

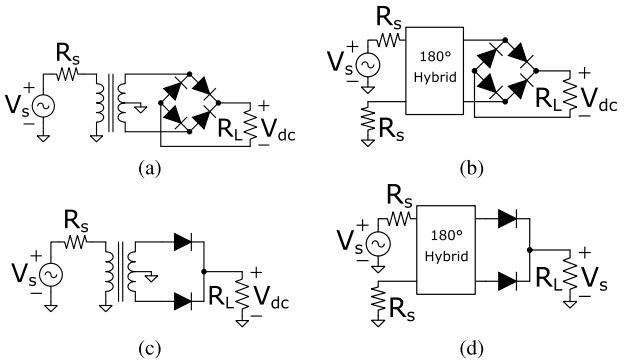

FIGURE 4. Example single-ended to differential conversion for different full-wave rectifier configurations. Full-bridge rectifiers connected to the output of (a) a center-tapped transformer or (b) a 180° hybrid, and full-wave rectifiers composed of half-wave branches connected to (c) a center-tapped transformer or (d) a 180° hybrid.

with the signal source, a conduction angle, θ, can be defined which determines the fraction of a cycle for which each rectifying device is ON. The conduction angle is given by

$$\cos\theta = \frac{V_{dc}}{V_{pk}}, \tag{1}$$

where V_{pk} is the peak amplitude of V_{in+} as shown in Figure 3. It can be shown that a conduction angle of $\theta \approx \frac{3\pi}{8}$ yields a maximum power efficiency of about 92% for a full-bridge rectifier or about 46% for a half-wave rectifier [16]. Importantly, these efficiencies are in the absence of additional filtering techniques that would re-capture energy in the harmonics that are produced by the nonlinear rectification process. For a half-wave rectifier, this filtering must also properly handle the DC component of the rectifier's input voltage, namely by forcing this DC component to be zero. However, if filtering is utilized at the input of the rectifier to re-capture this energy, then the efficiency of an ideal full-bridge or half-wave rectifier can approach 100% [16], although in practice this number is not achievable.

The implementation and modeling of the differential conversion is an important factor in the rectification system's behavior. In Figure 2, the single-ended to differential conversion is illustrated with a 180° hybrid since this is used in the final test setup. However, if the conversion to differential signals is achieved with a transformer, this can result in some differences in system behavior. To help illustrate the differences, Figure 4 shows different full-wave rectifier topologies consisting either of a full-bridge rectifier or two half-wave rectifiers in parallel and with either a transformer or a hybrid as the differential conversion element. These circuits are shown without matching networks to illustrate baseline behavior in the absence of the previously mentioned input filtering. For the rectifier setups shown in Figure 4(a) and (b), the circuit behavior will be the same since the full-bridge rectifier operates symmetrically on both halves of the RF waveform on each differential branch. As a result, both of these circuits can achieve about 92% efficiency. However, the behavior for Figure 4(c) and (d) can be significantly different from each other. Assuming the diodes are ideal, then the circuit of Figure 4(c) will be able to achieve about 92% efficiency while that of Figure 4(d) will be about 46%. This is due to the fact that the center-tapped transformer in Figure 4(c) provides a short-circuit to ground at DC. This forces the DC component of the input voltage for each half-wave branch to be zero which markedly improves the efficiency of each half-wave rectifier. The hybrid, on the other hand, presents an impedance of R_s to ground at DC, so the DC component of the half-wave rectifier input voltages are not forced to zero. This leads to a maximum power efficiency of about 46% for each half-wave rectifier, with the result that the overall efficiency of the circuit is 46% as well. As mentioned previously, it is still possible to approach 100% efficiency for any of the circuits in Figure 4 with additional input filtering. But, the use of a hybrid necessitates more input filtering to reach the same overall efficiency compared to if a transformer or similar device is used for the single-ended to differential conversion.

In order to ensure the maximum amount of power is transferred to the rectifier and its load as well as attempt to re-capture some of the energy in the harmonics, a matching network is needed for the rectification system. However, the highly nonlinear nature of the rectifying transistors causes increased complexity in the design of the matching network. Along with creating additional harmonics, the nonlinearities of the transistors cause the input impedance of the rectifier to be dependent on the signal power (and corresponding voltage swing) at the rectifier's inputs. This behavior means that achieving an optimal, or near-optimal, design of a rectifier system requires an iterative design procedure where the matching network design is incrementally adjusted in response to the rectifier's input impedance.

Once an impedance match is achieved, there will be a certain amount of passive voltage gain across the matching network which is dependent on the source and load impedances. For simplicity, we will assume the source impedance is purely real (R_s, as shown in Figure 2). The load of the matching network is the rectifier, for which the input can be represented as a parallel RC combination with an average admittance of $Y_{in} = \frac{1}{Z_{in}} = G_{in} + jB_{in}$. A positive sign is given to the B_{in} term since this susceptance is primarily due to parasitic capacitance. Additionally, real matching networks will have some loss. The amount of power lost in the matching network, P_{loss}, can be written as a fixed portion of the power entering the matching network, P_x (i.e. $\frac{P_{loss}}{P_x} = \alpha$). Accounting for this loss factor, when the input and output of the network are matched to the source and load impedances, the passive voltage gain across the matching network will be

$$\frac{V_{in}}{V_x} = \sqrt{\frac{1-\alpha}{R_s G_{in}}}. \tag{2}$$

In this equation, V_x is the signal amplitude at the matching network's input and V_{in} is the amplitude at the rectifier's input terminals as shown in Figure 2.

Therefore, losses in the matching network will reduce the passive voltage gain across it, resulting in a smaller RF signal amplitude at the inputs of the rectifier, thereby degrading the system's sensitivity. Additionally, if these losses are left unaccounted for, then the rectifier's input impedance will change as a result of its nonlinearities, resulting in impedance mismatches that further reduce the power entering the rectifier. This interdependence between the matching network's losses and the rectifier's input impedance leads to the iterative nature of the matching network design procedure.

III. PROPOSED CMOS RECTIFIER

When considering the PCE of a rectifier topology, two of the limiting factors are the device V_{th} and reverse leakage current, as mentioned in section I. The device V_{th} will limit the sensitivity of the RF rectifier, but the sensitivity can be improved by applying an optimal DC bias voltage to the gates of the transistors. On the other hand, reverse leakage becomes more problematic at higher input power levels. For a PMOS rectifier, as a larger voltage is developed at the output of the rectifier, the voltage between the output node and the transistor gate can begin to approach or exceed V_{th}. When this occurs, current flows from the load to the source, thereby limiting the voltage that can be developed at the output. This limiting of the output voltage due to leakage will ultimately limit the overall efficiency that is achievable at higher signal power levels.

As mentioned previously, self-biasing methods as in [11] and [12] may not produce an optimal gate biasing condition for maximizing the rectifier power efficiency. Furthermore, the sensitivity of self-biased schemes is still limited by the device V_{th}. To overcome these limitations, we propose the rectifier shown in Figure 5. The rectifier is composed of a voltage boosted PMOS transistor pair which utilizes an independent, tunable bias voltage at the gates of the transistors rather than the self-biasing from the output that is used in [11] and [12]. This bias voltage is varied in

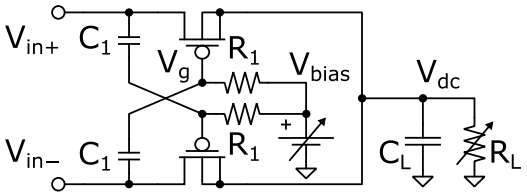

FIGURE 5. Proposed RF rectifier design with separation of bias voltage for optimization.

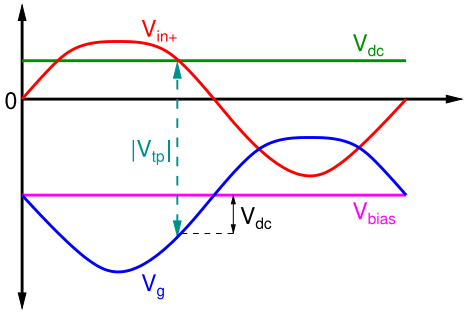

FIGURE 6. Waveforms at the positive input and gate of one rectifying transistor in Figure 5 demonstrating the relationship for minimizing reverse conduction, where V_{tp} is the threshold voltage of the PMOS device.

order to optimize the conduction angle of the rectifier for different input power and load conditions. Thus, the proposed rectifier preserves many of the advantages that [11], [12] have over [10] while further improving the rectifier's operation by mitigating the reverse leakage that still occurs at higher power levels. To accommodate the variable bias voltage, the PMOS pair is cross-coupled through high-pass filters. Each branch of the rectifier is a half-wave architecture which combine to make a full-wave rectifier due to the differential nature of the circuit.

There is a very small net current flow from the bias voltage source due to the non-zero average voltage at the gates of the transistors resulting from the asymmetric waveforms, as in Figure 6. However, simulations of the rectifier at −30 dBm show only about 32 nA of RMS current flowing from the bias voltage due to the low leakage current through the transistor gates as well as the large resistors in the high-pass filter. Therefore, negligible DC power is consumed by the bias voltage. As a result, the bias voltage could be supplied by a low-power auxiliary rectifier as in [13]. With an independent voltage source in place for biasing, we only need to know what value of the bias voltage optimizes the conduction angle.

Figure 6 shows the waveforms at various terminals in Figure 5, where $V_g = V_{bias} + V_{in-}$. If the transistors are modeled as ideal switches, then maximizing the power delivered to the load, and therefore maximizing the PCE of the rectifier, requires minimizing the reverse conduction over a period of the RF signal. Reverse conduction is minimized if $(V_{in+} - V_g) > |V_{tp}|$ only during the period $V_{in+} > V_{dc}$. This condition requires the difference $(V_{in+} - V_g)$ to be equal to $|V_{tp}|$ when $V_{in+} = V_{dc}$, as indicated in Figure 6, which yields

$$V_{dc} - (V_{bias} - V_{dc}) = |V_{tp}|, \tag{3}$$

resulting in the optimal bias voltage which minimizes reverse conduction as

$$V_{bias} = 2\,V_{dc} - |V_{tp}|. \tag{4}$$

This equation only ensures that the reverse leakage current is minimized, and minimizing the reverse leakage will maximize the PCE for a given loading condition, assuming that the transistors act as ideal switches. However, the efficiency is also dependent on the rectifier's load resistance, R_L, but this can be swept to find the optimal load for a given input power level. It should also be noted that for nonlinear devices where the switch resistance varies with bias voltage or input signal amplitude, as in the case of real transistors, the optimal bias may deviate from this condition.

IV. MATCHING NETWORK DESIGN

To ensure that the maximum amount of power is transferred to the rectifier, a matching network must be used to transform the impedance seen at the input of the rectifier to match the impedance of the RF signal source. Additionally, a matching network performs some filtering of the harmonics generated at the rectifier inputs. This allows some of the power in these harmonics to be re-captured and improve system efficiency. Due to the differential nature of the rectifier, a differential RF matching network is necessary for the system's operation while a 180° hybrid was used to create the differential RF signals at the input of the on-board matching network. For this design, a standard RF source impedance of 50 Ω was used. The matching network was designed to achieve an impedance match at a power level of −30 dBm. This provides a compromise in matching performance between the lowest and highest power levels that were tested while still emphasizing the impedance match at lower power levels where it is much more important for system efficiency.

As mentioned in section II, the design of the matching network is generally an iterative procedure due to the nonlinear nature of the rectifier. For this TL matching network design, an ideal LC matching network was first created in simulation, and the LC matching network parameters were tuned to maximize rectifier efficiency at the desired power level. This idealized matching network provided a starting point for the rectifier input impedance that must be transformed by the real matching network. Once the first iteration of the TL matching network design was created, an S-parameter model of the network replaced the ideal LC matching network in simulations. The losses of the real matching network led to a change in rectifier input impedance compared with the ideal simulations, thus providing a revised target for the rectifier input impedance that must be matched to the source. This cycle of revisions to the TL matching network and updated rectifier input impedance results was repeated until an acceptable level of impedance matching was achieved.

To achieve the necessary impedance match, a single-stub, PCB TL matching network was constructed due to the higher quality factor of PCB TLs compared to inductors at X-band frequencies. The impedance transformation of

the feed lines that join to the on-board RF connectors was accounted for as part of the design, although these feed lines would not be necessary in a system with a fully-integrated antenna, as in [17]. The matching network was designed as a 2-layer board structure utilizing a Rogers 3003 substrate for the dielectric. This substrate was chosen in order to minimize the losses of the matching network due to the ϵ_r of 3.0 and loss tangent of 0.001 at 10 GHz. The 2-D layout of the matching network and the impedance transformations at different reference planes along the matching network's construction are shown in Figure 7(a) and 7(b), respectively. The matching network was optimized for rectification at an input power level of −30 dBm and at a frequency of 10 GHz. Figure 7(b) shows the impedance transformations performed by the matching network on the rectifier's input impedance at this power level over a frequency range of 9.9 GHz to 10.1 GHz. The impedance at point 1 in Figure 7(b) is approximately $12-j347\ \Omega$ and is for the conditions that yielded maximum efficiency at an input power of −30 dBm. Across resistance and bias voltage at −30 dBm, the rectifier's input resistance varies from about 3.9 Ω to 71.5 Ω while the reactance varies from −320 Ω to −350 Ω. The loss of the structure in Figure 7(a) was estimated from simulations of its S-parameter model to be about 1.1 dB near the center frequency of 10 GHz.

Although only a 2-layer PCB is necessary for the matching network construction, characteristics of the chip bonding and board assembly processes necessitated additional rigidity. This resulted in the rectifiers and matching networks being manufactured on a 4-layer PCB. For PCB symmetry, the top and bottom dielectric layers utilized Rogers 3003 substrate while FR4 was used as the innermost dielectric between metal layers 2 and 3 to provide the added structural support. Except for the top layer with the matching networks and rectifier test structures, all other layers were solid metal planes apart from the necessary via holes. A flip-chip assembly procedure was utilized for placing the rectifier chips onto the test PCBs in order to minimize parasitic capacitances and inductances from packaging.

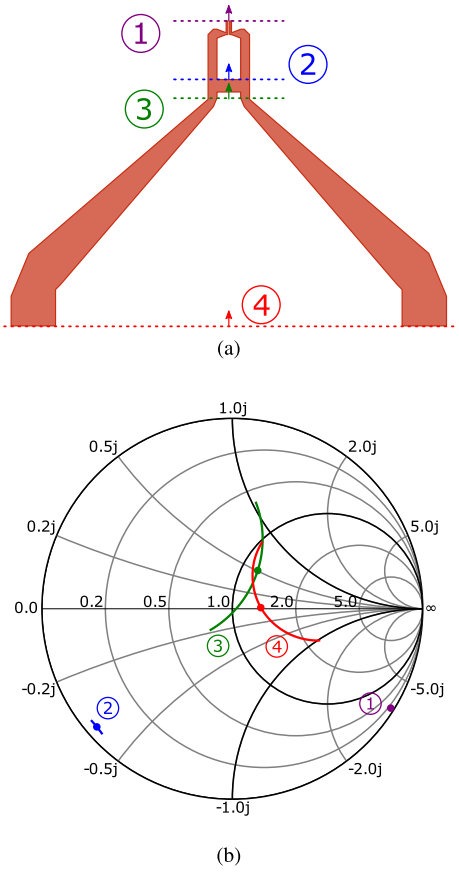

FIGURE 7. Images of (a) 2-D CAD model of single-stub TL matching network and (b) the simulated input impedance vs. frequency at the different reference planes shown on a 100 Ω Smith chart. S-parameters from layout simulations of the matching network were used, and the frequency was swept from 9.9 GHz to 10.1 GHz. The dot in each contour marks the impedance at 10 GHz for a given reference plane.

V. TESTING

A. TEST SETUP AND PROCEDURE

The layout and micrograph of the chip are shown in Figure 8(a) and (b), respectively. The large yellow rectangle at the top of the layout image is a ground plane underneath the input pads that was added to reduce RF losses to the substrate. At the bottom of Figure 8(a) are the output pads of the rectifier, with the pad for the DC output voltage in the center. Placed above the output pads are the coupling capacitors for the high-pass filters at each transistor gate. The ground plane, coupling capacitors, and transistors are hidden by the dummy metal fill in the fabricated chip. Utilizing the matching network designed above, a test structure was created with additional pads and traces for the peripheral components and connections needed to characterize the rectifier. The setup for this rectifier test structure is shown in Figure 8(c).

In order to characterize the rectifier chips, the boards were assembled with a digitally controlled load potentiometer to more easily enable sweeps of the load resistance. Digital multimeters were utilized for accurately measuring the DC output voltage and the bias voltage applied to the transistor gates. The bias voltage was provided by a digitally controlled variable voltage supply, and a network analyzer was used as the RF signal source. A 180° hybrid was used for the single-ended to differential conversion of the RF input signal, and a single-board computer was used to control the operation of the above components for better characterization of the rectifier's output voltage and efficiency across various parameters. An image of the test setup is shown in Figure 9.

B. LOSS CORRECTION

In order to more accurately estimate the true efficiency of the rectifiers, it was necessary to remove the effects of the test fixture losses (e.g. losses in the coaxial cables, 180° hybrid, and the on-PCB feed lines to the inputs of the matching network). The losses of the matching network itself were

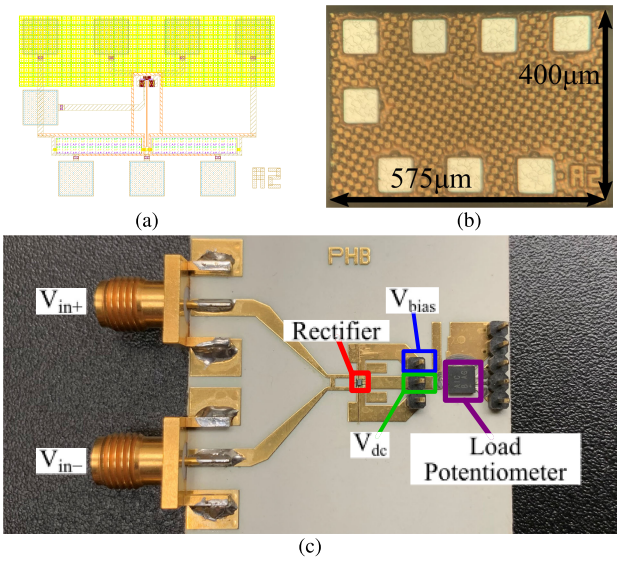

FIGURE 8. (a) Layout and (b) micrograph of rectifier chip, and (c) close-up of completed test setup for a single rectifier showing the input ports, PCB feed lines and matching network, rectifier chip, and digital load potentiometer.

not removed since these are still considered a part of the rectification system as a whole, as in Figure 2. S-parameter measurements were performed on the cables and hybrid up to the point at which this section of the fixture connected to the test PCB. Additional measurements were performed on the feed lines of the PCB structure (the region between reference planes 3 and 4 in Figure 7(a)) to leave only the losses of the matching network in the measurements of the rectification system's efficiency. For this purpose, an additional test board was fabricated with replica feed lines placed back-to-back in order to create a "2x-thru" structure. The S-parameter measurements of this 2x-thru board were used in conjunction with the S-parameters of the cables and hybrid to estimate the losses between the network analyzer and the inputs of the matching network.

From the S-parameter measurements of the test fixture components, the losses were estimated to be about −5 dB. However, this loss estimate does not account for phase and amplitude imbalances in the hybrid, which could lead to a small differential-to-common-mode conversion and therefore a reduction in power transferred to the rectifier's inputs. The loss estimate also does not account for power that is reflected from the inputs of the rectifier or the matching network due to impedance mismatches. After accounting for the losses in the test fixtures, the overall efficiency of the rectifier during testing is calculated as

$$\eta = \frac{\frac{V_{dc}^2}{R_L}}{1\ \text{mW} \times 10^{\frac{P_{rect}}{10}}} \times 100\%, \tag{5}$$

where V_{dc} is the rectifier's DC output voltage, R_L is the load resistance, and P_{rect} is the corrected amount of power entering the rectifier, in dBm. The power consumed by the bias voltage is considered to be negligible, for the reasons mentioned previously, and is thus ignored in the efficiency calculation.

C. CHARACTERIZATION RESULTS

The following steps were used to characterize the rectifier:

1) The RF signal power and the rectifier load resistance were held constant, and a gate bias of 0 V was applied.
2) The RF signal frequency was swept to determine the frequency at which the rectifier achieved the best impedance match. The optimal frequency was found to be about 9.64 GHz.
3) The RF signal frequency was held constant at 9.64 GHz, and the remaining variables were swept as follows:
   a) The load resistance was swept from about 400 Ω to 13.5 kΩ in steps of about 400 Ω.
   b) The gate bias voltage was swept from −400 mV to 0 V in steps of 20 mV.
   c) The RF signal power from the network analyzer was swept from −30 dBm to −5 dBm in steps of 5 dBm.

Once an iteration of loop (a) was completed, the bias voltage would increment by the step specified for loop (b). Similarly, loop (c) would increment once an iteration of loop (b) completed. In this way, the rectifier could be fully characterized across all input parameters. The upper limit of −5 dBm on the network analyzer was chosen to provide a margin of safety while testing the rectifier. After correcting for losses, the actual signal power entering the rectifier ranges from about −35 dBm to −10 dBm. The offset from the target frequency of 10 GHz is likely due to parasitic impedances in the on-chip routing and the packaging that were unaccounted for during the design process along with manufacturing error tolerances in the fabrication of the on-PCB TL matching network. Because the matching network must create a match from an impedance with a very large reflection coefficient, the impedance match and thus the optimal operating frequency are very sensitive to small changes in the rectifier's input impedance and to variations in the TLs from which the matching network is constructed.

The output voltage and efficiency of the rectifier at 9.64 GHz for a few of the tested power levels are shown in Figure 10. The contour plots in the left column of Figure 10 show the DC output voltage of the rectifier across the range of tested bias voltages and load resistances. In the right column of Figure 10 are plots of the combined efficiency of the rectifier and matching network over the same sweep of parameter values. The output voltage and efficiency plots in each row are associated with a single power level.

From these contour plots, we see that the optimal bias voltage increases as the input power level increases. Since the output voltage generally increases with increasing input power level, this agrees well with the general trend that is predicted by Equation 4. From the sweeps of load resistance we see that the optimal load decreases for increasing input power level, likely as a result of the decreasing equivalent

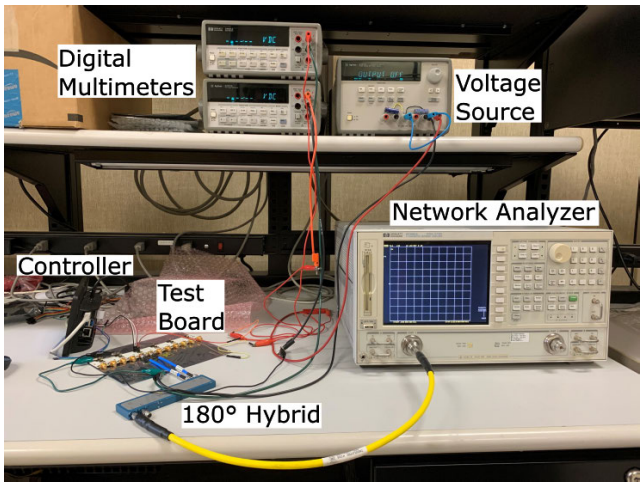

FIGURE 9. Lab bench setup for characterization of the RF rectifier.

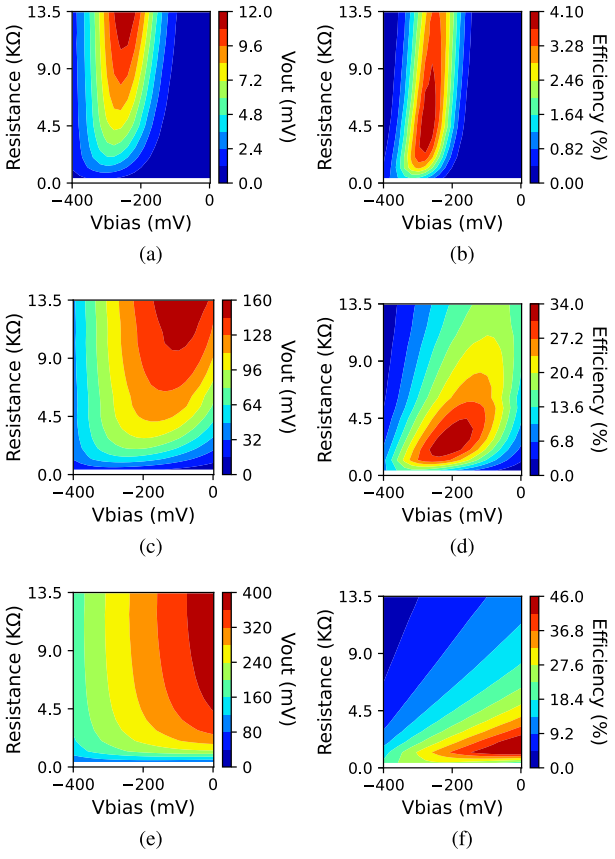

FIGURE 10. Plots of the rectifier output voltage (left column) and the efficiency (right column) as functions of the bias voltage and load resistance. Results are shown for input powers of −35 dBm (a, b), −20 dBm (c, d), and −10 dBm (e, f). These are the corrected power levels after accounting for test fixture losses. All measurements shown were taken at a frequency of 9.64 GHz which was determined to be the best operating frequency for the rectifier.

resistance of the transistors. As the input signal power level and signal amplitude increase, the transistors operate more in the triode region where their equivalent resistance, R_{sw}, is inversely related to the voltage across the device, leading to lower equivalent resistance as power increases. Because R_{sw} appears in series with the equivalent output impedance of the matching network, R_m, a larger load resistance will be needed for maximum power transfer to compensate for the addition of R_{sw}. Thus, as R_{sw} reduces with increasing signal power level, the optimal load resistance will similarly decrease. Additionally, the contour plots show that the sensitivity of the rectifier's power efficiency to the bias voltage and load resistance changes significantly as the power level increases. At lower power levels, the efficiency is clearly more sensitive to changes in bias voltage than it is to changes in load resistance. But as the power level increases, the power efficiency of the rectifier becomes much more sensitive to changes in the load resistance with significantly reduced sensitivity to bias voltage.

TABLE 1. Comparison of actual bias voltage and theoretical bias voltage predicted by Equation 4 for different input power levels.

Power	Measured V_{out}	Actual V_{bias}	Theoretical V_{bias}
−35 dBm	7.5 mV	−280 mV	−355 mV
−30 dBm	21.7 mV	−260 mV	−327 mV
−25 dBm	43.0 mV	−260 mV	−284 mV
−20 dBm	96.5 mV	−200 mV	−177 mV
−15 dBm	154.0 mV	−120 mV	−62 mV
−10 dBm	234.1 mV	−20 mV	98 mV

The conditions at which the maximum efficiency was achieved for different signal powers were also recorded and are plotted in Figure 11. The bias voltage and load resistance corresponding to each of the plotted measurements are annotated next to each point. The matching network was designed to achieve an impedance match in the −30 dBm case, so it is expected that some impedance mismatches will occur between the output of the matching network and the input of the rectifier as the signal power increases due to the rectifier's non-linearity. However, Figure 11 indicates that even with these impedance mismatches, an overall greater amount of power still enters the rectifiers. The efficiency contour plots of Figure 10 also indicate that some of the mismatch losses can be compensated for by an appropriate choice of bias voltage. This can be seen in that as the power level is increased, the point of maximum efficiency generally moves to the right in the contour plots (toward a more positive bias voltage) even if the resistance is held constant.

The data in Figure 11 also allows us to compare the actual bias voltage that was used during measurements against the theoretical bias voltage based on calculations using Equation 4. This comparison is made in Table 1 for each of the points plotted in Figure 11. A value of −370 mV is used for V_{tp} and was determined from characterization of the transistors in the simulation environment and is assumed to be constant in all cases for the calculations in Table 1. For input powers near the middle of the range, we can see that there is reasonable correlation between the actual and theoretical V_{bias} for the relatively simple approximation,

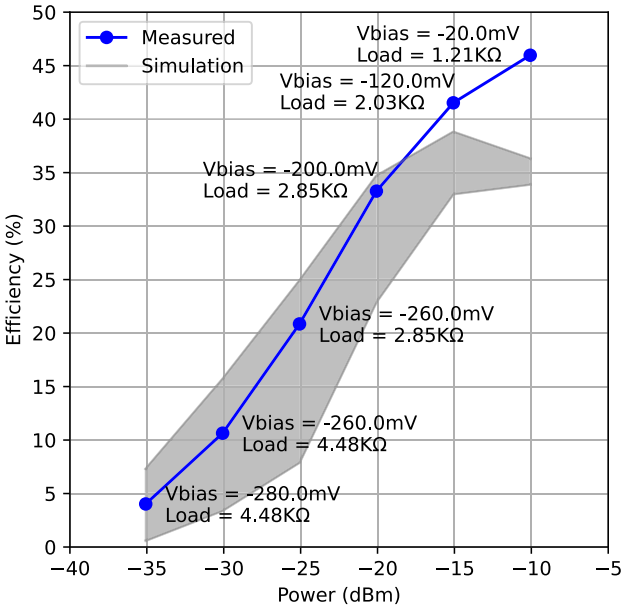

FIGURE 11. Plot of the maximum efficiency achieved at different input power levels for the PMOS rectifier setup. The gray region is the efficiency predicted across process corners in simulations while utilizing the same load and bias parameters as in the measurements. The model of the matching network and its associated losses are also included in the simulation results for equivalent comparison.

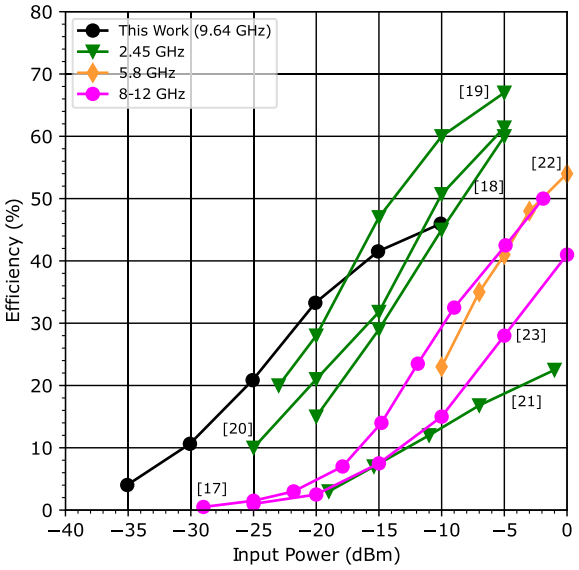

FIGURE 12. Comparison of proposed RF rectifier solution with the state-of-the-art for varying input power levels. It should be noted that the efficiency reported in this work is the total efficiency of the matching network and CMOS rectifier together as a unit.

but the differences grow at the lower and higher power levels.

At lower power levels, the difference can be attributed to subthreshold operation of the transistors. In the subthreshold region, the simplified switch-based model of the transistor's operation does not hold. Because of this, the use of $|V_{tp}|$ to approximate the boundary between forward and reverse conduction becomes much less effective. As a result, the optimum bias voltage relationship will deviate from the theoretical bias predicted by Equation 4.

For the higher power levels that were tested, the actual V_{bias} is lower than the theoretical V_{bias} that was calculated. Although a lower bias voltage would theoretically increase reverse leakage, it would also lead to a larger gate-source voltage that would reduce the equivalent resistance of the rectifying transistors. For these higher power levels, it is believed that this reduction in equivalent resistance is offsetting the losses of the reverse leakage, thereby leading to the shift in the actual optimal bias voltage level. We can also see from Figure 11 that the measured efficiency outperformed that of simulations using the same load and bias conditions. It is believed that this result is due to the body of the transistors being connected to the DC output voltage, as shown in Figure 5. Because of this connection, the voltage across the source-body junction will change over a cycle of the RF signal, and additional current will flow through the diode made by the source-body junction when it is sufficiently forward biased. Additional data also indicates that the models of these transistors, which are aimed more towards digital applications, underestimate the actual body current for larger forward-bias voltages compared with what would be measured under the same conditions. This would reduce the equivalent switch resistance of the transistors at higher power levels, thereby reducing the losses in the rectifier and leading to greater efficiency. These effects help to explain the difference between the measurements and simulations in the higher power tests as well as the difference between the actual and theoretical V_{bias} values in Table 1.

Figure 12 shows the rectifier efficiency compared against several other state-of-the-art RF rectifiers that were fabricated and tested at 2.45 GHz [18], [19], [20], [21], 5.8 GHz [22], and 8-12 GHz [17], [23]. This comparison is built on the survey in [17], and individual data points are estimated from rectifier efficiency plots presented in each of the above references. We can see from Figure 12 that the choice of optimal biasing and loading conditions enables us to achieve significantly greater efficiency with our rectifier topology at lower power levels than previous works in the same frequency range. Based on information in the above references, it appears that the matching networks used in [18], [19], and [21] were designed to match at −10 dBm, −14 dBm, and −15.4 dBm, respectively. The design in [20] does not have a matching network, and there does not appear to be enough information to determine what power level the matching networks were optimized for in the other designs. However, we see that our proposed solution has comparable efficiency at similar power levels even though the matching network for our solution was optimized for −30 dBm. For these higher power levels, it is expected that the impedance match provided by our matching network would show a modest degradation compared to the other designs. Therefore, even though the matching networks across the various designs are optimized for different power

levels, we believe that this comparison demonstrates the benefits of our proposed rectifier solution. The rectifier which is closest to achieving a similar level of performance is the one presented in [19] where a modified full-wave Greinacher rectifier based on discrete Schottky diodes was utilized. Since discrete components were used, the larger device dimensions and higher breakdown voltages compared with short-channel CMOS transistors should reduce the device ON resistance and reverse leakage, which may help to improve the rectifier efficiency, particularly at higher power levels as seen in the plot. Even so, our proposed solution is able to achieve greater sensitivity and efficiency at lower power levels while operating at a higher frequency where the task of RF rectification is more difficult.

VI. CONCLUSION

A rectifier has been designed for X-band frequencies utilizing PMOS transistors in a 45 nm process along with a differential, on-board, TL-based matching network. The addition of a variable DC bias voltage is shown to optimize the rectifier's efficiency across load and input power conditions, and an approximate relationship for the optimal bias voltage is given. It is shown that the optimal bias voltage is a function of the output voltage and the transistor threshold voltage, predicted by Equation 4. With optimal biasing of the rectifier, an efficiency of 4% is achieved at an incident RF power level of −35 dBm. For an input power level of −10 dBm, the rectifier achieves an efficiency of 46%.

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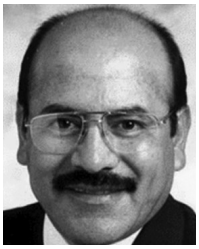

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