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RESEARCH ARTICLE

A Low-Phase-Noise Self-Aligned Sub-Harmonically Injection-Locked PLL Using Aperture Phase Detector-Based DLL Windowing Technique

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ABSTRACT This paper proposes a self-aligned sub-harmonically injection locked phase locked loop (SILPLL) in 180-nm Semi Conductor Laboratory (SCL) CMOS technology. In this work, an aperture phase detector (APD) based delay locked loop (DLL) with windowing technique is proposed to dynamically align the injection timing of pulse with the rising edge of sub-harmonically injection locked voltage controlled oscillator. In contrast to classical self-aligned SILPLL, this work replaces the commonly deployed tri-state based phase frequency detector (PFD) in DLL by an APD, which becomes active over a pulse-window. The APD deployed in DLL reduces the in-band phase noise due to the charge pump by 12 dBc at 200 KHz offset in comparison with the classical self-aligned DLL. A detailed mathematical model of the self-aligned injection with noise sources is presented for the proposed architecture. Additionally, this work includes noise analysis with the effect of different design aspects such as locking range, and realignment factor. The proposed architecture operates at 1.8 GHz output frequency, and the simulated phase noise is −120.6 dBc/Hz at 1 MHz offset with an integrated root-mean-square jitter of 0.96 ps from 10 kHz to 30 MHz. The implemented PLL consumes 6.6 mW from 1.8 V power supply.

INDEX TERMS Aperture phase detector (APD), delay locked loop (DLL), sub-harmonically injection locked phase locked loop (SILPLL), self-aligned injection timing.

I. INTRODUCTION

A phase locked loop (PLL) with low phase-noise and jitter is commonly used in various high performance systems, such as data converters [1], wireless communications [2] and clock generators [3]. The conventional PLL has various key performance parameters such as integrated jitter, phase-noise, power consumption, reference spur and power supply. To ensure the stability of a system, usually the PLL has tight trade-off among these above mentioned parameters. Owing to the stability limit [4] the loop bandwidth of conventional PLL is allowed to be at most one-tenth of reference frequency. As a result of limited bandwidth, the out-of-band phase-noise due to voltage-controlled oscillators (VCO) and in-band phase noise due to charge-pump cannot be efficiently suppressed. Recently, many research approaches have been presented to improve the phase noise of PLL such as utilizing a multiplying delay locked loop (MDLL) [5], [6], [7], [8], a sub-sampling-based PLL (SSPLL) [9], [10], [11], [12], [13], a sampling PLL (S-PLL) [14], a leakage-free digitally calibrated PLL [15] and a sub-harmonically injection locked PLLs [16], [17], [18], [19], [20], [21], [22], [23], [24], [25], [26].

Fig. 1 depicts the conventional architecture of an MDLL, this architecture offers the advantage to clean up the accumulated jitter of the noisy edges of the VCO. For this purpose,

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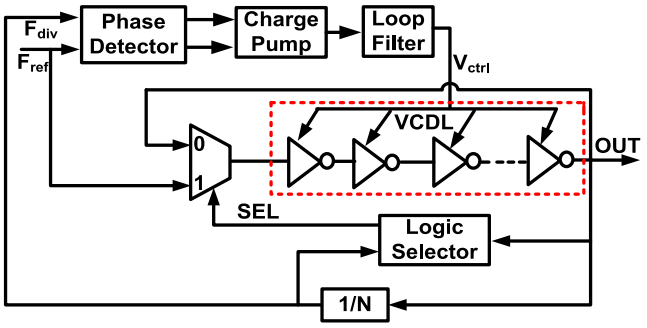

FIGURE 1. The architecture of conventional MDLL.

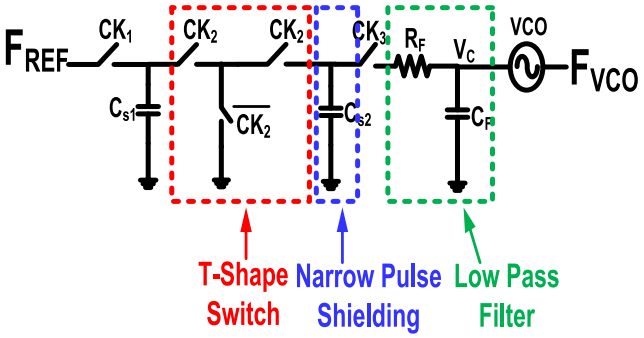

FIGURE 2. Single-path sampling phase detector with narrow pulse shielding [14].

a multiplexer is needed to switch between the reference clock and the noisy edges of the VCO clock. The divider is accountable for counting the clock pulses to generate the 'SEL' signal through logic selector block as shown in Fig. 1, to monitor the multiplexer's switching time in a back and forth manner respectively. As a result, the input reference clock edge is sent into the delay cells with the aid of this select logic circuitry. Meanwhile, at this stage, if any misalignment happens during the replacement of VCO noisy edges, it causes very high reference spur as well as deterministic jitter. This is the major drawback of this architecture.

Likewise, the sub-sampling-based PLL is commonly known for divider-less PLL. Which suppresses the noise of the charge pump (CP) by N^2, where N is the size of the divider. The effect of charge pump noise suppression directly reflects into the overall phase noise performance of the system. However, this architecture always requires an additional frequency tracking loop, to avoid such false locking that arises due to the absence of a divider block. Hence, this architecture has needed PLL with FLL and switching circuits. Proper synchronization is needed to control the switch back and forth between frequency locked loop (FLL) and divider-less PLL. Any misalignment leads towards a huge reference spur.

Fig. 2 shows the typical architecture of single-path sampling phase detector for the better suppression of reference-feedthrough (REF-feedthrough) with narrow pulse shielding (NPS) scheme [14] to improve the reference spur and RMS jitter, which are incorporated in a type-I PLL sampling PLL (S-PLL). The sampling phase detector (S-PD) effectively consists of master and slave sampling stage for detecting the phase error through the controlled switch CK_1 and outputting the sampled DC voltage as well as tackling the effect of reference-feedthrough using the controlled-T shape switch CK_2 respectively. Moreover, to alleviate the non-idealities of sampling operation, i.e, charge injection and varactor gate-leakage, a high-frequency narrow-pulse-shielding technique corresponding to switch CK_3 and first order low-pass filter (LPF) has been cascaded with the T-shape switch CK_2 to avoid the spur on the control line V_c.

In an injection-locked PLL (ILPLL), the injection timing of injected pulse can be calibrated either manually or

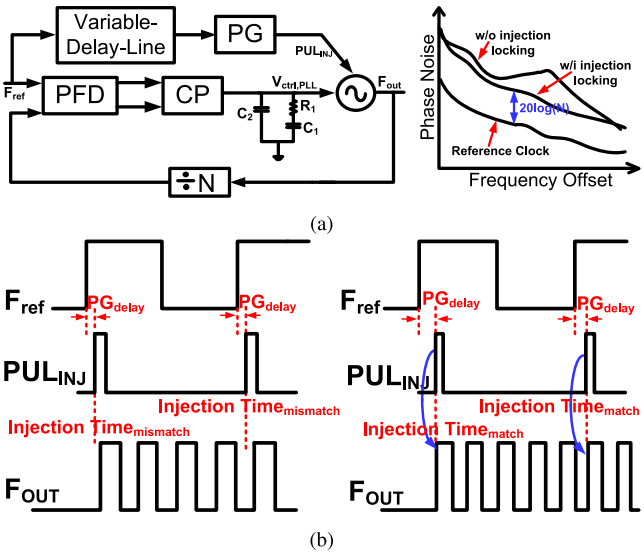

FIGURE 3. (a) Block diagram of the fundamental ILPLL and the principle regarding phase noise reduction of ILPLL (b) Timing diagram of a basic ILPLL.

automatically. Fig. 3(a) depicts the basic block diagram of injection-locked PLL (ILPLL) [27]. Additionally, the suppression of phase noise with the effect of the applied technique is also drawn in Fig. 3(a).The out-of-band phase noise is directly suppressed by injecting a clean pulse PUL_{INJ} through the output of the pulse generator (PG) to the input of VCO. Owing to this technique, the phase noise can be suppressed by N^2. Where N is divider size. In this basic ILPLL, the delay of the line is manually controlled. Owing to the absence of self-calibration control over delay-line, it makes the performance of ILPLL sensitive to the process, voltage, and temperature (PVT) variation. In addition to this variable delay line needs to be adjusted again and again manually once the frequency changes. Additionally, the timing waveform of basic ILPLL in Fig. 3(b) is also drawn to understand the injection time locking. When the ILPLL is locked, F_{OUT} is aligned with the reference input F_{ref}, and the injection signal is injected into the VCO with the delay (PG_{delay}) of the pulse generator. As the injection timing is controlled manually,

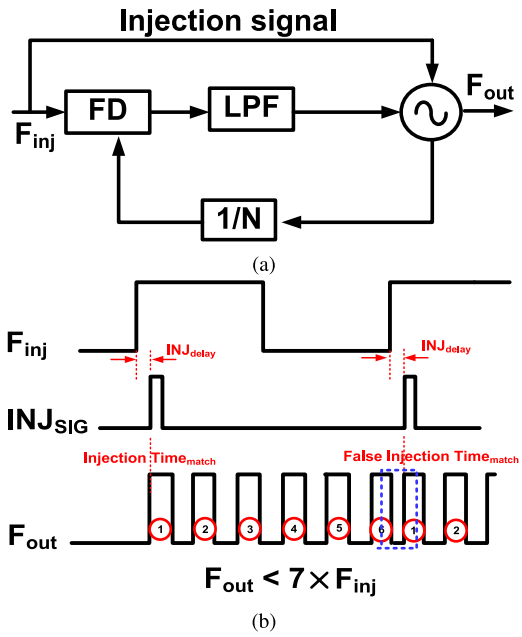

FIGURE 4. (a) Block diagram of the fundamental ILFLL (b) Timing diagram of a basic ILFLL.

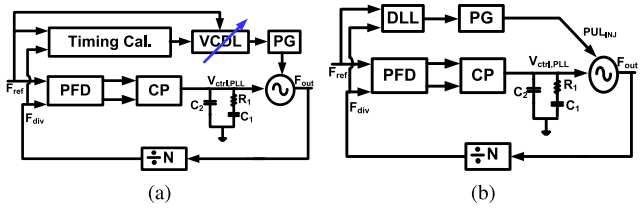

FIGURE 5. (a) Block diagram of the principle of injection time calibration (b) Block diagram of injection time calibration with DLL.

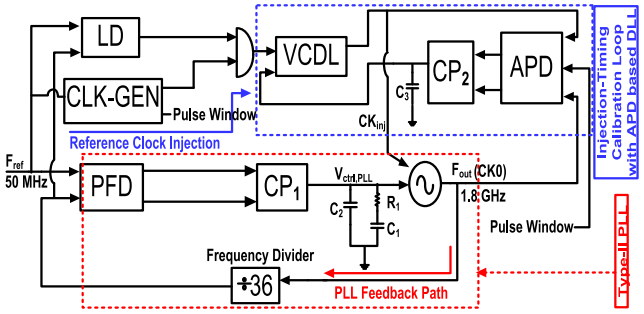

FIGURE 6. Block Diagram of the proposed sub-harmonically injection locked PLL with self-aligned APD based DLL.

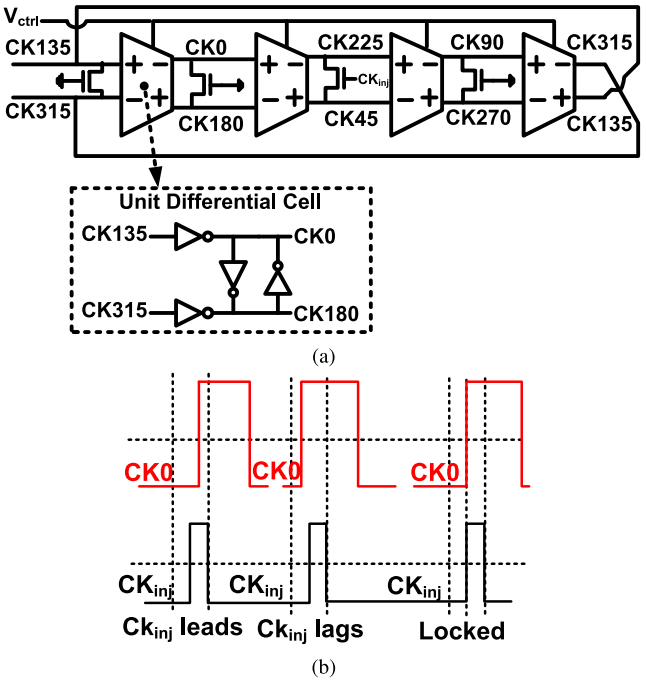

FIGURE 7. (a) Block diagram of the SILVCO (b) Injection locking timing diagram of SILVCO.

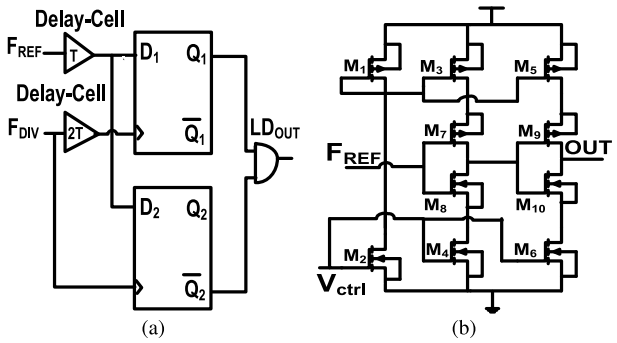

FIGURE 8. (a) Block diagram of Lock Detector (b) Schematic of two-stage delay cell with T delay.

therefore if this injection is not handled properly, it causes a huge reference spur.

Likewise, Fig. 4(a) shows the basic block diagram of injection locking with frequency locked loop (ILFLL) [28]. However, with the help of FLL this architecture can be managed to set the output frequency without harmonic locking. But, because of PVT variations despite of using an FLL frequency error may occur, which causes false locking as we can clearly see from Fig. 4(b). To overcome all these drawbacks, a self-adjusted injection time calibrator is needed to get rid of the timing mismatch difficulty along with frequency error problem. Fig. 5(a) shows a simple block diagram to explain, how the injection time calibration happens. Compared with the previous techniques, it is self-calibrated, and self-aligned technique. In this topology, once the VCO frequency changes the timing error is self-adjusted through a dedicated calibrator and VCDL. To validates this idea, an architecture [21] have been proposed. To adjust the injection timing automatically several techniques [21], [22], [29] are proposed to achieve the proper injection timing. However, in-band phase noise due to extra charge pumps other than main loop in [21], [22], and [29] has been not addressed yet.

Unlike the classical phase detectors based DLL [30], [31], [32], this paper includes an APD [33] based DLL to achieve the lower in-band phase noise along with self-aligned

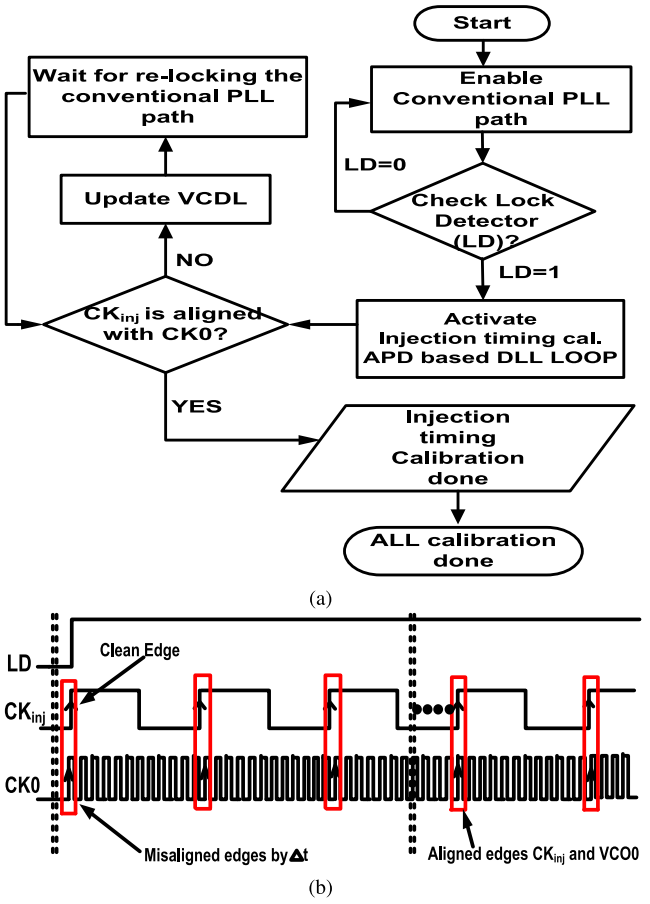

FIGURE 9. (a) Operational flow-chart of the proposed architecture (b) Timing diagram of the proposed ILPLL.

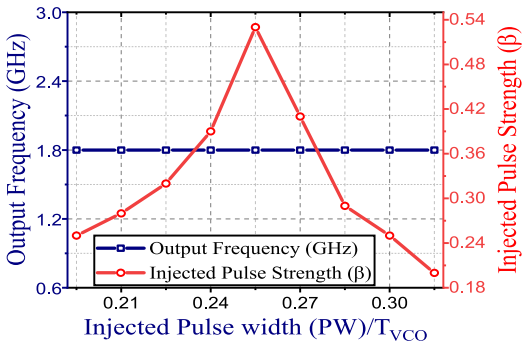

FIGURE 10. Simulated injection strength (β) as a function of $\frac{PW}{T_{VCO}}$ at 1.8 GHz output frequency.

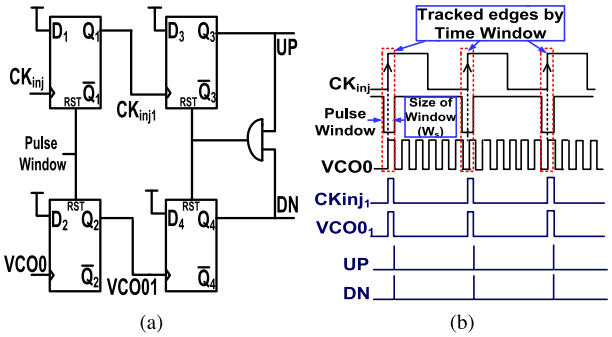

FIGURE 11. (a) Schematic of aperture phase detector (APD) (b) Timing-diagram at the output of the APD in the locked-state.

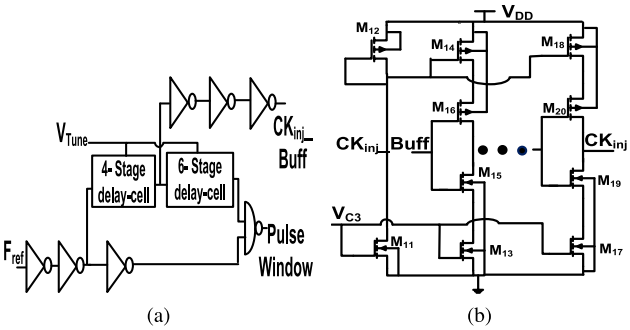

FIGURE 12. (a) Schematic of clock-generator (CLK-GEN) circuit (b) Schematic of voltage control delay line (VCDL).

injection timing. In this newly proposed DLL, the deployed APD directly measures the phase difference between reference input and VCO output within alotted time-window. Due to the existence of the deployed APD in the injection time calibration loop, it can work without using an output of frequency divider (N). This further leads to the suppression of in-band phase noise of CP, as deployed in APD-based DLL. Moreover, the out-of-band phase-noise due to ring-VCO is also suppressed using self-alignment of injection timing. Additionally, the incremented linear model of self-aligned SILPLL with the effect of various realignment factor (δ) and locking range (f_L) has been analysed. The theoretical comparison of in-band phase-noise of sub-harmonically injection-locked PLL with self-aligned DLL and APD based DLL are presented with the linear model. The calculated in-band phase-noise for the proposed architecture at 1.8 GHz output frequency is -122 dBc/Hz, whereas the in-band phase noise for the classical self-aligned SILPLL [21] is -110 dBc/Hz at an offset of 200 kHz. This newly designed architecture offers the requirement of low phase-noise, low integrated jitter and better figure-of-merit (FOM) among other injection locked techniques.

In this work, a PLL with self-calibrated injection timing is reported. This paper is organised as follows. In section II, the circuit description of sub-harmonically injection locked PLL with self-aligned APD based DLL is presented. In section III, the phase-noise analysis of the SILPLL along with design parameters of the proposed architecture is presented. The results and discussions are shown in section IV and the conclusions are given in section V.

II. CIRCUIT DESCRIPTION

Fig. 6 depicts the injection-locked PLL architecture, it consists of a conventional type-II PLL feedback path along with a reference injection path through self-aligned APD

based DLL. The type-II PLL is composed of the conventional building blocks, such as a phase-frequency detector (PFD), a source-switched charge pump (SSCP) [34], a loop filter (LF), a current-starved topology-based [35] pseudo-differential ring sub-harmonically injection-locked voltage-controlled-oscillator (SILVCO) [36] with injection as shown in Fig. 7(a) and 7(b) respectively, and a divide-by-36 divider. Moreover, the injection timing calibration loop is composed of the aperture phase detector (APD), a source-switched charge pump (SSCP), a loop filter capacitor, and a voltage-controlled delay line (VCDL). Furthermore, a clock generator (CLK-GEN) is deliberately employed in the reference injection path to generate the clean injection pulse and pulse window. Further, the generated pulse window encounters the input of APD to allot the timing window for comparing the phase error between CK_{inj} and CK0. The reference clock injection path is activated only after the locking between the reference clock and the feedback clock has been approved by the lock detector [37] (LD) circuit.

The proposed SILPLL with self-aligned APD based DLL has two modes of operation which is controlled by the lock detector (LD) as shown in Fig. 8(a). In the first mode, owing to LD = 0 the reference injection through DLL is disconnected and conventional PLL activated. Moreover, once the PLL is locked at the desired frequency of F_{out} ($F_{out} = 36 \times F_{ref}$), the lock detector (LD) switches it's mode from LD = 0 to LD = 1 by enabling the reference clock injection (CK_{inj}). The working of block diagram as shown in Fig. 6 is explained through flow-chart, as depicted in Fig. 9(a).

Fig. 9(a) depicts the flow-chart of the proposed architecture, whose injection timing is calibrated in three steps.

Step 1: In the unlocked state (LD = 0), the feedback path of conventional PLL is enabled whereas the injection locking path is disabled. The output frequency of conventional PLL is set to F_{out}, which is 1.8 GHz.

Step 2: Once the PLL is locked, the output of the lock detector becomes LD = 1. The injection of reference frequency through the output of AND gate in Fig. 6 is activated to start the injection timing calibration. In this mode (LD = 1), the APD compares the phase error of two different frequencies which is coming out of two different blocks (VCO and voltage-controlled delay line (VCDL)) within allotted time slots determined by pulse window. Furthermore, the output of APD is fed to charge pump (CP_2) whose output current through the loop filter capacitor (C_3) generates voltage corresponding to phase error between VCO output (CK0) and reference injection (CK_{inj}) as shown in Fig. 6. This voltage further updates the delay using VCDL. This process continues until the CK_{inj} is aligned with CK0 using the APD based DLL loop.

Step 3: Once the injection timing adjustment is done using DLL loop, the edges of CK_{inj} and CK0 are self-aligned as shown in Fig. 9(b).

Even though, With the injection timing calibration only, the performance of phase noise improves but the 2*N*th harmonic power of injection can be worse [19], which can be improved by optimizing the pulse width of the injected pulse. Hence, for better understanding, further simulation has been carried out using a variable pulse width at a fixed output frequency of 1.8 GHz and the corresponding result has been shown in Fig 10. In this simulation, the ratio of injected pulse width (PW) to the period of VCO (T_{VCO}) has been varied manually from 0.195 to 0.315 by fixing the size of the injection transistor to obtain the fix output frequency. Fig. 10 clearly depicts the maximum injection strength (β) can be obtained when injection pulse width (PW) is equal to one fourth of T_{VCO} [19], where the injection pulse strength (β) is directly related to the injection pulse width (PW) [19], [38], [39] and the 2Nth harmonic power of injection. The sub-blocks of APD based DLL are shown in Fig. 11 and Fig. 12 respectively.

A. APERTURE PHASE DETECTOR

Fig. 11(a) shows the schematic of the aperture phase detector, which directly compares the phase difference between CK_{inj} and VCO0 in an allotted time window, as shown in Fig. 11(b). Due to the direct comparison of the phase difference between CK_{inj} and VCO0, it works without a frequency divider. Moreover, the timing control signal (pulse window (W_s)) within which the operation of phase error comparison has to occur is generated through CLK-GEN circuit shown in Fig. 12(a). When the output of the pulse window becomes low for a window size of W_s, APD starts tracking the first rising edge of CK0 and CK_{inj} signals. The tracking continues until the window is open, once the window is closed both the signals will be reset to '0'. After the first truncation, a tri-state based classical PFD further compares the phase difference of the truncated signals. Once, the process is accomplished, it produces the output as UP and DN signal.

To avoid the edge missing during phase detection by APD, the window size (W_s) has been considered a little wider than the VCO0. Moreover, to sense the positive and negative phase errors by APD, the midpoint of W_s has to be aligned with the rising edge of CK_{inj}.

Fig. 11(b) shows the timing diagram of the APD. When the LD is high, the deployed APD is enabled. If the rising edge of CK_{inj} leads first rising edge of VCO0 within the allotted time slot. Then the phase error is represented by the first stage output of the APD as CK_{inj1} and VCO01. Accordingly, the UP and DN signals will be generated. In summary, according to the negative feedback concept of the injection timing calibration loop will adjust the VCDL through the output of loop filter capacitor (V_{C3}) to maintain the alignment between reference injection and SIL-VCO output. Eventually, the middle point of the pulse window signal (when the window is open) is aligned with the rising edge of VCO0+ or the falling edge of VCO0−. In this proposed architecture, the output of deployed SIL-VCO (VCO0+ and VCO0−) have the balanced capacitive loading.

B. INJECTION TIMING CALIBRATION ALGORITHM

Fig. 7(b) clearly depicts the misalignment between the VCO output at '0' phase (CK0) and injection signal (CK_{inj}). Therefore, this discussion includes the algorithm regarding self-alignment between CK0 and CK_{inj} when the PLL is locked. Since, in the locked state, a conventional PLL delivers the total charge dumped at the output of the charge pump is zero. In other words, the sum of individual charge becomes zero when the PLL is in the locked state, which can be further expressed as:

$$q_1 + q_2 + q_3 + q_4 + q_5 + \cdots\cdots + q_{36} = 0 \tag{1}$$

$$I \cdot \psi_1 + I \cdot \psi_2 + I \cdot \psi_3 + I \cdot \psi_4 + I \cdot \psi_5 + \cdots\cdots + I \cdot \psi_{36} = 0 \tag{2}$$

where $\psi_1, \psi_2, \psi_3 \ldots \psi_{36}$ are the phase disturbances between CK0 and CK_{inj} upto thirty six cycles of calibration. Here 'I' is used for charge pump output current.

Consider, if the self-alignment circuit deviates the first phase disturbance (ψ_1) by an amount of $\Delta\psi_1$, the new phase disturbances are changed to

$$\psi_1' = \psi_1 - \Delta\psi_1, \quad \psi_2' = \psi_2, \ \psi_3' = \psi_3 \cdots \psi_{36}' = \psi_{36} \tag{3}$$

Again according to Equ. (2) we can write as:

$$I \cdot \psi_1' + I \cdot \psi_2' + I \cdot \psi_3' + I \cdot \psi_4' + \cdots\cdots + I \cdot \psi_{36}' = 0 \tag{4}$$

To satisfy the Equ. (4), the phase disturbance ($\Delta\psi_1$) is equally distributed among thirty-six cycles. Hence, the net charge in the first step corresponds to the thirty-six cycles are as follows:

$$\begin{aligned}
&Start : I \cdot \psi_1,\ I \cdot \psi_2 \ \cdot\ I \cdot \psi_{36} \\
&1ststep : I\left(\psi_1 - \Delta\psi_1 + \frac{\Delta\psi_1}{36}\right),\ I\left(\psi_2 + \frac{\Delta\psi_1}{36}\right) \cdots I\left(\psi_{36} + \frac{\Delta\psi_1}{36}\right) \\
&2ndstep : I\left(\psi_1 - \Delta\psi_1 + \frac{\Delta\psi_1}{36} + \frac{\Delta\psi_2}{36}\right), \\
&I\left(\psi_2 - \Delta\psi_2 + \frac{\Delta\psi_1}{36} + \frac{\Delta I\psi_2}{36}\right) \ldots I\left(\psi_{36} + \frac{\Delta\psi_1}{36} + \frac{\Delta\psi_2}{36}\right) \\
&36thStep : I\left(\psi_1 - \Delta\psi_1 + \frac{\Delta\psi_1}{36} + \frac{\Delta\psi_2}{36} + \frac{\Delta\psi_3}{36} + .. \frac{\Delta\psi_{36}}{36}\right), \\
&I\left(\psi_2 - \Delta\psi_2 + \frac{\Delta\psi_1}{36} + \frac{\Delta\psi_2}{36} + \frac{\Delta\psi_3}{36} + \cdots . + \frac{\Delta\psi_{36}}{36}\right) \cdots I \\
&\times \left(\psi_{36} - \Delta\psi_{36} + \frac{\Delta\psi_1}{36} + \frac{\Delta\psi_2}{36} + \frac{\Delta\psi_3}{36} + \cdots . + \frac{\Delta\psi_{36}}{36}\right)
\end{aligned} \tag{5}$$

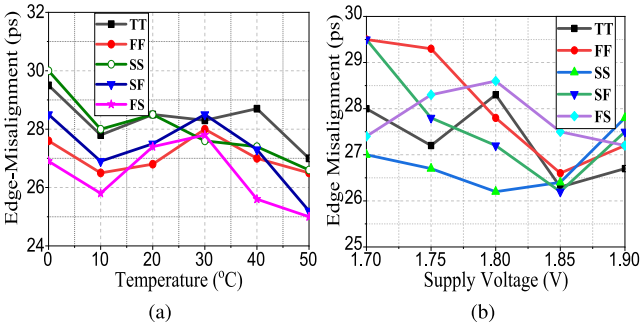

FIGURE 13. Simulated edge-misalignment at every process corner for the fixed output frequency of 1.8 GHz (a) over the temperature variation, and (b) the supply voltage variation.

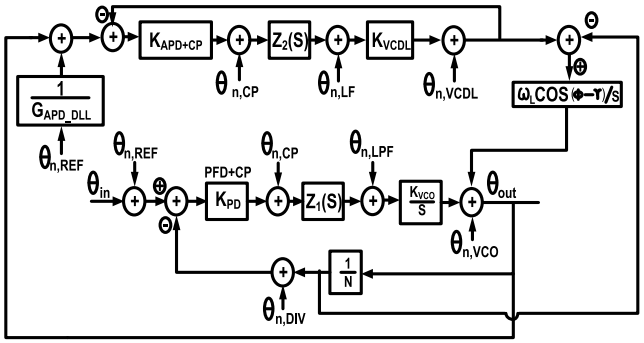

FIGURE 14. Phase domain model of the proposed SILPLL with self-aligned injection.

Hence, the resultant phase disturbance after its first iteration after thirty-six cycles can be expressed as:

$$\begin{aligned}
\psi_1^{36} &= \psi_1 - \Delta\psi_1 + \sum_{k=1}^{36} \frac{\Delta\psi_k}{36}, \\
\psi_2^{36} &= \psi_2 - \Delta\psi_2 + \sum_{k=1}^{36} \frac{\Delta\psi_k}{36} \cdots \psi_{36}^{36} \\
&= \psi_{36} - \Delta\psi_{36} + \sum_{k=1}^{36} \frac{\Delta\psi_k}{36}
\end{aligned} \tag{6}$$

where ψ_1^{36} is the phase disturbance because of the first output signal after thirty-six cycles of calibration and $\Delta\psi_1$ is the amount of calibration required for the first output signal.

The above-mentioned iteration is performed continuously until the phase disturbance for the first output (ψ_1) is nullified by the amount of calibration $\Delta\psi_1$. Likewise, all the phase disturbances become null after finishing calibration. Which further makes the total charge is null.

C. CLOCK-GENERATION AND VOLTAGE CONTROL DELAY LINE (VCDL)

It is very critical to design a clock-generation circuit in such a way so that the rising-edge of the injection signal falls exactly at the midpoint of the pulse window (as shown in Fig. 11(b)) to implement the self-alignment concept. Additionally, the

two identical delay cells with different stages are used for the generation of the pulse window. The schematic of the delay cell can be implemented by using the different buffer stages of VCDL, which as shown in Fig. 12(b) is usually represented by a current-starved delay cell. Each single-stage VCDL has an inverter delay cell stage (M_{15}-M_{16}) and a composition of control stage (M_{11}-M_{13}) and (M_{12}-M_{14}). The overall gain of the ten-stage VCDL is obtained as 2.5 ns/V, as shown in Fig. 25. The CLK-generation (CLK-GEN) and VCDL blocks play a very important role in edge detection and edge alignment in the proposed architecture. From Fig. 6 once the reference injection path is activated for LD = 1, the VCDL starts getting the CLK-GEN output. Thereafter, as per the output of loop filter capacitor (C_3), VCDL further updates the delay dynamically for the edge alignment.

Moreover, to obtain the accurate edge alignment, the resolution of VCDL should be sufficiently high. Hence, the deployed ten-stage current starved inverter (buffer) topology-based VCDL has the resolution of 0.22 ns with the edge misalignment of 28.3 ps at 1.8 V supply voltage, and across the 27° C temperature. The selected ten-stage VCDL resolution is sufficiently high enough, which provides the optimum edge alignment and covers higher frequency range of SILVCO (sub-harmonically injection locked VCO) without significantly degrading the wide band phase noise [38], [40]. Nonetheless, if the number of stages of the deployed VCDL in the proposed architecture is increased above ten for getting the more VCDL resolution, it will lead to more accurate edge alignment, however, at the cost of significant degradation in wide band phase noise [38], [40]. However, the variation in edge alignment across the voltage and temperature corner ranging from (0 - 50° C) and (1.7 V - 1.9 V), is as shown in Fig. 13(a) and 13(b) respectively. Fig. 13(a) clearly depicts the variation in maximum to minimum edge-misalignment is ranging from (30 ps - 25.2 ps) over the different temperature across the different corner variation at 1.8 V supply. Likewise, Fig. 13(b) shows the variation in maximum to minimum edge-misalignment over the different supply voltage across different process corner at room temperature is ranging from (29.8 ps - 26.2 ps).

III. PHASE NOISE ANALYSIS OF THE SILPLL WITH SELF ALIGNED INJECTION

A. CALCULATION OF PHASE NOISE DUE TO CP DEPLOYED IN APD BASED DLL WITH SILPLL

In the PLL, the phase noise can be splitted into two parts [11] such as (a) the in-band noise (thermal noise from the PD/CP, reference input and divider); (b) the out-of band noise (thermal noise due to VCO and LF).The focus of this paper is on reducing the PLL in-band phase noise due to CP in DLL loop. Unlike the classical phase detectors, an APD can work without divider (N). Hence, the CP noise is not multiplied by N^2 [11]. However, many research works are proposed in the area of self-aligned SILPLL without considering this issue. Therefore, in this article a comparison of in-band phase noise is done between SILPLL with self-aligned DLL [21] and SILPLL with APD based DLL. To understand this, a linear phase domain model of newly proposed architecture is shown in Fig. 14 along with the injection locked VCO [21]. Where (ω_L) is locking range in (rad/s), γ is the input phase before injection to the VCO whereas ϕ is the output phase after the injection respectively. Additionally, $G_{APD\text{-}DLL}$ and G_{PLL} are the forward path gain of DLL and classical PLL. In a classical PLL, charge pump feedback gain [11] (β_{cp}) can be expressed as:

$$\beta_{cp} = \left(\frac{I_{cp}}{2\pi} \cdot \frac{1}{N}\right),\ K = \frac{I_{cp}}{2\pi} \tag{7}$$

The β_{cp} of the self-aligned SILPLL with APD based DLL and the classical self-aligned SILPLL with DLL are related as:

$$\frac{\beta_{CP,(APD\text{-}DLL)SILPLL}}{\beta_{CP,(PFD\text{-}DLL)SILPLL}} = \frac{\frac{I_{cp}}{2\pi} + \frac{I_{cp}}{2\pi} \cdot \frac{1}{N}}{\frac{I_{cp}}{2\pi} \cdot \frac{1}{N} + \frac{I_{cp}}{2\pi} \cdot \frac{1}{N}} = \frac{N+1}{2} \tag{8}$$

$$G_{APD\text{-}DLL} = K_{APD+CP} \cdot Z_2(s) \cdot K_{VCDL} \tag{9}$$

$$G_{PLL} = K_{PFD+CP} \cdot Z_1(s) \cdot \frac{K_{VCO}}{s} \tag{10}$$

The noise transfer function (NTF) with the effect of charge pump noise ($\frac{\theta_{n,\,APD\text{-}DLL(PLL)}}{\theta_{n,\,CP}}$) in the proposed SILPLL with APD based DLL can be expressed as:

$$\frac{\left(\frac{1}{K}\right)\left(\frac{1}{1+G_{APD\text{-}DLL}} \cdot \frac{\omega_L \cos(\phi-\gamma)}{s}\right) + \left(\frac{N}{K}\right)(G_{PLL})}{1 + \frac{G_{PLL}}{N} + \frac{G_{APD\text{-}DLL}}{1+G_{APD\text{-}DLL}} \cdot \frac{\omega_L \cos(\phi-\gamma)}{s} \cdot \frac{1}{N} + \frac{\omega_L \cos(\phi-\gamma)}{s} \cdot \frac{1}{N}} \tag{11}$$

Likewise, the NTF due to charge pump noise ($\frac{\theta_{n,\,PFD\text{-}DLL(PLL)}}{\theta_{n,\,CP}}$) in the previously designed SILPLL with self-aligned PFD based DLL [21] can be given as:

$$\frac{\left(\frac{N}{K}\right)\left(\frac{1}{1+G_{PFD\text{-}DLL}} \cdot \frac{\omega_L \cos(\phi-\gamma)}{s} + G_{PLL}\right)}{1 + \frac{G_{PLL}}{N} + \frac{G_{PFD\text{-}DLL}}{1+G_{PFD\text{-}DLL}} \cdot \frac{\omega_L \cos(\phi-\gamma)}{s} \cdot \frac{1}{N} + \frac{\omega_L \cos(\phi-\gamma)}{s} \cdot \frac{1}{N}} \tag{12}$$

Therefore, inside the PLL loop bandwidth, the in-band phase noise contributed by the charge-pump in the self-aligned APD based DLL can be approximated [11] as:

$$\mathcal{L}_{\text{in-band, CP1}} = \frac{1}{2} \cdot 8kT\gamma \cdot g_m \cdot \left(\frac{\tau_{res}}{T_{ref}}\right) \cdot \left|\frac{\theta_{n,\,APD\text{-}DLL(PLL)}}{\theta_{n,\,CP}}\right|^2 \tag{13}$$

Similarly, the in-band phase noise of SILPLL with self-aligned DLL can be estimated as:

$$\mathcal{L}_{\text{in-band, CP2}} = \frac{1}{2} \cdot 8kT\gamma \cdot g_m \cdot \left(\frac{\tau_{res}}{T_{ref}}\right) \cdot \left|\frac{\theta_{n,\,PFD\text{-}DLL(PLL)}}{\theta_{n,\,CP}}\right|^2 \tag{14}$$

The ratio of the in-band phase noise of proposed APD based DLL to that of PFD based DLL is as follows:

$$\frac{\mathcal{L}_{\text{in-band, CP1}}}{\mathcal{L}_{\text{in-band, CP2}}} = \left(\frac{\frac{1}{N} \cdot \frac{1}{1+G_{APD\text{-}DLL}} \cdot \frac{\omega_L \cos(\phi-\gamma)}{s} + G_{PLL}}{\frac{1}{1+G_{PFD\text{-}DLL}} \cdot \frac{\omega_L \cos(\phi-\gamma)}{s} + G_{PLL}}\right)^2 \tag{15}$$

The noise transfer function (NTF) due to voltage-controlled delay line (VCDL) noise ($\frac{\theta_{\text{n, APD\_DLL(PLL)}}}{\theta_{\text{n, VCDL}}}$) at the output of the proposed architecture can be given by Equ. (16), where Q represents $\frac{\omega_{\text{L}}\cos(\phi-\gamma)}{\text{s}}$. Hence, the calculated in-band phase noise with the effect of VCDL at the output of PLL can be approximately given by Equ. (17).

$$\frac{\text{Q}}{1+\text{G}_{\text{APD\_DLL}}(1+\text{Q})+\frac{\text{G}_{\text{PLL}}}{\text{N}}(1+\frac{\text{G}_{\text{APD\_DLL}}}{\text{N}})+\frac{1}{\text{N}}\cdot\text{Q}} \tag{16}$$

$$\mathcal{L}_{\text{in-band, VCDL}}=\frac{1}{2}\cdot 8kT\gamma\cdot g_m\cdot\left|\frac{\theta_{\text{n, APD\_DLL(PLL)}}}{\theta_{\text{n, VCDL}}}\right|^2 \tag{17}$$

From Equ. (15), it is clear that, as N increases the ratio decreases implying that the in-band phase noise of APD-based DLL reduces compared to that of PFD based DLL. Correspondingly, from Fig. 16(a), it is evident that APD-based DLL offers low in-band phase noise compared to PFD-based DLL for the same N by an amount of 12 dB at 200 kHz offset. Whereas, Fig. 16(b) depicts the improvement in in-band phase noise of APD-based DLL by approximately 20 dB with the reduction in N by a factor of 2. Likewise the in-band phase noise contribution with the effect of VCDL has been also included, as shown in Fig. 17. The contribution of wideband phase noise due to VCDL is very less. Additionally, the noise transfer function with the effect of reference input, CP, and VCO for various locking ranges (f_{L}) is calculated as shown in Fig. 18(a), 19(a), and 20(a) respectively.

The noise transfer function (NTF) ($\frac{\theta_{\text{out}}}{\theta_{\text{n, REF}}}$) for the proposed SILPLL due to the reference input noise can be expressed by Equ. (18).

$$\frac{\text{G}_{\text{PLL}}+\frac{1}{1+\text{G}_{\text{APD-DLL}}}\cdot\frac{\omega_{\text{L}}\cos(\phi-\gamma)}{\text{s}}}{1+\frac{\text{G}_{\text{PLL}}}{\text{N}}+\frac{\text{G}_{\text{APD-DLL}}}{1+\text{G}_{\text{APD-DLL}}}\cdot\frac{\omega_{\text{L}}\cos(\phi-\gamma)}{s}\cdot\frac{1}{\text{N}}+\frac{\omega_{\text{L}}\cos(\phi-\gamma)}{\text{s}}\cdot\frac{1}{\text{N}}} \tag{18}$$

The NTF ($\frac{\theta_{\text{out}}}{\theta_{\text{n, CP}}}$) when the effect of charge pump noise is included which is given by Equ. (19).

$$\frac{\text{Z}_1(s)\cdot\frac{\text{K}_{\text{VCO}}}{s}}{1+\frac{\text{G}_{\text{PLL}}}{\text{N}}+\frac{\text{G}_{\text{APD-DLL}}}{1+\text{G}_{\text{APD-DLL}}}\cdot\frac{\omega_{\text{L}}\cos(\phi-\gamma)}{s}\cdot\frac{1}{\text{N}}+\frac{\omega_{\text{L}}\cos(\phi-\gamma)}{\text{s}}\cdot\frac{1}{\text{N}}} \tag{19}$$

Likewise, the NTF ($\frac{\theta_{\text{out}}}{\theta_{\text{n, VCO}}}$) due to VCO noise can be expressed by Equ. 20.

$$\frac{1}{1+\frac{\text{G}_{\text{PLL}}}{\text{N}}+\frac{\text{G}_{\text{APD-DLL}}}{1+\text{G}_{\text{APD-DLL}}}\cdot\frac{\omega_{\text{L}}\cos(\phi-\gamma)}{s}\cdot\frac{1}{\text{N}}+\frac{\omega_{\text{L}}\cos(\phi-\gamma)}{\text{s}}\cdot\frac{1}{\text{N}}} \tag{20}$$

As locking range (f_{L}) increases, the effect of noise due to reference clock on the injection locked PLL increases (shown in Fig. 18(a)), but the effect of charge-pump noise and four-stage VCO noise decreases (as shown in 19(a) and 20(a)). Hence, most of the injection locked architectures adopt the optimum value of locking range (f_{L}) between 20 MHz to 40 MHz. Commonly, a high f_{L} is required since the VCO noise is dominant among all noise sources in PLL. However, an excessive value of f_{L} can cause the distortion at the output of PLL. Therefore, in this proposed architecture, a fixed f_{L} is considered which is equal to 20 MHz for all analysis.

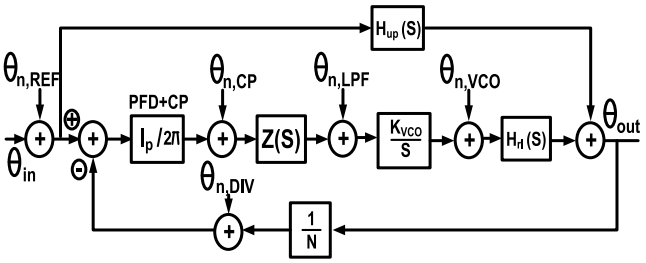

FIGURE 15. Linear phase domain model of the proposed self-aligned SILPLL.

B. NOISE ANALYSIS WITH THE EFFECT OF REALIGNMENT-FACTOR (δ)

The realignment factor can be defined as the magnitude of the slope of the curve, which has been drawn to analyze the VCO phase shift as a function of phase error, i.e., the error between VCO and reference phases just before the realignment begins, and it is denoted by δ.

Ideally, in the closed-loop of PLL, if both the reference and the VCO were noiseless, the edges of VCO would align with an edge of the reference for each reference period. However, in the real scenario, the presence of phase noise in the VCO and the reference cause misalignment between these two edges. This misalignment perturbs throughout the transient and owing to misalignment between the VCO delay cell and reference, it basically cause both amplitude and phase disturbances. Conventionally, the amplitude fluctuations vanish within several VCO cycles due to amplitude limiting mechanism in oscillators [38]. However, the phase disturbances carry indefinitely throughout the transient. Therefore, to analyze the factor by which the phase fluctuations due to noisy edges of VCO can be mitigated as a function of phase error linearly has been represented by the realignment factor (δ). Where, the realignment factor (δ) describes the strength of the realignment, which varies from 0 to 1. The linear incremental model of the proposed SILPLL including the effect of reference input, charge pump, and VCO noise sources is shown in Fig. 15. In contrast to the classical PLL linear model, $\text{H}_{\text{up}}(\text{s})$ and $\text{H}_{\text{rl}}(\text{s})$ are added, as elucidated in [41]. The effect of phase realignment within the pulse window by the injection of CK_{inj} and the up-conversion of thermal noise of reference signal to VCO output are denoted by $\text{H}_{\text{rl}}(\text{s})$ and $\text{H}_{\text{up}}(\text{s})$. It can be expressed as follows: N and T_{inj} are the division ratio and injection clock period respectively, and δ is used as realignment factor which lies between ($0 \leq \delta \leq 1$). Then $\text{H}_{\text{rl}}(\text{s})$, $\text{H}_{\text{up}}(\text{s})$ and the forward path gain G(s) of the SILPLL are given by:

$$\text{H}_{\text{rl}}(\text{s})=1-\frac{\delta}{1+(\delta-1)e^{-s\text{T}_{\text{inj}}}}e^{-s\text{T}_{\text{inj}}/2}\frac{\sin(\omega\text{T}_{\text{inj}}/2)}{(\omega\text{T}_{\text{inj}}/2)} \tag{21}$$

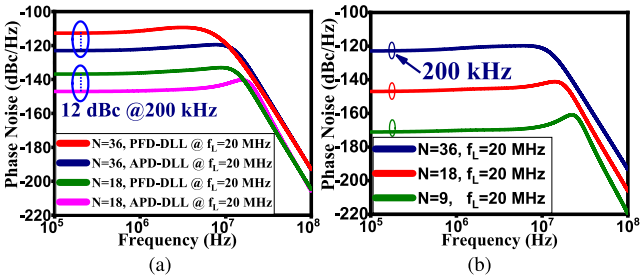

FIGURE 16. (a) Calculated in-band phase noise with the effect of CP at the output of the proposed self-aligned SILPLL with APD-based DLL and PFD-based DLL at the fixed locking range for two different division ratios (b) Calculated contribution of in-band phase noise of CP at the output of the proposed self-aligned SILPLL with APD based DLL for Different values of N.

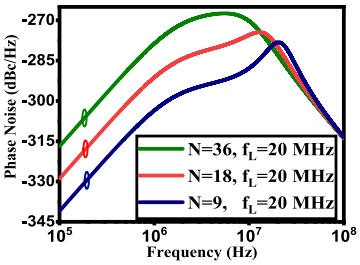

FIGURE 17. Calculated contribution of in-band phase noise of VCDL at the output of the proposed self-aligned SILPLL with APD-based DLL for Different values of N and fixed locking range of 20 MHz.

$$\mathrm{H_{up}(s)} = \frac{\mathrm{N}\delta}{1+(\delta-1)e^{-s\mathrm{T_{inj}}}} e^{-s\mathrm{T_{inj}}/2} \frac{\sin(\omega \mathrm{T_{inj}}/2)}{(\omega \mathrm{T_{inj}}/2)} \tag{22}$$

$$\mathrm{G}(s) = \frac{\mathrm{I}_p}{2\pi} \mathrm{Z}(s) \frac{\mathrm{K_{VCO}}}{s} \mathrm{H_{rl}(s)} \tag{23}$$

The calculated NTF due to reference noise, CP noise and VCO are given by Equ. (24), (25), and (26), which are plotted in Fig. 18(b), 19(b), and 20(b) respectively.

$$\frac{\theta_{\mathrm{out}}}{\theta_{\mathrm{n,REF}}} = \frac{G(s)+\mathrm{H_{up}}(s)}{1+\frac{G(s)}{N}} \tag{24}$$

$$\frac{\theta_{\mathrm{out}}}{\theta_{\mathrm{n,CP}}} = \frac{\mathrm{Z}(s)\frac{K_{\mathrm{VCO}}}{s}\mathrm{H_{rl}}(s)}{1+\frac{G(s)}{\mathrm{N}}} \tag{25}$$

$$\frac{\theta_{\mathrm{out}}}{\theta_{\mathrm{n,VCO}}} = \frac{\mathrm{H_{rl}}(s)}{1+\frac{\mathrm{G}(s)}{\mathrm{N}}} \tag{26}$$

Fig. 18(a) and 18(b) represents NTF with reference noise. When $\mathrm{f_L}$ and δ are 0, the behavior of NTF is equivalent to the clasical PLL. As, $\mathrm{f_L}$ and δ increase, the -3 dB bandwidth of the proposed architecture increases. Similarly, from Fig. 19(a) and 19(b) the calculated NTF decreases as $\mathrm{f_L}$ and δ increase over the PLL bandwidth. The calculated contribution of VCO noise as in Fig. 20(a) and 20(b) represents the increased -3 dB corner frequency when $\mathrm{f_L}$ and δ increase. Hence, the behavior of the proposed architecture with different locking ranges ($\mathrm{f_L}$) is as same as the previously designed architecture [41] with the variation of realignment factor δ. Hence, it is validated.

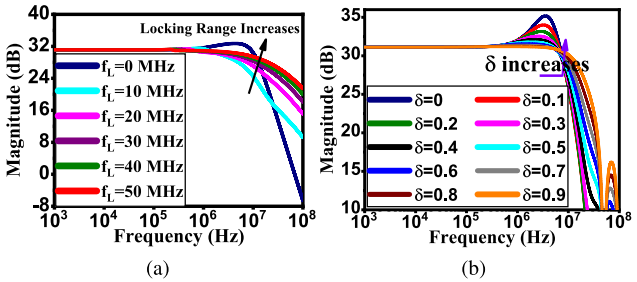

FIGURE 18. Calculated result of (a) reference noise transfer function with varying locking range ($\mathrm{f_L}$) (b) reference noise transfer function with varying realignment factor (δ).

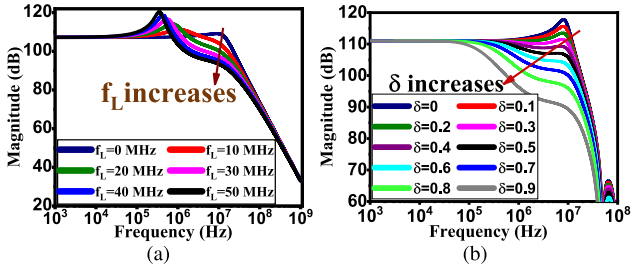

FIGURE 19. Calculated result of (a) charge pump noise transfer function with varying locking range ($\mathrm{f_L}$) (b) charge pump noise transfer function with varying realignment factor (δ).

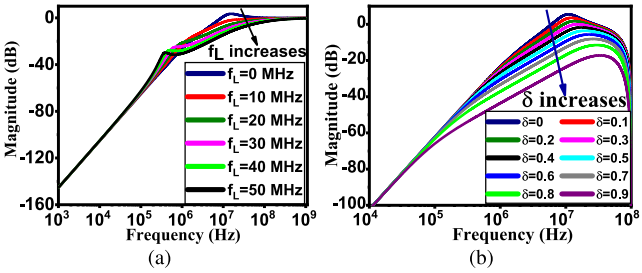

FIGURE 20. Calculated result of (a) VCO noise transfer function with varying locking range ($\mathrm{f_L}$) (b) VCO noise transfer function with varying realignment factor (δ).

C. DESIGN OF THE PROPOSED SELF-ALIGNED SILPLL

A four-stage current starved topology-based pseudo-differential ring VCO with an injection transistor and three dummies is shown in Fig. 7(a). The delay cell is composed of two inverters along with latch to realize the pseudo differential outputs. The simulated phase noise of standalone VCO is -89.2 dBc/Hz at 1 MHz frequency offset and VCO gain is 1.6 GHz/V. The design parameters for this proposed SILPLL are listed in Table 1.

Fig. 21 shows the calculated open-loop gain transfer functions of the type-II PLL, proposed SILPLL with specific locking range and the SILPLL with realigning factor ($\delta = 0.5$). Likewise, Fig. 22 depicts the calculated open-loop phase transfer functions for the conventional type-II PLL and the proposed architecture for the locking range of $\mathrm{f_L} = 20$ MHz and $\delta = 0.5$ respectively. The calculated loop bandwidth [4] and phase margin of the conventional type-II PLL

TABLE 1. Design parameters of the self-aligned silpll.

Conventional Type-II PLL		
Reference frequency	F_{ref}	50 MHz
Division ratio	N	36
VCO gain	K_{VCO}	1.6 GHz/V
Resistor	R_1	10.36 KΩ
Capacitor	C_1	10.2 pF
	C_2	1.02 pF
Self-Aligned Injection Timing Calibration Loop		
VCDL gain	K_{VCDL}	2.5 ns/V
Loop filter capacitor	C_3	1.5 pF
Charge pump current	I_p	75 μA
Injection clock period	T_{inj}	20 ns

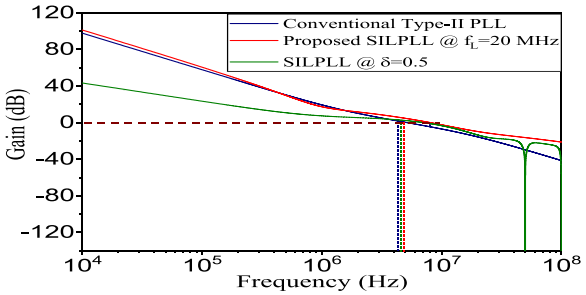

FIGURE 21. Calculated open-loop gain transfer function of the type-II PLL, proposed SILPLL with 20 MHz locking range and the SILPLL with realigning factor ($\delta = 0.5$).

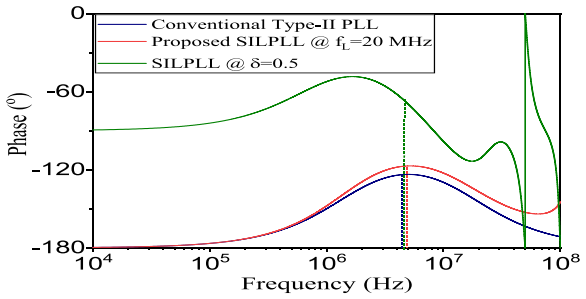

FIGURE 22. Calculated open-loop phase transfer function of the type-II PLL, proposed SILPLL with 20 MHz locking range and the SILPLL with realigning factor ($\delta = 0.5$).

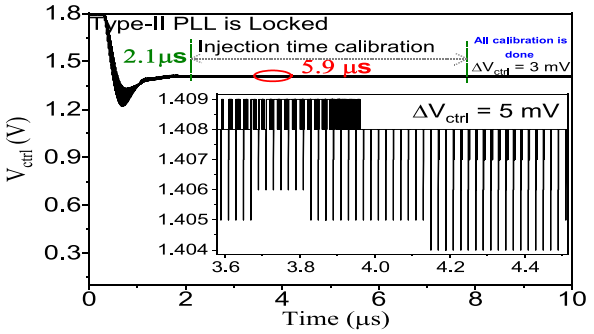

FIGURE 23. Simulation results of the control voltage V_{ctrl} (V) before the calibration process.

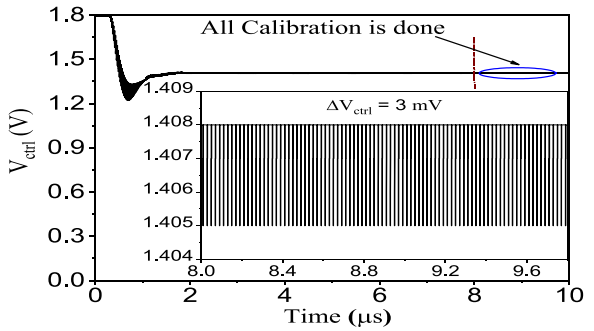

FIGURE 24. Simulation results of the control voltage V_{ctrl} (V) after the calibration process.

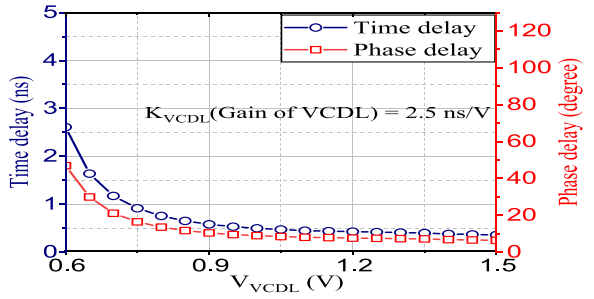

FIGURE 25. Simulated result of time and phase delay of the ten-stage VCDL.

are 5.1 MHz and 56.5° respectively as shown in Fig. 21 and 22. Moreover, for the proposed architecture while locking range (f_L) is 20 MHz, the acquired loop bandwidth and phase margin are 5.5 MHz and 63° respectively. Additionally, the open-loop gain transfer function calculation is also done for SILPLL including the effect of realignment factor $\delta = 0.5$, for which the obtained loop bandwidth and phase margin are 5.2 MHz and 95° respectively.

IV. RESULTS AND DISCUSSIONS

Fig. 23 presents, how the control voltage (V_{ctrl}) of VCO (V_{ctrl}) changes during the calibration of self-aligned SILPLL. According to Fig. 23, the injection time calibration is activated only after the locking of conventional PLL which is at 2.1 μs. Once the locking is detected by lock detector, the delay of the injected pulse is further controlled by the ten-stage of the VCDL as shown in Fig. 25. As the output voltage of the loop filter capacitor is changed on account of the phase mismatches between the injected pulse (CK_{inj}) and VCO output (VCO0), the delay is also updated through VCDL. Therefore, from Fig. 23, it can be seen that an additional time of 5.9 μs is required to complete the injection time calibration after the PLL locks which takes 2.1 μs.

The variation of V_{ctrl} during the calibration is shown in the inset of Fig. 23 and after the calibration is shown in Fig. 24 inset.

To verify the locked point is ''truly'' the optimum one, the open-loop ILPLL has been simulated across corner at 1.8 V supply after turning off the APD path with the VCDL delay sweep, as shown in Fig. 26(a). Moreover, across each corner

TABLE 2. Performance summary and comparison.

	[14]	[15]	[16]	[17]	[18]	[19]	[20]	[22]	[29]	[42]	[43]	This Work
Technology (nm)	28	180	180	65	90	40	28	45	65	65	65	180
VCO Type	LC	Ring	Ring	Ring	LC	Ring	Ring	Ring	LC	LC	Ring	Ring
Architecture	Type-I S-PLL	CP-leakage cancellation	SILPLL	SILPLL	SS-SIPLL	SILPLL	Analog ILPLL	SIL-TPLL	SILPLL	SILPLL	ILPLL+PNF	Self-aligned SILPLL
Type	Integer-N	Integer-N	Integer-N	Integer-N	Integer-N	Integer-N	Integer-N	Integer-N	Integer-N	Integer-N	Fractional-N	Integer-N
Output frequency (GHz)	3.36	1.6	2.4-2.48	1.7	2.4	0.4-1.6	4	2.4	2.4	8-12	1.2	1.8
Reference frequency (MHz)	105	50	5	566	40	50	125	150	150	2000-3000	50	50
Divider ratio	32	32	481-496	3	60	8-32	32	16	16	4	24	36
PN @1MHz (dBc/Hz)	-125.3	-121	-112	-128	-115	-106.7	-112.3	-119	-120	-127.6	-109.4	-120.6
RMS Jitter (ps)	0.124 10k-100M	0.57	N/A	0.197	0.37 (10k-30M)	2.29 1k-30M	0.71 (10k-30M)	0.91 (1k-40M)	0.145 (1k-40M)	0.1-0.11 1k-30M	1.48 (100k-100M)	0.96 (10k-30M)
Reference spur (dBc)	-78.6	N/A	-54	-47	-44	-44	-61.6	-44.4	-40	-47.6	-57	-47.2
Power (mW)	3.37	3.35	7.5	11.77	0.5	1.49	11.4	5.6	12.6	8.3-8.6	19.8	6.6
Area (mm^2)	0.22	0.15	N/A	0.017	0.26	0.140	0.09	0.013	0.64	0.6	0.6	0.023
FOM (dB)	-252.8	-179.8	N/A	-243.5	-251.6	-231	-232.4	-233.3	-246	-250/-248.8	-223.6	-239.5
Settling Time (μs)	-	15	28	-	-	-	-	1.8	17	14	-	8

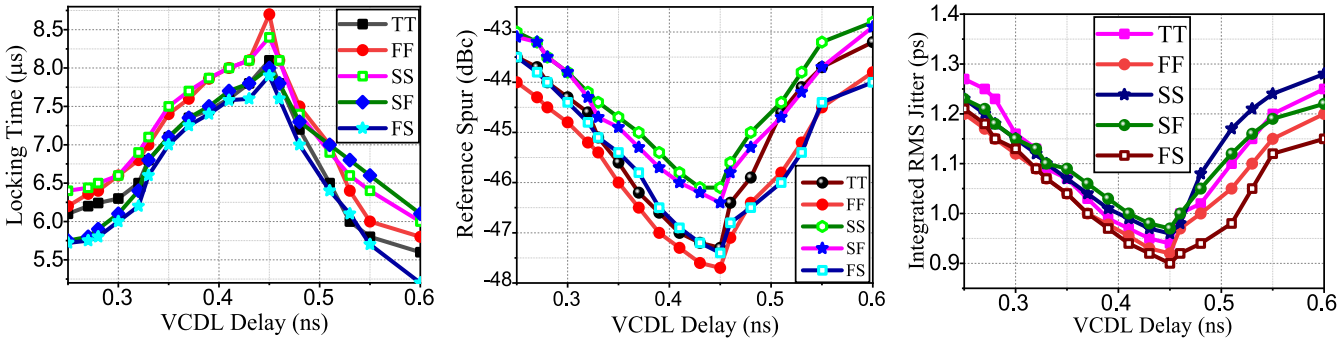

FIGURE 26. Simulation of open-loop ILPLL after turning off the APD path with VCDL delay sweep at 1.8 V supply includes the performance of (a) locking time (b) reference spur, and (c) integrated RMS jitter.

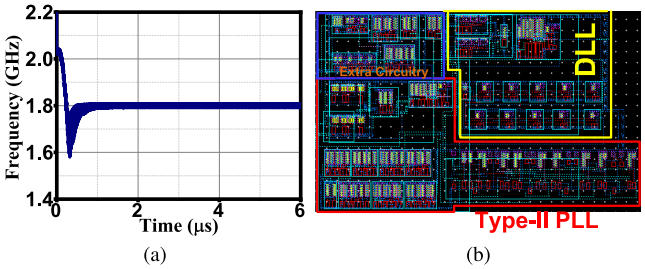

FIGURE 27. Calculated result of (a) Simulated transient response for the output frequency of self-aligned SILPLL (f_L) (b) Layout of the proposed architecture.

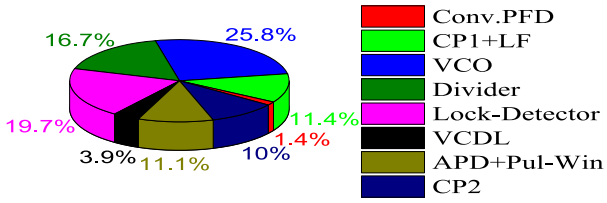

FIGURE 28. Power consumption of different sub-blocks in the proposed architecture.

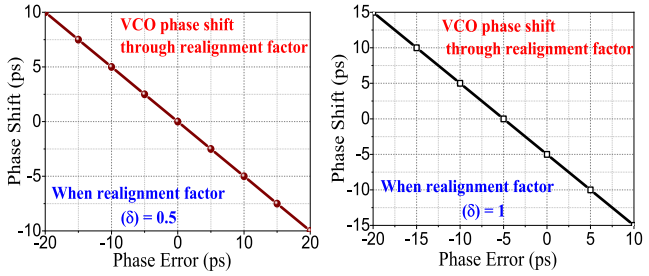

FIGURE 29. Simulated reference spur of the proposed SILPLL (a) without and (b) with injection at 1.8 GHz.

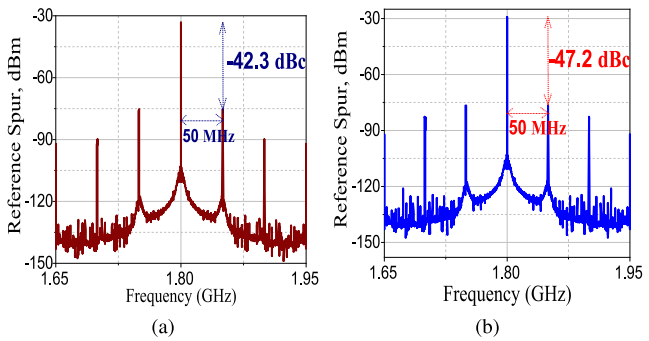

FIGURE 30. Simulated reference spur of the proposed SILPLL (a) without and (b) with injection at 1.8 GHz.

and locking time, the performance of reference spur and jitter has been also simulated, as depicted in Fig. 26(b) and 26(c) respectively. The simulated results of spur and jitter at 0.44 ns VCDL delay across every corner clearly shows that the overall locking time is optimum one. The simulated reference spur and jitter are −47.3 dBc and 0.94 ps at the TT corner for the above-mentioned VCDL delay with approximately 8 μs locking time.

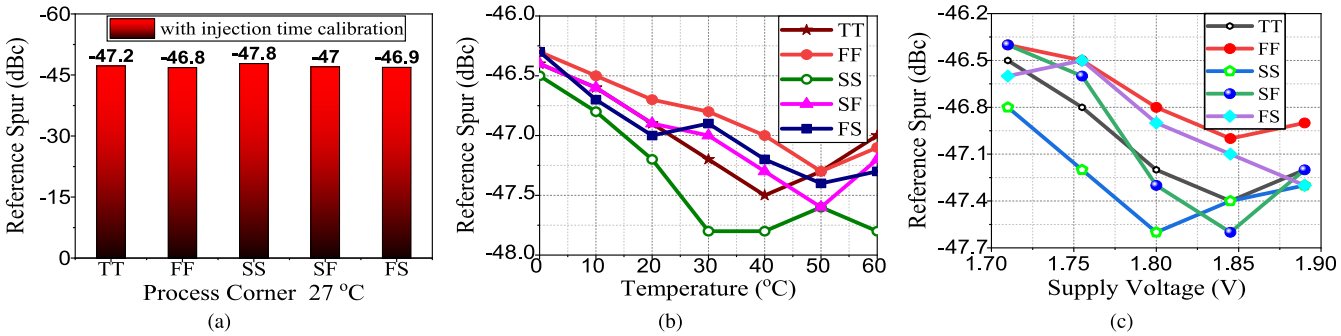

FIGURE 31. (a) Variation of reference spur over different process corner at room temperature. Simulated reference spur after enabling injection time calibration at every process corner (b) over temperature (c) over supply voltage.

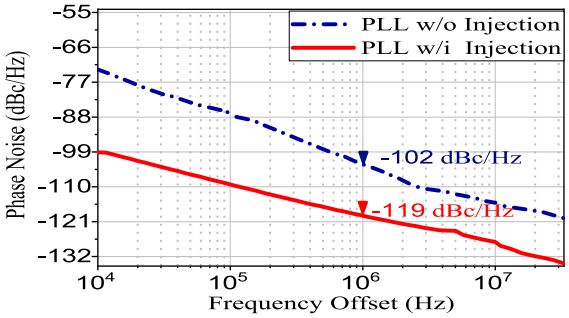

FIGURE 32. Simulated phase noise of the proposed self-aligned SILPLL output with and without injection at 1.8 GHz.

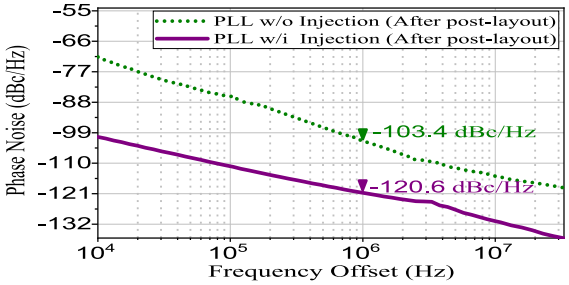

FIGURE 33. Simulated phase noise of the proposed self-aligned SILPLL output with and without injection at 1.8 GHz after post-layout.

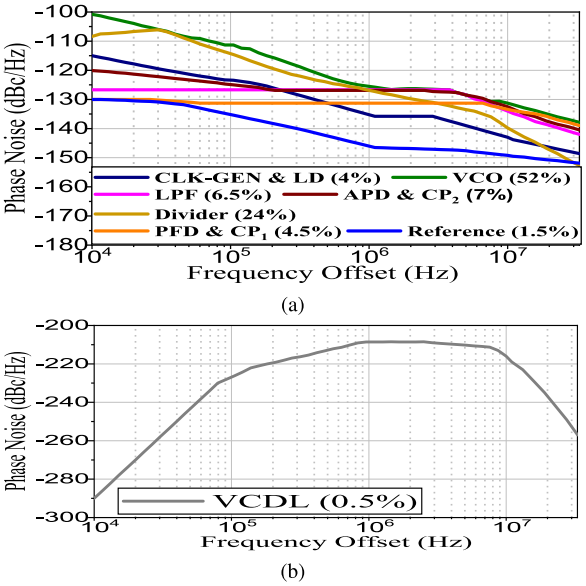

FIGURE 34. (a) Simulated phase noise curves of every sub-block's of the proposed architecture at 1.8 GHz, and (b) simulated phase noise curve of the VCDL.

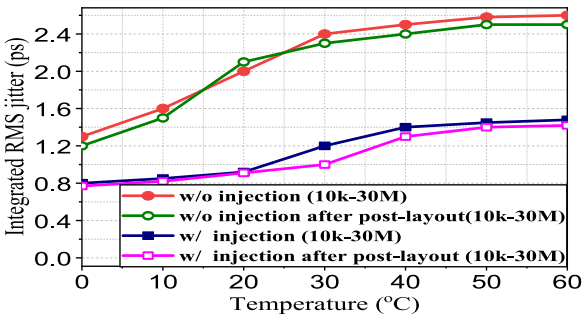

FIGURE 35. Simulated integrated rms jitter with the effect of temperature before and after post-layout.

The proposed architecture of PLL operates for 1.8 GHz output frequency as shown in Fig. 27(a). The proposed architecture of self-aligned SILPLL is implemented in a 180-nm SCL CMOS process. The core area is 0.023 mm^2 which is shown by Fig. 27(b). Moreover, it consumes 6.6 mW from 1.8 V power supply as shown in Fig. 28.

In a basic charge-pump-based PLL, a phase-frequency detector (PFD) is the only block, which is used to detect the phase error between VCO output and the reference clock. In contrast, the proposed technique includes an auxiliary loop that embodies an extra phase comparator at the phase realignment point using an aperture phase detector (APD). Hence, there is two dedicated signal path from the reference clock to the VCO output. Since, reference clock injection path incorporates an injection timing calibration loop with APD-based DLL, which further compares two different periodic signals under the influence of the windowing technique. Because of the output of APD, the charge pump becomes more sensitive to the output current. Based on the output current of the charge pump, the loop filter in APD-based DLL updates the

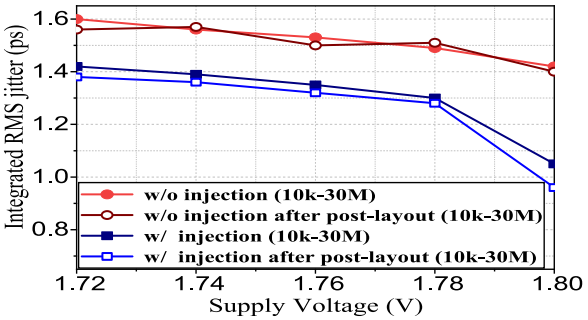

FIGURE 36. Simulated integrated rms jitter with the effect of supply voltage before and after post-layout.

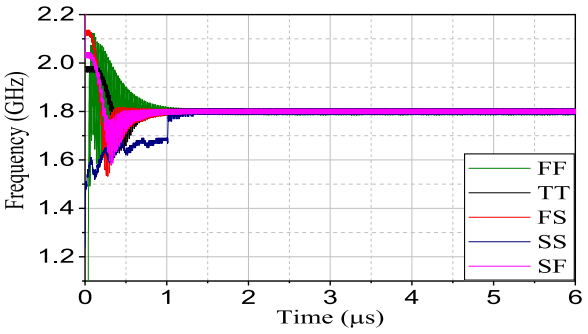

FIGURE 37. Simulation of output frequency at each corner.

voltage to the VCDL. Hence, the significant mismatches in the reference clock injection signal path degrades the spur performance. Furthermore, the overall mismatches between the two signal paths enhance the power of the reference spur relative to the carrier in the output of the proposed architecture. As,the proposed technique includes an APD-based DLL windowing technique for self-alignment, in which the APD produces some offset too between the VCO clock and injection clock, which further leads to the degradation in spur performance. However, the performance degradation in reference spur because of the relative delay between the two paths can be reduced by enhancing the realignment factor δ, which is defined as the magnitude of the slope of the curve drawn to analyze the VCO phase shift as a function of phase error i.e. the error between VCO and reference phases just before the realignment begins [41].

Theoretically, once the injection time calibration (or edge alignment) gets enabled through the path to the APD (or reference clock injection path), it adds very small phase shift to the VCO edges that further leads to small phase error, and the reference spur performance degrades. Therefore, to analyze the factor by which the phase misalignment due to noisy edges of VCO can be reduced linearly as a function of phase error has been represented by the realignment factor (δ), where the realignment factor (δ) describes the strength of the realignment, which varies from 0 to 1. Fig. 29(a) shows the corresponding curve of phase shift (in the VCO edges) versus phase error (between VCO edges and injected pulse) with a realignment factor of 0.5. In this curve, for every 5 ps of phase shift, the resultant phase error is 10 ps. Whereas, Fig. 29(b) shows the resultant phase error of 5 ps for every 5 ps of phase shift, which corresponds to the realignment factor of 1. However, by increasing the δ at a certain value, the performance degradation of reference spur can be improved at some level but it may cost less attenuation of the reference phase noise. It is due to the path to the APD (or reference clock injection path) through which reference noise power is coupled into the VCO at each realignment.

Fig. 30(a) and 30(b) depicts the simulated output spectrum i.e. without and with the injection time calibration. The obtained reference spur of the proposed SILPLL are −42.3 dBc and −47.2 dBc at 1.8 GHz output frequency. Comparing with the conventional PLL, the performance of reference spur after enabling the injection time calibration technique has been improved by 4.9 dB. It means that the injection timing is successfully performed. Moreover, once the injection timing calibration enabled, the simulation of reference spur with different process corner variation, at room temperature (27 ^{o}C) has been also performed, as shown in Fig. 31(a). When the injection timing calibration has activated, the variation of the reference spur level is negligible over process corner variation. Likewise, to show how robust it is against the temperature and supply voltage variation over each process corner, further simulations have been done after the injection timing calibration technique is enabled, as shown in Fig. 31(b) and 31(c) respectively.

As shown in Fig. 32 and 33, without the injection, before and after the post-layout simulation, the conventional type-II PLL achieves a phase noise of −102 dBc/Hz and −103.4 dBc/Hz at 1-MHz offset. Once the proposed technique is deployed, the simulated phase noise before and after the post-layout simulation are reduced to −119 dBc/Hz and −120.6 dBc/Hz at 1-MHz offset, as depicted in Fig. 32 and 33 respectively.

Additionally, the phase noise curves of the every sub-block's of the proposed architecture, once after the injection time is enabled, at 1.8 GHz output frequency, corresponding to a division ratio of 36, as shown in Fig. 34(a) and 34(b) respectively. The noise contribution by the VCO is maximum among all the blocks, on the contrary VCDL contributes very less noise. The shape of the phase noise contribution by the VCDL matches with its mathematical phase noise representation, as plotted in Fig. 17, according to the Equ. (17). Moreover, the simulated integrated RMS jitter over 10 kHz to 30 MHz before post-layout is reduced from 2.3 ps to 1.1 ps at room temperature, as shown in Fig. 35. Likewise, after the post-layout simulation, the obtained integrated RMS jitter with injection over the same frequency range is reduced from 2.2 ps to 0.96 ps at room temperature, as depicted in Fig. 35. Additionally, Fig. 35 includes the integrated RMS jitter of the without injection and with injection over the temperature range of 0-60 °C with the 1.8 V power supply. Moreover, Fig. 36 shows the simulated integrated rms jitter of the without and with injection over the supply voltage of 1.72 - 1.8 V at the temperature of 27 °C. The maximum supply voltage

with which the proposed technique can work is 1.8 V due to process and voltage variation. The minimum and maximum integrated jitter for type-II PLL (without injection after post-layout simulation) are 1.2 ps and 2.5 ps as shown in Fig. 35 respectively. Correspondingly, the minimum and maximum integrated jitter for the proposed SILPLL (with injection after post-layout simulation) are 0.77 ps and 1.42 ps at temperature 0°C and 60°C respectively. Likewise, from Fig. 36 the minimum and maximum integrated jitter for type-II PLL (without injection after post-layout simulation) are 1.4 ps and 1.56 ps respectively. With injection, the minimum and maximum integrated jitter after post-layout simulation are 0.96 ps and 1.38 ps at 1.8 V and 1.72 V respectively. The corner analysis is also done for the proposed architecture which is shown in Fig. 37. Table 1 summarizes the performance summary of the proposed work and compares it with that of other recently published work. The figure of merit (FOM) given in Table 2 is calculated as [22]:

$$\text{FOM} = 20\log(\frac{\text{jitter}}{1\text{s}}) + 10\log(\frac{\text{P}_{\text{DC}}}{1\text{mW}}). \tag{27}$$

V. CONCLUSION

In this paper, a SILPLL with self-aligned APD based DLL is presented, and its circuit implementation is described. In the proposed technique, the rising edge of the VCO output is self-aligned with the injected clock edge. The in-band phase noise due to charge pump is lowered as compared with the classical SILPLL with self-aligned DLL. The proposed SILPLL can be used either as a low phase noise-based applications or as a frequency synthesizer in wireless or wireline communication.

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